Serial Infrared Transceiver
SIR, 115.2 kbit/s, 2.7 V to 5.5 V Operation

Description

The TFDU4100 is a part of the 4000 – family of low – current consumption infrared transceiver modules compliant to the IrDA standard for serial infrared (SIR) data communication, supporting IrDA speeds up to 115.2 kbit/s. Integrated within the transceiver modules are a photo PIN diode, infrared emitter (IRED), and a low–power analog control IC to provide a total front–end solution in a single package. The transceivers are capable of directly interfacing with a wide variety of I/O chips which perform the pulse–width modulation/demodulation function, including Vishay Semiconductors' TOIM4232. At a minimum, a current– limiting resistor in series with the infrared emitter and a VCC bypass capacitor are the only external components required to implement a complete solution.

Features

- Compliant to the latest IrDA physical layer specification (Up to 115.2 kbit/s), HP–SIR® and TV Remote Control
- For 3.0 V and 5 V Applications
- 2.7 to 5.5 V Wide Operating Voltage Range
- Low–Power Consumption (1.3 mA Supply Current)
- Power Sleep Mode Through V_{CC1}/SD Pin (5 nA Sleep Current)
- Surface Mount Package
  – Universal ($9.7 \times 4.7 \times 4.0$ mm^3)
- Open Collector Receiver Output, with 20 kΩ internal pull–up
- BabyFace (Universal) Package Capable of Surface Mount Solderability to Side and Top View Orientation
- Directly Interfaces with Various Super I/O and Controller Devices and Vishay Semiconductors-TOIM3232 I/Os
- Built–In EMI Protection – No External Shielding Necessary
- Only One External Component Required
- Few External Components Required
- Backward Compatible to all Vishay Semiconductors SIR Infrared Transceivers
- Split power supply, transmitter and receiver can be operated from two power supplies with relaxed requirements saving costs

Applications

- Notebook Computers, Desktop PCs, Palmtop Computers (Win CE, Palm PC), PDAs
- Digital Still and Video Cameras
- Printers, Fax Machines, Photocopiers, Screen Projectors
- Telecommunication Products (Cellular Phones, Pagers)
- Internet TV Boxes, Video Conferencing Systems
- External Infrared Adapters (Dongles)
- Medical and Industrial Data Collection Devices

Package

Baby Face (Universal)
weight 020g

Ordering Information

Part Number	Qty / Reel	Description
TFDU4100–TR3	1000 pcs	Oriented in carrier tape for side view surface mounting
TFDU4100–TT3	1000 pcs	Oriented in carrier tape for top view surface mounting

Functional Block Diagram

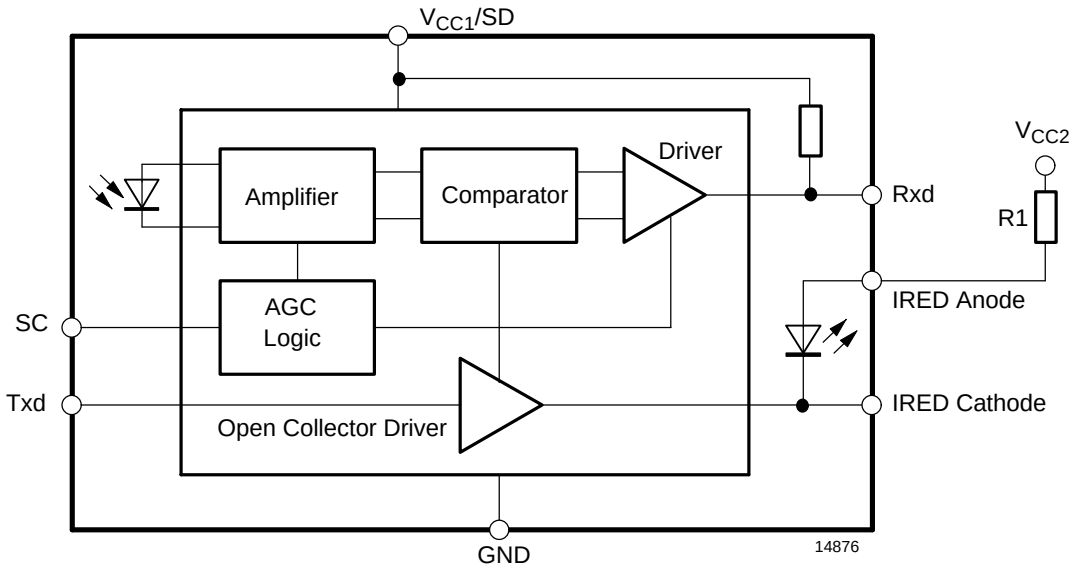


Figure 1. Functional Block Diagram

Pin Description

Pin Number	Function	Description	I/O	Active
1	IRED Anode	IRED anode, should be externally connected to V_{CC2} through a current control resistor		
2	IRED Cathode	IRED cathode, internally connected to driver transistor		
3	Txd	Transmit Data Input	I	HIGH
4	Rxd	Received Data Output, open collector. No external pull–up or pull–down resistor is required (20 kΩ resistor internal to device). Pin is inactive during transmission.	O	LOW
5	NC	Do not connect		
6	V_{CC1} / SD	Supply Voltage / Shutdown		
7	SC	Sensitivity control	I	HIGH
8	GND	Ground		

BabyFace (Universal)

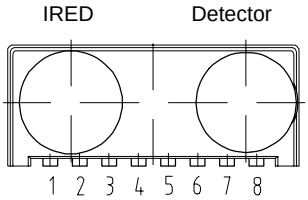


Figure 2. Pinnings

Definitions:

In the Vishay transceiver data sheets the following nomenclature is used for defining the IrDA operating modes:
SIR: 2.4 kbit/s to 115.2 kbit/s, equivalent to the basic serial infrared standard with the physical layer version IrPhy 1.0
MIR: 576 kbit/s to 1152 kbit/s
FIR: 4 Mbit/s
VFIR: 16 Mbit/s
MIR and FIR were implemented with IrPhy 1.1, followed by IrPhy 1.2, adding the SIR Low Power Standard. IrPhy 1.3 extended the Low Power Option to MIR and FIR and VFIR was added with IrPhy 1.4.A new version of the standard in any case obsoletes the former version.
With introducing the updated versions the old versions are obsolete. Therefore the only valid IrDA standard is the actual version IrPhy 1.4 (in Oct. 2002).

Absolute Maximum Ratings

Reference point Pin GND unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage Range	$0\ V \le V_{CC2} \le 6\ V$	V_{CC1}	– 0.5		6	V
	$0\ V \le V_{CC1} \le 6\ V$	V_{CC2}	– 0.5		6	V
Input Currents	For all Pins, except IRED Anode Pin				10	mA
Output Sink Current					25	mA
Power Dissipation	See Derating Curve	P_D			200	mW
Junction Temperature		T_J			125	°C
Ambient Temperature Range (Operating)		T_{amb}	–25		+85	°C
Storage Temperature Range		T_{stg}	–25		+85	°C
Soldering Temperature	See Recommended Solder Profile			215	240	°C
Average IRED Current		I_{IRED} (DC)			100	mA
Repetitive Pulsed IRED Current	$t < 90\ \mu s$, $t_{on} < 20\%$	I_{IRED} (RP)			500	mA
IRED Anode Voltage		V_{IREDA}	– 0.5		6	V
Transmitter Data Input Voltage		V_{Txd}	– 0.5		V_{CC1}+0.5	V
Receiver Data Output Voltage		V_{Rxd}	– 0.5		V_{CC1}+0.5	V

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Virtual Source Size	Method: (1–1/e) encircled energy	d		2.5	2.8	mm
Maximum Intensity for Class 1	IEC60825–1 or EN60825–1, edition Januar 2001	I_e			*) (500**)	mW/sr

*) The device is a “class 1” device
**) IrDA specifies the max. intensity with 500 mW/sr

Electrical Characteristics

T_{amb} = 25°C, V_{CC} = 2.7 V to 5.5 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameters	Test Conditions / Pins	Symbol	Min.	Typ.	Max.	Unit
Transceiver						
Supply Voltage	Receive Mode Transmit Mode, R2 = 47 Ω (see Recommended Application Circuit)	V_{CC1} V_{CC2}	2.7 2.0		5.5 5.5	V V
Supply Current Pin V_{CC1} (Receive Mode)	V_{CC1} = 5.5 V V_{CC1} = 2.7 V	$I_{CC1\ (Rx)}$		1.3 1.0	2.5 1.5	mA mA
Supply Current Pin V_{CC1} (avg) (Transmit Mode)	I_{IRED} = 210 mA (at IRED Anode Pin) V_{CC1} = 5.5 V V_{CC1} = 2.7 V	$I_{CC1\ (Tx)}$		5.0 3.5	5.5 4.5	mA mA
Leakage Current of IR Emitter, IRED Anode Pin	V_{CC1} = OFF, T_{XD} = LOW, V_{CC2} = 6 V, T = 25 to 85°C	$I_{L\ (IREDA)}$		0.005	0.5	µA
Transceiver Power On Settling Time		T_{PON}		50		µs

Optoelectronic Characteristics

T_{amb} = 25°C, V_{CC} = 2.7 V to 5.5 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Receiver						
Minimum Detection Threshold Irradiance	BER = 10^{-8} (IrDA Specification)					
	α = ±15°, SIR Mode, SC = LOW	E_e		20	35	mW/m^2
	α = ± 15°, SIR Mode, SC = HIGH	E_e	6	10	15	mW/m^2
Maximum Detection Threshold Irradiance	α = ± 90°, SIR Mode, V_{CC1} = 5 V	E_e	3.3	5		kW/m^2
	α = ± 90°, SIR Mode, V_{CC1} = 3 V	E_e	8	15		kW/m^2
Logic LOW Receiver Input Irradiance	SC = HIGH or LOW	E_e			4	mW/m^2
Output Voltage – Rxd	Active, C = 15 pF, R = 2.2 kΩ	V_{OL}		0.5	0.8	V
	Non–active, C = 15 pF, R = 2.2 kΩ	V_{OH}	V_{CC1}–0.5			V
Output Current – Rxd	V_{OL} < 0.8 V	I_{OL}		4		mA
Rise Time – Rxd	C = 15 pF, R = 2.2 kΩ	$t_{r\ (Rxd)}$	20		1400	ns
Fall Time – Rxd	C = 15 pF, R = 2.2 kΩ	$t_{f\ (Rxd)}$	20		200	ns
Pulse Width – Rxd Output	Input pulse width = 1.6 µs, 115.2 kbit/s	t_{PW}	1.41		8	µs
Jitter, Leading Edge of Output Signal	Over a Period of 10 bit, 115.2 kbit/s	t_j			2	µs
Latency		t_L		100	500	µs

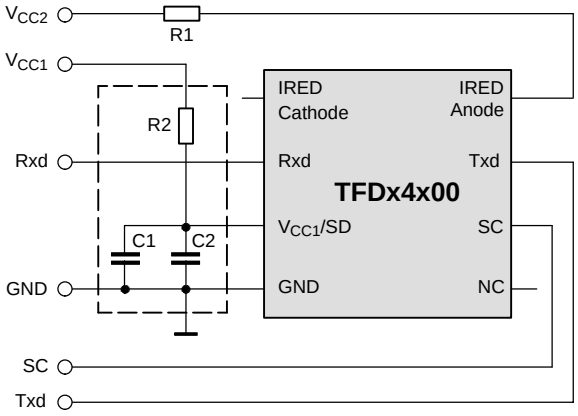
Optoelectronic Characteristics

T_{amb} = 25°C, V_{CC} = 2.7 V to 5.5 V unless otherwise noted.
Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

Parameters	Test Conditions	Symbol	Min.	Typ.	Max.	Unit
Transmitter						
IRED Operating Current	IRED Operating Current can be adjusted by Variation of R1. Current Limiting Resistor is in Series to IRED: R1 = 14 Ω, V_{CC2} = 5.0 V	I_{IRED}		0.2	0.28	A
Logic LOW Transmitter Input Voltage		V_{IL} (Txd)	0		0.8	V
Logic HIGH Transmitter Input Voltage		V_{IH} (Txd)	2.4		V_{CC1}+0.5	V
Output Radiant Intensity	In Agreement with IEC825 Eye Safety Limit, if Current Limiting Resistor is in Series to IRED: R1 = 14 Ω, V_{CC2} = 5.0 V, α = ±15°	I_e	45	140	200	mW/sr
	Txd Logic LOW Level	I_e			0.04	mW/sr
Angle of Half Intensity		a		± 24		°
Peak Wavelength of Emission		λ_P	880		900	nm
Half–Width of Emission Spectrum				60		nm
Optical Rise Time, Fall Time		t_{ropt}, t_{fopt}		200	600	ns
Optical Overshoot					25	%
Rising Edge Peak–to-Peak Jitter of Optical Output Pulse	Over a Period of 10 bits, Independent of Information content				0.2	µs

Recommended Circuit Diagram

The only required components for designing an IrDA 1.2 compatible design using Vishay Semiconductors SIR transceivers are a current limiting resistor to the IRED. However, depending on the entire system design and board layout, additional components may be required (see figure 3). It is recommended that the capacitors C1 and C2 are positioned as near as possible to the transceiver power supply pins. A tantalum capacitor should be used for C1, while a ceramic capacitor should be used for C2 to suppress RF noise. Also, when connecting the described circuit to the power supply, low impedance wiring should be used.



Note: outlined components are optional depending on the quality of the power supply

Figure 3. Recommended Application Circuit

R1 is used for controlling the current through the IR emitter. For increasing the output power of the IRED, the value of the resistor should be reduced. Similarly, to reduce the output power of the IRED, the value of the resistor should be increased. For typical values of R1 (see figures 4 and 5), e.g. for IrDA compliant operation (V_{CC2} = 5 V ± 5%), a current control resistor of 14 Ω is recommended. The upper drive current limitation is dependent on the duty cycle and is given by the absolute maximum ratings on the data sheet and the eye safety limitations given by IEC825–1.
R2, C1 and C2 are optional and dependent on the quality of the supply voltage V_{CC1} and injected noise. An unstable power supply with dropping voltage during transmission may reduce sensitivity (and transmission range) of the transceiver.

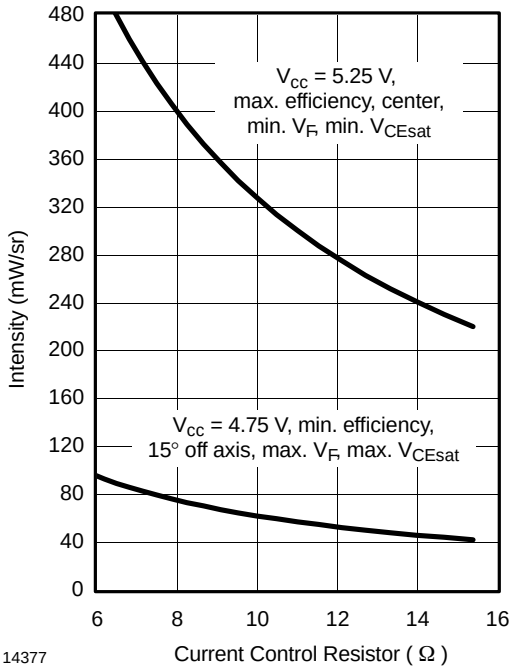


Figure 4. Ie vs. R1

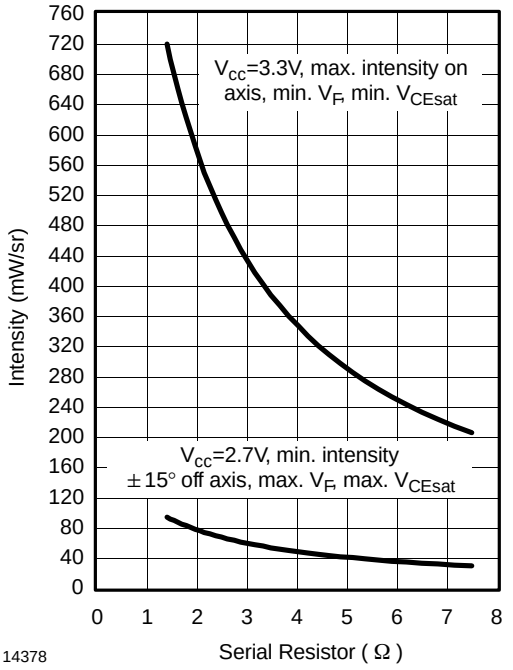


Figure 5. Ie vs. R1

Table 1. Recommended Application Circuit Components

Component	Recommended Value	Vishay Part Number
C1	4.7 µF, Tantalum	293D 475X9 016B 2T
C2	0.1 µF, Ceramic	VJ 1206 Y 104 J XXMT
R1	14 Ω, 0.25 W (recommended using two 7 Ω, 0.125 W resistors in series)	CRCW–1206–7R00–F–RT1
R2	47 Ω , 0.125 W	CRCW–1206–47R0–F–RT1

The sensitivity control (SC) pin allows the minimum detection irradiance threshold of the transceiver to be lowered when set to a logic HIGH. Lowering the irradiance threshold increases the sensitivity to infrared signals and increases transmission range up to 3 meters. However, setting the Pin SC to logic HIGH also makes the transceiver more susceptable to transmission errors due to an increased sensitivity to fluorescent light disturbances. It is recommended to set the Pin SC to logic LOW or left open if the increased range is not required or if the system will be operating in bright ambient light.

The guide pins on the side-view and top-view packages are internally connected to ground but should not be connected to the system ground to avoid ground loops. They should be used for mechanical purposes only and should be left floating.

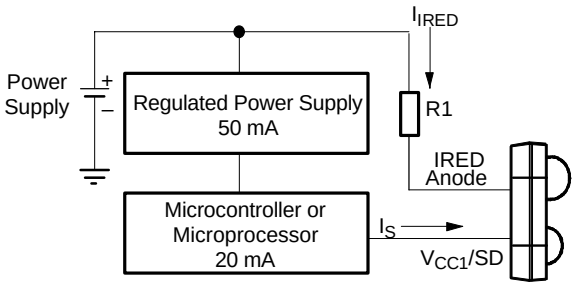
Shutdown

The internal switch for the IRED in Vishay Semiconductors SIR transceivers is designed to be operated like an open collector driver. Thus, the V_{cc2} source can be an unregulated power supply while only a well regulated power source with a supply current of 1.3 mA connected to V_{CC1}/SD is needed to provide power to the remainder of the transceiver circuitry in receive mode. In transmit mode, this current is slightly higher (approximately 4 mA average at 3 V supply current) and the voltage is not required to be kept as stable as in receive mode. A voltage drop of V_{CC1} is acceptable down to about 2.0 V when buffering the voltage directly from the Pin V_{CC1} to GND see figure 3).

This configuration minimizes the influence of high current surges from the IRED on the internal analog control circuitry of the transceiver and the application circuit. Also board space and cost savings can be achieved by eliminating the additional linear regulator normally needed for the IRED's high current requirements.

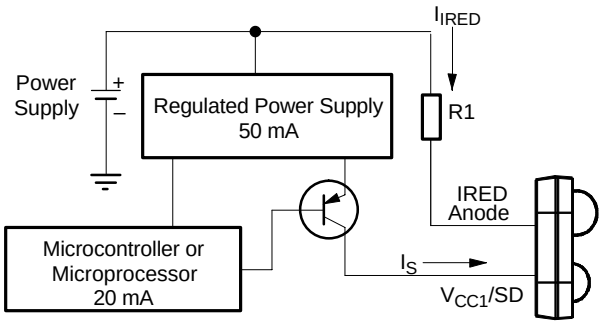
The transceiver can be very efficiently shutdown by keeping the IRED connected to the power supply V_{CC2} but switching off V_{CC1}/SD. The power source to $V_{CC1/SD}$ can be provided directly from a microcontroller (see figure 6). In shutdown, current loss is realized only as leakage current through the current limiting resistor to the IRED (typically 5 nA). The settling time after switching $V_{CC1/SD}$ on again is approximately 50 µs. Vishay Semiconductor's TOIM3232 interface circuit is designed for this shutdown feature. The V_{CC_SD}, S0 or S1 outputs on the TOIM3232 can be used to power the transceiver with the necessary supply current.

If the microcontroller or the microprocessor is unable to drive the supply current required by the transceiver, a low–cost SOT23 pnp transistor can be used to switch voltage on and off from the regulated power supply (see figure 7). The additional component cost is minimal and saves the system designer additional power supply costs.



TFDU4100 (Note: Typical Values Listed)
Receive Mode
@ 5 V: I_{IRED} = 210 mA, I_S = 1.3 mA
@ 2.7 V: I_{IRED} = 210 mA, I_S = 1.0 mA
Transmit Mode
@ 5 V: I_{IRED} = 210 mA, I_S = 5 mA (Avg.)
@ 2.7 V: I_{IRED} = 210 mA, I_S = 3.5 mA (Avg.) 14878

Figure 6.



TFDU4100 (Note: Typical Values Listed)
Receive Mode
@ 5 V: I_{IRED} = 210 mA, I_S = 1.3 mA
@ 2.7 V: I_{IRED} = 210 mA, I_S = 1.0 mA
Transmit Mode
@ 5 V: I_{IRED} = 210 mA, I_S = 5 mA (Avg.)
@ 2.7 V: I_{IRED} = 210 mA, I_S = 3.5 mA (Avg.) 14879

Figure 7.

Recommended SMD Pad Layout

The leads of the device should be soldered in the center position of the pads.

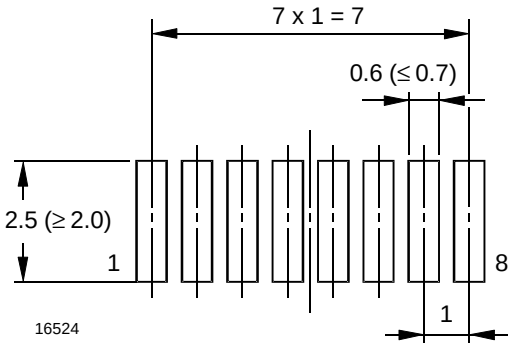


Figure 8. TFDU4100, BabyFace (Universal)
Note: Leads of the device should be at least 0.3 mm within the ends of the pads

Recommended Solder Profile

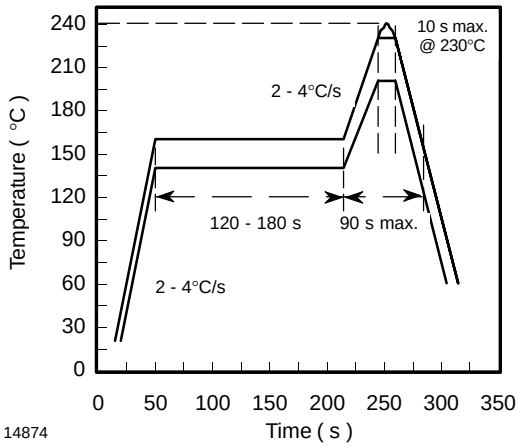


Figure 9. Recommended Solder Profile

Current Derating Diagram

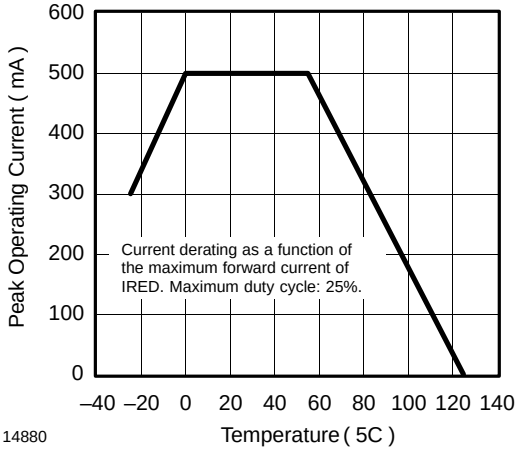
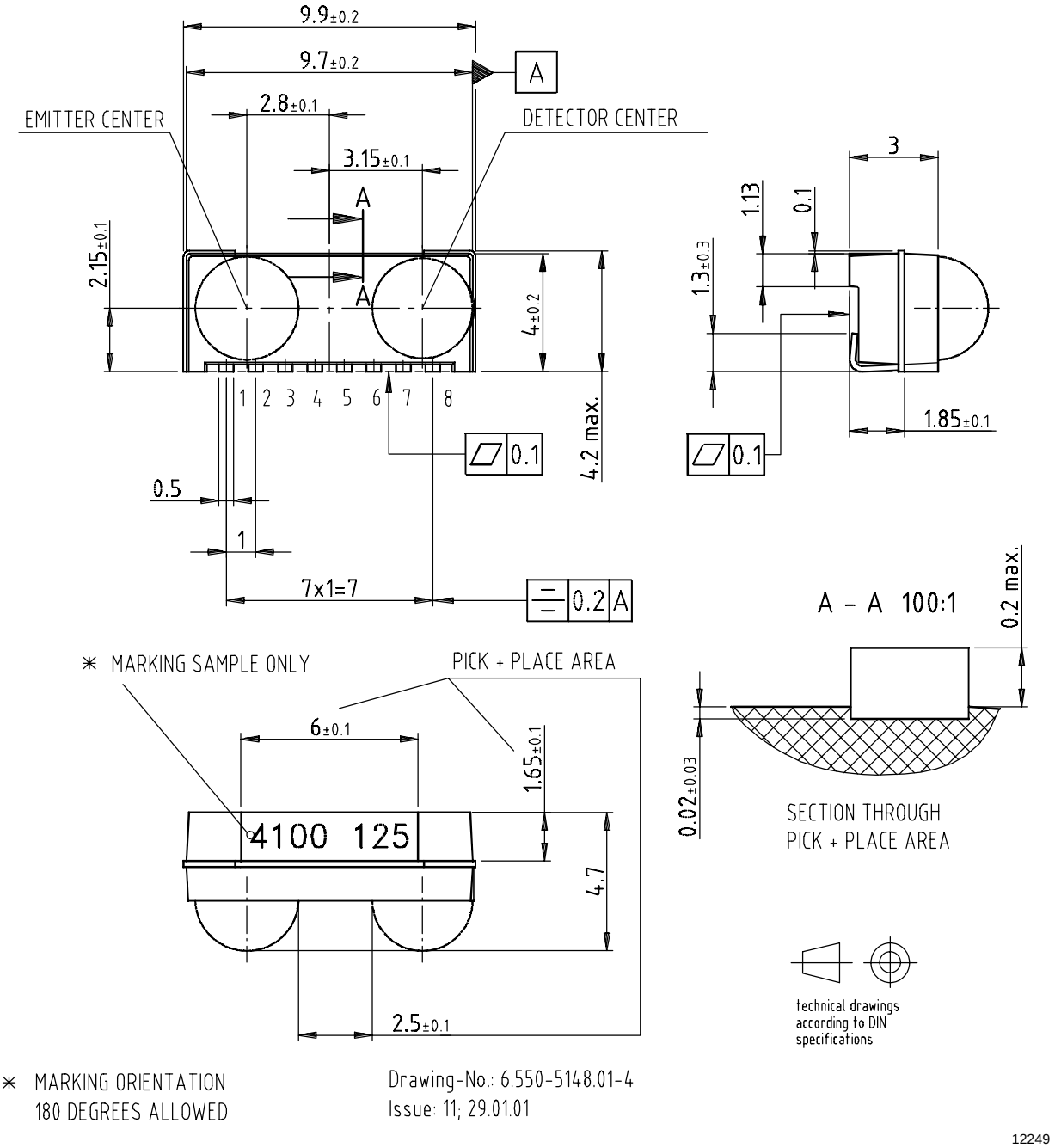


Figure 10. Current Derating Diagram

TFDU4100 – BabyFace (Universal) Package (Mechanical Dimensions)



Revision History:

A1.1, 30/10/2002 Technically unchanged data sheet of TFDU4100 extracted from the latest vers. A1.1 4000–series data sheet.

Ozone Depleting Substances Policy Statement

It is the policy of **Vishay Semiconductor GmbH** to

1. Meet all present and future national and international statutory requirements.

2. Regularly and continuously improve the performance of our products, processes, distribution and operating systems with respect to their impact on the health and safety of our employees and the public, as well as their impact on the environment.

It is particular concern to control or eliminate releases of those substances into the atmosphere which are known as ozone depleting substances (ODSs).

The Montreal Protocol (1987) and its London Amendments (1990) intend to severely restrict the use of ODSs and forbid their use within the next ten years. Various national and international initiatives are pressing for an earlier ban on these substances.

Vishay Semiconductor GmbH has been able to use its policy of continuous improvements to eliminate the use of ODSs listed in the following documents.

1. Annex A, B and list of transitional substances of the Montreal Protocol and the London Amendments respectively

2. Class I and II ozone depleting substances in the Clean Air Act Amendments of 1990 by the Environmental Protection Agency (EPA) in the USA

3. Council Decision 88/540/EEC and 91/690/EEC Annex A, B and C (transitional substances) respectively.

Vishay Semiconductor GmbH can certify that our semiconductors are not manufactured with ozone depleting substances and do not contain such substances.

Vishay Semiconductor GmbH, P.O.B. 3535, D-74025 Heilbronn, Germany
Telephone: 49 (0)7131 67 2831, Fax number: 49 (0)7131 67 2423