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MUNICH128X
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MUNICH128X **Revision History:**		**Current Version: 1997-12-01**
Previous Version:		Product Overview 1997-08-01
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)
7	7	M/bit/s have been changed to MBit/s.
7	7	Configuration Register has been changed to Command Register.
15	15	FALC54LH LUI/framer has been changed to FALC®54/FALC®-LH transceiver.
17	17	Pin Names in Figure 5 have been completely updated.
18	18	Pin Names in Table 1 have been completely updated.
19	19	Pin Names in Table 2 have been completely updated.
20	20	Pin Names in Table 3 have been completely updated.
21	21	Pin Names in Table 4 have been completely updated.
22	22	Pin Names in Table 5 have been completely updated.
27	27	Pin Names in Table 7 have been completely updated.
30, 31, 32	30, 31, 32	DOCI(1:0) has been changed to DPCI(1:0).
35	35	Pin Names in Figure 9 have been completely updated.
38	38	Pin Names in Figure 15 have been completely updated.
		MUNICH32X, MQ32 and MQ32P have been changed to MUNICH128X (whole document).

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1 General Description

The MUNICH128X is a 128-channel WAN Protocol Controller which provides four independent 24/32-channel HDLC controllers, each with a dedicated 64-channel DMA Controller and a Serial PCM Interface Controller. The device is offered in a 160-pin MQFP package, making it ideal for high-port-density applications.

The MUNICH128X provides capability for up to 128 full duplex serial PCM channels. The chip performs layer 2 HDLC formatting/deformatting or V.110 or X.30 protocols up to a data rate of 38.4 kbit/s (V.110) or 64 kbit/s (HDLC). The MUNICH128X also performs transparent transmission for DMI modes 0, 1, and 2. Processed data is transferred to host memory via the PCI interface or de-multiplexed bus interface.

The MUNICH128X is compatible with the LAPD ISDN (Integrated Services Digital Network) protocol specified by CCITT, as well as with HDLC, SDLC, LAPB and DMI protocols. It provides rate adaptation for time slot transmission from 64 kbit/s down to 8 kbit/s and the concatenation of time slots, supporting the ISDN H0, H11, H12 superchannels.

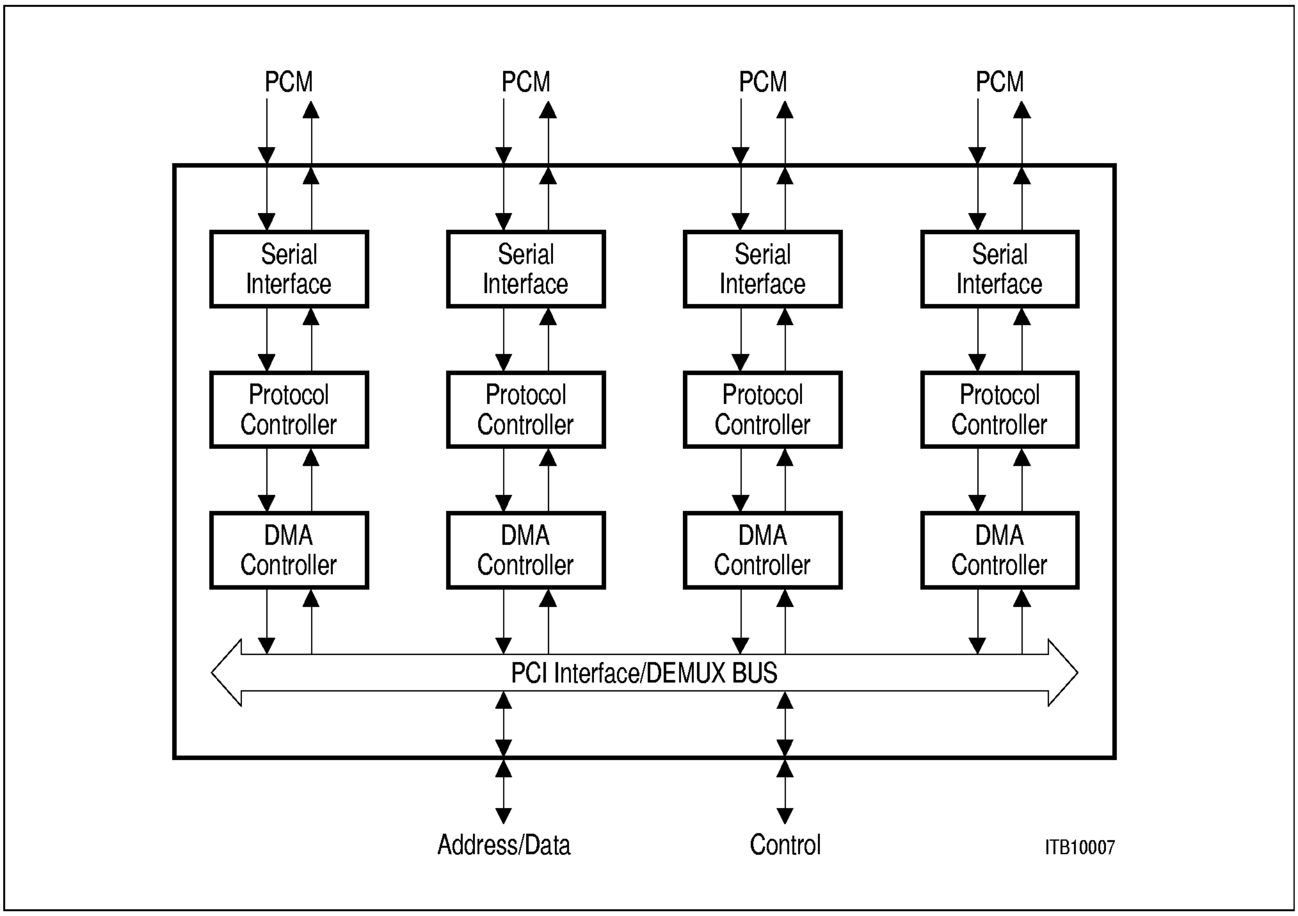


Figure 1 Simplified Block Diagram

1.1 Features

Four Independent 24/32-Channel HDLC Controllers
Each of them provides:

- Dedicated 256 byte Tx Buffer
- Dedicated 256 byte Rx Buffer
- Dedicated Serial PCM Interface Controller
  – T1 rates: 1.536, 1.544, 3.088, 6.176 Mbit/s
  – E1 rates: 2.048, 4.096, 8.192 Mbit/s
- Dedicated 64-channel DMA Controller
  – Supports linked-list buffer processing
  – 16-DWord Tx DMA FIFO
  – 16-DWord Rx DMA FIFO
  – 4-DWord burst of Rx descriptors
  – 3-DWord burst of Tx descriptors
  – n-DWord burst of configuration blocks
  (n is unlimited according the MUNICH128X, but internal port arbitration may lead to a lower typical burst size of 4 or 8 DWords)
- Programmable via Register Set

32 Bit / 33 MHz PCI 2.1 Interface

32 Bit / 33 MHz De-multiplexed Bus Interface Option

0.35 µm, 3.3 V-Optimized Technology

3.3 V I/O Capability with 5.0 V Input Tolerance

160-pin MQFP Package

1.2 Differences from the MUNICH32

- 128-channel capability
- Symmetrical Rx and Tx Buffer Descriptor formats for faster switching
- Improved Tx idle channel polling process for significantly reducing bus occupancy of idle Tx channels
- Additional PCM modes supported: 3.088 MBit/s, 6.176 MBit/s, 8.192 MBit/s
- 32 Bit / 33 MHz PCI 2.1 master/slave interface;
  this interface can be configured in De-mux mode
- Separate Rx and Tx Status Queues in host memory
  (the MUNICH128X provides one set for each of the four HDLC Controllers)
- Slave access to on-chip registers
- Time Slot-shift capability:
  - Programmable from -4 clock edges to +3 clock edges relative to the synchronization pulse
  - Programmable to sample Tx and/or Rx data at either falling or rising edge of clock
- Software initiated action request (via the Command Register)
- Tx End-of-Packet transmitted-on-wire interrupt capability for each channel
- Tx packet size increased to 64 Kbytes (HDLC mode)
- Rx packet size 8 Kbyte limit interrupt disable
- Tx data TRISTATE™ control line
- Synchronized data transfer in TMA mode
  for complete transparency when using fractional T1/PRI
- Little/Big Endian data formats

2 Operational Overview

The MUNICH128X is a “channelized” WAN protocol controller that performs protocol processing on up to 128 full duplex serial PCM channels. It performs HDLC-based layer 2 protocol formatting and deformatting, as well as rate adaptation, for each of the 128 channels independently.

The MUNICH128X provides dedicated registers for each of the four HDLC controllers, with each set similar to the “core” registers of the MUNICH32X. Software developed for the “core” of the MUNICH32X requires minimal modification to run optimally on the MUNICH128X. The architecture of the register sets allows any number of HDLC controllers within an MUNICH128X device to operate with host software images that differ only in their offset from the PCI base address and their pointers into host memory.

Host software sets the operating mode, rate adaptation method and time slot assignment of each channel by configuring “blocks” (CCBs) within host memory.

During “run-time” the MUNICH128X performs all data and descriptor transfers as a bus master. Additionally, host software may access any register of a particular HDLC Controller within the MUNICH128X, with the device acting as a bus slave.

The MUNICH128X provides a single Status Register, which maintains information of all interrupt events for the controller.

3 Functional Block Description

The MUNICH128X provides four independent “cores” as well as global functional blocks (see **Figure 2**).

3.1 Core Functional Blocks

Each core consists of dedicated circuitry: Serial PCM Interface Controller, Configuration and State RAM (CSR), 24/32-channel HDLC Controller with internal Transmit and Receive Buffers, 64-Channel DMA Controller, and Register Set.

3.1.1 Serial PCM Interface Controller

This block controls both Parallel–to-Serial (Tx) and Serial-to-Parallel (Rx) conversion and PCM timing. Additionally, this block controls the multiplexing of channels through the HDLC controller, as well as switching for the test loops.

3.1.2 Configuration and State RAM (CSR)

This block contains internal RAM which maintains the state of each channel. The Multiplex Control Block of the Serial PCM Interface Controller handles the switching of the CSR information into and out of the 24/32-channel HDLC Controller.

3.1.3 24/32-channel HDLC Controller

The HDLC Controller performs protocol processing for each channel independently, based on the CSR information for each channel.

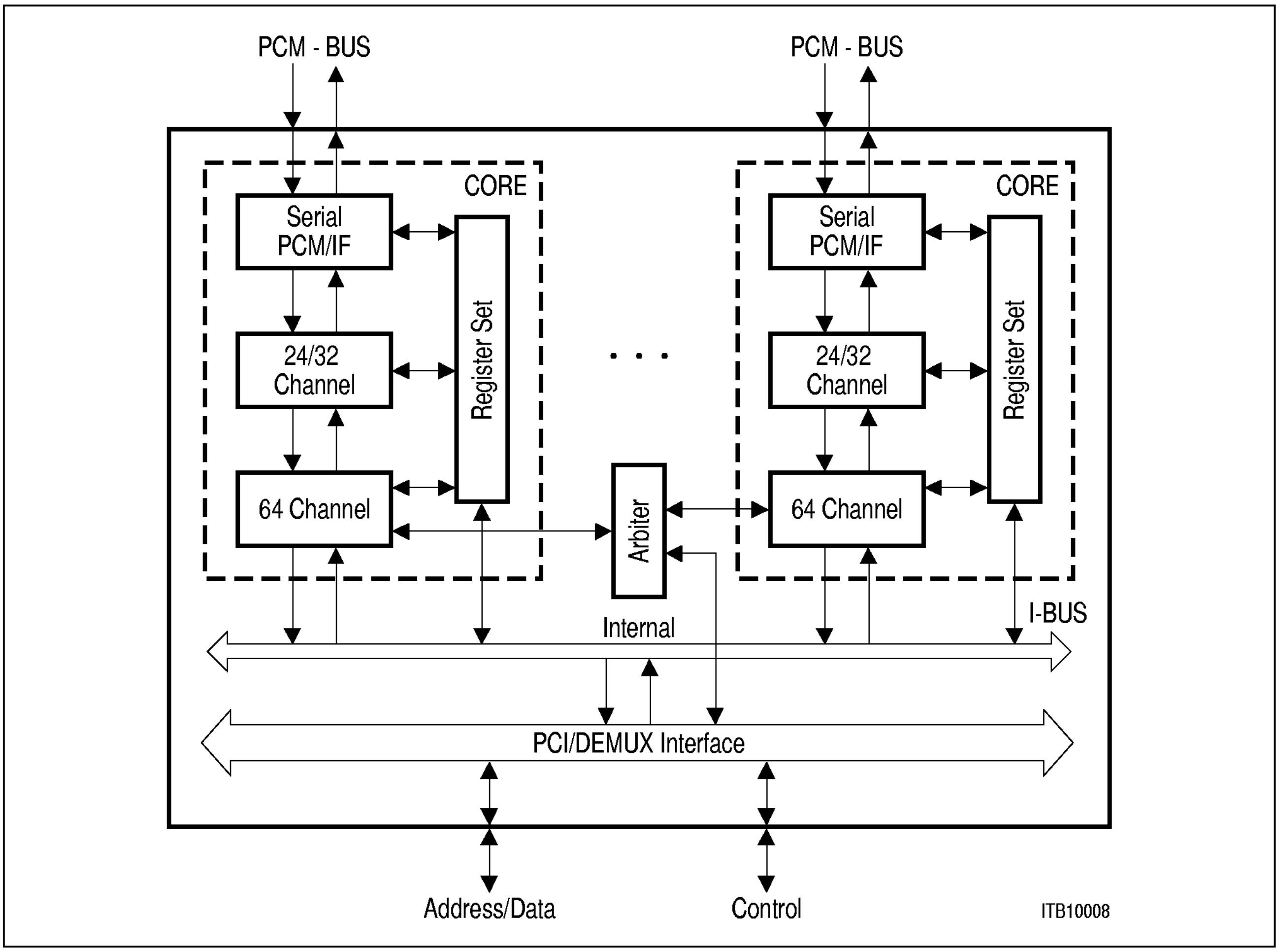


Figure 2 Functional Block Diagram

3.1.3.1 Tx Block

Transmit Buffer (TB)

The Tx Block of the HDLC Controller contains a 256 byte buffer (TB) which may be allocated to all 32 channels of one cove equally (i.e., 2-DWords per channel) or may be allocated based on superchannel considerations (e.g., 8–DWords per channel for 8 channels).

HDLC Protocol

Bit stuffing, flag generation, flag stuffing and adjustment, and CRC generation (either 16-bit or 32-bit) are performed.

V.110 and V.30 Protocol

Bit framing from 600 bit/s to 38.4 Kbit/s, automatic generation of the synchronization pattern, generation of loss of synchronization, programmable E/SX bits (including during run-time) are performed.

Transparent Mode A

This mode supports slot synchronous, transparent transmission without frame structure. It provides flag generation, flag stuffing, flag generation in the abort case with programmable flag, and synchronized data transfer for fractional T1/E1 PRI applications.

Transparent Mode B

This mode supports transparent transmission in frames delimited by 00_H flags, shared closing and opening flag, flag stuffing and flag generation in the abort case.

Transparent Mode R

This mode supports transparent transmission with GSM 08.60 frame structure with automatic 0000_H flag generation and support of 40, 39.5, and 40.5 octet frames.

Protocol Independence

Channel inversion (data, flags, idle code) follows the format conventions as in CCITT Q.921.

3.1.3.2 Rx Block

Receive Buffer (RB)

The Rx Block of the HDLC Controller contains a 256 byte buffer (RB) which is allocated to channels via requests from the protocol controller, as determined by the received data for each channel.

HDLC Protocol

Flag detection (supports multiple flags between packets or a single flag shared as a closing flag and an opening flag between packets), abort character detection, idle code detection, zero-bit detection and deletion, packet length count, and CRC checking (either 16-bit or 32-bit) are performed.

V.110 and V.30 Protocol

Bit framing from 600 bit/s to 38.4 Kbit/s, automatic synchronization of the synchronization pattern, detection of loss of synchronization, programmable E/SX bits (including during run–time) are performed.

Transparent Mode A

Mode A supports slot synchronous transparent reception without frame structure. It provides flag detection, flag extraction and synchronized data transfer for fractional T1/E1 PRI applications.

Transparent Mode B

This mode supports transparent reception in frames delimited by 00_H flags. Sharing closing flag and opening flag, and flag detection.

Transparent Mode R

This mode supports transparent reception with GSM 08.60 frame structure with automatic 0000_H flag detection. Support of 40, 39.5, and 40.5 octet frames, and error detection (non–octet frame contents, short frame, long frame).

Protocol Independence

Channel inversion (data, flags, idle code) follows the format conventions as in CCITT Q.921, data overflow and underflow detection.

3.1.3.3 64-channel DMA Controller Block

This block controls memory address calculation, buffer management (including linked-lists) and interrupt processing. The 24/32-channel HDLC Controller has a dedicated DMA channel for each channel and direction. During run-time, the DMA Controller performs operations with host memory primarily as a bus master. This block provides 32 input and 32 output channels.

3.1.3.4 Register Set

This block provides configuration and control of the Serial PCM Interface Controller, the HDLC Controller and the DMA Controller. Also, a shared status register STAT provides status and interrupt information associated with each of the four cores.

3.2 Global Functional Blocks

The MUNICH128X provides global functional blocks for the Internal Bus, Arbiter, and 32 Bit / 33 MHz PCI 2.1 Interface as well as De-multiplexed Bus Interface Controller.

3.2.1 Internal Bus

This block of the MUNICH128X interfaces the Bus Interface Controller to the four DMA Controllers. This is a 33 MHz, 32 Bit demultiplexed bus that operates in a synchronous, non–burst manner for data transfers and operates in a synchronous burst manner for descriptor transfers.

3.2.2 Arbiter

The Arbiter provides access control of the Internal Bus. A "round-robin" Arbiter is used which provides "fairness" for the four master DMA controllers.

3.2.3 32 Bit / 33 MHz Bus Interface Controller

The MUNICH128X may be configured either for 32 Bit / 33 MHz PCI bus operation or for a 32 Bit / 33 MHz De-multiplexed bus interface. The MUNICH128X input pins DPCI(1:0) are used to select the desired configuration.

The De-multiplexed bus interface is a synchronous interface very similar to the PCI interface with the following exceptions:

1. The W/$\overline{R}$ input/output signal replaces the function of the PCI command nibble of the C/BE(3:0) bit field.
2. Note, that in DEMUX mode as in PCI mode the MUNICH128X provides only the first address of a Master burst read or write transaction. If burst transactions are not supported by the local bus environment, burst capability can be disabled by bit DBE in the global configuration register (CONF).

4 System Integration

The MUNICH128X provides protocol processing and host memory buffer management for four independent T1/E1 PRI ports. As such, the MUNICH128X fits into a system between the framer or LIU/framer devices (e.g., the Siemens FALC®54/FALC®54-LH transceiver) and the host bus (e.g. PCI Bus), as illustrated in **Figure 3**.

The MUNICH128X provides four independent Serial PCM ports which connect directly into the framer devices. In PCI based systems a dedicated microcontroller or PCI bridge chip is necessary to configure the framer or LIU/framer devices.

Additionally, the MUNICH128X provides a PCI 2.1 interface which connects directly to the system PCI bus. Optionally, this bus can be configured in De-multiplexed Mode.

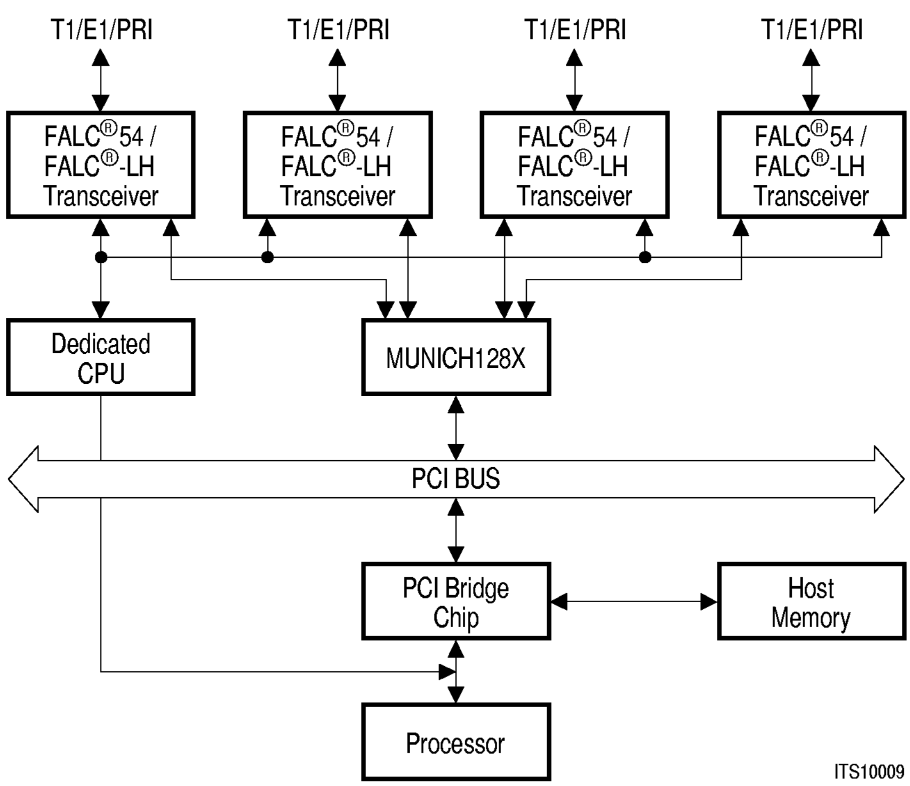


Figure 3 System Integration of the MUNICH128X in PCI-Based System

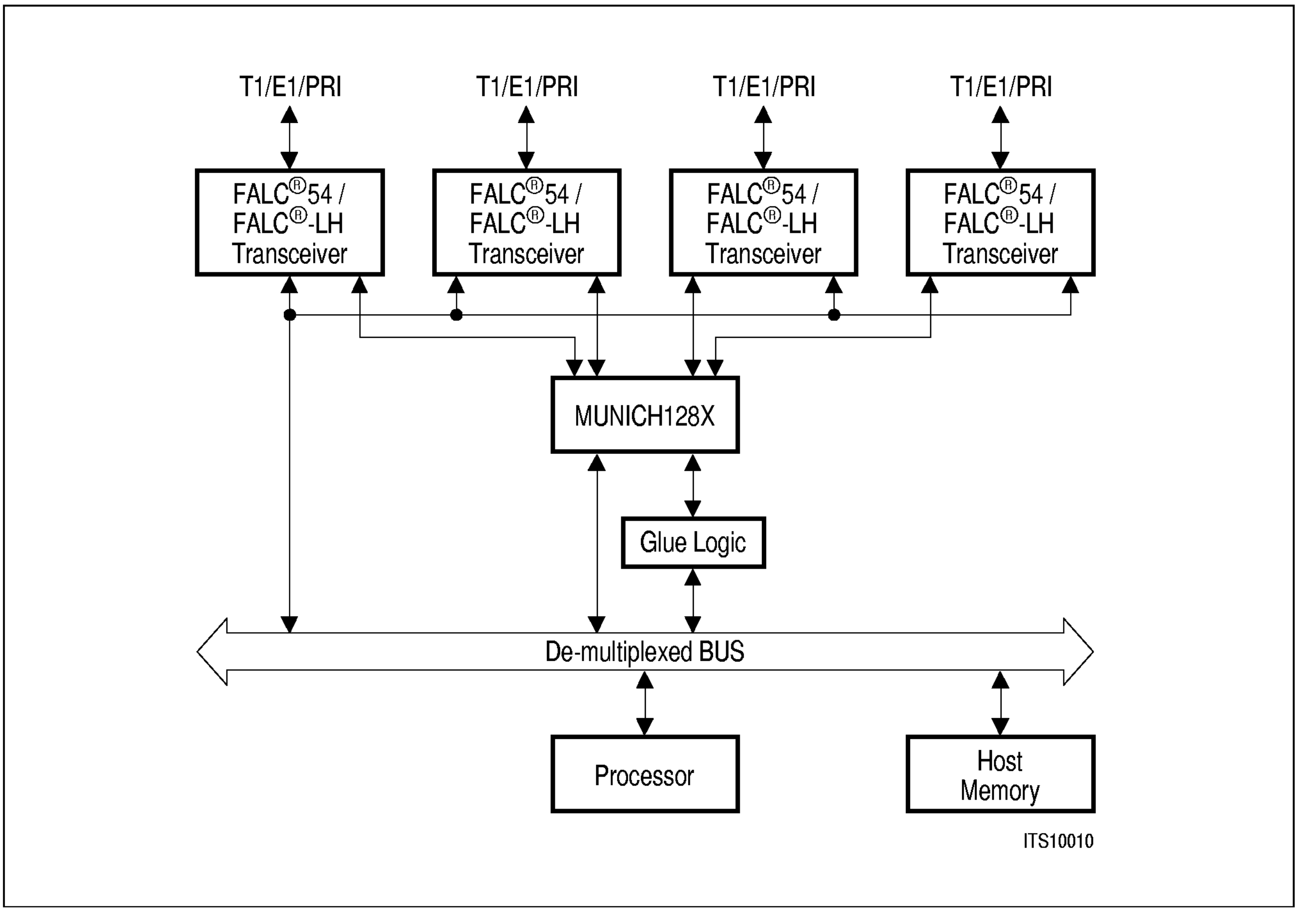


Figure 4 System Integration of the MUNICH128X in De-multiplexed System

5 Pin Descriptions

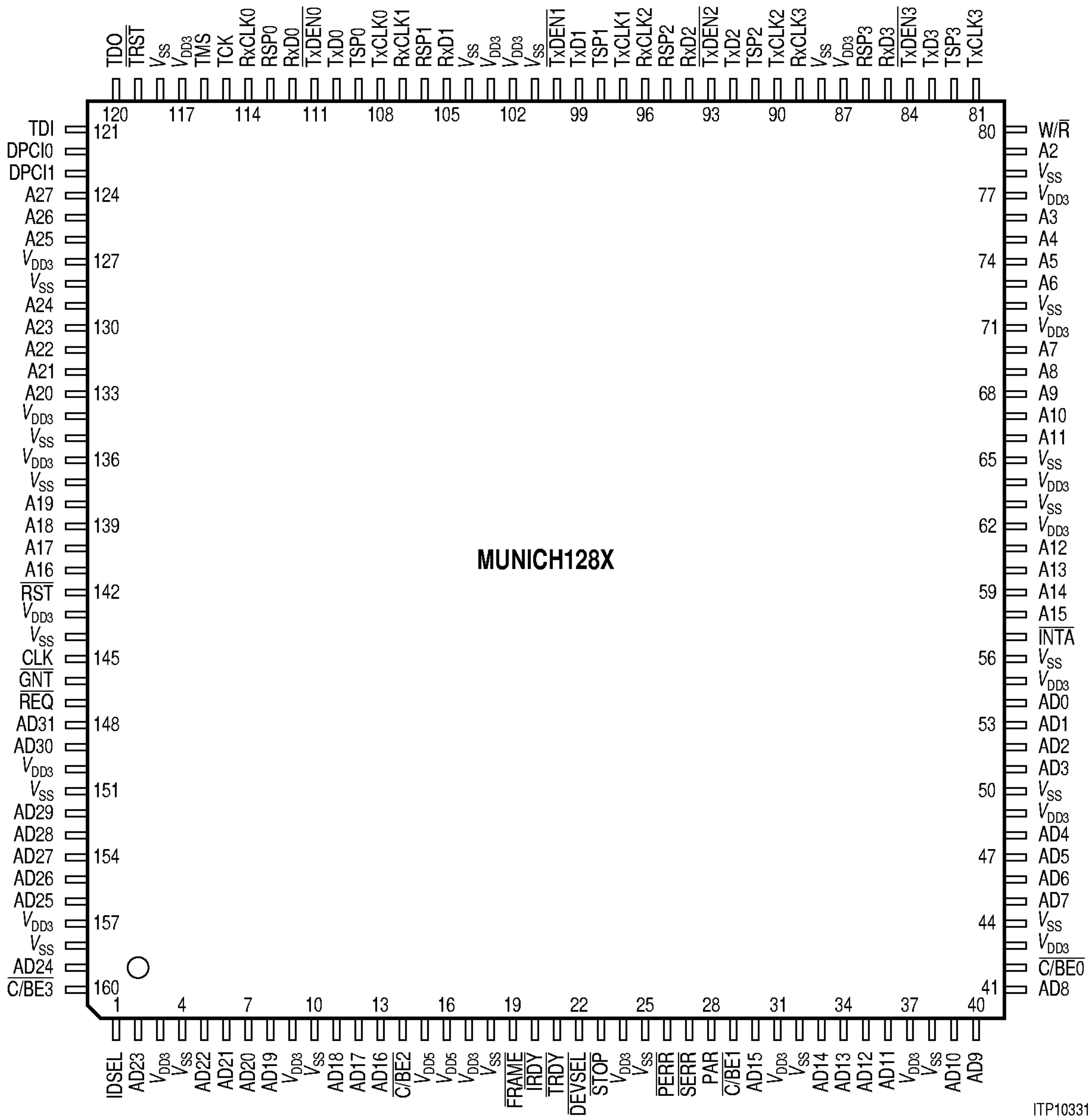


Figure 5 Pin Assignments for the MUNICH128X

Pin descriptions in **Tables 1 - 8** are grouped by functional block, as shown by the heading for that group. Pin types are indicated by abbreviations: Input (I), Output (O), Open Drain (o/d), Input/Output (I/O), Tri-State (t/s), sustained Tri-State (s/t/s).

Table 1 Pin Descriptions by Functional Block
Port 0 Serial Interface

Pin No.	Symbol	Type	Description
114	RxCLK0	I	**Receive Clock 0** The clock input pin used for sampling the data on RxD0. The MUNICH128X supports the following PCM clock rates; programmed via the MODE1 register: T1: 1.536 MHz, 1.544 MHz, 3.088 MHz, 6.176 MHz; E1: 2.048 MHz, 4.096 MHz, 8.192 MHz.
112	RxD0	I	**Receive Data 0** The data input pin which is sampled using RxCLK0.
113	RSP0	I	**Receive Synchronization Pulse 0** The input pin used for Rx PCM frame synchronization; the synchronization pulse marks the *first* bit in the PCM frame.
108	TxCLK0	I	**Transmit Clock 0** The clock input used for clocking out the data on TxD0. In most applications, the signal that drives this pin is externally connected to RxCLK0.
110	TxD0	O	**Transmit Data 0** Provides the data which is clocked out of the MUNICH128X by TxCLK0; data is push-pull for active bits in the PCM frame and TRISTATE™ for inactive bits.
109	TSP0	I	**Transmit Synchronization Pulse 0** The input pin used for Tx PCM frame synchronization; the synchronization pulse marks the *last* bit in the PCM frame.
111	$\overline{\text{TxDEN0}}$	O	**Transmit Data Enable 0** An active low output signal which specifies data on the TxD0 output pin is valid.

Table 2 Pin Descriptions by Functional Block
Port 1 Serial Interface

Pin No.	Symbol	Type	Description
107	RxCLK1	I	**Receive Clock 1** The clock input pin used for sampling the data on RxD1 The MUNICH128X supports the following PCM clock rates, programmed via the MODE1 register: T1: 1.536 MHz, 1.544 MHz, 3.088 MHz, 6.176 MHz; E1: 2.048 MHz, 4.096 MHz, 8.192 MHz.
105	RxD1	I	**Receive Data 1** The data input pin which is sampled using RxCLK1.
106	RSP1	I	**Receive Synchronization Pulse 1** The input pin used for Rx PCM frame synchronization; the synchronization pulse marks the *first* bit in the PCM frame.
97	TxCLK1	I	**Transmit Clock 1** The clock input used for clocking out the data on TxD1. In most applications, the signal that drives this pin is externally connected to RxCLK1.
99	TxD1	O	**Transmit Data 1** Provides the data which is clocked out of the MUNICH128X by TxCLK1; data is push-pull for active bits in the PCM frame and TRISTATE™ for inactive bits.
98	TSP1	I	**Transmit Synchronization Pulse 1** The input pin used for Tx PCM frame synchronization; the synchronization pulse marks the *last* bit in the PCM frame.
100	$\overline{\text{TxDEN1}}$	O	**Transmit Data Enable 1** An active low output signal which specifies data on the TxD1 output pin is valid.

Table 3 Pin Descriptions by Functional Block
Port 2 Serial Interface

Pin No.	Symbol	Type	Description
96	RxCLK2	I	**Receive Clock 2** The clock input pin used for sampling the data on RxD2. The MUNICH128X supports the following PCM clock rates, programmed via the MODE1 register: T1: 1.536 MHz, 1.544 MHz, 3.088 MHz, 6.176 MHz; E1: 2.048 MHz, 4.096 MHz, 8.192 MHz.
94	RxD2	I	**Receive Data 2** The data input pin which is sampled using RxCLK2.
95	RSP2	I	**Receive Synchronization Pulse 2** The input pin used for Rx PCM frame synchronization; the synchronization pulse marks the *first* bit in the PCM frame.
90	TxCLK2	I	**Transmit Clock 2** The clock input used for clocking out the data on TxD2. In most applications, the signal that drives this pin is externally connected to RxCLK2.
92	TxD2	O	**Transmit Data 2** Provides the data which is clocked out of the MUNICH128X by TxCLK2; data is push-pull for active bits in the PCM frame and TRISTATE™ for inactive bits.
91	TSP2	I	**Transmit Synchronization Pulse 2** The input pin used for Tx PCM frame synchronization; the synchronization pulse marks the *last* bit in the PCM frame.
93	$\overline{\text{TxDEN2}}$	O	**Transmit Data Enable 2** An active low output signal which specifies data on the TxD2 output pin is valid.

Table 4 Pin Descriptions by Functional Block
Port 3 Serial Interface

Pin No.	Symbol	Type	Description
89	RxCLK3	I	**Receive Clock 3** The clock input pin used for sampling the data on RxD3. The MUNICH128X supports the following PCM clock rates, programmed via the MODE1 register: T1: 1.536 MHz, 1.544 MHz, 3.088 MHz, 6.176 MHz; E1: 2.048 MHz, 4.096 MHz, 8.192 MHz.
85	RxD3	I	**Receive Data 3** The data input pin which is sampled using RxCLK3.
86	RSP3	I	**Receive Synchronization Pulse 3** The input pin used for Rx PCM frame synchronization; the synchronization pulse marks the *first* bit in the PCM frame.
81	TxCLK3	I	**Transmit Clock 3** The clock input used for clocking out the data on TxD3. In most applications, the signal that drives this pin is externally connected to RxCLK3.
83	TxD3	O	**Transmit Data 3** Provides the data which is clocked out of the MUNICH128X by TxCLK3; data is push-pull for active bits in the PCM frame and TRISTATE™ for inactive bits.
82	TSP3	I	**Transmit Synchronization Pulse 3** The input pin used for Tx PCM frame synchronization; the synch. pulse marks the *last* bit in the PCM frame.
84	$\overline{\text{TxDEN3}}$	O	**Transmit Data Enable 3** An active low output signal which specifies data on the TxD3 output pin is valid.

Table 5 Pin Descriptions by Functional Block PCI Interface

Pin No.	Symbol	Type	Description
2, 5…8, 11…13, 30, 33…36, 39…41, 45…48, 51…54, 148, 149, 152…156, 159	AD(31:0)	t/s	**Address/Data Bus** A bus transaction consists of an address phase followed by one or more data phases. When MUNICH128X is Master, AD(31:0) are outputs in the address phase of a transaction. During the data phases, AD(31:0) remain outputs for write transactions, and become inputs for read transactions. When MUNICH128X is Slave, AD(31:0) are inputs in the address phase of a transaction. During the data phases, AD(31:0) remain inputs for write transactions, and become outputs for read transactions. AD(31:0) is sampled on the rising edge of CLK.
14, 29, 42, 160	$\overline{\text{C/BE}}$(3:0)	t/s	**Command/Byte Enable** During the address phase of a transaction, $\overline{\text{C/BE}}$(3:0) define the bus command. During the data phase, $\overline{\text{C/BE}}$(3:0) are used as Byte Enables. The Byte Enables are valid for the entire data phase and determine which byte lanes carry meaningful data. $\overline{\text{C/BE0}}$ applies to byte 0 (lsb) and $\overline{\text{C/BE3}}$ applies to byte 3 (msb). When MUNICH128X is Master, $\overline{\text{C/BE}}$(3:0) are outputs. When MUNICH128X is Slave, $\overline{\text{C/BE}}$(3:0) are inputs. $\overline{\text{C/BE}}$(3:0) is sampled on the rising edge of CLK.
28	PAR	t/s	**Parity** PAR is even parity across AD(31:0) and $\overline{\text{C/BE}}$(3:0). PAR is stable and valid one clock after the address phase. PAR has the same timing as AD(31:0) but delayed by one clock. When MUNICH128X is Master, PAR is output during address phase and write data phases. When MUNICH128X is Slave, PAR is output during read data phases. Parity errors detected by the MUNICH128X are indicated on $\overline{\text{PERR}}$ output. PAR is sampled on the rising edge of CLK.

Table 5 Pin Descriptions by Functional Block (cont'd)
PCI Interface

Pin No.	Symbol	Type	Description
19	FRAME	s/t/s	**Frame** FRAME indicates the beginning and end of an access. FRAME is asserted to indicate a bus transaction is beginning. While FRAME is asserted, data transfers continue. When FRAME is deasserted, the transaction is in the final phase. When MUNICH128X is Master, FRAME is an output. When MUNICH128X is Slave, FRAME is an input. FRAME is sampled on the rising edge of CLK.
20	IRDY	s/t/s	**Initiator Ready** IRDY indicates the bus master's ability to complete the current data phase of the transaction. It is used in conjunction with TRDY. A data phase is completed on any clock where both IRDY and TRDY are sampled asserted. During a write, IRDY indicates that valid data is present on AD(31:0). During a read, it indicates the master is prepared to accept data. Wait cycles are inserted until both IRDY and TRDY are asserted together. When MUNICH128X is Master, IRDY is an output. When MUNICH128X is Slave, IRDY is an input. IRDY is sampled on the rising edge of CLK.
21	TRDY	s/t/s	**Target Ready** TRDY indicates a slave's ability to complete the current data phase of the transaction. During a read, TRDY indicates that valid data is present on AD(31:0). During a write, it indicates the target is prepared to accept data. When MUNICH128X is Master, TRDY is an input. When MUNICH128X is Slave, TRDY is an output. TRDY is sampled on the rising edge of CLK.
23	STOP	s/t/s	**STOP** STOP is used by a slave to request the current master to stop the current bus transaction. When MUNICH128X is Master, STOP is an input. When MUNICH128X is Slave, STOP is an output. STOP is sampled on the rising edge of CLK.

Table 5 Pin Descriptions by Functional Block (cont'd)
PCI Interface

Pin No.	Symbol	Type	Description
1	IDSEL	I	**Initialization Device Select** When MUNICH128X is slave in a transaction, if IDSEL is active in the address phase and $\overline{\text{C/BE}}$(3:0) indicates a Config read or write, the MUNICH128X assumes a read or write to a configuration register. In response, the MUNICH128X asserts $\overline{\text{DEVSEL}}$ during the subsequent CLK cycle. IDSEL is sampled on the rising edge of CLK.
22	$\overline{\text{DEVSEL}}$	s/t/s	**Device Select** When activated by a slave, it indicates to the current bus master that the slave has decoded its address as the target of the current transaction. If no bus slave activates $\overline{\text{DEVSEL}}$ within six bus CLK cycles, the master should abort the transaction. When MUNICH128X is Master, $\overline{\text{DEVSEL}}$ is input. If $\overline{\text{DEVSEL}}$ is not activated within six clock cycles after an address is output on AD(31:0), the MUNICH128X aborts the transaction and generates an $\overline{\text{INTA}}$. When MUNICH128X is Slave, $\overline{\text{DEVSEL}}$ is output.
26	$\overline{\text{PERR}}$	s/t/s	**Parity Error** When activated, indicates a parity error over the AD(31:0) and $\overline{\text{C/BE}}$(3:0) signals (compared to the PAR input). It has a delay of one CLK cycle with respect to AD and $\overline{\text{C/BE}}$(3:0) (i.e., it is valid for the cycle immediately following the corresponding PAR cycle). $\overline{\text{PERR}}$ is asserted relative to the rising edge of CLK.
27	$\overline{\text{SERR}}$	o/d	**System Error** The MUNICH128X asserts this signal to indicate a fatal system error. $\overline{\text{SERR}}$ is sampled on the rising edge of CLK.
147	$\overline{\text{REQ}}$	t/s	**Request** Used by the MUNICH128X to request control of the PCI. $\overline{\text{REQ}}$ is sampled on the rising edge of CLK.

Table 5 Pin Descriptions by Functional Block (cont'd)
PCI Interface

Pin No.	Symbol	Type	Description
146	$\overline{\text{GNT}}$	t/s	**Grant** This signal is asserted by the arbiter to grant control of the PCI to the MUNICH128X in response to a bus request via $\overline{\text{REQ}}$. After $\overline{\text{GNT}}$ is asserted, the MUNICH128X will begin a bus transaction only after the current bus Master has deasserted the $\overline{\text{FRAME}}$ signal. $\overline{\text{GNT}}$ is sampled on the rising edge of CLK.
145	CLK	I	**Clock** Provides timing for all PCI transactions. Most PCI signals are sampled or output relative to the rising edge of CLK. The maximum CLK frequency is 33 MHz.
142	$\overline{\text{RST}}$	I	**Reset** An active $\overline{\text{RST}}$ signal brings all PCI registers, sequencers and signals into a consistent state. All PCI output signals are driven to their initial state.
57	$\overline{\text{INTA}}$	O (o/d)	**Interrupt Request** When an interrupt status is active and unmasked, the MUNICH128X activates this open-drain output. Examples of interrupt sources are transmission/reception error, completion of transmit or receive packets etc. The MUNICH128X deactivates $\overline{\text{INTA}}$ when the global interrupt status register STAT is read. $\overline{\text{INTA}}$ is activated/deactivated asynchronous to the CLK.

Table 6 Pin Descriptions by Functional Block
DEMUX Interface (additional signals to PCI Interface)

Pin No.	Symbol	Type	Description
122, 123	DPCI(1:0)	I	**PCI/De-multiplexed Mode select** DPCI(1:0) = 00_2 : PCI Mode DPCI(1:0) = 01_2 : reserved DPCI(1:0) = 10_2 : PCI/De-multiplexed Mode DPCI(1:0) = 11_2 : reserved
58…61, 66…70, 73…76, 79, 124…126, 129…133, 138…141	A(27:2)	I/O	**DEMUX Address Bus** These pins provide the address bus for the De-multiplexed Interface, when DPCI(1:0) = 10_2.
80	W/$\overline{R}$	I/O	**Write/Read** This signal distinguishes write and read operations in the De-multiplexed mode. It is tristate when the MUNICH128X is in PCI mode.

Table 7 Pin Descriptions by Functional Block Power Supply

Pin No.	Symbol	Type	Description
4, 10, 18, 25, 32, 38, 44, 50, 56, 63, 65, 72, 78, 88, 101, 104, 118, 128, 135, 137, 144, 151, 158	V_{SS}	-	**Ground (0 V)** All pins must have the same reference level.
3, 9, 17, 24, 31, 37, 43, 49, 55, 62, 64, 71, 77, 87, 102, 103, 117, 127, 134, 136, 143, 150, 157	V_{DD3}	-	**Supply Voltage (3.3 V ± 0.3 V)** All pins must have the same reference level.
15, 16	V_{DD5}	-	**Supply Voltage** These pins MUST be supplied with 5 V. The MUNICH128X uses 3.3 V I/O pads that always require 5 V. The 5 V power allows the MUNICH128X I/O pads to provide 5 V input tolerance.

Table 8 Pin Descriptions by Functional Block Test

Pin No.	Symbol	Type	Description
115	TCK	I	JTAG Test Clock
116	TMS	I	JTAG Test Mode Select
121	TDI	I	JTAG Test Data Input
120	TDO	O	JTAG Test Data Output
119	$\overline{\text{TRST}}$	I	JTAG Reset

6 Electrical Specifications

It must be guaranteed during all power-up and power failure situations of the MUNICH128X, that the difference between V_{DD5} and V_{DD3} never exceeds 3.6 V.

Note, therefore, that the following conditions apply to the MUNICH128X:

- V_{DD3} slope < 0.4 V/µs, and V_{DD3} voltage breakdown
  or switch off > 20 ns combined with a V_{DD3} voltage breakdown to 0 V will cause a power-on reset to the boundary scan state machine.
  V_{DD3} voltage breakdowns < 5 ns ***or*** V_{DD3} voltage breakdowns to 2.6 V will *not* cause a power-on reset to the boundary scan state machine.
- V_{DD3} slope > 0.5 V/µs, and V_{DD3} voltage breakdowns between 5 ns and 20 ns *or* V_{DD3} voltage breakdowns to a voltage between 0 V and 2.6 V will result in a non-specified device behavior for boundary scan and normal operation.

6.1 Absolute Maximum Ratings

Table 9 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Ambient temperature under bias	T_A	0	70	°C
Storage temperature	T_{stg}	– 65	125	°C
Voltage at any pin with respect to ground	V_S	– 0.4	V_{DD5} + 0.4	V

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.2 DC Characteristics

a) Non-PCI Interface Pins

Table 10 Non-PCI Interface Pins
T_A = 0 to + 70°C; V_{DD5} = 5 V ± 5%, V_{DD3} = 3.3 V ± 0.3 V, V_{SS} = 0 V

Parameter		Symbol	Limit Values		Unit	Test Condition
			min.	max.		
L-input voltage		V_{IL}	– 0.4	0.8	V	
H-input voltage		V_{IH}	2.0	V_{DD5} + 0.4	V	
L-output voltage		V_{QL}		0.45	V	I_{QL} = 7 mA (pin TXD) I_{QL} = 2 mA (all others / non-PCI)
H-output voltage		V_{QH}	2.4		V	I_{QH} = – 400 µA
Power supply current	operational	I_{CC}		< 400	mA	V_{DD} = 3.3 V / 5 V inputs at 0 V/V_{DD}, no output loads
	power down (no clocks)	I_{CC}		< 2	mA	
Input leakage current Output leakage current		I_{LI} I_{LQ}		10	µA	0 V < V_{IN} < V_{DD} to 0 V 0 V < V_{OUT} < V_{DD} to 0 V

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25 °C and the given supply voltage.

Note: The electrical characteristics described in ***section 6.1*** *also apply here!*

b) PCI Pins

According to the PCI specification V2.1 from June 1, 1995
(Chapter 4: Electrical Specification for 5 V signalling)

Note: According the electrical characteristics all DEMUX Interface pins (DPCI(1:0), A(27:2), W/$\overline{R}$) are treated as PCI Interface pins.

6.3 Capacitances

a) Non-PCI Interface Pins

Table 11 Non-PCI Interface Pins
T_A = 25°C; V_{DD5} = 5 V ± 5%, V_{DD3} = 3.3 V ± 0.3 V, V_{SS} = 0 V

Parameter	Symbol	Limit Values		Unit	Test Condition
		min.	max.		
Input capacitance	C_{IN}	1	5	pF	
Output capacitance	C_{OUT}	5	10	pF	
I/O-capacitance	C_{IO}	6	15	pF	

b) PCI Pins

According to the PCI specification V2.1 from June 1, 1995
(Chapter 4: Electrical Specification for 5 V signalling)

Note: According the electrical characteristics all DEMUX Interface pins DPCI(1:0), A(27:2), W/$\overline{R}$) are treated as PCI Interface pins.

6.4 AC Characteristics

a) Non-PCI Interface Pins

T_A = 0 to + 70°C; V_{DD5} = 5 V ± 5%; V_{DD3} = 3.3 V ± 0.3 V

Inputs are driven to 2.4 V for a logical “1” and to 0.4 V for a logical “0”. Timing measurements are made at 2.0 V for a logical “1” and at 0.8 V for a logical “0”.

The AC testing input/output waveforms are shown below.

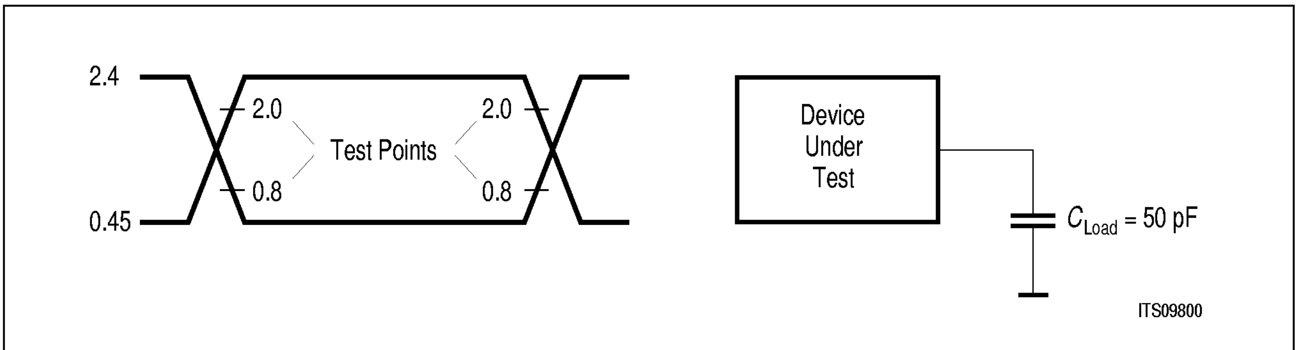


Figure 6 Input/Output Waveform for AC Tests

b) PCI Pins

According to the PCI specification V2.1 from June 1, 1995
(Chapter 4: Electrical Specification for 5 V signalling)

Note: According the electrical characteristics all DEMUX Interface pins DPCI(1:0), A(27:2), W/$\overline{R}$) are treated as PCI Interface pins.

6.4.1 PCI Bus Interface Timing

The AC testing input/output waveforms are shown in **figures 7** and **8** below.

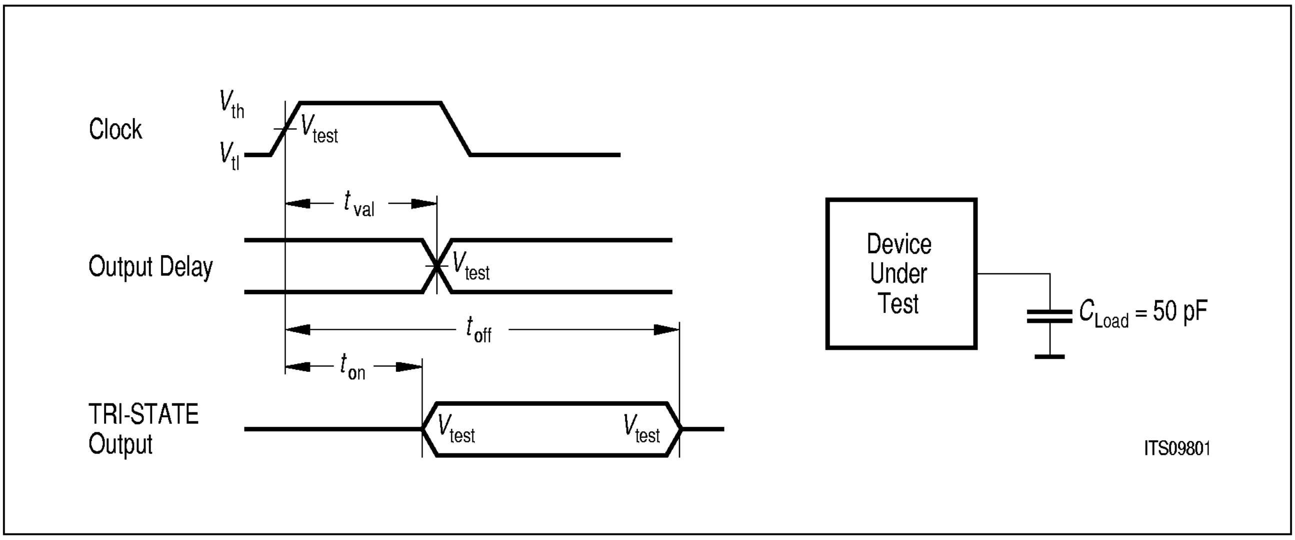


Figure 7 PCI Output Timing Measurement Waveforms

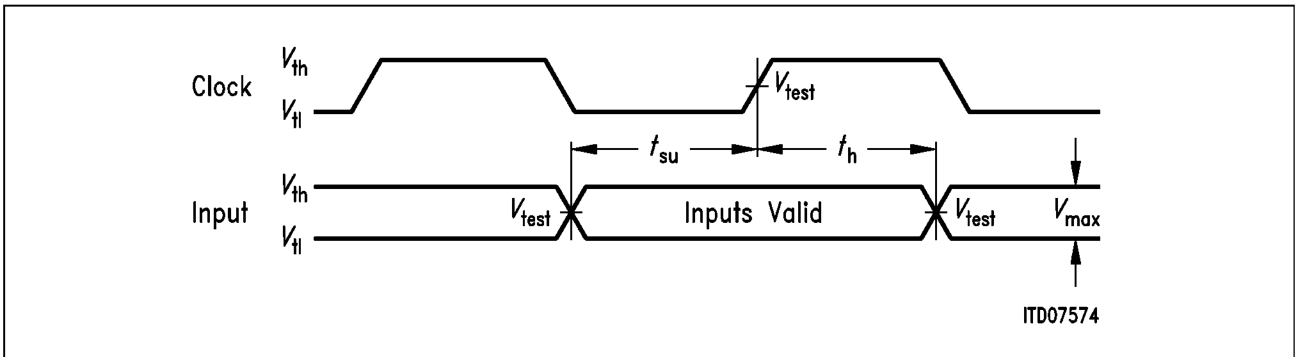


Figure 8 PCI Input Timing Measurement Waveforms

Table 12 PCI Input and Output Measurement Conditions

Symbol	Value	Unit
V_{th}	2.4	V
V_{tl}	0.4	V
V_{test}	1.5	V
V_{max}	2.0	V

The timings below show the basic read and write transaction between an initiator (Master) and a target (Slave) device. The MUNICH128X is able to work both as master and slave. The former mode is used by the MUNICH128X to write and read data to/from the host memory using the integrated DMA controller and the burst capability of the PCI interface. The latter mode enables for an external entity (a host) to read and write the MUNICH128X registers.

6.4.2 PCM Serial Interface Timing

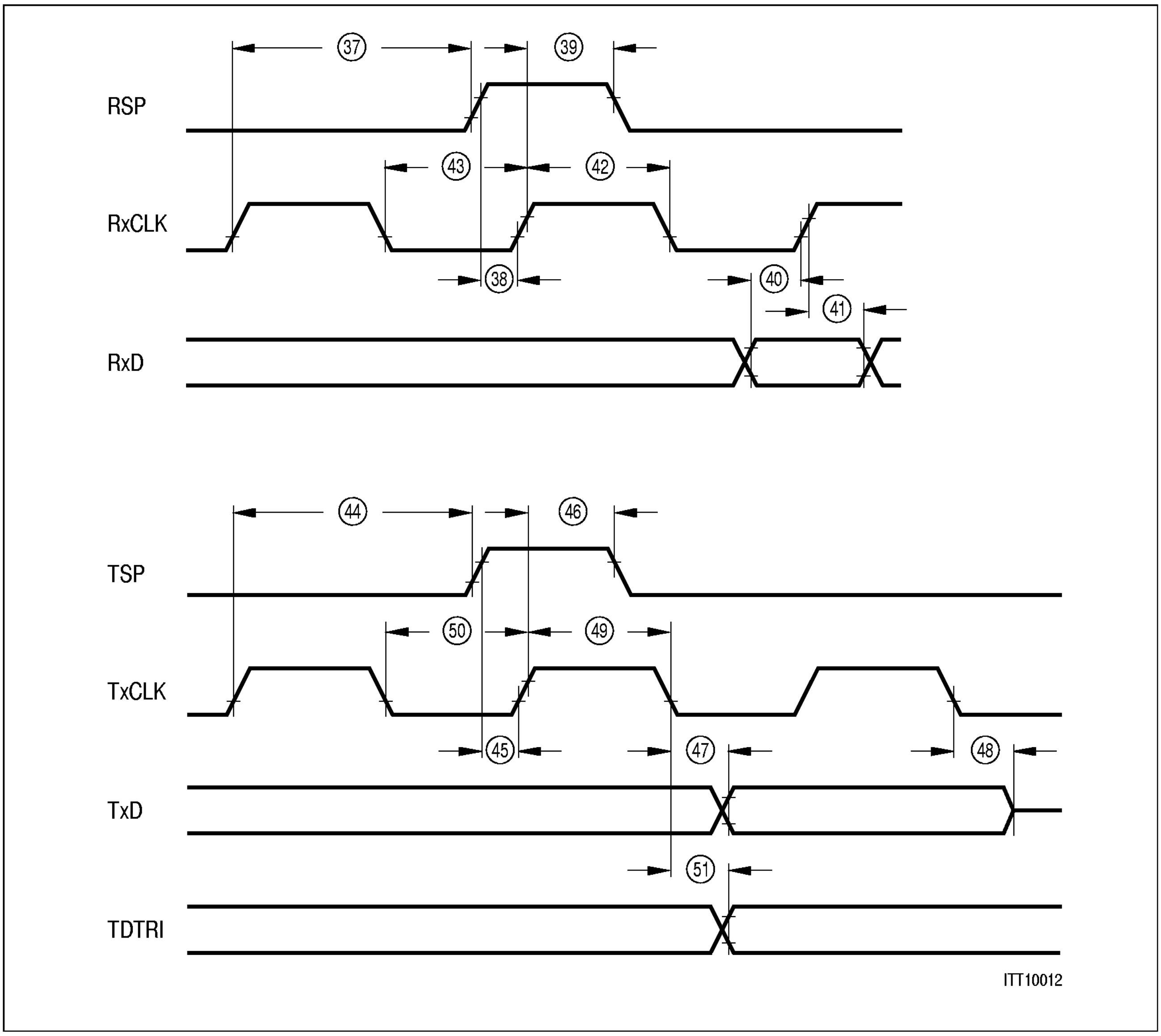


Figure 9 PCM Serial Interface Timing

Table 13 PCM Serial Interface Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
37	Receive strobe guard time	10		ns
38	Receive strobe setup	5		ns
39	Receive strobe hold	5		ns
40	Receive data setup	5		ns
41	Receive data hold	5		ns
42	Receive clock high width	30		ns
43	Receive clock low width	30		ns
44	Transmit strobe guard time	20		ns
45	Transmit strobe setup	5		ns
46	Transmit strobe hold	5		ns
47	Transmit data delay		25	ns
48	Transmit clock to high impedance		25	ns
49	Transmit clock high width	30		ns
50	Transmit clock low width	30		ns
51	Transmit tristate delay	25		ns

Note: The frequency on the serial line ***must*** *be smaller or equal to*
$^1/_8{}^{th}$ of the frequency on the μP bus for 1.536 MHz, 1.544 MHz, 2.048 MHz
$^1/_4{}^{th}$ of the frequency on the μP bus for 4.096 MHz.

Note: For complete internal or complete external loop t_{42} and t_{49} must be greater or equal to 3 times T.

System Interface Timing

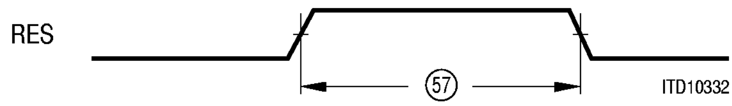


Figure 10 System Interface Timing

Table 14 System Interface Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
57	RESET pulse width	4 CLK cycles		

6.4.3 JTAG-Boundary Scan Timing

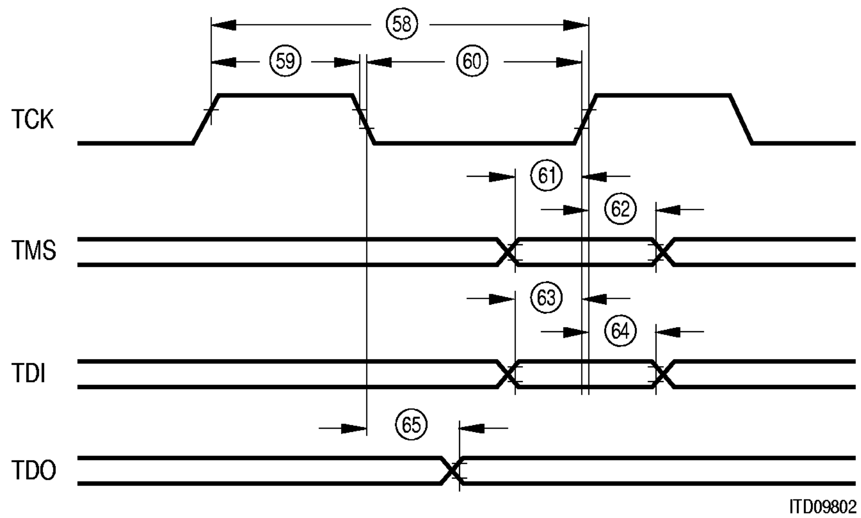


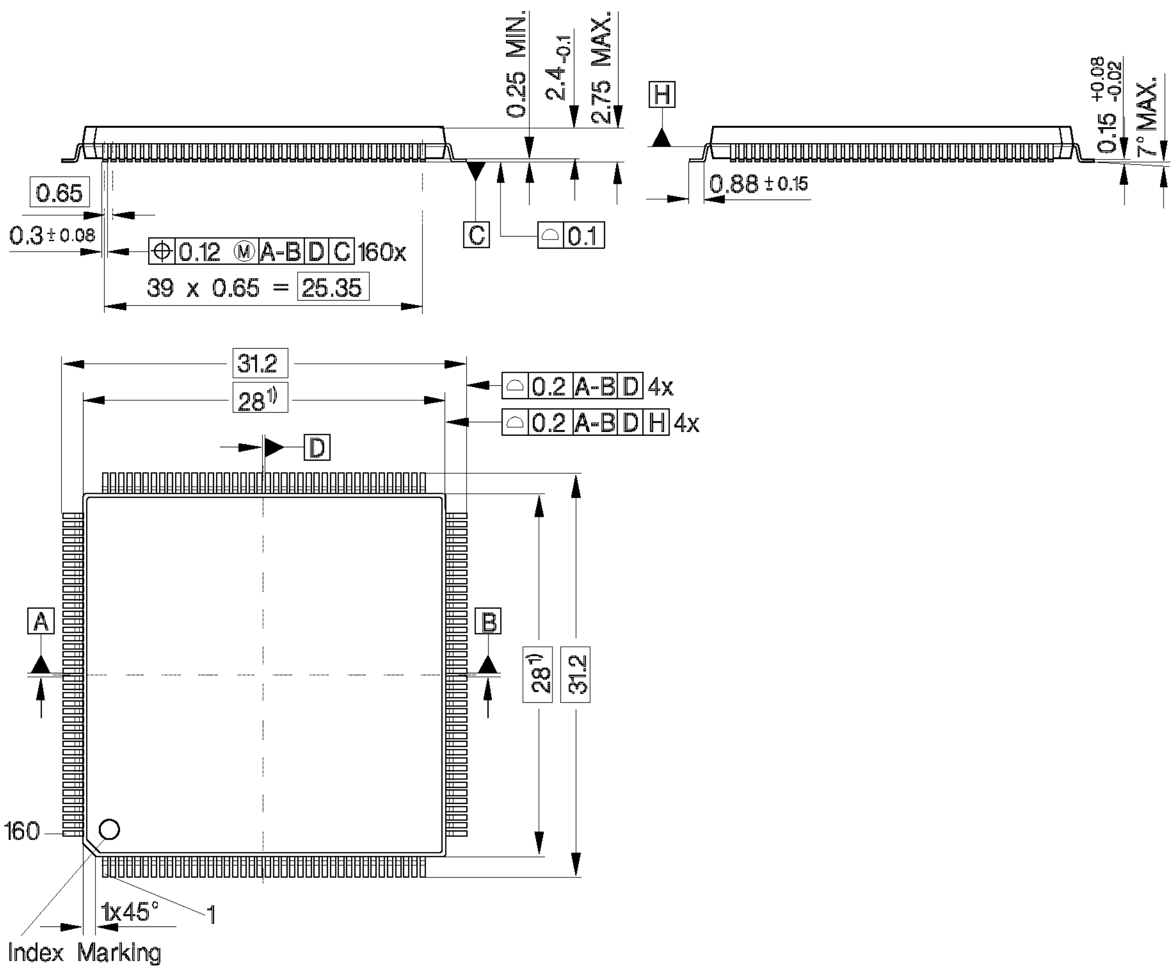
Figure 11 JTAG-Boundary Scan Timing

Table 15 Intel Bus Timing

No.	Parameter	Limit Values		Unit
		min.	max.	
58	TCK period	166	∞	ns
59	TCK high time	80		ns
60	TCK low time	80		ns
61	TMS setup time	30		ns
62	TMS hold time	10		ns
63	TDI setup time	30		ns
64	TDI hold time	20		ns
65	TDO valid delay	60		ns

7 Package Information

P-MQFP-160-1
(Plastic Metric Quad Flat Package)



1) Does not include plastic or metal protrusion of 0.25 max. per side

GPM05247

Figure 12 Physical Dimensions

Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".
SMD = Surface Mounted Device

Dimensinons in mm