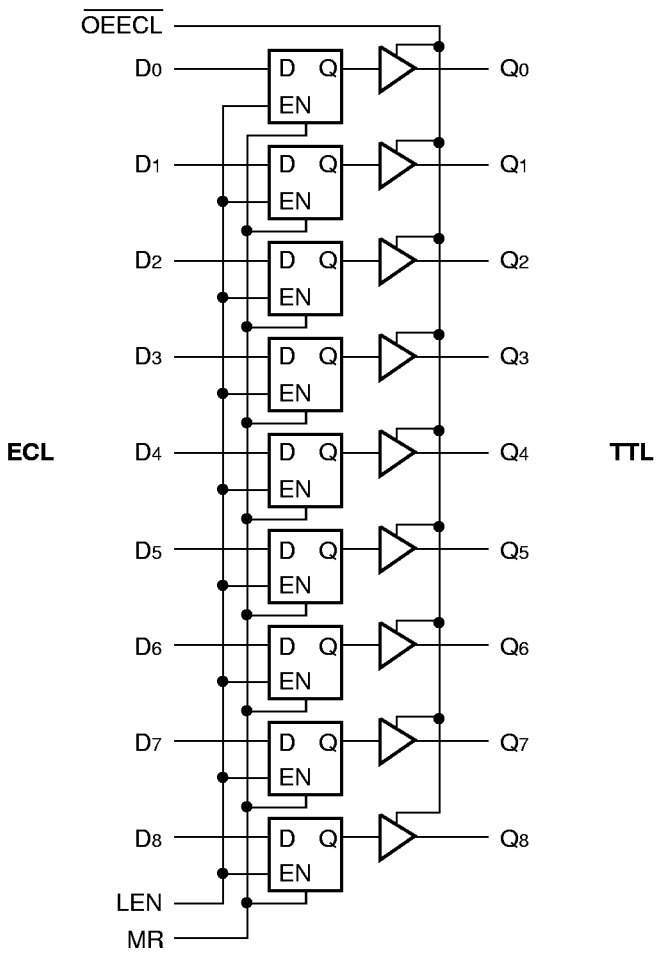
FEATURES

- 9-bit ideal for byte-parity applications
- 3-state TTL outputs
- Flow-through configuration
- Extra TTL and ECL power/ground pins to minimize switching noise
- Dual supply
- 6.0ns max. delay into 50pF, 12ns into 200pF (all outputs switching)
- PNP TTL inputs for low loading
- Choice of ECL compatibility: MECL 10KH (10Hxxx) or 100K (100Hxxx)
- ESD protection of 2000V
- Fully compatible with Motorola MC10H/100H603
- Available in 28-pin PLCC package

BLOCK DIAGRAM



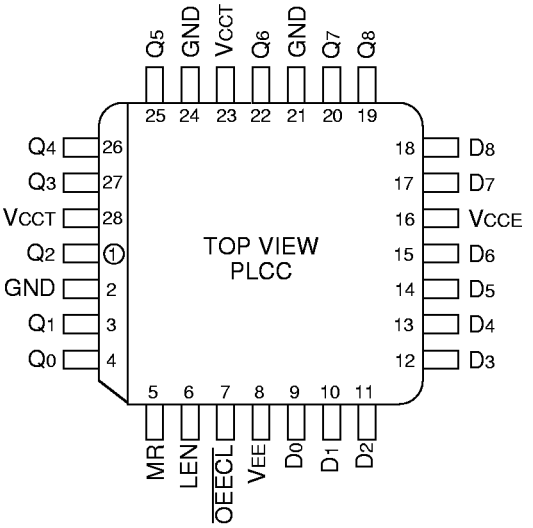
DESCRIPTION

The SY10/100H603 are 9-bit, dual supply ECL-to-TTL translators. Devices in the Synergy 9-bit translator series utilize the 28-lead PLCC for optimal power pinning, signal flow-through and electrical performance.

The devices feature a 48mA TTL output stage and AC performance is specified into both a 50pF and 200pF load capacitance. Latching is controlled by Latch Enable (LEN) and Master Reset (MR) resets the latches. A HIGH on $\overline{\text{OEECL}}$ sends the outputs into the high impedance state. All control inputs are ECL level.

The 10H version is compatible with MECL 10KH ECL logic levels. The 100H version is compatible with 100K levels.

PIN CONFIGURATION



PIN NAMES

Pin	Function
GND	TTL Ground (0V)
V_{CCE}	ECL V_{CC} (0V)
V_{CCT}	TTL Supply (+5.0V)
V_{EE}	ECL Supply (–5.2/–4.5V)
D_0–D_8	Data Inputs (ECL)
Q_0–Q_8	Data Outputs (TTL)
$\overline{\text{OEECL}}$	3-state Control (ECL)
LEN	Latch Enable (ECL)
MR	Master Reset (ECL)

Rev.: D Amendment: /0
Issue Date: April, 1998

TRUTH TABLE

D	LEN	MR	$\overline{OEECL}$	Q
L	L	L	L	L
H	L	L	L	H
X	H	L	L	Q_0
X	X	H	L	L
X	X	X	H	Z

DC ELECTRICAL CHARACTERISTICS

V_{CCT} = 5.0V ± 10%; V_{EE} = –4.75V to –5.5V (10H Version); V_{EE} = –4.2V to –5.5V (100H Version)

Symbol	Parameter	T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{EE}	Power Supply Current, ECL	45	63	45	64	45	68	mA	—
I_{CC}	Power Supply Current, TTL	80	110	80	110	80	110	mA	—
I_{OS}	Output Short Circuit Current	–100	–225	–100	–225	–100	–225	mA	V_{OUT} = 0V
I_{OZH}	Output Disable Current, HIGH	—	50	—	50	—	50	µA	V_{OUT} = 2.7V
I_{OZL}	Output Disable Current, LOW	—	–50	—	–50	—	–50	µA	V_{OUT} = 0.5V

AC ELECTRICAL CHARACTERISTICS

V_{CCT} = 5.0V ± 10%; V_{EE} = –4.75V to –5.5V (10H Version); V_{EE} = –4.2V to –5.5V (100H Version)

Symbol	Parameter		T_A = 0°C		T_A = +25°C		T_A = +85°C		Unit	Condition
			Min.	Max.	Min.	Max.	Min.	Max.		
t_{PLH} t_{PHL}	Propagation Delay to Output	D	3.2 6.4	6.0 12	3.2 6.4	6.0 12	3.2 6.4	6.0 12	ns	C_L = 50pF C_L = 200pF
		LEN	3.5 7.0	6.5 13	3.5 7.0	6.5 13	3.5 7.0	6.5 13	ns	C_L = 50pF C_L = 200pF
		MR	3.0 6.0	6.0 12	3.0 6.0	6.0 12	3.0 6.0	6.0 12	ns	C_L = 50pF C_L = 200pF
t_S	Set-up Time, D to LEN		1.5	—	1.5	—	1.5	—	ns	—
t_H	Hold Time, D to LEN		0.8	—	0.8	—	0.8	—	ns	—
$t_{w(L)}$	LEN Pulse Width, LOW		2.0	—	2.0	—	2.0	—	ns	—
t_{PLZ} t_{PHZ}	Output Disable Time		2.5 4.2	6.5 13	2.5 4.2	6.5 13	2.5 4.2	6.5 13	ns	C_L = 50pF C_L = 200pF
t_{PZL} t_{PZH}	Output Enable Time		2.0 4.0	5.0 10	2.0 4.0	5.0 10	2.0 4.0	5.0 10	ns	C_L = 50pF C_L = 200pF
t_r t_f	Output Rise/Fall Time 1.0V – 2.0V		0.2 0.2	1.2 3.0	0.2 0.2	1.2 3.0	0.2 0.2	1.2 3.0	ns	C_L = 50pF C_L = 200pF

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range
SY10H603JC	J28-1	Commercial
SY10H603JCTR	J28-1	Commercial
SY100H603JC	J28-1	Commercial
SY100H603JCTR	J28-1	Commercial

28 LEAD PLASTIC LEADED CHIP CARRIER (J28-1)