April 1990
Edition 6.0

FUJITSU

DATA SHEET

MB501/501L/503/504/504L
TWO MODULUS PRESCALERS

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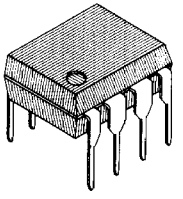
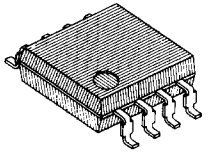
TWO MODULUS PRESCALERS

The Fujitsu MB 501/503/504 are two modulus prescalers, which are used in Phase Locked Loop (PLL) frequency synthesizer and will divide the input frequency by the modulus of 64/65 or 128/129, 16/17 or 32/33, and 32/33 or 64/65 respectively. MB 501L/MB 504L is the low-power version of MB 501/MB 504; it will perform exactly the same function as MB 501/MB 504 but with much lower power dissipation.

The output is 1.6 V peak to peak on ECL level.



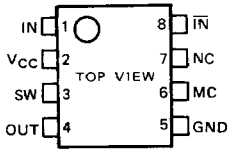
PLASTIC PACKAGE
DIP-08P-M01



PLASTIC PACKAGE
FPT-08P-M01

- High Operating Frequency, Low Power Operation.
  - 1.0 GHz at 150 mW typ. (MB 501)
  - 1.1 GHz at 50 mW typ. (MB 501L)
  - 200 MHz at 40 mW typ. (MB 503)
  - 520 MHz at 50 mW typ. (MB 504)
  - 520 MHz at 25 mW typ. (MB 504L)
- Pulse Swallow Function
- Wide Operation Temperature T_A = -40°C to +85°C
- Stable Output Amplitude V_{OUT} = 1.6 V_{P-P}
- Complete PLL synthesizer circuit with the Fujitsu MB 87001A, PLL synthesizer IC
- Plastic 8-pin Standard Dual-In-Line Package or space saving Flat Package

PIN ASSIGNMENT



ABSOLUTE MAXIMUM RATINGS (See NOTE)

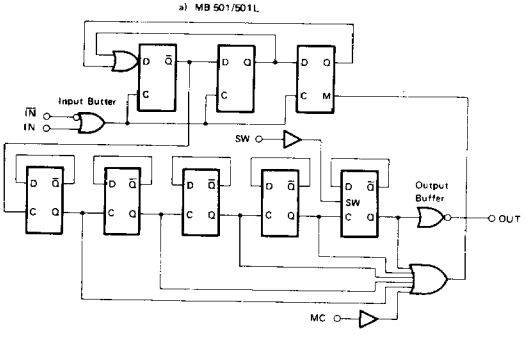
Rating		Value	Unit
Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_{IN}	-0.5 to V_{CC}	V
Output Current	V_O	10	mA
Ambient Temperature	T_A	-40 to +85	°C
Storage Temperature	T_{STG}	-55 to + 125	°C

Note: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields. However, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Fig. 1 – BLOCK DIAGRAMS

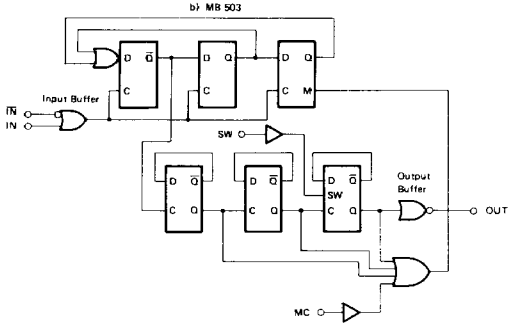
a) MB 501/501L



	SW	MC	Divide Ratio
MB 501/ MB 501L	H	H	1/64
	H	L	1/65
	L	H	1/128
	L	L	1/129

Note: SW: H = V_{CC}, L = open
MC: H = 2.0 V to V_{CC},
L = GND to 0.8 V

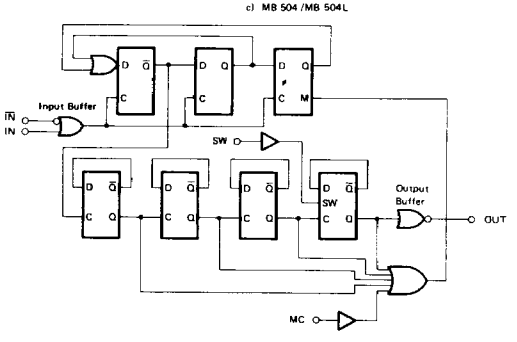
b) MB 503



	SW	MC	Divide Ratio
MB 503	H	H	1/16
	H	L	1/17
	L	H	1/32
	L	L	1/33

Note: SW : H = V_{CC}, L = open
MC : H = 2.0 V to V_{CC},
L = GND to 0.8 V

c) MB 504 /MB 504L



	SW	MC	Divide Ratio
MB 504/ MB 504L	H	H	1/32
	H	L	1/33
	L	H	1/64
	L	L	1/65

Note: SW: H = V_{CC}, L = open
MC: H = 2.0 V to V_{CC},
L = GND to 0.8 V

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Output Current	I_O		1.2		mA
Ambient Temperature	T_A	−40		+85	°C
Load Capacitance	C_L			12	pF

PIN DESCRIPTION

Pin Number	Symbol	Function
1	IN	Input
2	V_{CC}	DC Supply Voltage
3	SW	Divide Ratio Control Input (See Divide Ratio Table)
4	OUT	Output
5	GND	Ground
6	MC	Modulus Control Input (See Divide Ratio Table)
7	NC	Non Connection
8	$\overline{IN}$	Complementary Input

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ELECTRICAL CHARACTERISTICS

(Recommended Operating Conditions unless otherwise noted)

Parameter		Symbol	Conditions	Value			Unit
				Min	Typ	Max	
Power Supply Current	MB501	I_{CC}	I/O pins are open		30	42*	mA
	MB501L				10	14*	mA
	MB503				8	12*	mA
	MB504				10	14*	mA
	MB504L				5	7*	mA
Output Amplitude		V_O		1.0	1.6		V_{P-P}
Input Frequency	MB501	f_{IN}	With input coupling capacitor 1000pF	10		1000	MHz
	MB501L			10		1100	MHz
	MB503			10		200	MHz
	MB504			10		520	MHz
	MB504L			10		520	MHz
Input Signal Amplitude for IN	MB501	V_{IN}		-4		5.5	dBm
	MB501L			-4		5.5	dBm
	MB503			-12		10	dBm
	MB504			-12		10	dBm
	MB504L			-12		10	dBm
High Level Input Voltage for MC		V_{IHM}		2.0			V
Low Level Input Voltage for MC		V_{ILM}				0.8	V
High Level Input Voltage for SW		V_{IHS}**		V_{CC}-0.1	V_{CC}	V_{CC}+0.1	V
Low Level Input Voltage for SW		V_{ILS}		Open			V
High Level Input Current for MC		I_{IHM}	V_{IH} = 2.0V			0.4	mA
Low Level Input Current for MC		I_{ILM}	V_{IL} = 0.8V	-0.2			mA
Modulus Set-up Time MC to OUT	MB501	t_{SET}			18	28	ns
	MB501L				16	26	ns
	MB503				38	46	ns
	MB504				20	30	ns
	MB504L				18	28	ns

NOTE: * V_{CC} = 5V, T_A = 25°C
** Design Guarantee

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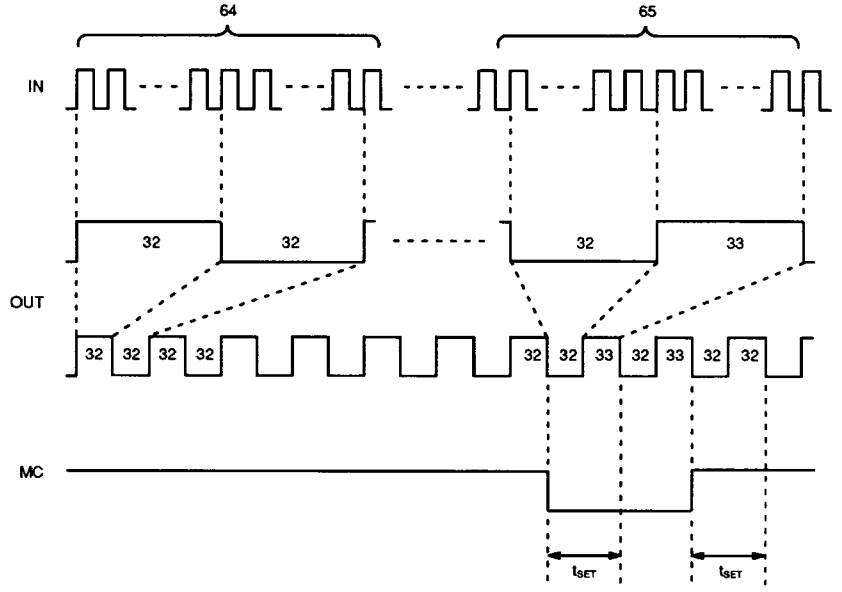
MB501/MB501L TIMING CHART (2 MODULUS)

Example: Divide ratio = 64/65



Note: When divide ratio of 65 is selected, positive pulse is applied by one to 33.
The typical set up time is 18 ns (MB501), 16 ns (MB501L) from the MC signal input to the timing of change of prescaler divide ratio.

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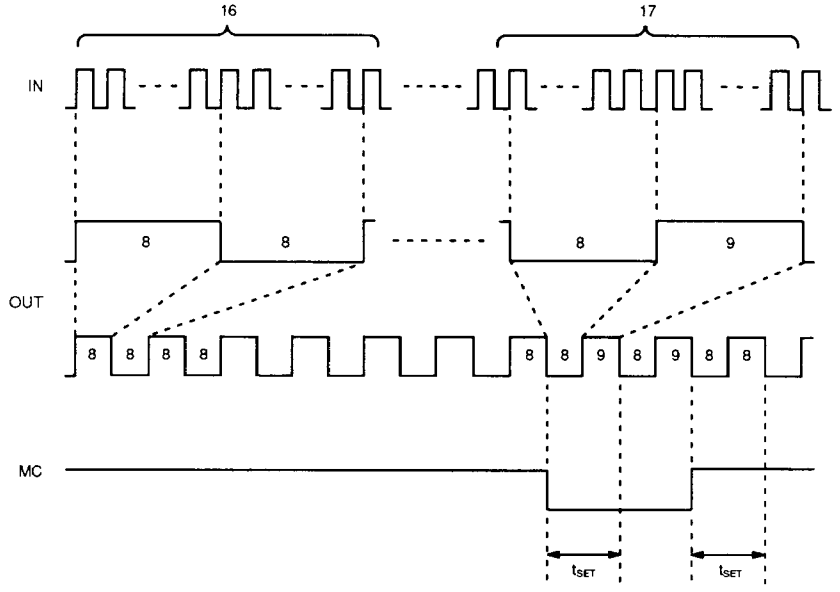
MB503 TIMING CHART (2 MODULUS)

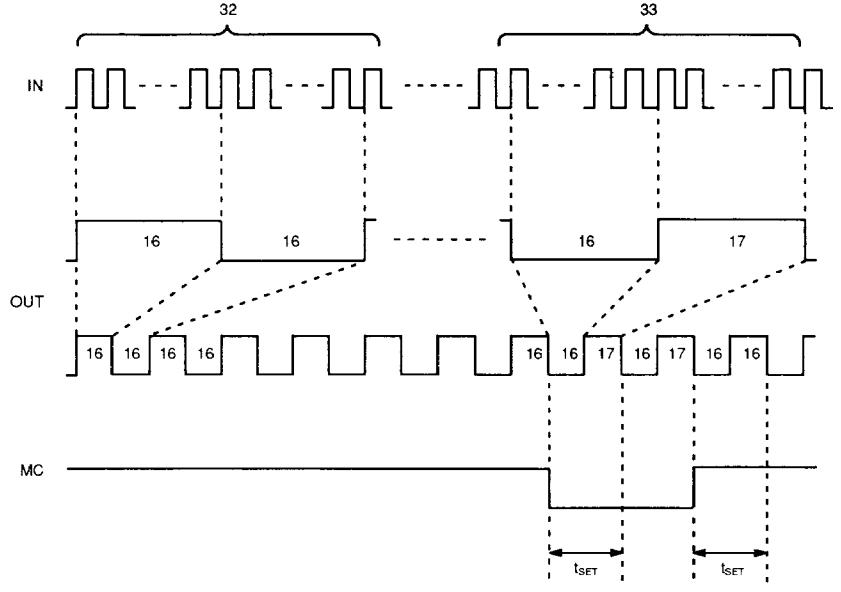
Example: Divide ratio = 16/17



Note: When divide ratio of 17 is selected, positive pulse is applied by one to 9.
The typical set up time is 38 ns from the MC signal input to the timing of change of prescaler divide ratio.

MB504/MB504LV TIMING CHART (2 MODULUS)

Example: Divide ratio = 32/33



Note: When divide ratio of 33 is selected, positive pulse is applied by one to 17.
The typical set up time is 20 ns (MB504), 18 ns (MB504L) from the MC signal input to the timing of change of prescaler divide ratio.

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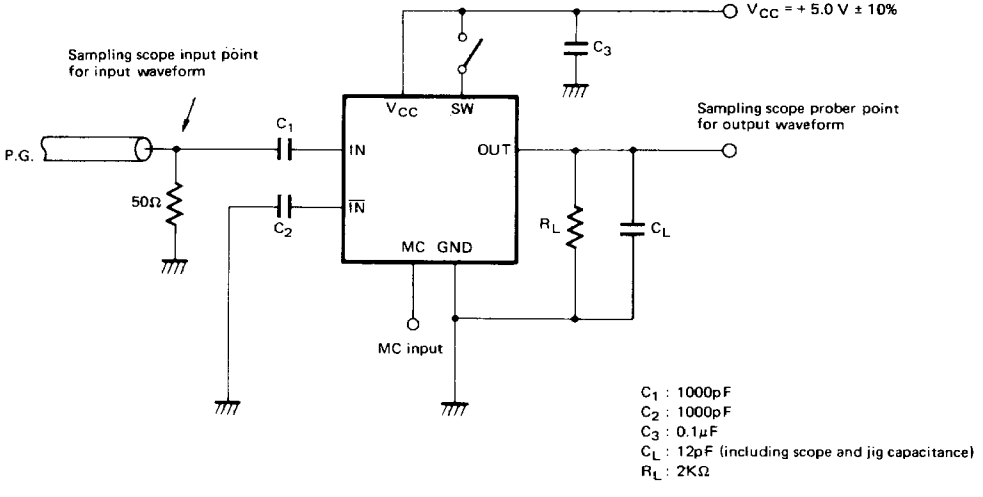
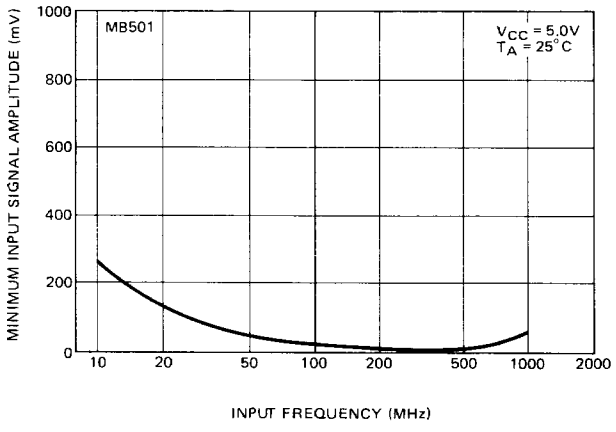
Fig. 2 – TEST CIRCUIT



TYPICAL CHARACTERISTICS CURVES

Fig. 3 – INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY



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TYPICAL CHARACTERISTICS CURVES (continued)

Fig. 4 – INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY

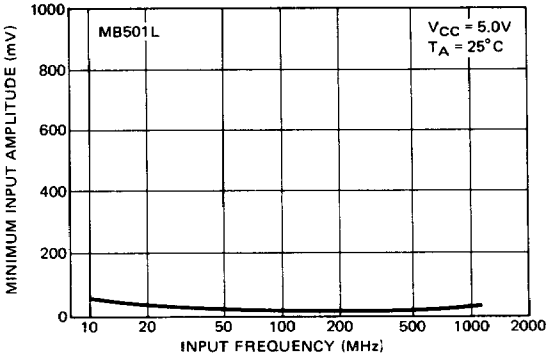


Fig. 5 – INPUT SIGNAL AMLITUDE vs. INPUT FREQUENCY

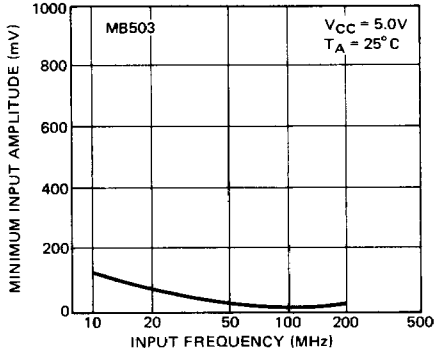
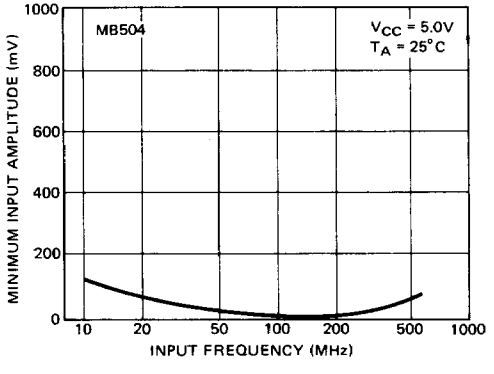


Fig. 6 – INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY



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TYPICAL CHARACTERISTICS CURVES (continued)

Fig. 7 – INPUT SIGNAL AMPLITUDE vs. INPUT FREQUENCY

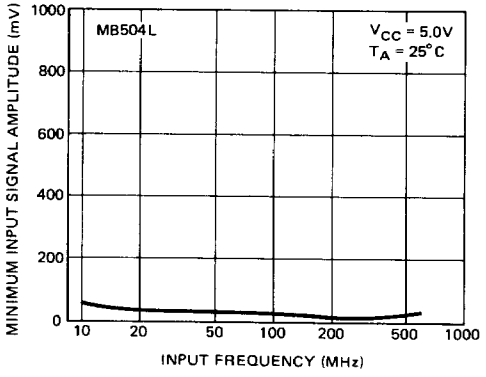
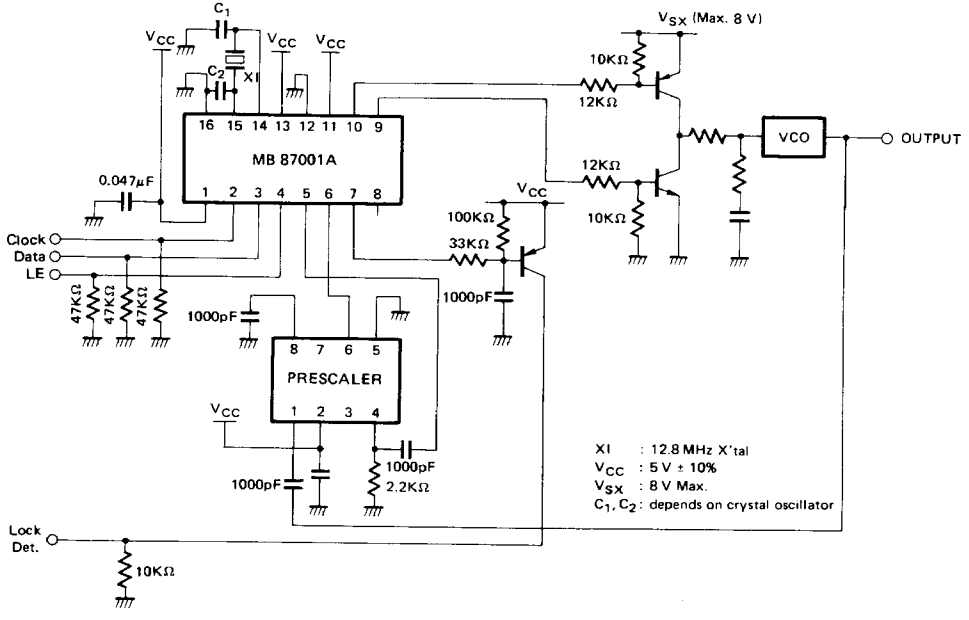


Fig. 8 – TYPICAL APPLICATION EXAMPLE



An example of application of MB501/501L/503/504/504L with PLL Synthesizer IC MB87001A

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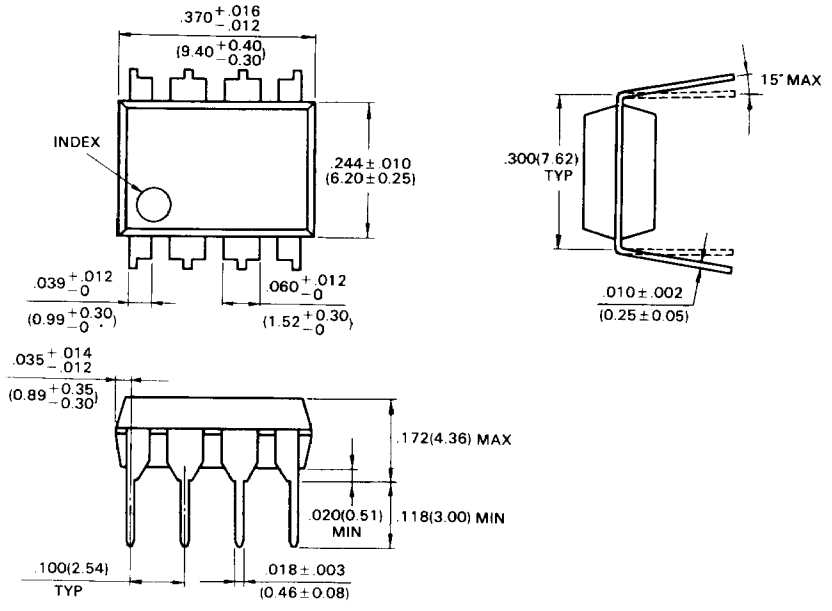
PACKAGE DIMENSIONS

8-LEAD PLASTIC DUAL IN-LINE PACKAGE
(CASE No.: DIP-08P-M01)



Dimensions in
inches (millimeters)

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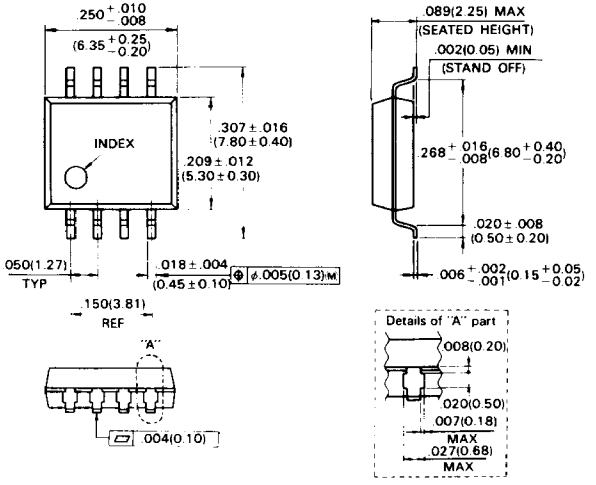
PACKAGE DIMENSIONS (Continued)

8-LEAD PLASTIC FLAT PACKAGE
(CASE No.: FPT-08P-M01)



Dimensions in
inches (millimeters)