HARRIS SEMICONDUCTOR

HIP0045

June 1997

1A/50V Octal Low Side Power Driver With Serial Bus Control and Fault Protection

Features

- Octal NDMOS Output Drivers in a High Voltage Power BiMOS Process
- Over-Stress Protection - Each Output:
  - Over-Current Protection . . . . . 1A Min
  - Over-Voltage Clamp Protection. . . . . 50V Typ
  - Thermal Shutdown Protection (2 Channels)
- Open-Load Detection
- Power BiMOS Output Configuration
  - Current Latch-Off Protection for 6 Channels; 2 with External Drive Input and ORed with SPI Bus Control
  - 2 Channels Configured for Lamp Drivers with Current Limiting and Over-Temperature Latch-Off
- High Speed CMOS Logic Control
  - SPI Bus Controlled Interface
  - Individual Output Latch
  - Individual Fault Unlatch and Feedback
  - Common Reset Line
- Low Quiescent Current . . . . . 5mA Max
- Ambient Operating Temp. Range. . . . . $-40^{o}C$ to $125^{o}C$

Applications

- Automotive and Industrial Systems
- Solenoids, Relays and Lamp Drivers
- Logic and µP Controlled Drivers
- Robotic Controls

Description

The HIP0045 is a logic controlled, eight channel Octal Serial Power Low Side Driver. The serial peripheral interface (SPI) utilized by the HIP0045 is a serial synchronous bus compatible with Harris CDP68HC05, or equivalent, microcomputers. As shown in the Block Diagram for the HIP0045, each of the open drain MOS Output Drivers have individual protection for over-voltage and over-current. Each output channel has separate output latch control with fault unlatch and diagnostic or status feedback. Under normal ON conditions, each output driver is in a low voltage, high current state of saturated turn-on. Comparators in the diagnostic circuitry monitor the output drivers to determine if an out of saturation condition exists. If a fault is sensed, the respective output driver for Channels 0 - 5 have overcurrent latch-off. Channels 6 and 7 are configured for lamp drivers and have current limiting with over-temperature latch-off. Channels 0 and 1 have direct parallel drive control for PWM applications and are ORed with the SPI Bus control. All channels are SPI Bus controlled and sense the output states for diagnostic feedback.

The HIP0045 is fabricated in a Power BiMOS IC process, and is intended for use in automotive and other applications having a wide range of temperature and electrical stress conditions. It is particularly suited for driving relays, solenoids and lamps in applications where low standby power, high operating voltage, and high output current in high ambient temperature conditions is required.

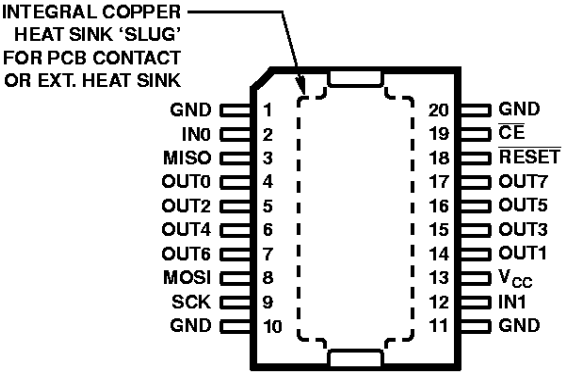
The HIP0045 is in a 20 lead plastic Power SOP (PSOP) Package with an integral copper 'slug' to conduct heat directly to a PCB interface or heat sink on the bottom of the package.

Ordering Information

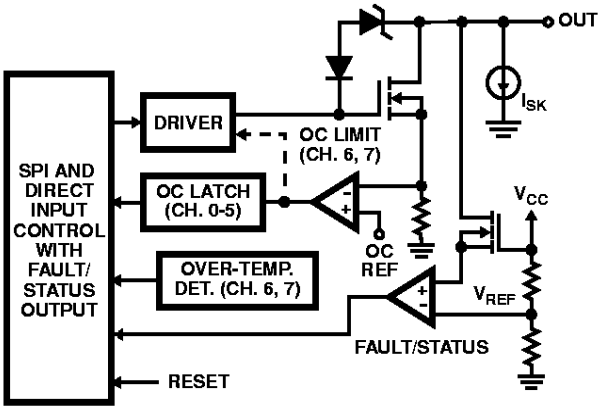
PART NO.	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HIP0045AB	-40 to 125	20 Ld PSOP	M20.3A

Pinout

HIP0045 (PSOP W/HEAT SLUG)
TOP VIEW



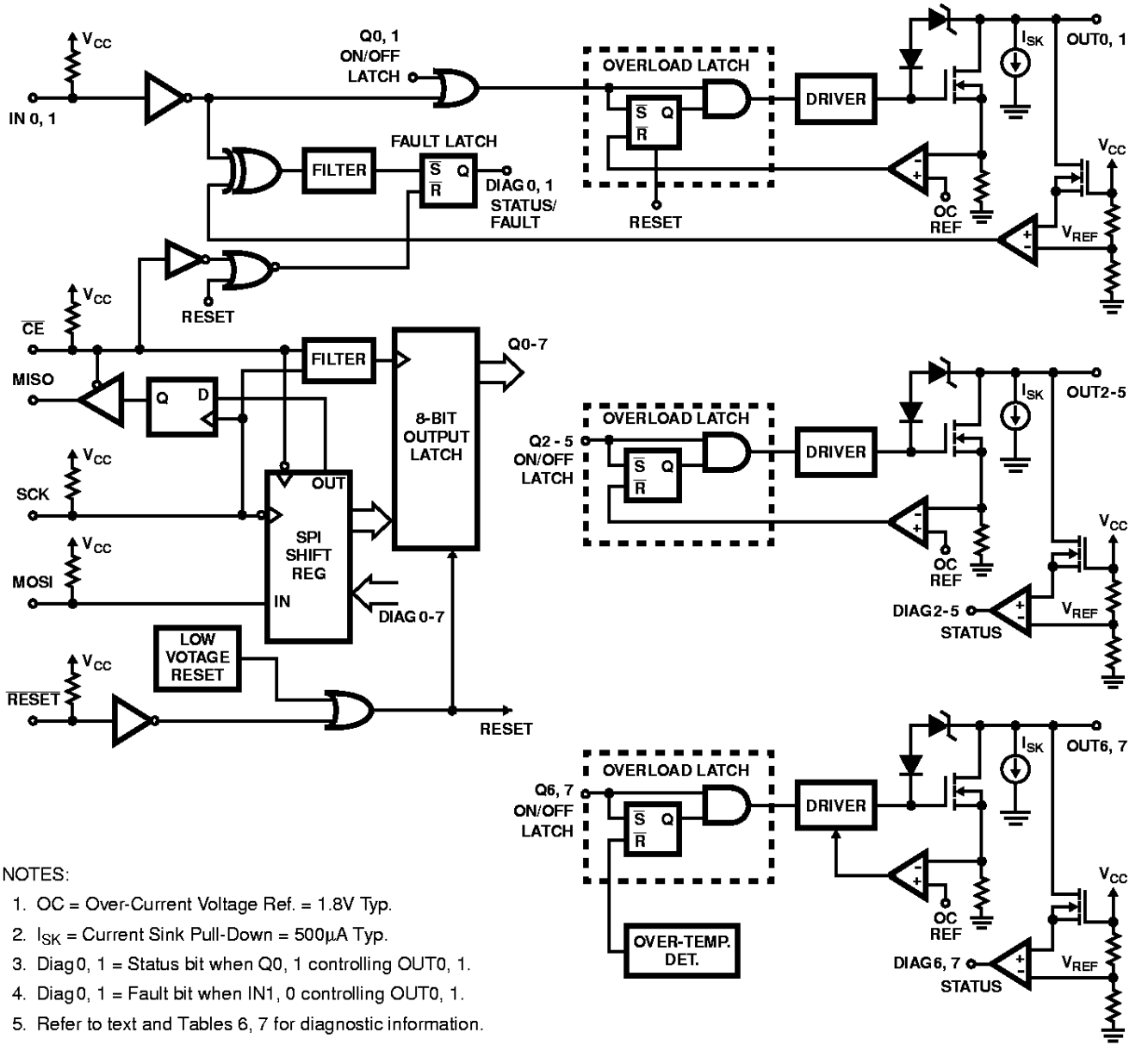
Driver Block Diagram



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper IC Handling Procedures.

File Number **4047.1**

Detailed Block Diagram



NOTES:

1. OC = Over-Current Voltage Ref. = 1.8V Typ.
2. I_{SK} = Current Sink Pull-Down = 500µA Typ.
3. Diag 0, 1 = Status bit when Q0, 1 controlling OUT0, 1.
4. Diag 0, 1 = Fault bit when IN1, 0 controlling OUT0, 1.
5. Refer to text and Tables 6, 7 for diagnostic information.

Input to Output Control Tables

TABLE 1. OUTPUT 0

SPI BIT 0	IN0	OUT0
0	1	OFF
0	0	ON
1	0	ON
1	1	ON

TABLE 2. OUTPUT 1

SPI BIT 1	IN1	OUT1
0	1	OFF
0	0	ON
1	0	ON
1	1	ON

TABLE 3. OUTPUT 2 - 7

SPI BIT 2 - 7	OUT2 - 7
0	OFF
1	ON

TABLE 4. OUTPUT CONTROL REGISTER, Q0 - 7

Q1 (D7I)	Q3 (D6I)	Q5 (D5I)	Q7 (D4I)	Q0 (D3I)	Q2 (D2I)	Q4 (D1I)	Q6 (D0I)
MSB							LSB

NOTE: The Output Control Register bits Q0 -7 have the same order as the Diagnostic Failure Register bits Diag0 - 7 as defined in Table 5. Data bits D0I - D7I give the MOSI SPI serial data input flow sequence.

Absolute Maximum Ratings

Maximum Output Voltage, V_{OUT} . . . . . -0.7 to V_{OC}
Peak Output Load Current, I_{LOAD} . . . . . As Specified for I_{SC}, I_{LIM}
Continuous Output Load Current, I_{OUT} (All 8 Outputs ON) 0.5A
Continuous Output Load Current, I_{OUT} (Any one Output ON) . . . 1A
Total Average Current, I_{OUT} (All 8 Outputs) 4.5A
Reverse Peak Current Drive, Any one Output, I_{RD}; $t \leq 2ms$ . . . . -3A
DC Logic Supply, V_{CC} . . . . . -0.3 to 7V
Input Voltage, All Inputs and Data Lines . . . . . -0.3 to V_{CC} +0.3V

Operating Conditions

Temperature Range . . . . . -40°C to 125°C
Logic Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V

Thermal Information

Thermal Resistance (Typical, Note 6)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
PSOP Package	40	2

Maximum Junction Temperature, T_J . . . . . 150°C
Maximum Storage Temperature Range, T_{STG} . . . . -55°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 265°C

Die Characteristics

Back Side Potential . . . . . V- (GND Pin, Heat Sink)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

6. θ_{JA} Rated with standard PC Board, θ_{JC} rated with infinite heat sink.

Electrical Specifications

V_{CC} = 4.5V to 5.5V, T_A = -40°C to 125°C, Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Standby Current, No Load	I_{CCO}	No Load	-	-	5	mA
Supply Current, Full Load	I_{CC}	All Outputs ON, 0.5A Load Per Output	-	-	5	mA
Output Clamping Voltage (Note 7)	V_{OC}	I_{LOAD} = 0.5A, Output Programmed OFF	45	-	62	V
Output Clamping Energy	E_{OC}	1ms Single Pulse Width, T_A = 25°C, (Refer to Figure 4 for SOA)	20	45	-	mJ
Output Leakage Current 1 (Note 8)	$I_{O\ LEAK1}$	V_{OUT} = 25V, Outputs OFF	-	-	100	µA
Output Leakage Current 2 (Note 8)	$I_{O\ LEAK2}$	V_{OUT} = 16V, Outputs OFF	-	-	100	µA
Output Leakage Current 3 (Note 8)	$I_{O\ LEAK3}$	V_{OUT} = 16V, Outputs OFF, V_{CC} = 1V	-	-	10	µA
Drain-to-Source On Resistance, OUT0 - 7	r_{DSON}	I_{LOAD} = 0.5A; T_J = 150°C	-	-	1.5	Ω
Output Capacitance	C_{OUT}	V_{OUT} = 16V, f = 1MHz	-	-	20	pF
Turn-On Delay, OUT0, 1	$t_{d(ON)}$	R_L = 500Ω, V_{CE} = 50% to V_{OUT} = 0.9 x V_{BATT}, $V_{IN0,1}$ = 50% to V_{OUT} = 0.9 x V_{BATT}, V_{BATT} = 16V	-	-	5	µs
Turn-On Delay, OUT2 - 7	$t_{d(ON)}$	R_L = 500Ω, V_{CE} = 50% to V_{OUT} = 0.9 x V_{BATT}, V_{BATT} = 16V	-	-	10	µs
Turn-Off Delay	$t_{d(OFF)}$	R_L = 500Ω, $V_{\overline{CE}}$ = 50% to V_{OUT} = 0.1 x V_{BATT}, $V_{IN0,1}$ = 50% to V_{OUT} = 0.9 x V_{BATT}, V_{BATT} = 16V	-	-	10	µs
Turn-On Voltage Slew-Rate, OUT2 - 7	$\frac{dV_{ON1}}{dt}$	For V_{OUT} = 90% to 30% of V_{BATT}; V_{BATT} = 16V, R_L = 500Ω	-	0.7	3.5	V/µs
Turn-On Voltage Slew-Rate, OUT0, 1	$\frac{dV_{ON2}}{dt}$	For V_{OUT} = 90% to 30% of V_{BATT}; V_{BATT} = 16V, R_L = 500Ω	-	2	10	V/µs
Turn-Off Voltage Slew-Rate, OUT0 - 7	$\frac{dV_{OFF1}}{dt}$	For V_{OUT} = 30% to 90% of V_{BATT}; V_{BATT} = 16V, R_L = 500Ω	-	2	10	V/µs
Turn-Off Voltage Slew-Rate, OUT0 - 7	$\frac{dV_{OFF2}}{dt}$	For V_{OUT} = 30% to 80% of V_{OC}; V_{BATT} = 0.9 x V_{OC}, R_L = 500Ω	-	2	15	V/µs
FAULT PARAMETERS						
Reverse Current Drive, OUT0 - 7	I_{RD}		-500	-	-	mA
Reverse Voltage Drop, OUT0 - 7	V_{RD}	I_{OUT} = -3A, t ≤2ms	-1.5	-	-	V
ΔI_{CC} during Reverse Current Drive	ΔI_{CC}	I_{OUT} = -3A, t ≤2ms	-	-	100	mA
Open Load Threshold Voltage	V_{REF}	Open Load Fault Condition, Fault Detected If V_{OUT} < V_{REF}	0.32 x V_{CC}	-	0.4 x V_{CC}	V

Electrical Specifications

V_{CC} = 4.5V to 5.5V, T_A = -40°C to 125°C, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Open Load Pull-Down Current	I_{SK}	No Load, $V_{OUT} = V_{BATT}$ = 16V	20	-	100	µA
Over-Current Shutdown Threshold, OUT0 - 5	I_{SC}	V_{CC} = 5V	1.05	1.4	2	A
Short Circuit Current Limit, OUT6, 7	I_{LIM}	V_{CC} = 5V	1.05	1.4	1.75	A
Short Circuit Shutdown Delay, OUT0 - 5	t_{SC}		0.2	-	12	µs
Disable Fault Detection Time, Channel IN0, IN1 After Input Switch Transition	t_{DF}		15	-	50	µs
Over-Temperature Detection Threshold	T_{OFF}		155	165	175	°C
LOGIC INPUTS ($\overline{IN0}$, $\overline{IN1}$, MOSI, SCK, $\overline{RESET}$, $\overline{CE}$)						
Threshold Voltage at Falling Edge	V_T-		0.2xV_{CC}	-	-	V
Threshold Voltage at Rising Edge	V_T+		-	-	0.7xV_{CC}	V
Hysteresis Voltage	V_H	V_T+ - V_T-	0.65	-	-	V
Input Current	I_{IN}	$V_{IN} = V_{CC}$	-	-	+10	µA
Input Pull-Up Resistance	R_{IN}		50	80	200	kΩ
Input Capacitance	C_{IN}		-	-	10	pF
Input Frequency, IN0, IN15	f_{IN}		DC	-	2	kHz
Active Supply Range for Reset State Change at $\overline{RESET}$ Pin	V_{HCC_RST}	$\overline{RESET}$ Pin Forced Reset. (Note: Normal V_{CC} Functional Operating Range is 4.0V to 5.5V)	3.1	-	5.5	V
Low V_{CC} Active Reset Threshold	V_{LCC_RST}	Low V_{CC} Forced Reset, (Low Voltage Reset Active for 0 < V_{CC} < V_{LCC_RST})	3.1	-	4	V
LOGIC OUTPUT (MISO)						
Data Output LOW Voltage	V_{SOL}	I_{SO} = -3.2mA	-	0.2	0.4	V
Data Output HIGH Voltage	V_{SOH}	I_{SO} = -4mA	V_{CC} -0.4V	-	-	V
Output Three-State Leakage Current	I_{SOL}	$\overline{CE}$ = High, 0V ≤ V_{SO} ≤ V_{CC}	-10	-	+10	µA
Output Capacitance	C_{SO}	f_{OPER} = 3MHz	-	-	10	pF

Serial Peripheral Interface Timing

(MOSI, MISO Load Capacitor = 100pF, See Figure 1)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNITS
Clock Frequency, 50% Duty Cycle	f_{CLK}		3	-	-	MHz
Enable Lead Time (SCK Change Low to High after $\overline{CE}$ = Low)	t_{LEAD}		100	-	-	ns
Enable Lag Time (Time for SCK Low before $\overline{CE}$ goes High)	t_{LAG}		150	-	-	ns
Minimum Time SCK = High	t_{WSCKH}		160	-	-	ns
Minimum Time SCK = Low	t_{WSCKL}		160	-	-	ns
Data Setup Time (SCK Change from High to Low after MOSI Data Valid)	t_{SU}		20	-	-	ns
Data Hold Time (MOSI Data Hold Time SCK Change from High to Low)	t_H			-	20	ns
Enable Time from $\overline{CE}$ = Low to Data at MISO	t_{EN}		-	-	100	ns
Disable Time (Time for $\overline{CE}$ Low to High to Output Data Float)	t_{DIS}		-	-	100	ns