



V827432U24SC
2.5 VOLT 32M x 72 HIGH PERFORMANCE
LOW PROFILE (1U) REGISTERED ECC
DDR SDRAM MODULE

Features

- 184 Pin Registered 33,554,432 x 72 bit Organization DDR SDRAM Modules
- Utilizes High Performance 32M x 8 DDR SDRAM in TSOPII-66 and FBGA Packages
- Single +2.5V ($\pm 0.2V$) Power Supply
- Programmable CAS Latency, Burst Length, and Wrap Sequence (Sequential & Interleave)
- Auto Refresh (CBR) and Self Refresh
- All Inputs, Outputs are SSTL-2 Compatible
- 8192 Refresh Cycles every 64 ms
- Serial Presence Detect (SPD)
- 1.2 or 1.125 inches Low Profile Registered DIMM

Description

The V827432U24SC memory module is organized 33,554,432 x 72 bits in a 184 pin memory module. The 32M x 72 memory module uses 9 ProMOS 32M x 8 DDR SDRAM. The x72 low profile modules are ideal for use in high performance computer systems where increased memory density, fast access times and small form factors are required.

| | Module Speed | D0 | D3 | C0 | Units |
|-----------|---|-----------------|-----------------|----------------|-------|
| | Clock Frequency (max.) | 200 (PC400A) | 200 (PC400B) | 166 (PC333) | MHz |
| t_{CK} | Clock Cycle Time \overline{CAS} Latency = 2 | 7.5 | 7.5 | 7.5 | ns |
| | Clock Cycle Time \overline{CAS} Latency = 2.5 | 5 | 6 | 6 | ns |
| | Clock Cycle Time \overline{CAS} Latency = 3 | 5 | 5 | - | ns |
| t_{RCD} | t_{RCD} parameter | 3 | 3 | 3 | CLK |
| t_{RP} | t_{RP} parameter | 3 | 3 | 3 | CLK |

Part Number Information

| | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|----|----|----|----|----|----|----|----|
| 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | 17 |
| V | 8 | 2 | 7 | 4 | 3 | 2 | U | 2 | 4 | S | C | I | X | - | D | 3 |

ProMOS TYPE
8 : DDR

VOLTAGE
2 : 2.5V

DATA DEPTH
16 : 16Mb
32 : 32 Mb
64 : 64 Mb
65 : 128 Mb
66 : 256 Mb

REFRESH RATE
0: 4K
2: 8K

BANKS
4 : 4 Banks

DATA WIDTH & COMP DENSITY
65 X64 using 128M
66 X64 using 256M
67 X64 using 512M
68 X64 using 1G
69 X64 using 2G
73 X72 using 128M
74 X72 using 256M
75 X72 using 512M
76 X72 using 1G
77 X72 using 2G

MODULE TYPE & COMP WIDTH

| BASED ON | X4 | X16 | X8 |
|------------------------|----|-----|----|
| 184PIN DIMM UNBUFFERED | I | J | K |
| 184PIN DIMM REGISTERED | N | O | U |
| 200PIN SO-DIMM | V | B | G |
| 172PIN Micro-DIMM | | | M |

COMPONENT REV LEVEL

PCB TYPE
G : GOLD_LEAD PLATING
W : GOLD_RoHS
L : LOW PROFILE_LEAD PLATING
X : LOW PROFILE_RoHS

COMPONENT PKG

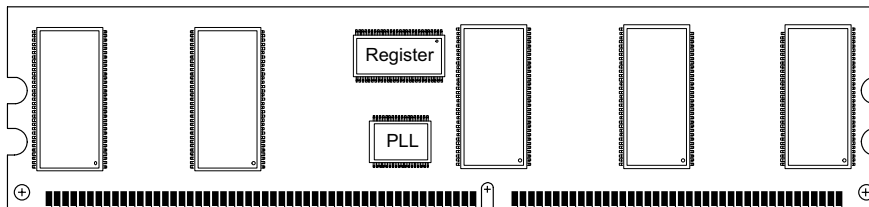
| LEAD PLATING | GREEN | PACKAGE DESCRIPTION |
|--------------|-------|---------------------|
| T | I | TSOP |
| S | J | FBGA |
| D | N | Die-stacked TSOP |
| Z | P | Die-stacked FBGA |

I/O INTERFACE
S: SSTL_2

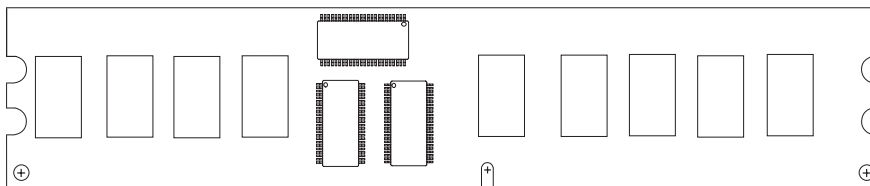
SPEED
B0 : PC2100B (133MHz @CL2.5-3-3)
B1 : PC2100A (133MHz @CL2-2-2)
C0 : PC2700 (166MHz @CL2.5-3-3)
D0 : PC3200 (200MHz @CL2.5-3-3)
D3 : PC3200 (200MHz @CL3-3-3)

*RoHS: Restriction of Hazardous Substances
*GREEN: RoHS-compliant and Halogen-Free

Low Profile Module (1.2 in)

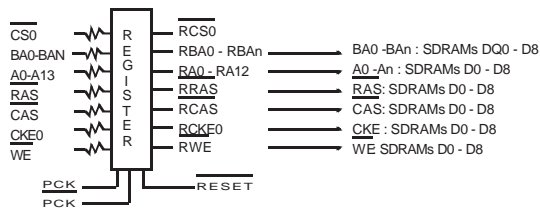
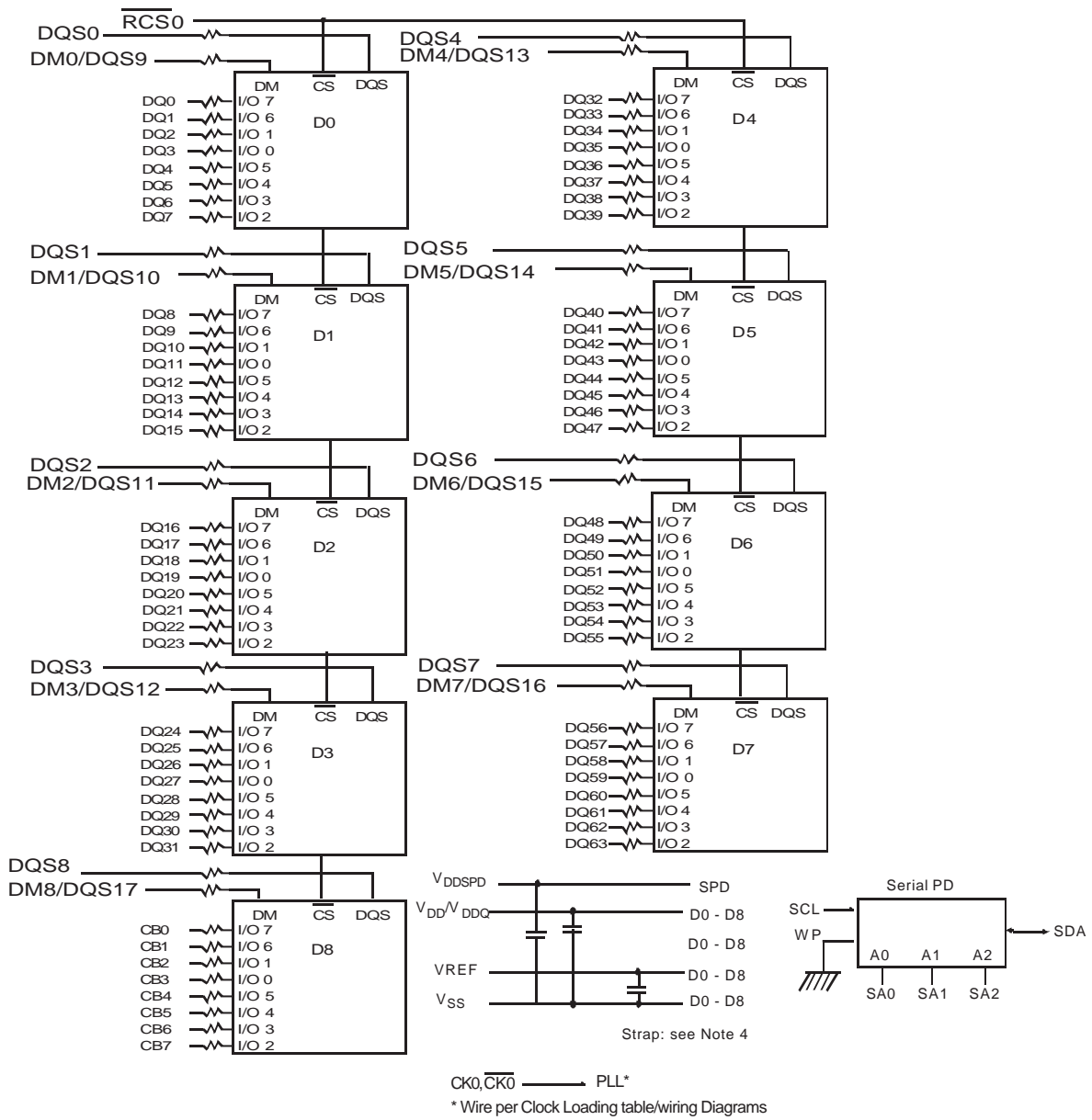


FBGA-Based Low Profile Module (1.125 in)



This 256MB Registered ECC DDR DIMM is available in three different heights: 1.7", 1.2", and 1.125". Please refer to pages 12 to 14 for the detailed mechanical diagrams of all three PCB heights.

Block Diagram



Pin Configurations (Front Side/Back Side)

| Pin | Front | Pin | Front | Pin | Front | Pin | Back | Pin | Back | Pin | Back |
|-----|-------|-----|-------|-----|-------|-----|------|-----|------|-----|--------|
| 1 | VREF | 32 | A5 | 62 | VDDQ | 93 | VSS | 124 | VSS | 154 | RAS |
| 2 | DQ0 | 33 | DQ24 | 63 | WE | 94 | DQ4 | 125 | A6 | 155 | DQ45 |
| 3 | VSS | 34 | VSS | 64 | DQ41 | 95 | DQ5 | 126 | DQ28 | 156 | VDDQ |
| 4 | DQ1 | 35 | DQ25 | 65 | CAS | 96 | VDDQ | 127 | DQ29 | 157 | CS0 |
| 5 | DQS0 | 36 | DQS3 | 66 | VSS | 97 | DM0 | 128 | VDDQ | 158 | CS1 |
| 6 | DQ2 | 37 | A4 | 67 | DQS5 | 98 | DQ6 | 129 | DM3 | 159 | DM5 |
| 7 | VDD | 38 | VDD | 68 | DQ42 | 99 | DQ7 | 130 | A3 | 160 | VSS |
| 8 | DQ3 | 39 | DQ26 | 69 | DQ43 | 100 | VSS | 131 | DQ30 | 161 | DQ46 |
| 9 | NC | 40 | DQ27 | 70 | VDD | 101 | NC | 132 | VSS | 162 | DQ47 |
| 10 | NC | 41 | A2 | 71 | NC | 102 | NC | 133 | DQ31 | 163 | NC |
| 11 | VSS | 42 | Vss | 72 | DQ48 | 103 | A13* | 134 | CB4* | 164 | VDDQ |
| 12 | DQ8 | 43 | A1 | 73 | DQ49 | 104 | VDDQ | 135 | CB5* | 165 | DQ52 |
| 13 | DQ9 | 44 | CB0* | 74 | VSS | 105 | DQ12 | 136 | VDDQ | 166 | DQ53 |
| 14 | DQS1 | 45 | CB1* | 75 | CK2 | 106 | DQ13 | 137 | CK0* | 167 | NC |
| 15 | VDDQ | 46 | VDD | 76 | CK2 | 107 | DM1 | 138 | CK0* | 168 | VDD |
| 16 | CK1 | 47 | DQS8* | 77 | VDDQ | 108 | VDD | 139 | VSS | 169 | DM6 |
| 17 | CK1 | 48 | A0 | 78 | DQS6 | 109 | DQ14 | 140 | DM8* | 170 | DQ54 |
| 18 | VSS | 49 | CB2* | 79 | DQ50 | 110 | DQ15 | 141 | A10 | 171 | DQ55 |
| 19 | DQ10 | 50 | VSS | 80 | DQ51 | 111 | CKE1 | 142 | CB6* | 172 | VDDQ |
| 20 | DQ11 | 51 | CB3* | 81 | VSS | 112 | VDDQ | 143 | VDDQ | 173 | NC |
| 21 | CKE0 | 52 | BA1 | 82 | VDDID | 113 | BA2* | 144 | CB7* | 174 | DQ60 |
| 22 | VDDQ | Key | | 83 | DQ56 | 114 | DQ20 | Key | | 175 | DQ61 |
| 23 | DQ16 | 53 | DQ32 | 84 | DQ57 | 115 | A12 | 145 | VSS | 176 | VSS |
| 24 | DQ17 | 54 | VDDQ | 85 | VDD | 116 | VSS | 146 | DQ36 | 177 | DM7 |
| 25 | DQS2 | 55 | DQ33 | 86 | DQS7 | 117 | DQ21 | 147 | DQ37 | 178 | DQ62 |
| 26 | VSS | 56 | DQS4 | 87 | DQ58 | 118 | A11 | 148 | VDD | 179 | DQ63 |
| 27 | A9 | 57 | DQ34 | 88 | DQ59 | 119 | DM2 | 149 | DM4 | 180 | VDDQ |
| 28 | DQ18 | 58 | VSS | 89 | VSS | 120 | VDD | 150 | DQ38 | 181 | SA0 |
| 29 | A7 | 59 | BA0 | 90 | NC | 121 | DQ22 | 151 | DQ39 | 182 | SA1 |
| 30 | VDDQ | 60 | DQ35 | 91 | SDA | 122 | A8 | 152 | VSS | 183 | SA2 |
| 31 | DQ19 | 61 | DQ40 | 92 | SCL | 123 | DQ23 | 153 | DQ44 | 184 | VDDSPD |

Pin Names

| Pin | Pin Description |
|--------------------|----------------------------|
| CK1, CK1, CK2, CK2 | Differential Clock Inputs |
| CS0 | Chip Select Input |
| CKE0 | Clock Enable Input |
| RAS, CAS, WE | Command Sets Inputs |
| A0 ~ A12 | Address |
| BA0, BA1 | Bank Address |
| DQ0~DQ63 | Data Inputs/Outputs |
| DQS0~DQS7 | Data Strobe Inputs/Outputs |
| DM0~DM7 | Data-in Mask |

| Pin | Pin Description |
|---------|------------------------------------|
| VDD | Power Supply |
| VDDQ | DQs Power Supply |
| VSS | Ground |
| VREF | Reference Power Supply |
| VDDSPD | Power Supply for SPD |
| SA0~SA2 | E ² PROM Address Inputs |
| SCL | E ² PROM Clock |
| SDA | E ² PROM Data I/O |
| VDDID | VDD Identification Flag |
| DU | Do not Use |
| NC | No Connection |

Serial Presence Detect Information

Bin Sort:

D0 (PC3200 @ CL 2.5-3-3)

D3 (PC3200 @ CL 3-3-3)

C0 (PC2700 @ CL 2.5-3-3)

| Byte # | Function described | Function Supported | | | Hex value | | |
|--------|--|---|---------|---------|-----------|-----|-----|
| | | D0 | D3 | C0 | D0 | D3 | C0 |
| 0 | Defines # of Bytes written into serial memory at module manufacturer | 128bytes | | | 80h | | |
| 1 | Total # of Bytes of SPD memory device | 256bytes | | | 08h | | |
| 2 | Fundamental memory type | SDRAM DDR | | | 07h | | |
| 3 | # of row address on this assembly | 13 | | | 0Dh | | |
| 4 | # of column address on this assembly | 10 | | | 0Ah | | |
| 5 | # of module Rows on this assembly | 1 Bank | | | 01h | | |
| 6 | Data width of this assembly | 72 bits | | | 48h | | |
| 7 |Data width of this assembly | - | | | 00h | | |
| 8 | VDDQ and interface standard of this assembly | SSTL 2.5V | | | 04h | | |
| 9 | DDR SDRAM cycle time at highest CAS Latency | 5ns | 5ns | 6ns | 50h | 50h | 60h |
| 10 | DDR SDRAM Access time from clock at highest CL | ±0.65ns | ±0.65ns | ±0.70ns | 65h | 65h | 70h |
| 11 | DIMM configuration type(Non-parity, Parity, ECC) | Non-parity, ECC | | | 02h | | |
| 12 | Refresh rate & type | 7.8us & Self refresh | | | 82h | | |
| 13 | Primary DDR SDRAM width | x8 | | | 08h | | |
| 14 | Error checking DDR SDRAM data width | x8 | | | 08h | | |
| 15 | Minimum clock delay for back-to-back random column address | t _{CCD} =1CLK | | | 01h | | |
| 16 | DDR SDRAM device attributes : Burst lengths supported | 2,4,8 | | | 0Eh | | |
| 17 | DDR SDRAM device attributes : # of banks on each DDR SDRAM | 4 banks | | | 04h | | |
| 18 | DDR SDRAM device attributes : CAS Latency supported | 2,2.5,3 | | | 1Ch | 1Ch | 0Ch |
| 19 | DDR SDRAM device attributes : CS Latency | 0CLK | | | 01h | | |
| 20 | DDR SDRAM device attributes : WE Latency | 1CLK | | | 02h | | |
| 21 | DDR SDRAM module attributes | Registered address & control inputs and On-card DLL | | | 26h | | |
| 22 | DDR SDRAM device attributes : General | +/-0.2V voltage tolerance | | | 00h | | |
| 23 | DDR SDRAM cycle time at second highest CL | 5.0ns | 6.0ns | 7.5ns | 50h | 60h | 75h |
| 24 | DDR SDRAM Access time from clock at second highest CL | ±0.65ns | ±0.70ns | ±0.70ns | 65h | 70h | 70h |
| 25 | DDR SDRAM cycle time at third highest CL | 7.5ns | 7.5ns | - | 75h | 75h | 00h |
| 26 | DDR SDRAM Access time from clock at third highest CL | ±0.75ns | ±0.75ns | - | 75h | 75h | 00h |
| 27 | Minimum row precharge time (=t _{RP}) | 15ns | 15ns | 18ns | 3Ch | 3Ch | 48h |
| 28 | Minimum row activate to row active delay (=t _{RRD}) | 10ns | 10ns | 12ns | 28h | 28h | 30h |

Serial Presence Detect Information (cont.)

| Byte # | Function described | Function Supported | | | Hex value | | |
|-------------|--|----------------------------|--------|---------|-----------|-----|-----|
| | | D0 | D3 | C0 | D0 | D3 | C0 |
| 29 | Minimum RAS to CAS delay ($=t_{RCD}$) | 15ns | 15ns | 18ns | 3Ch | 3Ch | 48h |
| 30 | Minimum active to precharge time ($=t_{RAS}$) | 40ns | 40ns | 42ns | 28h | 28h | 2Ah |
| 31 | Module ROW density | 256MB | | | 40h | | |
| 32 | Command and address signal input setup time | 0.6ns | 0.6ns | 0.75ns | 60h | 60h | 75h |
| 33 | Command and address signal input hold time | 0.6ns | 0.6ns | 0.75ns | 60h | 60h | 75h |
| 34 | Data signal input setup time | 0.4ns | 0.4ns | 0.45ns | 40h | 40h | 45h |
| 35 | Data signal input hold time | 0.4ns | 0.4ns | 0.45ns | 40h | 40h | 45h |
| 36-40 | Superset information (may be used in future) | | | | 00h | | |
| 41 | SDRAM device minimum active to active/auto-refresh time ($=t_{RC}$) | 60ns | 60ns | 60ns | 3Ch | 3Ch | 3Ch |
| 42 | SDRAM device minimum active to autorefresh to active/auto-re- fresh time ($=t_{RFC}$) | 70ns | 70ns | 72ns | 46h | 46h | 48h |
| 43 | SDRAM device maximum device cycle time ($=t_{CK MAX}$) | 12ns | 12ns | 12ns | 30h | 30h | 30h |
| 44 | SDRAM device maximum skew between DQS and DQ signals ($=t_{DQSQ}$) | 0.4ns | 0.4ns | 0.45ns | 28h | 28h | 2Dh |
| 45 | SDRAM device maximum read datahold skew factor ($=t_{QHS}$) | 0.55ns | 0.55ns | 0.60 ns | 55h | 55h | 60h |
| 46-61 | Superset information (may be used in future) | - | | | 00h | | |
| 62 | SPD data revision code | Initial release | | | 11h | 11h | 00h |
| 63 | Checksum for Bytes 0 ~ 62 | - | | | BBh | D6h | 63h |
| 64 | Manufacturer JEDEC ID code | ProMOS | | | 40h | | |
| 65-71 | Manufacturer JEDEC ID code | | | | 00h | | |
| 72 | Manufacturing location | 02=Taiwan 05=China 0A=S-CH | | | | | |
| 73-90 | Module part number (ASCII) | V827432U24SC | | | | | |
| 91 | Manufacturer revision code (For PCB) | 0 | | | 00 | | |
| 92 | Manufacturer revision code (For component) | 0 | | | 00 | | |
| 93 | Manufacturing date (Year) | - | | | - | | |
| 94 | Manufacturing date (Week) | - | | | - | | |
| 95-98 | Assembly serial # | - | | | - | | |
| 99- 127 | Manufacturer specific data (may be used in future) | Undefined | | | 00h | | |
| 128- 255 | Open for customer use | Undefined | | | 00h | | |

DC Operating Conditions

(T_A = 0 to 70°C, Voltage referenced to V_{SS} = 0V)

| Parameter | Symbol | Min | Typ. | Max | Unit | Note |
|--|------------------|---------------------------|------------------|---------------------------|------|------|
| Power Supply Voltage | V _{DD} | 2.3 | 2.5 | 2.7 | V | |
| Power Supply Voltage for DDR400 | V _{DD} | 2.5 | 2.6 | 2.7 | V | |
| Power Supply Voltage | V _{DDQ} | 2.3 | 2.5 | 2.7 | V | 1 |
| Power Supply Voltage for DDR400 | V _{DDQ} | 2.5 | 2.6 | 2.7 | V | 1 |
| Input High Voltage | V _{IH} | V _{REF} + 0.15 | - | V _{DDQ} + 0.3 | V | |
| Input Low Voltage | V _{IL} | -0.3 | - | V _{REF} - 0.15 | V | 2 |
| I/O Termination Voltage | V _{TT} | V _{REF} - 0.04 | V _{REF} | V _{REF} + 0.04 | V | |
| Reference Voltage | V _{REF} | V _{DDQ/2} - 0.05 | - | V _{DDQ/2} + 0.05 | V | |
| Input Leakage Current | I _I | -2 | - | 2 | μA | |
| Output Leakage Current | I _{OZ} | -5 | - | 5 | μA | |
| Output High Current (V _{OUT} = 1.95V) | I _{OH} | -16.8 | - | - | mA | |
| Output Low Current (V _{OUT} = 0.35V) | I _{OL} | 16.8 | - | - | mA | |

- Notes:** 1. V_{DDQ} must not exceed the level of V_{DD}.
 2. V_{IL} (min) is acceptable -1.5V AC pulse width with <= 5ns of duration.

AC Operating Conditions

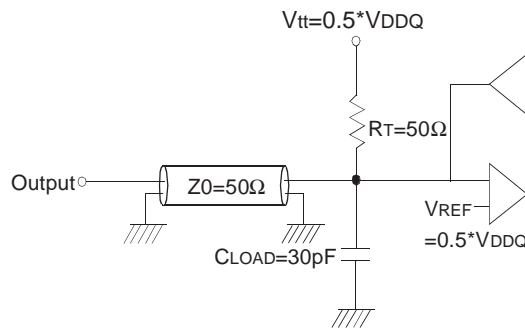
(T_A = 0 to 70 °C, Voltage referenced to V_{SS} = 0V)

| Parameter | Symbol | Min | Max | Unit | Note |
|---|---------------------|--------------------------|--------------------------|------|------|
| Input High (Logic 1) Voltage, DQ, DQS and DM signals | V _{IH(AC)} | V _{REF} + 0.31 | | V | |
| Input Low (Logic 0) Voltage, DQ, DQS and DM signals | V _{IL(AC)} | | V _{REF} - 0.31 | V | |
| Input Differential Voltage, CK and \overline{CK} inputs | V _{ID(AC)} | 0.7 | V _{DDQ} + 0.6 | V | 1 |
| Input Crossing Point Voltage, CK and \overline{CK} inputs | V _{IX(AC)} | 0.5*V _{DDQ-0.2} | 0.5*V _{DDQ+0.2} | V | 2 |

- Notes:** 1. VID is the magnitude of the difference between the input level on CK and the input on \overline{CK} .
 2. The value of VIX is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same.

AC Operating Test Conditions ($T_A = 0$ to 70°C , Voltage referenced to $V_{SS} = 0\text{V}$)

| Parameter | Value | Unit |
|---|----------------------|------|
| Reference Voltage | $V_{DDQ} \times 0.5$ | V |
| Termination Voltage | $V_{DDQ} \times 0.5$ | V |
| AC Input High Level Voltage (V_{IH} , min) | $V_{REF} + 0.31$ | V |
| AC Input Low Level Voltage (V_{IL} , max) | $V_{REF} - 0.31$ | V |
| Input Timing Measurement Reference Level Voltage | V_{REF} | V |
| Output Timing Measurement Reference Level Voltage | V_{TT} | V |
| Input Signal maximum peak swing | 1.5 | V |
| Input minimum Signal Slew Rate | 1 | V/ns |
| Termination Resistor (R_T) | 50 | Ohm |
| Series Resistor (R_S) | 25 | Ohm |
| Output Load Capacitance for Access Time Measurement (C_L) | 30 | pF |



Output Load Circuit (SSTL_2)

Input/Output Capacitance

($V_{DD} = 2.5\text{V}$, $V_{DD} = 2.6\text{V}$ for DDR400, $V_{DDQ} = 2.5\text{V}$, $V_{DDQ} = 2.6\text{V}$ for DDR400, $T_A = 25^\circ\text{C}$, $f = 1\text{MHz}$)

| Parameter | Symbol | Min | Max | Unit |
|--|-----------|-----|-----|------|
| Input capacitance ($A_0 \sim A_{11}$, $BA_0 \sim BA_1$, \overline{RAS} , \overline{CAS} , \overline{WE}) | C_{IN1} | 60 | 75 | pF |
| Input capacitance (CKE_0) | C_{IN2} | 40 | 48 | pF |
| Input capacitance (\overline{CS}_0) | C_{IN3} | 40 | 48 | pF |
| Input capacitance (CLK_1 , CLK_2) | C_{IN4} | 30 | 32 | pF |
| Data & DQS input/output capacitance ($DQ_0 \sim DQ_{63}$) | C_{OUT} | 10 | 12 | pF |
| Input capacitance ($DM_0 \sim DM_8$) | C_{IN5} | 10 | 12 | pF |

DDR SDRAM I_{DD} SPEC TABLE

| Symbol | | D0 / D3 PC3200A@ CL=3 | C0 PC2700A@ CL=2.5 | Unit |
|--------|-----------|-----------------------------|--------------------------|------|
| IDD0 | | 1100 | 990 | mA |
| IDD1 | | 1340 | 1260 | mA |
| IDD2P | | 260 | 225 | mA |
| IDD2F | | 450 | 405 | mA |
| IDD2Q | | 350 | 396 | mA |
| IDD3P | | 260 | 225 | mA |
| IDD3N | | 1060 | 720 | mA |
| IDD4R | | 2300 | 2070 | mA |
| IDD4W | | 2100 | 1890 | mA |
| IDD5 | | 1900 | 1800 | mA |
| IDD6 | Normal | 27 | 27 | mA |
| | Low power | 17 | 17 | mA |
| IDD7 | | 3200 | 3150 | mA |

* Module I_{DD} was calculated on the basis of component I_{DD} and can be differently measured according to DQ loading cap.

Detailed test conditions for DDR SDRAM IDD1 & IDD

IDD1 : Operating current: One bank operation

1. Typical Case : V_{dd} = 2.5V, T=25' C
2. Worst Case : V_{dd} = 2.7V, T= 10' C
3. Only one bank is accessed with t_{RC}(min), Burst Mode, Address and Control inputs on NOP edge are changing once per clock cycle. I_{out} = 0mA
4. Timing patterns
 - DDR333 (166MHz, CL=2.5) : t_{CK}=6ns, CL=2.5, BL=4, t_{RCD}=3*t_{CK}, t_{RC}=10*t_{CK}, t_{RAS}=7*t_{CK}
Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
*50% of data changing at every burst
 - DDR400B (200MHz, CL=3) : t_{CK}=5ns, CL=3, BL=4, t_{RCD}=3*t_{CK}, t_{RC}=12*t_{CK}, t_{RAS}=8*t_{CK}
Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
*50% of data changing at every burst
 - DDR400A (200MHz, CL=2.5) : t_{CK}=5ns, CL=2.5, BL=4, t_{RCD}=3*t_{CK}, t_{RC}=12*t_{CK}, t_{RAS}=8*t_{CK}
Read : A0 N N R0 N P0 N N N A0 N - repeat the same timing with random address changing
*50% of data changing at every burst

Legend : A=Activate, R=Read, W=Write, P=Precharge, N=NOP

AC Characteristics (AC operating conditions unless otherwise noted)

| Parameter | Symbol | DDR400A D0 | | DDR400B D3 | | DDR333 C0 | | Unit | Note | |
|--|--------------------------------|-------------------------|------|-------------------------|------|-------------------------|------|------|---------|--|
| | | Min | Max | Min | Max | Min | Max | | | |
| Row Cycle Time | t_{RC} | 60 | - | 60 | - | 60 | - | ns | | |
| Auto Refresh Row Cycle Time | t_{RFC} | 70 | - | 70 | - | 72 | - | ns | | |
| Row Active Time | t_{RAS} | 40 | 120K | 40 | 120K | 42 | 120K | ns | | |
| Row Address to Column Address Delay | t_{RCD} | 15 | - | 15 | - | 18 | - | ns | | |
| Row Active to Row Active Delay | t_{RRD} | 10 | - | 10 | - | 12 | - | ns | | |
| Column Address to Column Address Delay | t_{CCD} | 1 | - | 1 | - | 1 | - | CLK | | |
| Row Precharge Time | t_{RP} | 15 | - | 15 | - | 18 | - | ns | | |
| Write Recovery Time | t_{WR} | 15 | - | 15 | - | 12 | - | ns | | |
| Last Data-In to Read Command | t_{DRL} | 1 | - | 1 | - | 1 | - | CLK | | |
| Auto Precharge Write Recovery + Precharge Time | t_{DAL} | 35 | - | 35 | - | 35 | - | ns | | |
| System Clock Cycle Time | \overline{CAS} Latency = 3 | t_{CK} | 5 | 12 | 5 | 12 | - | - | ns | |
| | \overline{CAS} Latency = 2.5 | | 5 | 12 | 6 | 12 | 6 | 12 | ns | |
| | \overline{CAS} Latency = 2 | | 7.5 | 12 | 7.5 | 12 | 7.5 | 12 | ns | |
| Clock High Level Width | t_{CH} | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | CLK | | |
| Clock Low Level Width | t_{CL} | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | CLK | | |
| Data-Out edge to Clock edge Skew | t_{AC} | 0.45 | 0.55 | 0.45 | 0.55 | -0.75 | 0.75 | ns | | |
| DQS-Out edge to Clock edge Skew | t_{DQSK} | -0.65 | 0.65 | -0.65 | 0.65 | -0.75 | 0.75 | ns | | |
| DQS-Out edge to Data-Out edge Skew | t_{DQSQ} | -0.60 | 0.60 | -0.60 | 0.60 | - | 0.45 | ns | | |
| Data-Out hold time from DQS | t_{QH} | - | 0.40 | - | 0.40 | t_{HPmin} -0.75 ns | - | ns | 1 | |
| Clock Half Period | t_{HP} | t_{HPmin} -0.75 ns | - | t_{HPmin} -0.75 ns | - | $t_{CH/L}$ min | - | ns | 1 | |
| Input Setup Time (fast slew rate) | t_{IS} | $t_{CH/L}$ min | - | $t_{CH/L}$ min | - | 0.75 | - | ns | 2,3,5,6 | |
| Input Hold Time (fast slew rate) | t_{IH} | 0.6 | - | 0.6 | - | 0.75 | - | ns | 2,3,5,6 | |
| Input Setup Time (slow slew rate) | t_{IS} | 0.6 | - | 0.6 | - | 0.8 | - | ns | 2,4,5,6 | |
| Input Hold Time (slow slew rate) | t_{IH} | 0.75 | - | 0.75 | - | 0.8 | - | ns | 2,4,5,6 | |
| Input Pulse Width | t_{IPW} | 0.75 | - | 0.75 | - | 0.4 | 0.6 | ns | 6 | |
| Write DQS High Level Width | t_{DQSH} | 0.4 | 0.6 | 0.4 | 0.6 | 0.4 | 0.6 | CLK | | |
| Write DQS Low Level Width | t_{DQSL} | 0.35 | | 0.35 | | 0.75 | 1.25 | CLK | | |
| CLK to First Rising edge of DQS-In | t_{DQSS} | 0.35 | | 0.35 | | 0.45 | - | CLK | | |
| Data-In Setup Time to DQS-In (DQ & DM) | t_{DS} | 0.72 | 1.25 | 0.72 | 1.25 | 0.45 | - | ns | 7 | |
| Data-in Hold Time to DQS-In (DQ & DM) | t_{DH} | 0.40 | - | 0.40 | - | 1.75 | - | ns | 7 | |

AC Characteristics (cont.)

| Parameter | Symbol | DDR400A D0 | | DDR400B D3 | | DDR333 C0 | | Unit | Note |
|---------------------------------------|-------------|------------|-----|------------|-----|-----------|-----|------|------|
| | | Min | Max | Min | Max | Min | Max | | |
| DQ & DM Input Pulse Width | t_{DIPW} | 1.75 | - | 1.75 | - | 0.9 | 1.1 | ns | |
| Read DQS Preamble Time | t_{RPRE} | 0.9 | 1.1 | 0.9 | 1.1 | 0.4 | 0.6 | CLK | |
| Read DQS Postamble Time | t_{RPST} | 0.4 | 0.6 | 0.4 | 0.6 | 0 | - | CLK | |
| Write DQS Preamble Setup Time | t_{WPRES} | 0 | - | 0 | - | 0.25 | - | CLK | |
| Write DQS Preamble Hold Time | t_{WPREH} | 0.25 | - | 0.25 | - | 0.4 | 0.6 | CLK | |
| Write DQS Postamble Time | t_{WPST} | 0.4 | 0.6 | 0.4 | 0.6 | 2 | - | CLK | |
| Mode Register Set Delay | t_{MRD} | 2 | - | 2 | - | 10 | - | CLK | |
| Power Down Exit Time | t_{PDEX} | 1 | - | 1 | - | 75 | - | ns | |
| Exit Self Refresh to Non-Read Command | t_{XSNR} | 75 | - | 75 | - | 75 | - | ns | |
| Exit Self Refresh to Read Command | t_{XSRD} | 200 | - | 200 | - | 200 | - | CLK | 8 |
| Average Periodic Refresh Interval | t_{REFI} | - | 7.8 | - | 7.8 | - | 7.8 | us | |

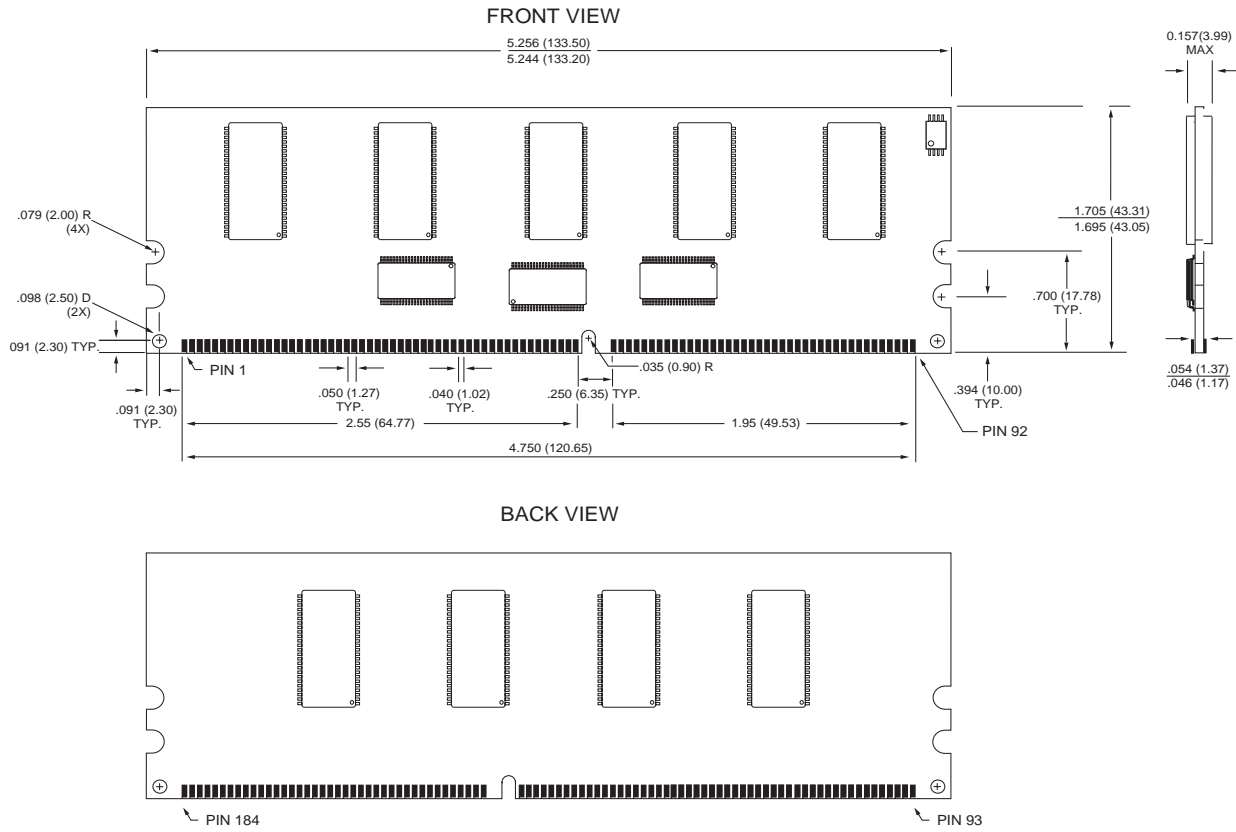
- Notes:**
1. This calculation accounts for $t_{DQSQ(max)}$, the pulse width distortion of on-chip circuit and jitter.
 2. Data sampled at the rising edges of the clock : A0~A11, BA0~BA1, CKE, CS, RAS, CAS, WE.
 3. For command/address input slew rate $\geq 1.0V/ns$
 4. For command/address input slew rate $\geq 0.5V/ns$ and $< 1.0V/ns$
 5. CK, \overline{CK} slew rates are $\geq 1.0V/ns$
 6. These parameters guarantee device timing, but they are not necessarily tested on each device, and they may be guaranteed by design or tester correlation.
 7. Data latched at both rising and falling edges of Data Strobes(DQS) : DQ, DM
 8. Minimum of 200 cycles of stable input clocks after Self Refresh Exit command, where CKE is held high, is required to complete Self Refresh Exit and lock the internal DLL circuit of DDR SDRAM

Absolute Maximum Ratings

| Parameter | Symbol | Rating | Unit |
|---|-------------------|------------|----------|
| Ambient Temperature | T_A | 0 ~ 70 | °C |
| Storage Temperature | T_{STG} | -55 ~ 125 | °C |
| Voltage on Any Pin relative to V_{SS} | V_{IN}, V_{OUT} | -0.5 ~ 3.6 | V |
| Voltage on V_{DD} relative to V_{SS} | V_{DD} | -0.5 ~ 3.6 | V |
| Voltage on V_{DDQ} relative to V_{SS} | V_{DDQ} | -0.5 ~ 3.6 | V |
| Output Short Circuit Current | I_{OS} | 50 | mA |
| Power Dissipation | P_D | 11 | W |
| Soldering Temperature • Time | T_{SOLDER} | 260 • 10 | °C • Sec |

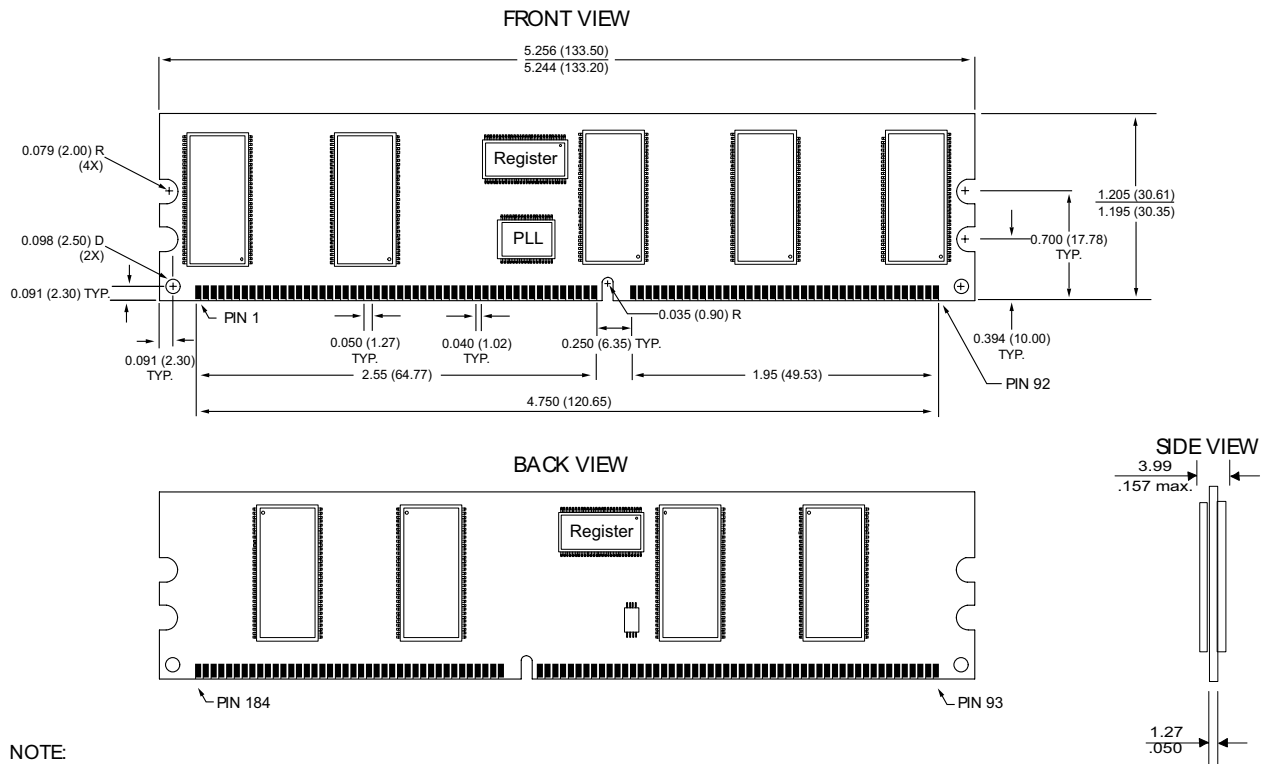
Note: Operation at above absolute maximum rating can adversely affect device reliability

Module Dimensions (V827432U24SXTG)



NOTE: 1. All dimensions in inches (millimeters) $\frac{MAX}{MIN}$ or typical where noted.

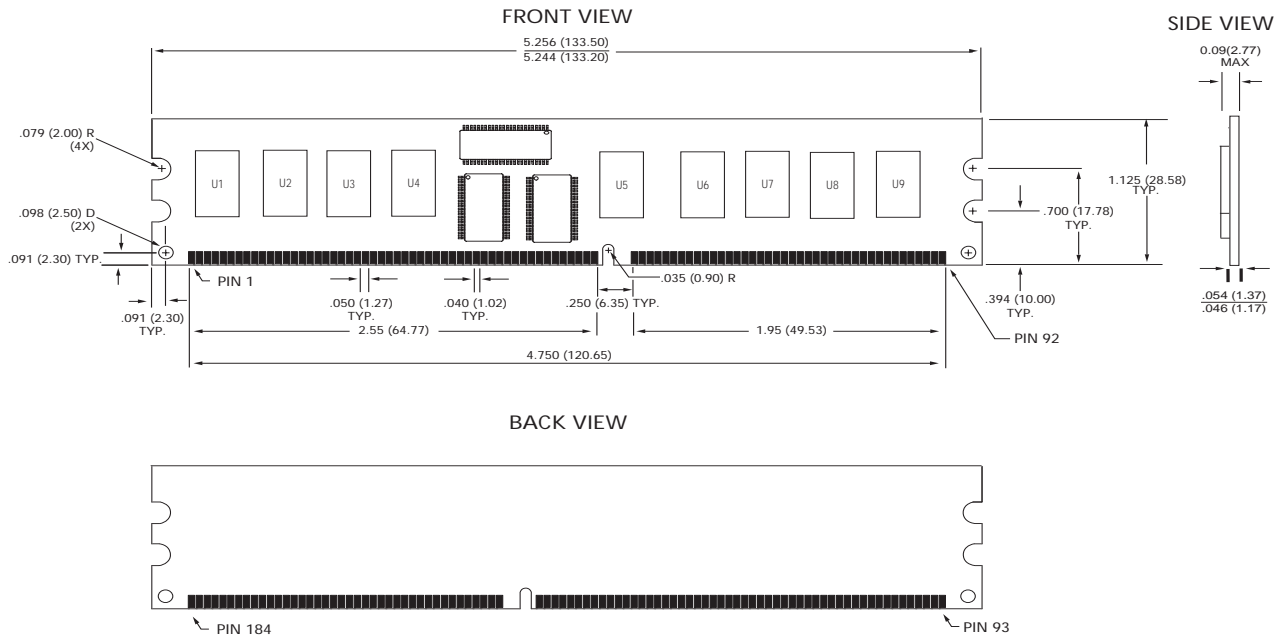
Module Dimensions (Low Profile V827432U24SXTL)



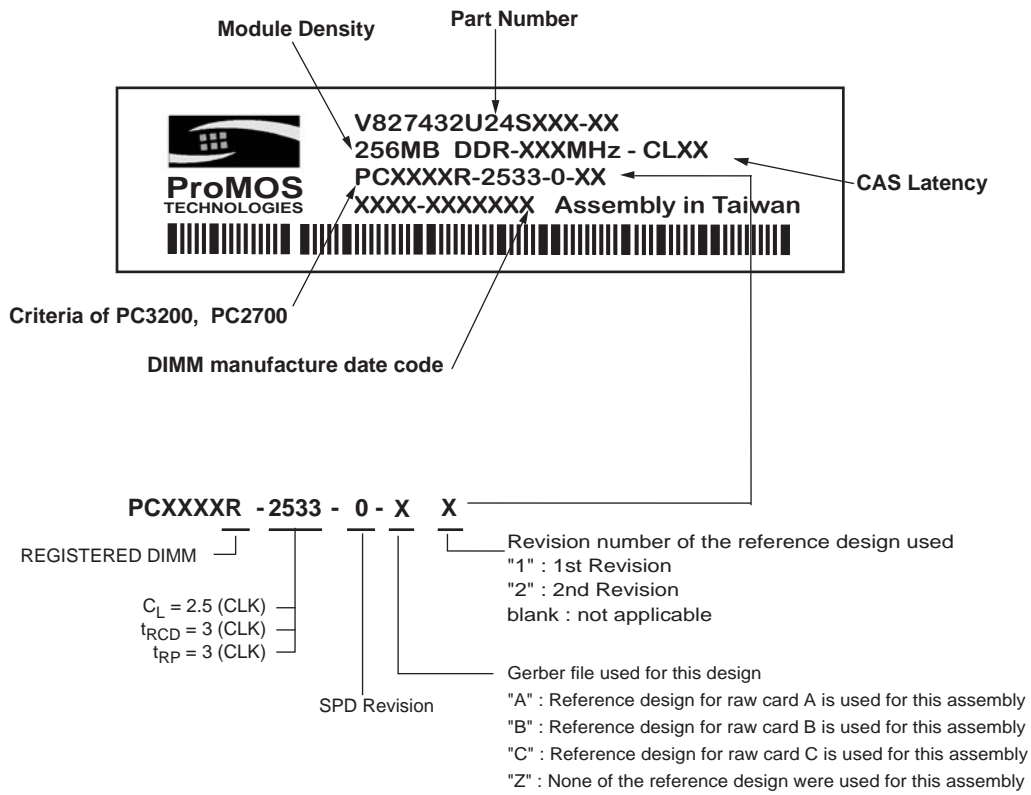
NOTE:

All dimensions are in inches (millimeters) $\frac{\text{MAX}}{\text{MIN}}$ or typical where noted.

Module Dimensions (FBGA-Based V827432U24SXSG)



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