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# M61556FP

## 100 W 1-Channel Amplifier Predriver

REJ03F0089-0100Z

Rev.1.0

Sep.19.2003

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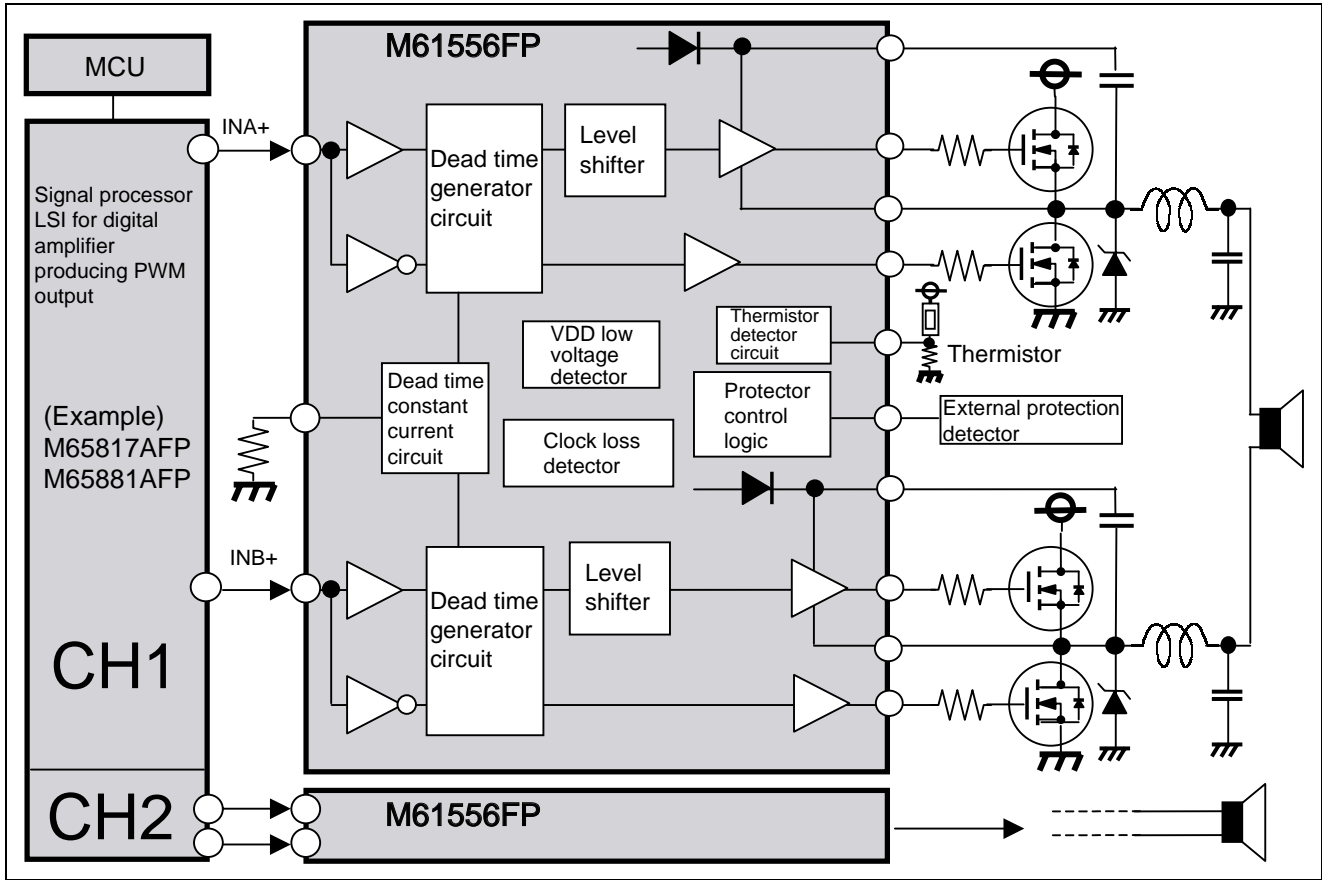
### Description

The M61556FP is a predriver IC developed for use as the output driver of a digital audio power amplifier. It can be combined with an N-channel MOSFET to create a 100 W, 1-channel (8 $\Omega$  load) digital amplifier. (The 200 W version, the M61557FP, is pin compatible with the M61556FP.)

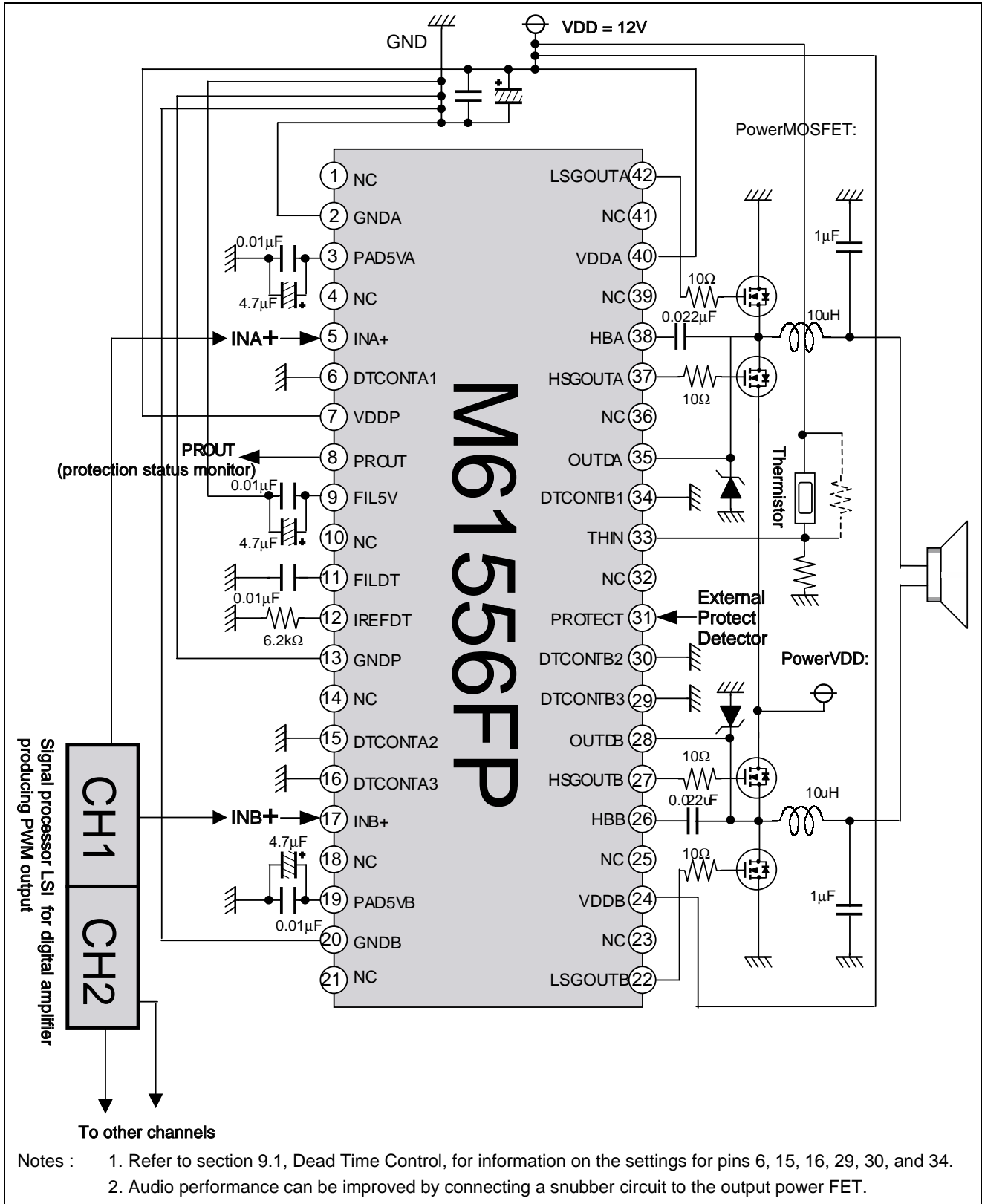
### Features

- On-chip dead time adjustment circuit: Supports easy adjustment by connecting a single resistor. (H-L dead time can be fine adjusted independently for sides A and B.)
- Suitable for driving full-bridge N-channel MOSFET devices.
- Maximum bootstrap supply voltage: 88 V (peak value)
- Supports high-speed switching.
- On-chip diode for bootstrap circuit.
- On-chip VDD low voltage detector circuit.
- On-chip clock loss detector circuit.
- Output impedance: 2.5  $\Omega$
- Input is TTL level, allowing connecting to 3.3 V or 5 V processors.

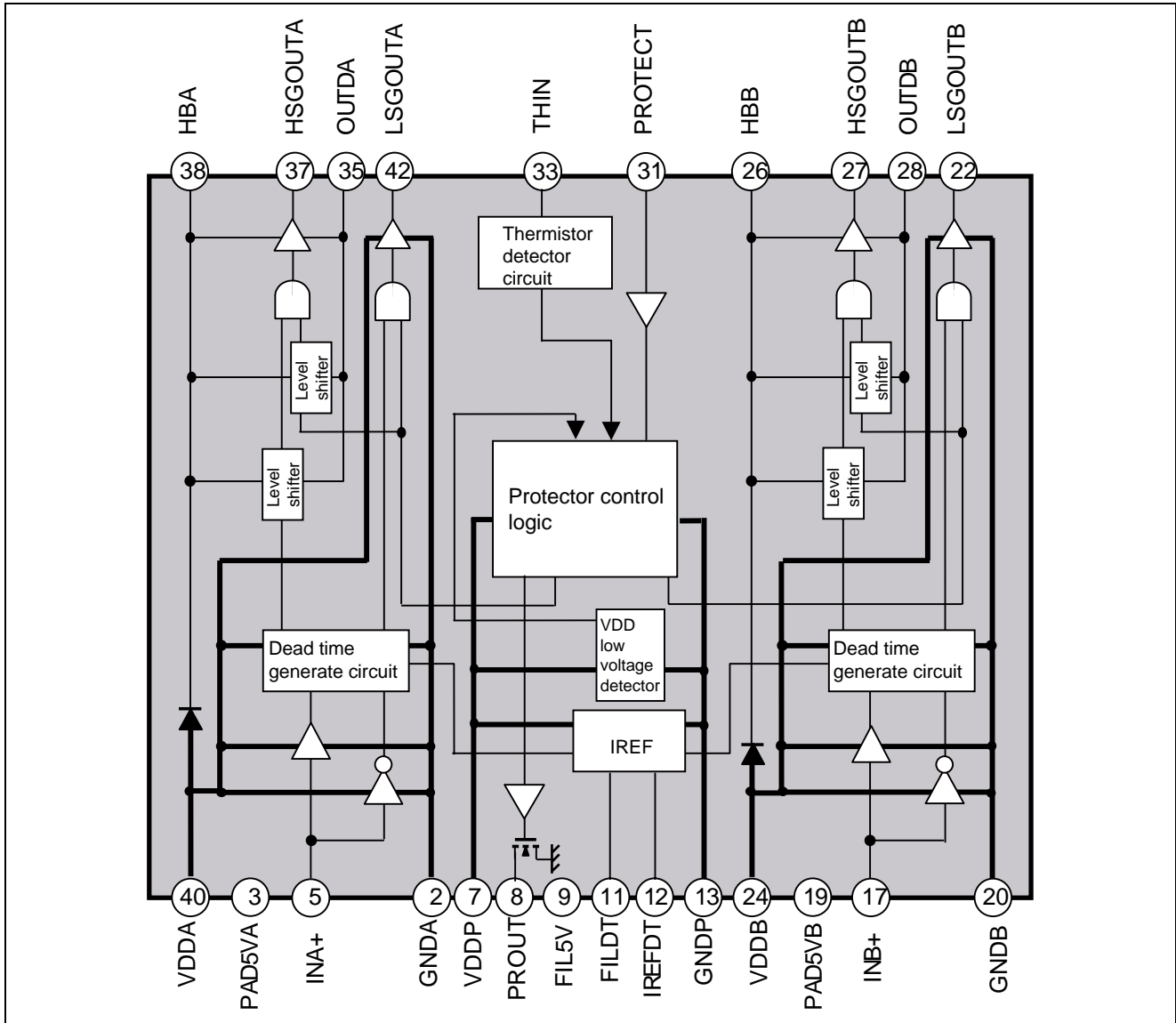
System Block Diagram (Stereo Configuration)



Sample Application Circuit



Block diagram



## Pin Descriptions

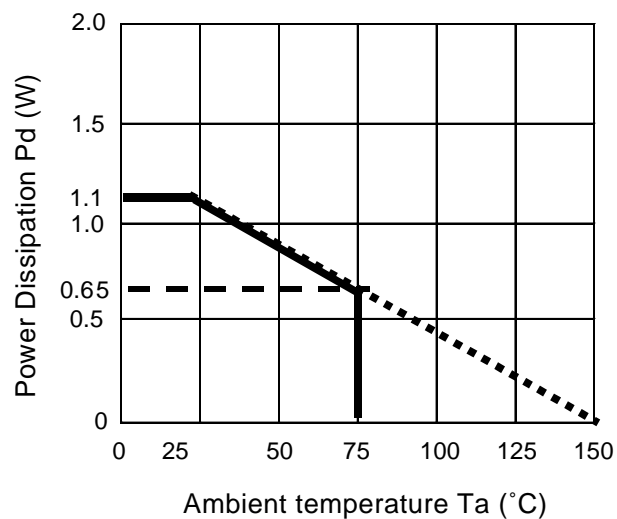
Pin No.	Pin Name	Pin Description	
Side-A control (pre) block	2	GNDA	Ground pin for side-A control circuit
	3	PADVA	Side-A filter pin for generating 5 V power supply on-chip
	5	INA+	Side-A PWM + input pin (high side)
	40	VDDA	Power supply pin for side-A control circuit
	42	LSGOUTA	Side-A low side prebuffer output
	35	OUTDA	Virtual VSS connector pin for side-A high side bootstrap capacitor
	37	HSGOUTA	Side-A high side prebuffer output
	38	HBA	Bootstrap capacitor connector pin power supply pin for side-A high side. Power is supplied to the high side control circuit from a bootstrap circuit.
	6	DTCONTA1	Pin 1 for adjusting dead time high/low differential
	15	DTCONTA2	Pin 2 for adjusting dead time high/low differential
16	DTCONTA3	Pin 3 for adjusting dead time high/low differential	
A/B common protection block	7	VDDP	Power supply pin for common circuit block
	8	RPOUT	Protection factor detect output pin. A low-level signal (when pull-up is applied) is output if protection factor is detected (open drain output).
	9	FIL5V	Filter pin for generating 5 V power supply on-chip
	11	FILDT	Filter pin for dead time circuit
	12	IREFDT	Connector pin for dead time adjustment resistor
	13	GNDP	Ground pin for common circuit block
	31	PROTECT	Input pin for external protection control signals
	33	THIN	Input pin for external thermistor circuit detect voltage
Side-B control (pre) block	17	INB+	Side-B PWM + input pin (high side)
	19	PAD5VB	Side-B filter pin for generating 5 V power supply on-chip
	20	GNDB	Ground pin for side-B control circuit
	26	HBB	Bootstrap capacitor connection pin power supply pin for side-B high side. Power is supplied to the high side control circuit from a bootstrap circuit.
	27	HSGOUTB	Side-B high side prebuffer output
	28	OUTDB	Virtual VSS connector pin for side-B high side bootstrap capacitor
	22	LSGOUTB	Side-B low side prebuffer output
	24	Vddb	Power supply pin for side-B control circuit
	34	DTCONTB1	Pin 1 for adjusting dead time high/low differential
	30	DTCONTB2	Pin 2 for adjusting dead time high/low differential
	29	DTCONTB3	Pin 3 for adjusting dead time high/low differential

## Absolute Maximum Ratings

Parameter	Symbol	Ratings	Units	Conditions
HBA, HBB	HBA, HBB	88*	V	HBA and HBB pin voltage
Maximum rated operating voltage				
Absolute maximum rated voltage	VDD	16	V	VDD power supply voltage
Input pin application voltage	V <sub>in</sub>	-0.3 to 5.5	V	
Internal power consumption	P <sub>d</sub>	1.1	W	
Junction temperature	T <sub>j</sub>	150	°C	
Operating temperature range	T <sub>a</sub>	-20 to +75	°C	
Storage temperature	T <sub>stg</sub>	-40 to +125	°C	

Note : \* HB pin values include peak values for ringing voltage, etc.

Derating Curve



### Recommended Operating Condition

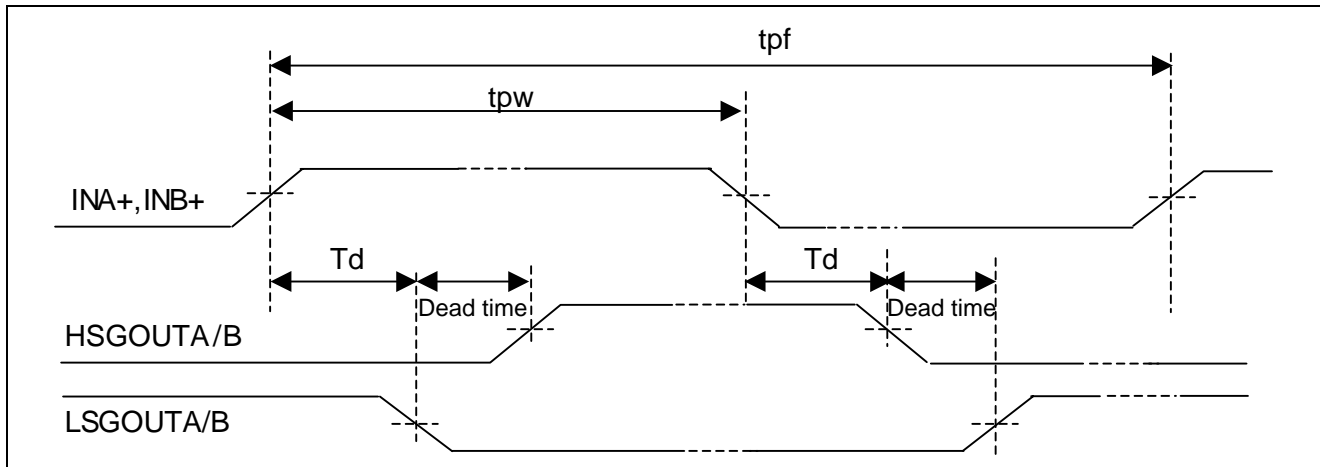
Item	Symbol	Rated value			Unit	Condition
		Min.	Typ.	Max.		
Power supply voltage for common circuit and control circuit blocks	VDD	10.8	12	13.2	V	VDDA (pin 40), VDDB (pin 24) VDDP (pin 7)
High input voltage	VIH	2.2	—	5.3	V	INA+ (pin 5), INB+ (pin 17)
Low input voltage	VIL	-0.25	—	0.8	V	

## Electrical characteristics

(Unless otherwise specified, Ta = 25°C, VDDP, VDDA, B = 12 V, VDA, B = 21 V)

Item	Symbol	Limits			Unit	Measuring Conditions
		Min.	Typ.	Max.		
Circuit current						
VDD circuit current	IDD (A, B)	—	5	TBD	mA	No input
	IDDF (A, B)	—	30	TBD	mA	During operation (f = 768 kHz, duty = 50%)
	IDDP	—	5	TBD	mA	No input
Input voltage						
High input voltage	VIH	2.2	—	—	V	
Low input voltage	VIL	—	—	0.8	V	
Low voltage detection						
VDD low voltage detect level	VDDR	TBD	7	TBD	V	Between VDD and GND
VDD detect hysteresis voltage	VDDH	TBD	0.5	TBD	V	Detection → Recovery
Thermistor voltage detection						
Thermistor voltage detect level	THR	TBD	6.0	TBD	V	THIN pin (pin 33)
Thermistor detect hysteresis voltage	THH	TBD	4.8	TBD	V	Detection → Recovery
Bootstrap diode						
Diode forward voltage	VFL	—	1.5	TBD	V	HB output current = 100μA
Diode forward voltage	VFH	—	2.0	TBD	V	HB output current = 100mA
Diode operating resistance	RDON	—	1.2	TBD	Ω	HB output current = 100mA
Low side gain driver						
High input voltage	VOLL	—	0.25	0.3	V	ILO = 100mA
Low input voltage	VOHL	—	0.25	0.3	V	ILO = -100mA, VOHL = VDD-VHO
Pull-up output current	IOHL	—	2	—	A	VLO = 0V
Pull-down output current	IOLL	—	2	—	A	VLO = 12V
High side gain driver						
High input voltage	VOLH	—	0.25	0.3	V	IHO = 100mA
Low input voltage	VOHH	—	0.25	0.3	V	IHO = -100mA, VOHH = VHB-VHO
Pull-up output current	IOHH	—	2	—	A	VHO = 0V
Pull-down output current	IOLH	—	2	—	A	VHO = 12V
Switching characteristics						
Output rise time	trc	—	TBD	—	ns	f = 500KHz, CL = 1000pF
Output fall time	tfc	—	TBD	—	ns	f = 500KHz, CL = 1000pF
Output rise time (3 V to 9 V)	tr	—	TBD	TBD	μs	f = 50KHz, CL = 0.1μF
Output fall time (9 V to 3 V)	tf	—	TBD	TBD	μs	f = 50KHz, CL = 0.1μF
Operation input frequency	1/tpf	TBD	768	TBD	KHz	
Minimum input pulse width	tpw	40	—	—	ns	Cycle = 1.3 μs (f = 768 kHz)

## I/O Timing



### Dead Time

To prevent the M61556FP from being destroyed by the shoot-through current from an external MOSFET device, dead time is provided between HSGOUTA and LSGOUTA as well as between HSGOUTB and LSGOUTB. Refer to the Dead Time Control section below for information on adjusting the dead time.

## Function

### Signal System

#### 1. Dead Time Control Settings

The dead time, which protects the M61556FP from being destroyed by the shoot-through current from an external MOSFET device, can be adjusted as desired by the user by adjusting the external resistor (R) connected to pin 12.

It is possible to adjust the dead times of the high and low sides by setting the dead time control pins of side-A and side-B to 0 V or 12 V. This makes it easy to tailor the dead time to account for minute variations due to circuit board layout and to match the characteristics of the connected MOSFET devices.

#### Relationship Between Pin 12 Resistor, Dead Time Setting, and Output Shoot-Through Current

Pin 12 Resistance Value	Small	← →	Large
Dead time setting	Short	← →	Long
Output stage shoot-through current	Large shoot-through current	← →	Small shoot-through current

Note: Dead time values are averages for the high and low sides.

## Dead Time Control Pin and High/Low Dead Time Balance

DTCONT*1	DTCONT*2	DTCONT*3	High Side Dead Time	Low Side Dead Time
12V	0V	0V	Long	Short
12V	0V	12V	↑	↑
12V	12V	0V	↑	↑
12V	12V	12V	(INIT)	(INIT)
0V	0V	0V	INIT	INIT
0V	0V	12V	↓	↓
0V	12V	0V	↓	↓
0V	12V	12V	Short	Long

Note: The sums of the dead times for the high and low sides produced by the above adjustments are constant.

## DTCONT Pin No. list

	Side-A	Side-B
DTCONT*1	Pin 6	Pin 34
DTCONT*2	Pin 15	Pin 30
DTCONT*3	Pin 16	Pin 29

("INIT" refers to the initial status with no setting made by the user.)

**Protection System**

## 2. VDD Low Voltage Detector Circuit

In order to prevent internal malfunctioning caused by abnormally low power supply voltage, the M61556FP is equipped with a VDD low voltage detector circuit that is triggered if a drop occurs on the VDD power supply voltage. When abnormally low voltage is detected, a low-level signal is output to the HSGOUTA and HSGOUTB pins and a high-level signal to the LSGOUTA and LSGOUTB pins, the Nch totem pole output is kept low, and a low-level signal, indicating a malfunction, is output to PROUT. (The VDD output circuit is connected to the common power supply VDDP pin (pin 7), so for VDDA and VDDB (pins 24 and 40) an external connection should be made to VDDP.)

## 3. Clock Loss Detector Circuit

The major operation performed by the M61556FP is the input and output of PWM pulse waveforms, so protection is provided to ensure stable bootstrap operation in cases where no signal is input for a set period of time. In the protected state, a low-level signal is output to the HSGOUTA, HSGOUTB, LSGOUTA, and LSGOUTB pins, the high and low sides of the external Nch MOS FET are both turned off, and a low-level signal, indicating a malfunction, is output to PROUT.

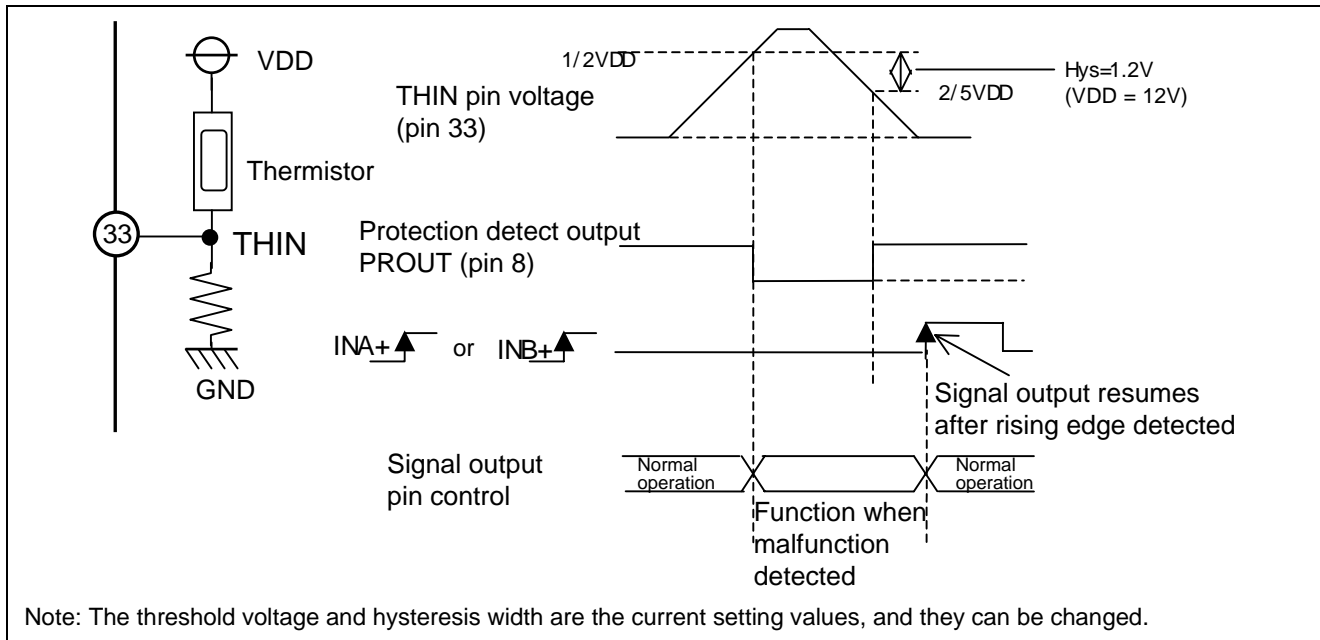
## 4. External Protection Detect Signal Input Pin (PROTECT)\*

Pin 31 of the M61556FP is the external protection detect signal input pin (PROTECT). If a low-level signal is to pin 31, the on-chip logic circuitry causes a low-level signal to be output to the HSGOUTA, HSGOUTB, LSGOUTA, and LSGOUTB pins, the high and low sides of the external Nch MOS FET to both turn off, and a low-level signal, indicating under protection, to be output to PROUT.

## 5. External Thermistor Circuit Detect Voltage Input Pin (THIN)

Pin 33 of the M61556FP is the external thermistor circuit detect voltage input pin (THIN). If the pin 33 voltage becomes one-half VDD or higher, through resistance division by the external thermistor and resistor, the on-chip logic circuitry causes a low-level signal to be output to the HSGOUTA, HSGOUTB, LSGOUTA, and LSGOUTB pins, the high and low sides of the external Nch MOS FET to both turn off, and a low-level signal, indicating a malfunction, to be output to PROUT.

## Overheating Detection Function Diagram



## Functions When Protection Detection Occurs

When protection detection occurs, a low-level signal is output to the HSGOUTA, HSGOUTB, LSGOUTA, and LSGOUTB pins, asynchronously to the PWM inputs (INA+, INA-, INB+, INB-), the high and low sides of the external Nch MOS FET are both turned off, and a low-level signal, indicating a malfunction, is output to PROUT. The PROUT output and signal output pins states when a malfunction is detected are listed in the table below.

Table of Signal Output Pin States During Protection Operation

	PROUT output when malfunction detected	PROTECT input pin	HSGOUTA/B	LSGOUTA/B	Power transistor output status
VDD low voltage protection	L	—	L	H	L
Clock loss detection	L	—	L	L	Hi-Z
External protection	L	L (*)	L	L	Hi-Z
Thermistor	L	—	L	L	Hi-Z

## Recovery from Protection Detection Status

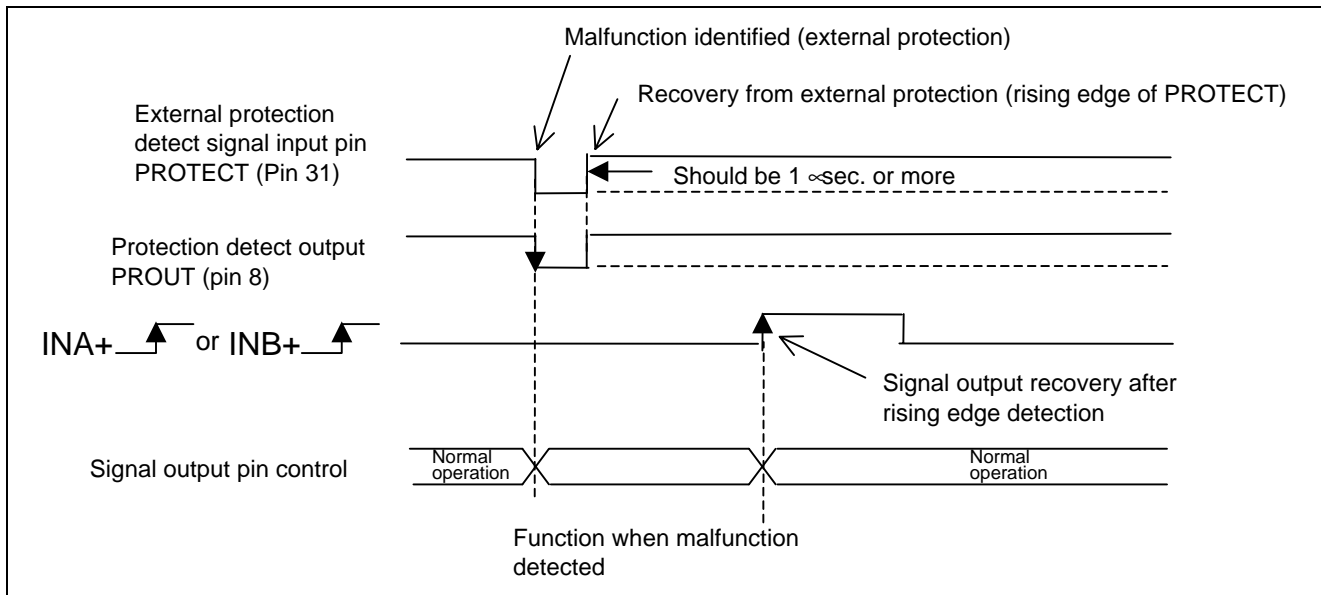
The manner in which recovery to signal output from protection detection status takes place varies depending on the protection circuit involved. Once the recovery conditions have been met, recovery takes place at the rising edge of INA+ or INB+ to high level, whichever is first. The recovery conditions for the different protection functions are listed in the table below.

Necessary Conditions for Recovery from Protection Detection Status

	<b>Recovery Conditions</b>
External protection*	PROTECT pin low: protection status, high: normal operation Recovery: After a rising edge from low to high is input to the PROTECT pin, normal operation resumes at the rising edge of the first signal. If a low-level signal is input to the PROTECT pin, the M61556FP is forced into protected status, regardless of the other modes.
Thermistor	After the overheating condition has been corrected and the THIN pin voltage drops to $(1/2 VDD - 1.5) V$ , recovery to normal operation takes place at the rising edge of INA+ or INB+ to high level, whichever is first.
VDD low voltage detector	After the low voltage condition has been corrected and the on-chip VDD detect circuit determines that the voltage is normal, recovery to normal operation takes place at the rising edge of INA+ or INB+ to high level, whichever is first.
Clock loss detector	After the abnormal input condition has been corrected and the on-chip abnormal input detect circuit determines that the input is normal, recovery to normal operation takes place at the rising edge of INA+ or INB+ to high level, whichever is first.

\* Note that the high and low settings are the reverse of those in the old specifications.

**External Protection Detect Signal Input Pin PROTECT (Pin 31)/Protection Detect Output PROUT (Pin 9) Timing Diagram**

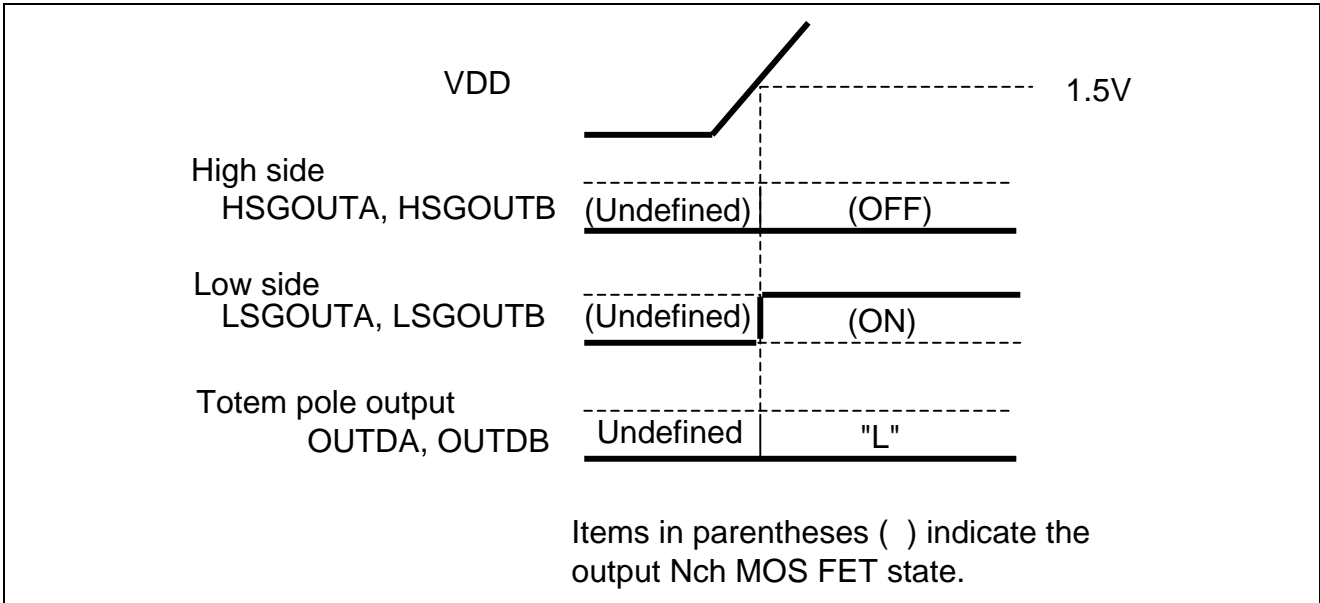


The above diagram shows the timing from the start of external protection control through recovery from protection status. With the other protection functions, recovery from protected status also occurs when the leading edge is detected, as in the diagram above.

**Functions at Power-On**

To prevent control malfunctions when the M61556FP is powered on, the logic circuitry determines when VDD has risen to approximately 1.5 V or higher and then outputs a low-level signal to HSGOUTA and HSGOUTB, outputs a high-level signal to LSGOUTA and LSGOUTB, and switches the Nch totem pole output to low-level. This charges the external bootstrap capacitor and ensures stable bootstrap operation.

Power-On Function Diagram



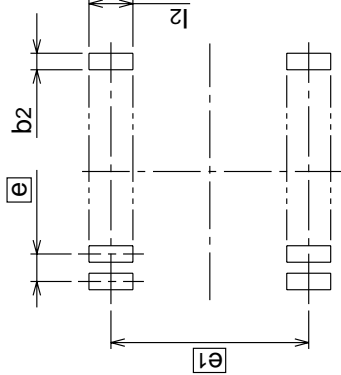
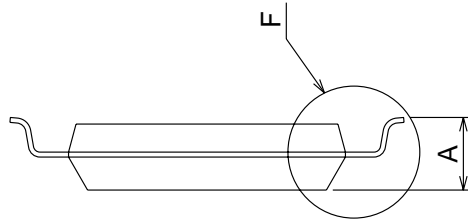
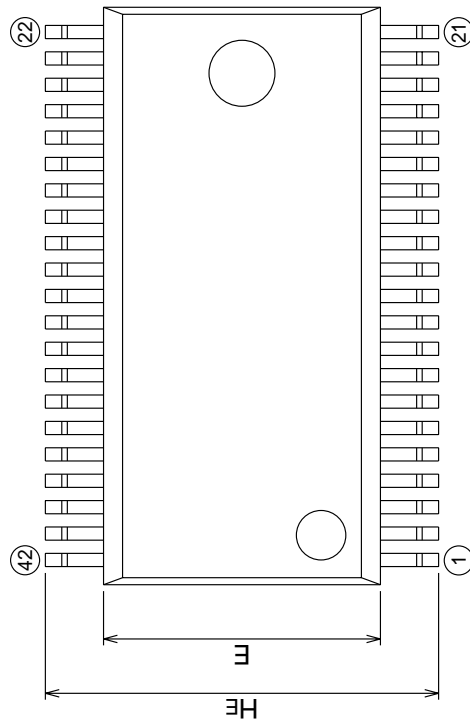
Package Dimensions

**42P2R-A**

(MMP)

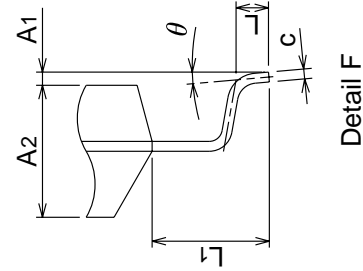
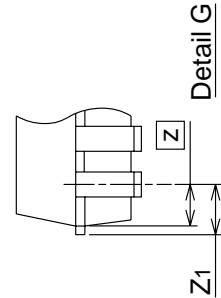
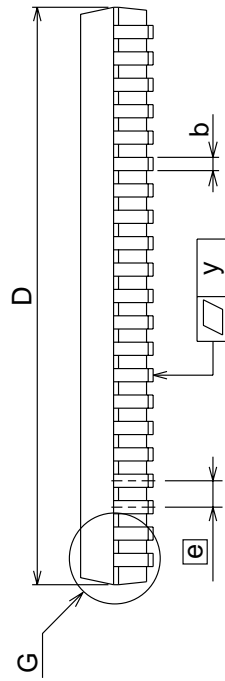
**Plastic 42pin 450mil SSOP**

EIAJ Package Code SSOP42-P-450-0.80	JEDEC Code —	Weight(g) 0.63	Lead Material Alloy 42/Cu Alloy
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Recommended Mount Pad

Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	—	—	2.4
A1	0.05	—	—
A2	—	2.0	—
b	0.35	0.4	0.5
c	0.13	0.15	0.2
D	17.3	17.5	17.7
E	8.2	8.4	8.6
e	—	0.8	—
HE	11.63	11.93	12.23
L	0.3	0.5	0.7
L1	—	1.765	—
Z	—	0.75	—
Z1	—	—	0.9
Y	—	—	0.15
θ	0°	—	10°
b2	—	0.5	—
e1	—	11.43	—
l2	1.27	—	—



Detail F

Detail G

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