54AC/74AC1016 • 54ACT/74ACT1016

16 × 16 Parallel Multiplier

Description

The 'AC/ACT1016 is a high-speed, low power 16 × 16-bit parallel multiplier that is ideally suited for real-time digital signal processing applications. Fabricated using advanced FACT technology, the '1016 offers a very low power alternative and exceptional performance.

The 'AC/ACT1016 is a pin and functional replacement for TRW's MPY016H; the 'AC/ACT1016 operates from a single Vcc supply and is compatible with standard TTL logic levels.

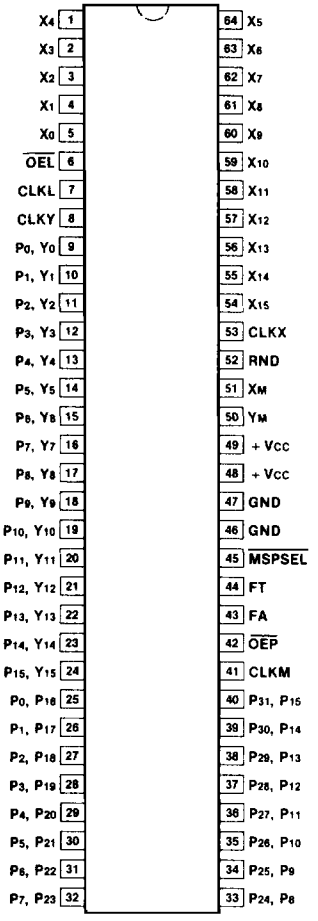
The architecture of the 'ACT1016 features one 16-bit port dedicated to the X input registers (controlled by CLKX), one 16-bit I/O port used for loading the Y input registers (controlled by CLKY) and for displaying the Least Significant Product (LSP), and one 16-bit output port multiplexed between displaying the Least Significant Product (LSP) and the Most Significant Product (MSP). The I/O port direction is controlled by $\overline{OEL}$ and the output port 3-state control is controlled by $\overline{OEP}$. The result is registered if FT is LOW (controlled by CLKL for the LSP and CLKM for the MSP) and unregistered if FT is held HIGH.

Twos complement, unsigned magnitude and mixed mode multiplications are possible through the twos complement X and Y mode controls, X_M and Y_M, respectively. These mode controls are registered, controlled by the input clocks CLKX and CLKY.

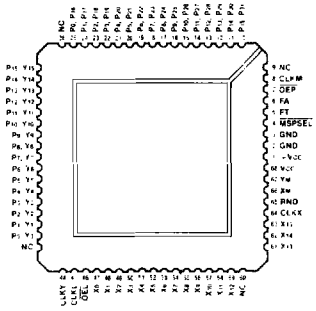
Result rounding is controlled by the registered RND signal (controlled by both CLKX and CLKY). Selection of one of the two rounding modes is determined by the FA signal.

- **16 × 16 Parallel Multiplier**
- **Selectable Rounding Modes**
- **Twos Complement, Unsigned Magnitude and Mixed Mode Multiplication**
- **Pin and Functionally Compatible with TRW MPY016H**
- **Provides Low Voltage, High-Speed Operation**
- **Single Vcc Supply**
- **± 2000 V ESD Protection**
- **Source/Sink 8 mA**
- **3-State Outputs**
- **'ACT1016 has TTL-Compatible Inputs**

Connection Diagrams



Pin Assignment for DIP



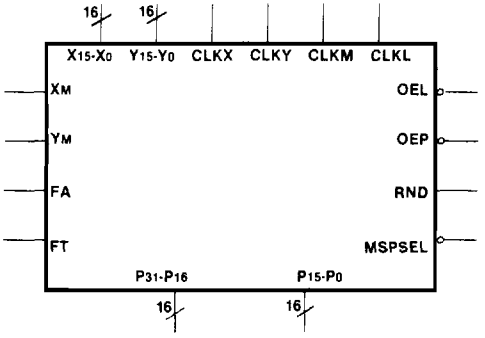
Pin Assignment for PCC

Ordering Code: See Section 6

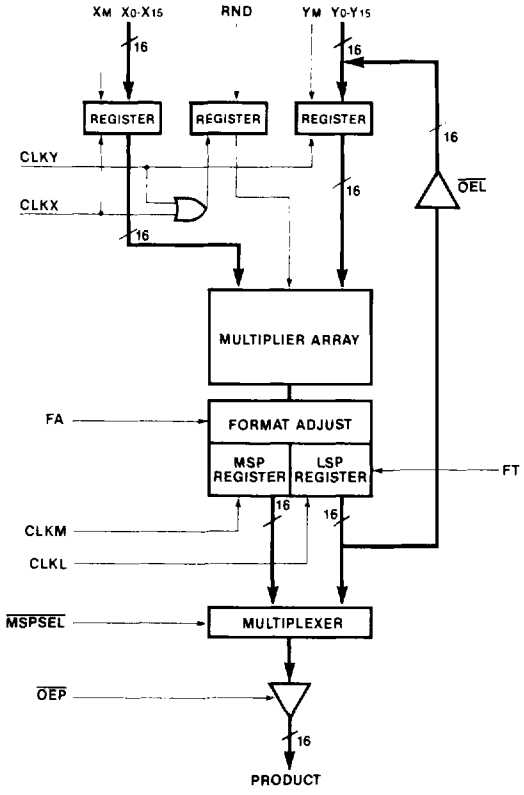
Pin Names

X_{15} - X_0	Multiplicand Data Inputs
Y_{15} - Y_0	Multiplier Data Inputs
CLKX, CLKY	Input Clocks
CLKM	Input Clock, MSP
CLKL	Input Clock, LSP
X_M, Y_M	Mode Control Inputs
FA	Format Adjust Control
FT	Format Transparent Control
$\overline{OEL}$	3-State Enable, LSP Routing
$\overline{OEP}$	3-State Enable, Product Output Port
RND	Round Control, MSP
$\overline{MSPSEL}$	MSP Select
P_{31} - P_{16}	MSP Outputs
P_{15} - P_0	LSP Outputs

Logic Symbol



Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

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Signal Descriptions

Inputs

X_{IN} (X_{15} - X_0)
Sixteen multiplicand data inputs.

Y_{IN} (Y_{15} - Y_0)
Sixteen multiplier data inputs. This is also an output port for P_{15} - P_0.

Input Clocks

CLKX
The rising edge of this clock loads the X_{15} - X_0 data input register along with the X mode and round registers.

CLKY
The rising edge of this clock loads the Y_{15} - Y_0 data input register along with the Y mode and round registers.

CLKM
The rising edge of this clock loads the Most Significant Product (MSP) register.

CLKL
The rising edge of this clock loads the Least Significant Product (LSP) register.

Controls

X_M, Y_M
Mode control inputs for each data word. A LOW input designates an unsigned data input, and a HIGH input designates twos complement.

FA
When the Format Adjust (FA) Control is HIGH, a full 32-bit product is selected. When this control is LOW, a left-shifted 31-bit product is selected with the sign bit replicated in the Least Significant Product (LSP). This control is normally HIGH except for certain fractional twos complement applications (see multiplier input/output formats).

FT
When the Format Transparent (FT) Control is HIGH, both the MSP and LSP registers are transparent.

$\overline{OEL}$
The $\overline{OEL}$ input is the 3-state enable for routing LSP through Y_{IN}/LSP_{OUT} port.

$\overline{OEP}$
The $\overline{OEP}$ is the 3-state enable for the product output port.

RND
The Round control is used for the rounding of the MSP. When this control is HIGH, A '1' is added to the Most Significant Bit (MSB) of the LSP. Note that this bit depends on the state of the format adjust (FA) control.

If FA is LOW when RND is HIGH, a '1' will be added to the 2^{-16} bit (P_{14}). If FA is HIGH when RND is HIGH, a '1' will be added to the 2^{-15} bit (P_{15}). In either case, the LSP output will reflect this addition when RND is HIGH.

Note also that rounding always occurs in the positive direction which may introduce a systematic bias. The RND input is registered and clocked in at the rising edge of the logical OR of both CLKX and CLKY.

$\overline{MSPSEL}$
When $\overline{MSPSEL}$ is LOW, the Most Significant Product (MSP) is selected. When HIGH, the Least Significant Product (LSP) is available at the product output port.

Outputs

MSP (P_{31} - P_0)
The MSP is the Most Significant Product output.

LSP (P_{15} - P_0)
The LSP is the Least Significant Product output.

$Y_{15\text{-}0}$/LSP_{OUT} (Y_{15} - Y_0 or P_{15} - P_0)
This is the Least Significant Product (LSP) output available when $\overline{OEL}$ is LOW. It is also an output port for Y_{15} - Y_0.

Figure 1: Fractional Twos Complement Notation

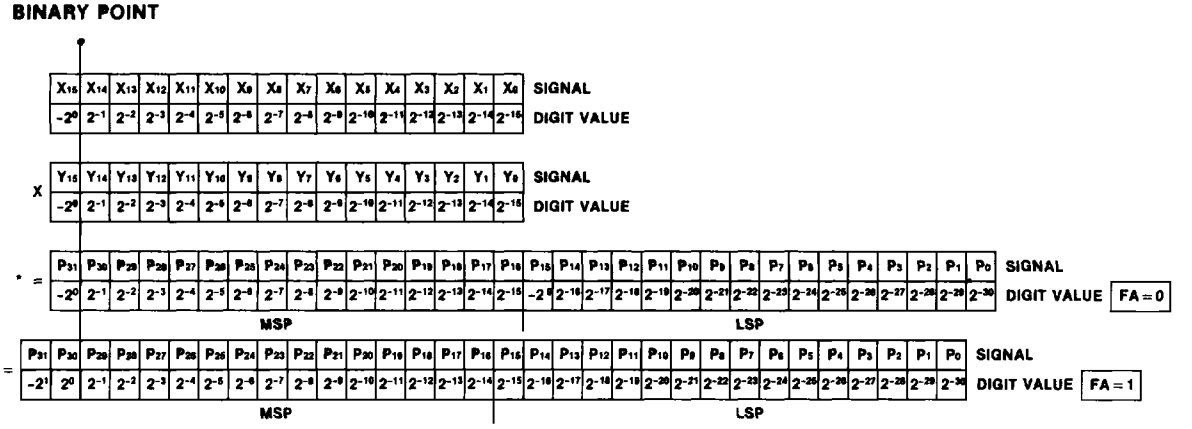


Figure 2: Fractional Unsigned Magnitude Notation

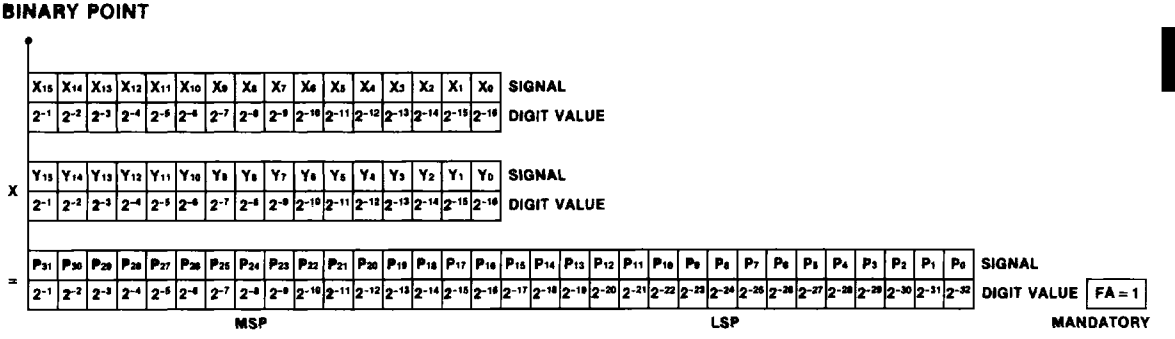
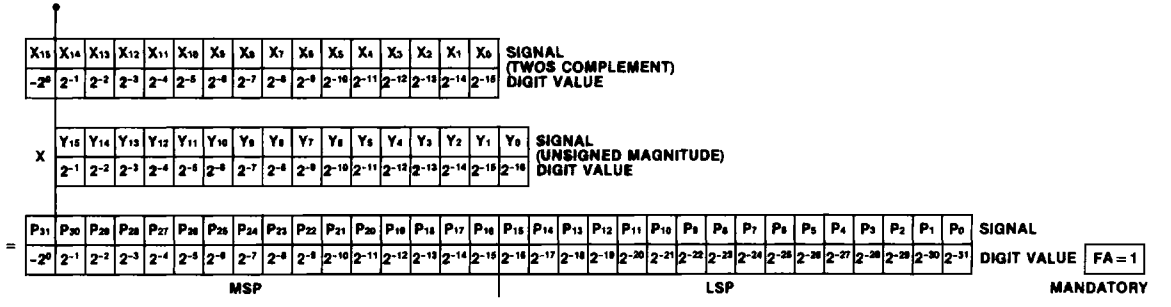


Figure 3: Fractional Mixed-Mode Notation



*In this format an overflow occurs in the attempted multiplication of the twos complement number 1000...0 with 1000.00 yielding an erroneous product of -1 in the fraction case and -2^{30} in the integer case.

Figure 4: Integer Twos Complement Notation

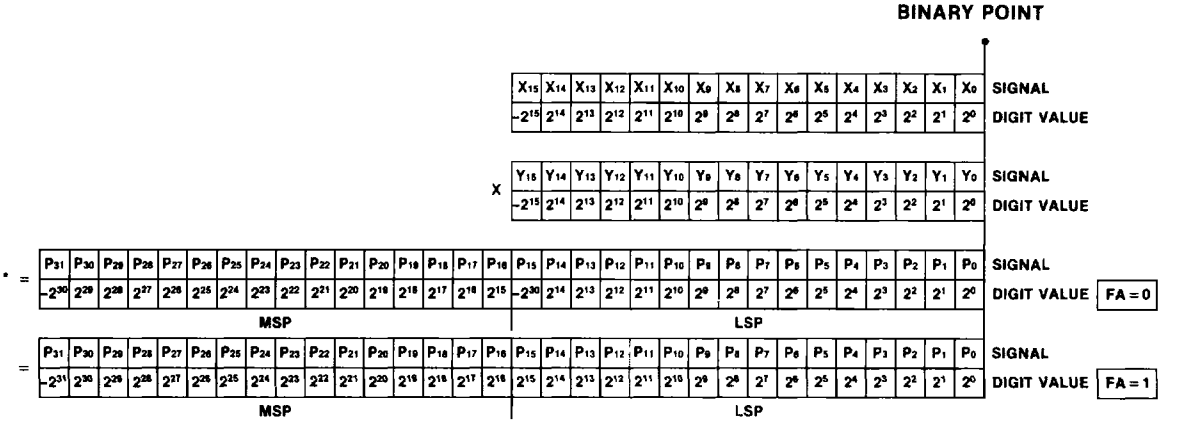


Figure 5: Integer Unsigned Magnitude Notation

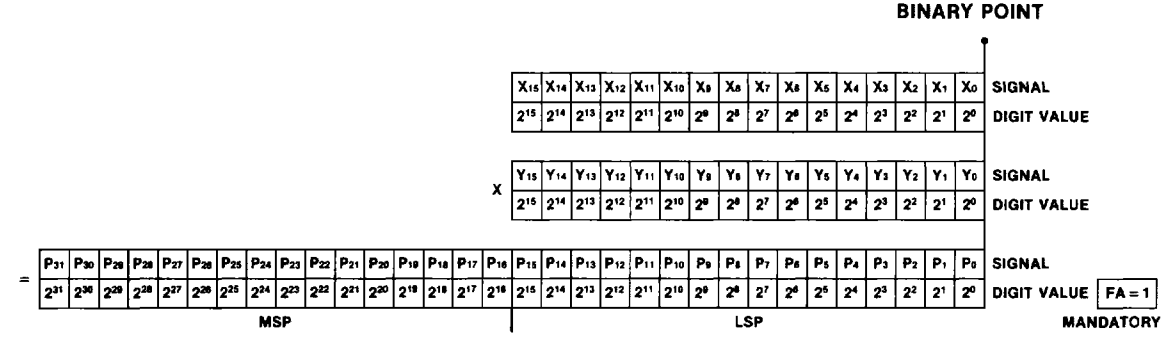
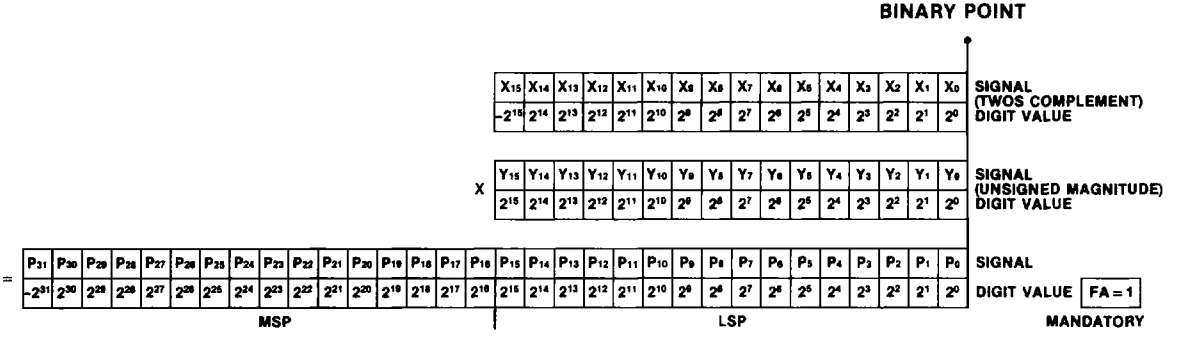


Figure 6: Integer Mixed Mode Notation



*In this format an overflow occurs in the attempted multiplication of the twos complement number 1000...0 with 1000.00 yielding an erroneous product of -1 in the fraction case and -2^{30} in the integer case.

Recommended Operating Conditions

Symbol	Parameter		Conditions	Limits	Units
V_{CC}	Supply Voltage (unless otherwise specified)			2.0 to 6.0	V
V_I	Input Voltage			0 to V_{CC}	V
V_O	Output Voltage			0 to V_{CC}	V
T_A	Operating Temperature	74AC/ACT 54AC/ACT		−40 to +85 −55 to +125	°C °C
S_r	Maximum Slew Rate (except for Schmitt inputs)		V_{IN} V_{meas} V_{CC}@4.5V V_{CC}@5.5V	0.8 to 2.0 0.8 to 2.0 10.0 8.0	V V ns ns

Absolute Maximum Ratings*

Symbol	Parameter	Conditions	Limits	Units
V_{CC}	Supply Voltage		−0.5 to 7.0	V
I_{IK} V_I	DC Input Diode Current or DC Input Voltage	$V_I = 0.5$ $V_I = V_{CC} + 0.5$	−20 20 −0.5 to V_{CC} + 0.5	mA mA V
I_{OK} V_O	DC Output Diode Current or DC Output Voltage	$V_O = -0.5$ $V_O = V_{CC} + 0.5$	−20 20 −0.5 to V_{CC} + 0.5	mA mA V
I_O	DC Output Source or Sink Current, Per Output Pin		±15	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current		±20	mA
T_{STG}	Storage Temperature		−65 to +150	°C

*Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

AC Test Conditions

Input Pulse Levels	GND to 3.0 V
Input Rise and Fall Times	3 ns
Input Timing Reference Levels	1.5 V
Output Reference Levels	1.5 V
Output Load	See Figures 7 and 8

Capacitance

Symbol	Parameter	Max	Unit	Conditions
C_{IN}	Input Capacitance	7.0	pF	$V_{IN} = 0$ V
C_{OUT}	Output Capacitance	5.0	pF	$V_{OUT} = 0$ V

DC Characteristics over Operating Temperature Range (unless otherwise specified)

Symbol	Parameter	74AC/ACT		54AC/ACT	74AC/ACT	Units	Conditions
		Typ	Guaranteed Limit				
I_{IN}	Maximum Input Current		± 0.1	± 10.0	± 1.0	μA	V_{CC} = Max V_{IN} = V_{CC}, 0
I_{OZ}	Maximum 3-State Current		0.5	10.0	5.0	μA	High Z, V_{CC} = Max V_{OUT} = 0, V_{CC}
I_{CCQ}	Supply Current, Quiescent	0.50	2.0	10.0	10.0	mA	V_{CC} = Max, V_{IN} = 0 V
I_{CCD}	Supply Current, 12.4 MHz Loaded	300		325	325	mA	V_{CC} = Max, f = 12.4 MHz Test Load: See Note 1
I_{CCD}	Supply Current, 20 MHz Loaded	325		350	350	mA	V_{CC} = Max, f = 20 MHz Test Load: See Note 1
V_{OH}*	Minimum HIGH Level Output	4.49	4.4	4.4	4.4	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = -50 μA, V_{CC} = 4.5 V
		5.49	5.4	5.4	5.4	V	V_{IN} = V_{IL} or V_{IH} I_{OUT} = -50 μA, V_{CC} = 5.5 V
			3.86	3.70	3.76	V	I_{OH} = – 8 mA, V_{CC} = 4.5 V
			4.86	4.70	4.76	V	I_{OH} = – 8 mA, V_{CC} = 5.5 V
V_{OL}*	Maximum HIGH Level Output	0.001	0.1	0.1	0.1	V	V_{IN} = V_{IL} or V_{IH}, I_{OUT} = 50 μA, V_{CC} = 4.5 V
		0.001	0.1	0.1	0.1	V	V_{IN} = V_{IL} or V_{IH}, I_{OUT} = 50 μA, V_{CC} = 5.5 V
			0.45	0.50	0.50	V	I_{OL} = 8 mA, V_{CC} = 4.5 V
			0.45	0.50	0.50	V	I_{OL} = 8 mA, V_{CC} = 5.5 V
I_{OLD}	Minimum Dynamic Output Current			32	32	mA	V_{CC} = 5.5 V, V_{OLD} = 2.2 V. See Note 2.
I_{OHD}	Minimum Dynamic Output Current			– 32	– 32	mA	V_{CC} = 5.5 V, V_{OHD} = 3.3 V. See Note 2.

Note 1: Test Load 50 pF, 500 ohm to Ground

Note 2: Only one output loaded at a time, maximum duration of test 2 ms.

*All outputs loaded.

AC Characteristics

Symbol	Parameter	Vcc* (V)	54AC				74AC				Units	Fig. No.
			$T_A = -55°C$ to $+125°C$				$T_A = -40°C$ to $+85°C$					
			1016-80		1016-65		1016-65		1016-55			
			Min	Max	Min	Max	Min	Max	Min	Max		
t_{MUC}	Unclocked Multiply Time	3.3 5.0									ns	11
t_{MC}	Clocked Multiply Time	3.3 5.0									ns	11, 12
t_{PDSEL}	MSPSEL to Product Out	3.3 5.0									ns	11
t_{PDP}	Output Clock to P	3.3 5.0									ns	11
t_{PDY}	Output Clock to Y	3.3 5.0									ns	11
t_{ENA}	3-State Enable Time[2]	3.3 5.0									ns	10
t_{DIS}	3-State Disable Time[2]	3.3 5.0									ns	10
t_{HCL}	Clock LOW Hold Time CLKXY Relative to CLKML[1]	3.3 5.0									ns	11, 12
t_s	Setup Time X,Y, RND	3.3 5.0									ns	9, 11
t_h	Hold Time X, Y, RND	3.3 5.0									ns	9, 11
t_w	Clock Pulse Width HIGH or LOW	3.3 5.0									ns	11

Note 1: To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.

Note 2: Transition is measured to ±500 mV from steady state voltage with loading specified in Figure 8.

*Voltage Range 3.3 is 3.3 V ± 0.3 V
Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

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AC Characteristics

Symbol	Parameter	Vcc* (V)	54ACT				74ACT				Units	Fig. No.
			$T_A = -55°C$ to $+125°C$				$T_A = -40°C$ to $+85°C$					
			1016-80		1016-65		1016-65		1016-55			
			Min	Max	Min	Max	Min	Max	Min	Max		
t_{MUC}	Unclocked Multiply Time	5.0						80.0		65.0	ns	11
t_{MC}	Clocked Multiply Time	5.0						65.0		55.0	ns	11, 12
t_{PDSEL}	$\overline{\text{MSPSEL}}$ to Product Out	5.0						13.0		13.0	ns	11
t_{PDP}	Output Clock to P	5.0						20.0		20.0	ns	11
t_{PDY}	Output Clock to Y	5.0						20.0		20.0	ns	11
t_{ENA}	3-State Enable Time[2]	5.0						10.0		10.0	ns	10
t_{DIS}	3-State Disable Time[2]	5.0						12.5		12.5	ns	10
t_{HCL}	Clock LOW Hold Time CLKXY Relative to CLKML[1]	5.0					0		0		ns	11, 12
t_s	Setup Time X,Y, RND	5.0					5.5		5.5		ns	9, 11
t_h	Hold Time X, Y, RND	5.0					1.0		1.0		ns	9, 11
t_w	Clock Pulse Width HIGH or LOW	5.0					3.5		3.5		ns	11

Note 1: To ensure that the correct product is entered in the output registers, new data may not be entered into the registers before the output registers have been clocked.

Note 2: Transition is measured to ±500 mV from steady state voltage with loading specified in Figure 8.

*Voltage Range 5.0 is 5.0 V ± 0.5 V

Military parameters given herein are for general references only. For current military specifications and subgroup testing information please request Fairchild's Table I data sheet from your Fairchild sales engineer or account representative.

Figure 7: AC Output Test Load

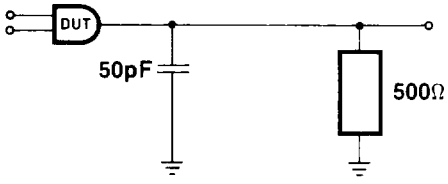

Figure 8: Output 3-State Delay Load

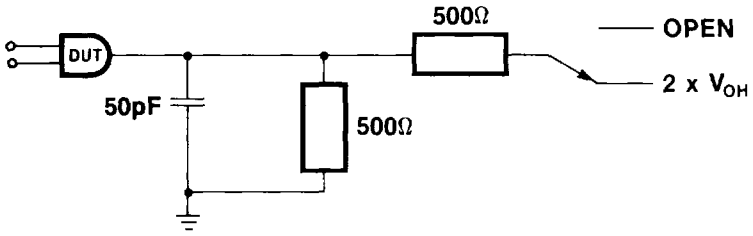

Figure 9: Setup and Hold Time

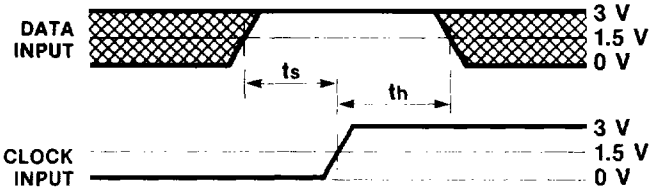

Figure 10: 3-State Control Timing Diagram

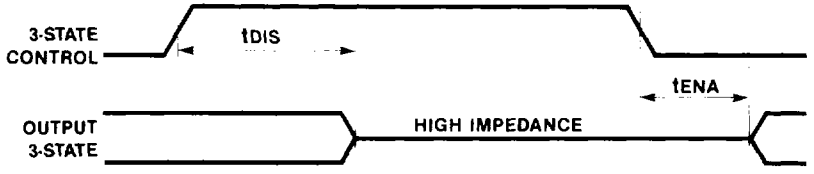

Figure 11: '1016 Timing Diagram

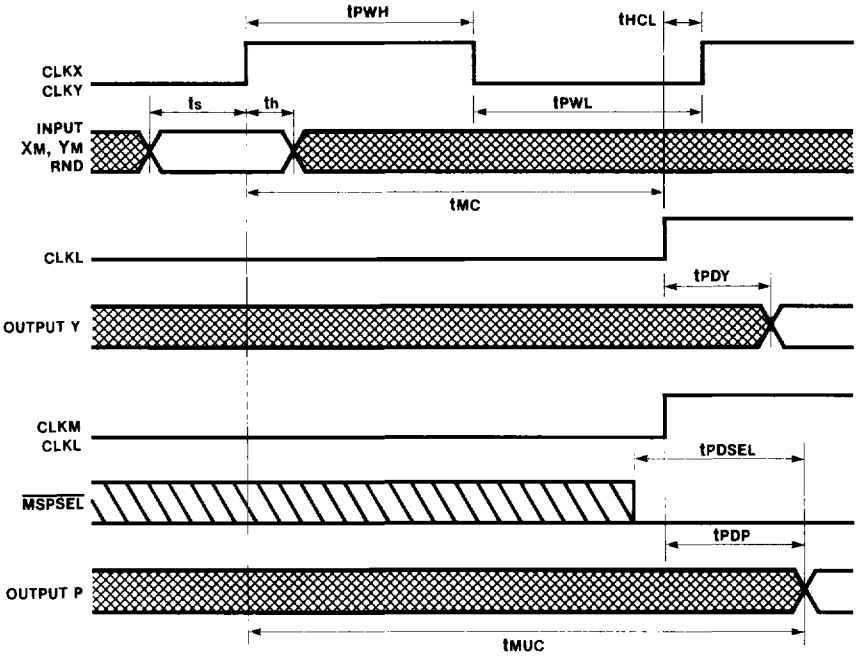

Figure 12: Simplified Timing Diagram — Typical Application