ATM-LP

ATM Layer Processor

PXB 4350 E, Version 1.1

Wired Communications

Never stop thinking.

Edition 2003-12-17

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Revision History:	**2003-12-17**	Rev. 2
Previous Version:	**08.2000, DS1**	

Page	**Subjects (major changes since last revision)**
	Device name has been changed to ATM-LP

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1 Overview

The PXB 4350 E ATM Layer Processor ATM-LP is a member of the Infineon ATM622 chip set. The whole chip set consists of:

- PXB 4330 E ATM Buffer Manager ABM
- PXB 4340 E ATM OAM Processor AOP
- PXB 4350 E ATM Layer Processor ATM-LP
- PXB 4360 F Content Addressable Memory Element CAME

Main ATM Layer functionality is achieved with only two chips, ATM-LP and ABM. The combination of these two devices provide elementary ATM functionality like header translation, policing, OAM support, multicast and traffic management (Fig.1). The functionality is upgradeable to full OAM support by the AOP (Fig.2) and to arbitrary header translation by CAME (Fig.3).

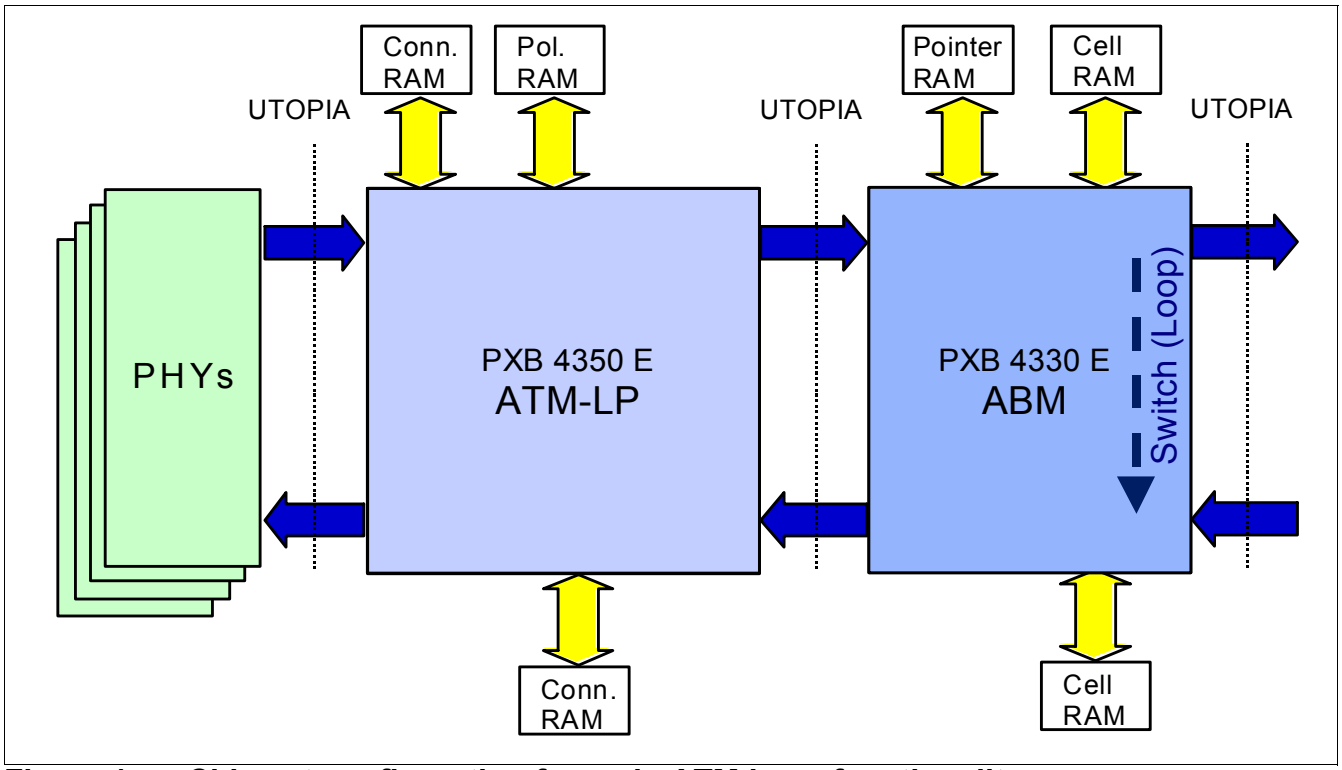


Figure 1 Chip set configuration for main ATM layer functionality

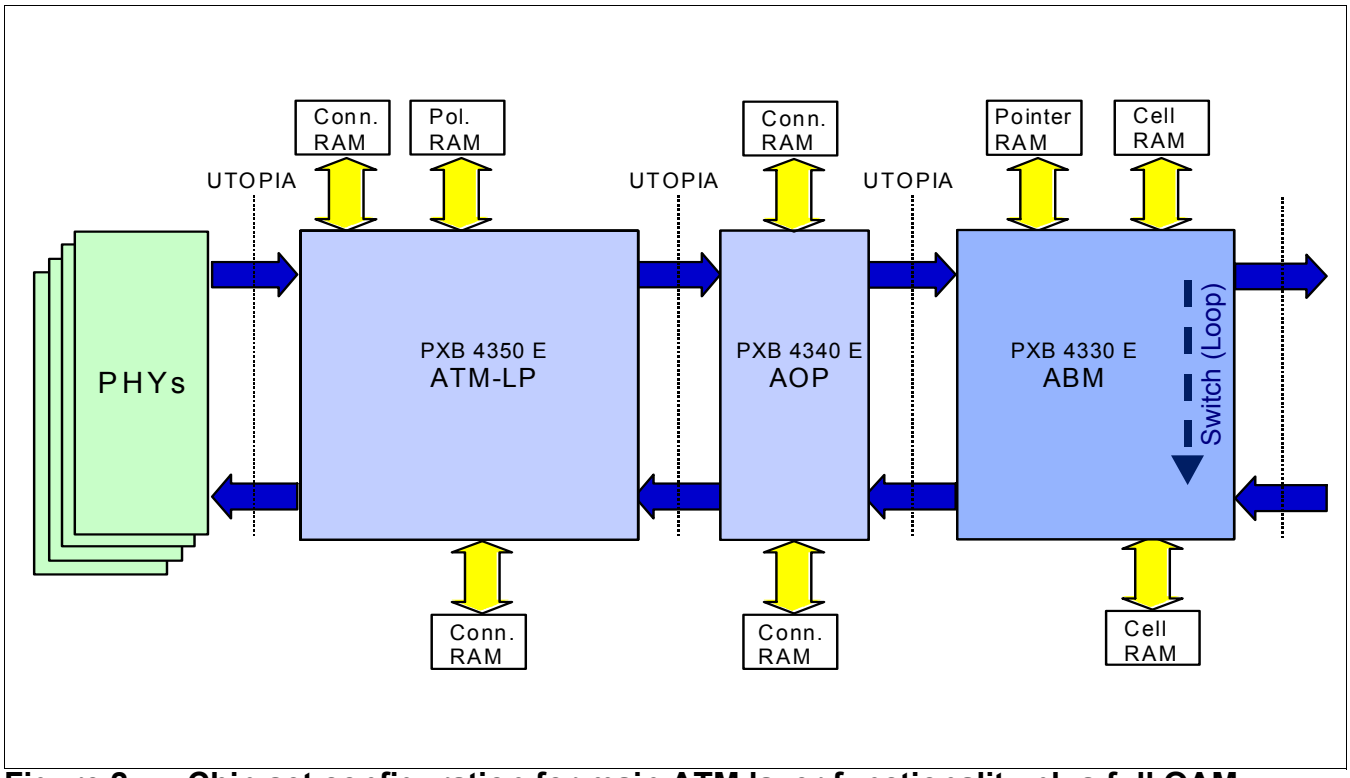


Figure 2 Chip set configuration for main ATM layer functionality plus full OAM

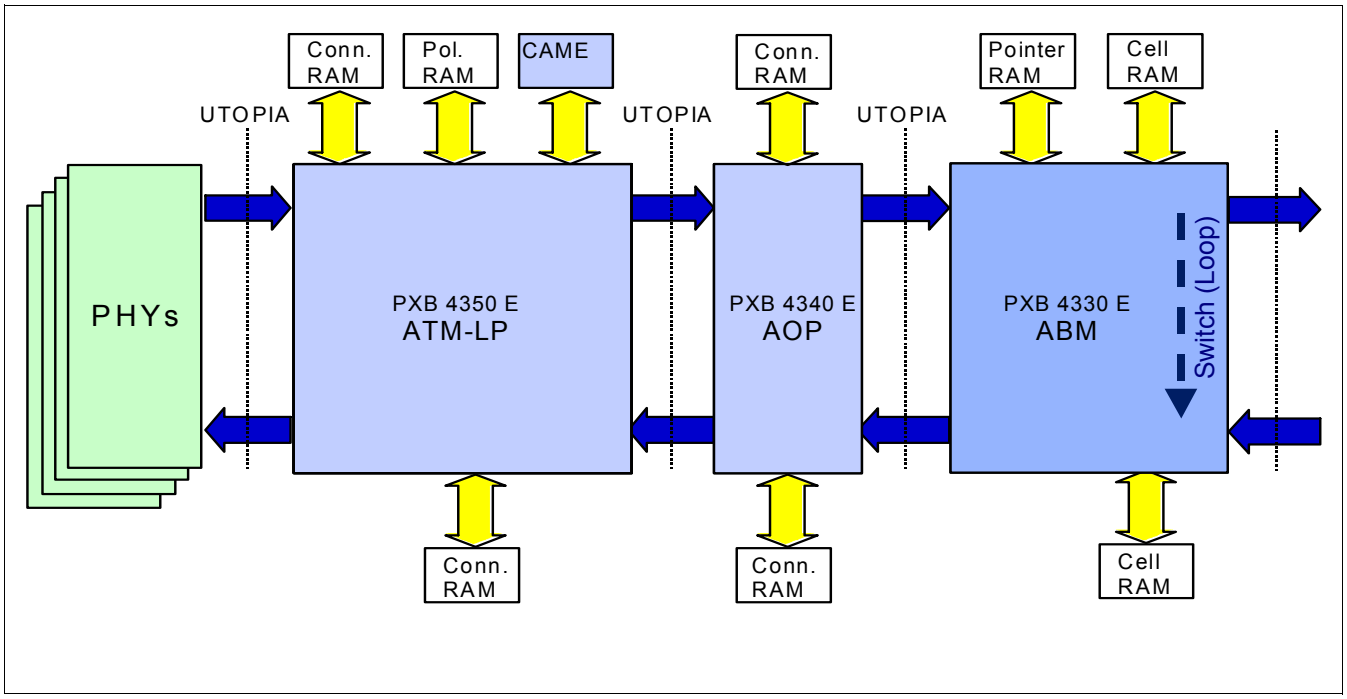


Figure 3 Chip set configuration for main ATM layer functionality plus full OAM and arbitrary header translation

The ATM 622 Layer devices can be used as ....

...a full switch in:
ADSL Concentrators / Multiplexers (DSLAM)

Access Multiplexers
Access Concentrators
Multiservice switches

...Line card in:
Workgroup Switches
Edge Switches
Core Switches

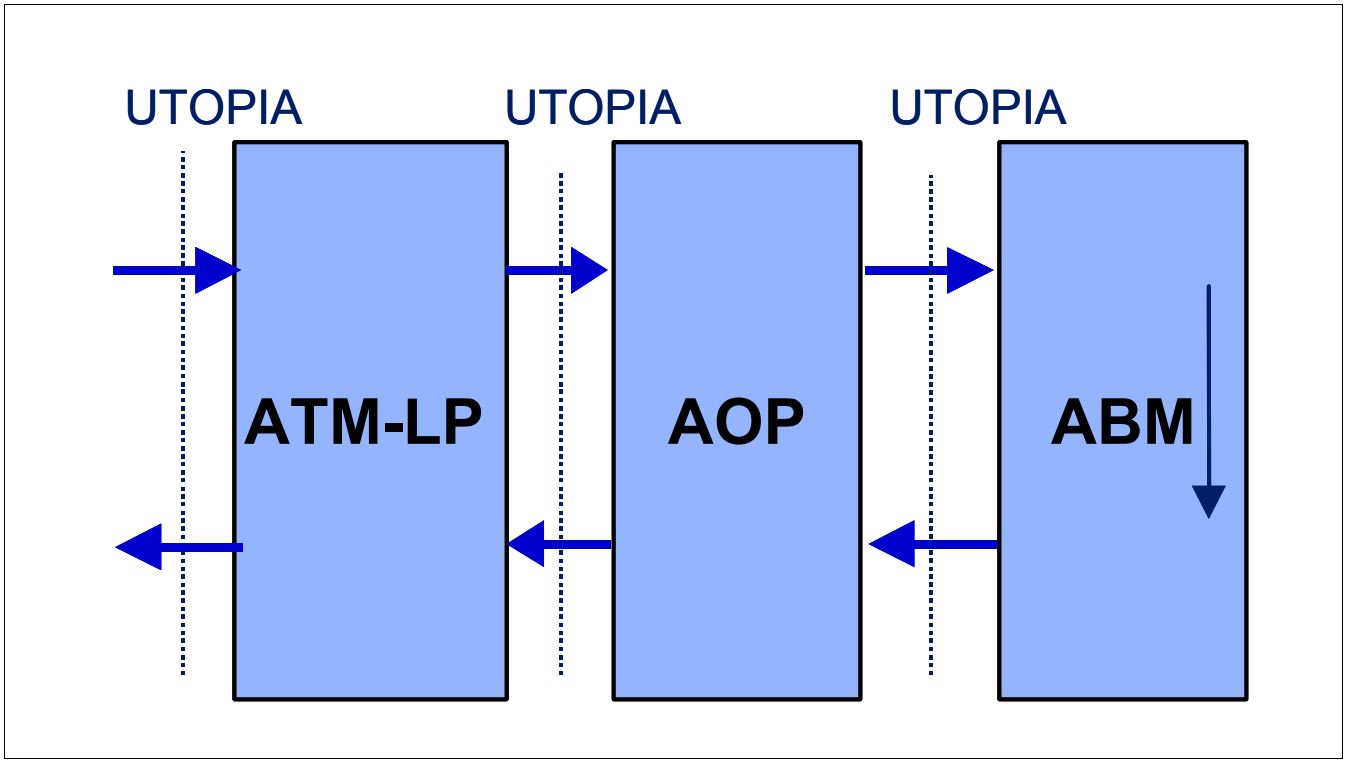


Figure 4 Miniswitch configuration

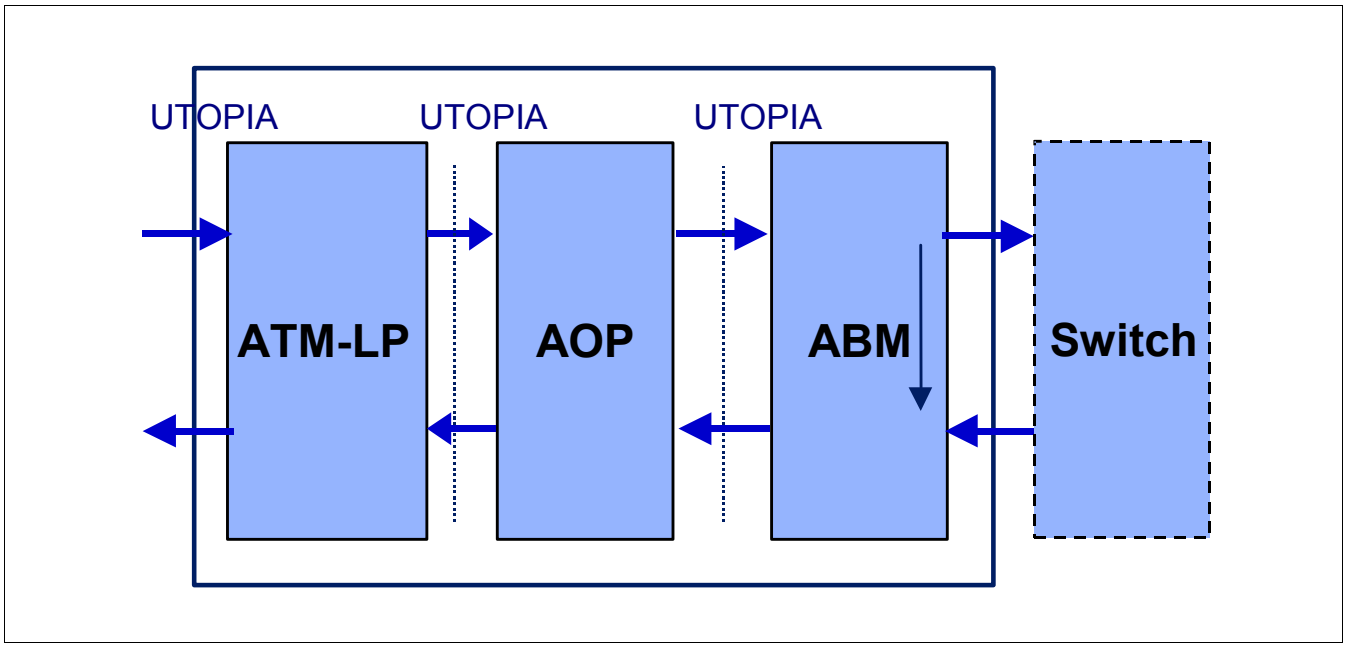
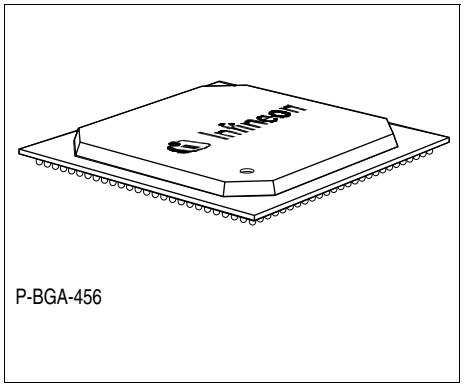


Figure 5 Line card configuration

Due to their most flexible scaling facilities, feature set and throughput the Infineon ATM622 layer chips are the ideal devices for almost any ATM system.

1.1 Features



Performance

- Performance up to STM-4/OC-12 equivalent ATM layer processing
- Throughput up to 687 Mbit/s bi-directional
- Up to 16384 connections in both directions (VPC/ VCC)

Header Translation

- Header Verification and discarding of unallocated PN/ VPI/VCIs
- Address Reduction in upstream direction (PN/VPI/VCIs -> LCI); two modes
  - –Built-in, programmable, versatile address reduction
  - –Optional external address reduction
- Header translation in downstream direction (LCI -> PN/VPI/VCIs)

Policing for Upstream Direction

- Policing according to ITU-T I.371 and ATM Forum UNI Specification
- UPC/NPC function capability on a per connection basis for up to 16384 connections
- Modification of adjusted UPC/NPC parameters on a per established connection basis without additional cell losses
- Up to 3 Leaky Buckets (LB) per connection with 2 parallel branches: branch 1 containing LB1 and optionally LB2; branch 2 containing LB3
- 4 Leaky Bucket configurations selectable per connection
- Flexible Policing of each port specific cell flow (user data, F4 RM, F5 RM, F4 segment OAM, F5 segment OAM, F4 end-to-end OAM, F5 end-to-end OAM) with SW programmable control flags indicating whether the flow is policed in branch 1, branch 2 or is not policed at all
- CDV tolerance (i.e. size of PCR Leaky Bucket) up to 4s
- Maximum Burst Size (MBS) given by the size of SCR Leaky Bucket of up to 2^{10} s
- 2^{32} PCR values ranging between 1 cell/s and 1,620,000 cells/s. PCR and SCR can be adjusted with a granularity of at least 2^{-10} cells/s

Multicast in downstream direction

- Spatial (different ports) and logical (different VPI/VCI for one port) Multicast light

Type	Package
PXB 4350 E	BGA-456

OAM Management for up- and downstream

- OAM Levels and Flows (F4/F5) according to ITU-T/I.610 and Bellcore GR-1248-core
- Extraction and insertion of OAM, RM and 2 programmable cell types for both up- and downstream direction via a 12 cell extraction and 1 cell insertion buffer to the microprocessor
- Supported OAM cells are AIS, RDI, Continuity Check and Loopback cells
- Check and Generation of CRC-10 for incoming and outgoing cells
- Extraction point can be configured as originating, intermediate or terminating point for F4 and F5 Flow (segment and end-to-end)
- Cell processing options as forwarding, dropping, copying and discarding of cells at the extraction and insertion point

Traffic Measurement for up- and downstream

- Traffic Measurement (can be dis/enabled) according to Bellcore GR-1248
- Traffic Measurement intervals of at least 44 minutes
- At VCC level
  - –Total Incoming and Outgoing Cells
  - –Total Incoming and Outgoing Cells with CLP=0
  - –Total Discarded Cells due to UPC/NPC with CLP=1 and CLP=0 for incoming cells respectively
  - –Total Tagged Cells due to UPC/NPC for incoming cells
- At VPC level
  - –VPC specific Total Incoming and Outgoing Cells
  - –VPC specific Total Incoming and Outgoing Cells with CLP=0
- At Port level
  - –Total Discarded Cells due to unallocated PN/VPI/VCI
  - –Total Incoming Cells with non-zero GFC field
  - –Total Incoming and Outgoing Cells
  - –Total Incoming and Outgoing OAM/RM Cells enabled per connection

UTOPIA Interface

- Multiport UTOPIA [**1, 2**] Level 1 and Level 2 interface in up- and downstream direction according to ATM forum, UTOPIA level 2 specification for up to 24 ports
- PHY side is Master, ATM side is Master/Slave configurable for both TX and RX direction
- UTOPIA frequency up to 51.84 MHz
- Statistical Demultiplexing with 64 cell shared buffer for up to 24 queues with flexible queue size at UTOPIA downstream transmit interface
- Support of up to 24 PHYs with one queue respectively
- In addition to the UTOPIA-PN a second PN in UDF1 is supported for enhanced PHY addressing

External SSRAM

- Policing Data SSRAM; can be omitted if policing is not needed.
- Connection Data upstream SSRAM; can be omitted if traffic statistic and OAM is not needed.
- Connection Data downstream SSRAM; mandatory for header translation and multicast
- All SSRAMs scale with the number of connections; usable Pipelined Burst SSRAM Types:
  - –e.g. Toshiba TC55V1325FF-7 1MSSRAM(32k*32) or TC55V2325FF-7 2M(64k*32).

Microcomputer Interface

- Intel 386 EX microprocessor interface
- Support of DMA for fast data transfer between external RAM and microprocessor

Boundary Scan

- Boundary scan support according to JTAG

Internal Loops

- Internal hardwired loop: upstream to downstream and downstream to upstream

Technology

- BGA-456 package
- 0,35 µm CMOS
- typ. power dissipation 1.7 W
- Extended temperature range -40°C to 85°C

1.2 Logic Symbol

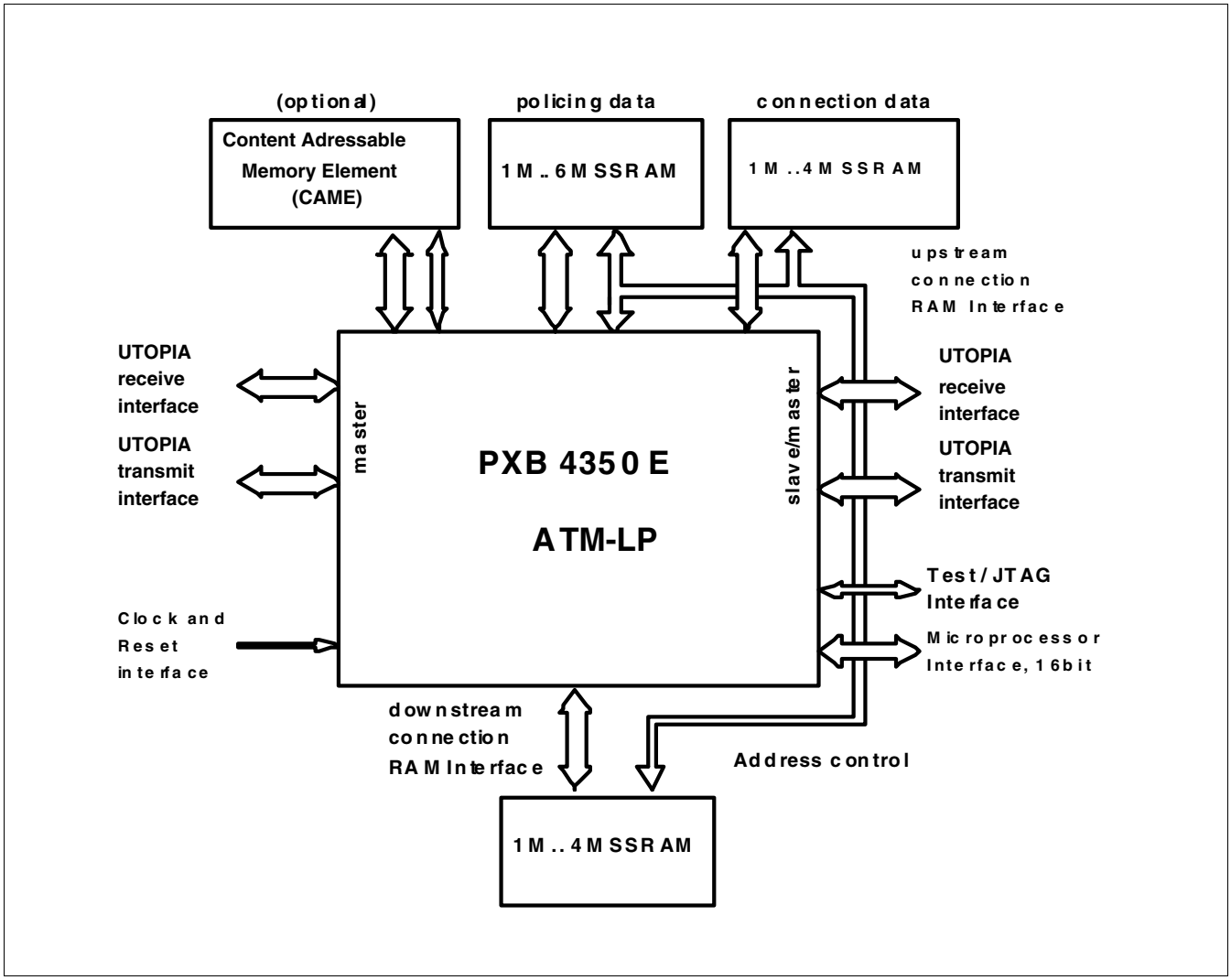


Figure 6 ATM-LP Logic Symbol

1.3 Pin Configuration

(Bottom view)

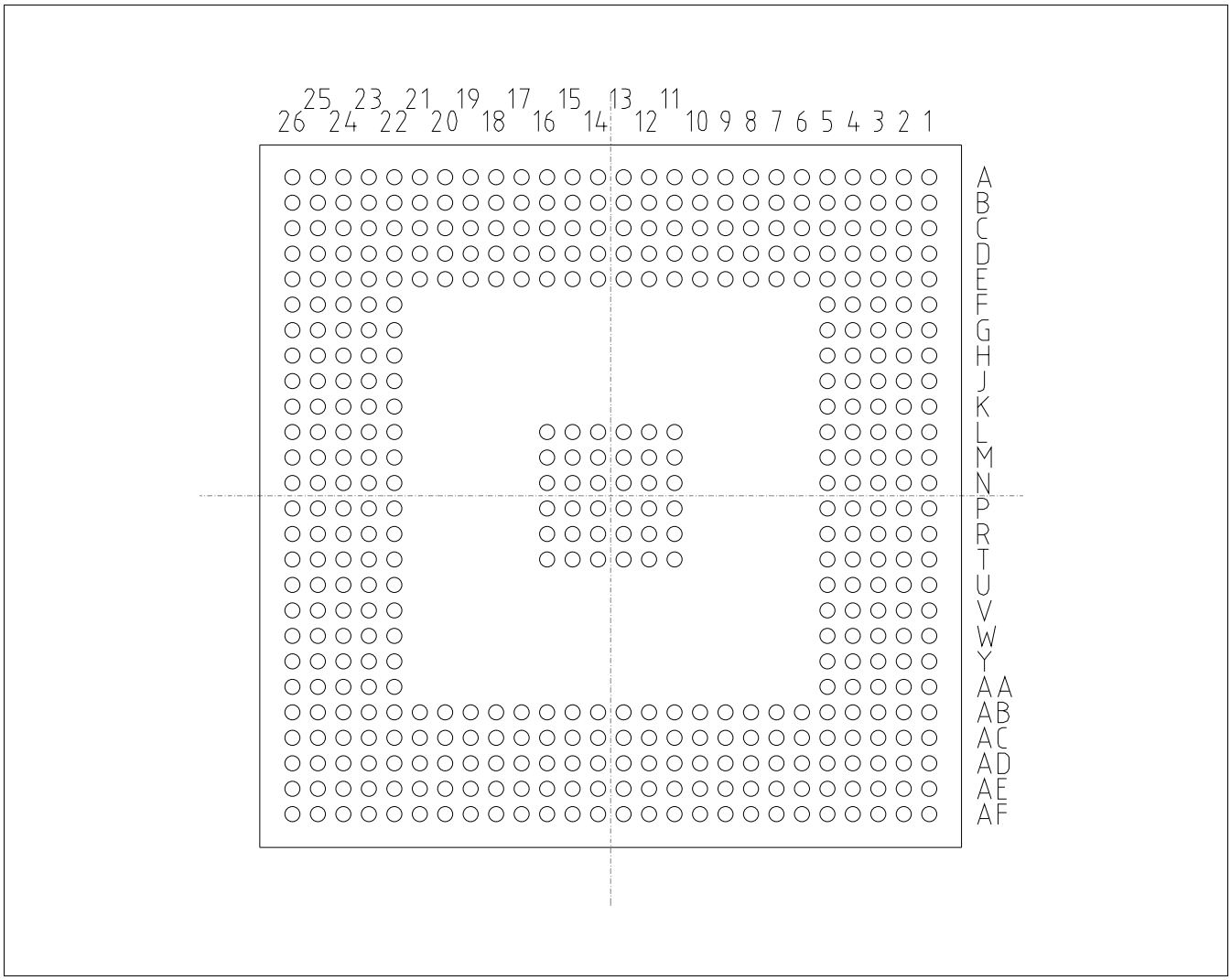


Figure 7 ATM-LP Pin Configuration

1.4 Pin Definitions and Functions

The following explanations applies for all pins of a field in the table respectively:

- Pins with a [1] attached are connected with an internal pull up resistor.
- Pins with a [2] attached are connected with an internal pull down resistor.
- Pins with a [3] attached are 5V compatible.
- Pins with a [4] attached are tristate when not active.
- Pins with a [5] attached are open drain output.

Table 1 Pin Definitions and Functions

Pin No.	Symbol	Input (I) Output (O)	Function
General (5 pins)			
AD17	$\overline{\text{RESET}}$	I	Chip reset
AC16	SYSCLK	I	Core operating clock
A11	UTPHYCLK	I	UTOPIA clock at PHY side.
R26	UTATMCLK	I	UTOPIA clock at ATM side.
AD25 [2]	RAMVERS	I	Selection of 1M (low) or 2M (high) SSRAM-type.
UTOPIA Receive Interface, upstream (30 pins)			
C15, D14, B15, A16, C16, B16, D15, A17, C17, B17, D16, A18, C18, B18, D17, A19 [2] [3]	RXDATU (15:0)	I	Receive data from PHY side. C15 corresponds to RXDATU(15) ... A19 corresponds to RXDATU(0).
C14, A14, B14, A15 [3]	RXADRU (3:0)	O	Address to PHY side. C14 corresponds to RXADRU(3) ... A15 corresponds to RXADRU(0).
C13 [2] [3]	RXPRTYU	I	Odd parity of RXDATU(15:0) from PHY side.
C12, D13, A13, B13 [3]	$\overline{\text{RXENBU}}$ (3:0)	O	Enable signal to PHY side. C12 corresponds to $\overline{\text{RXENBU}}$(3) ... B13 corresponds to $\overline{\text{RXENBU}}$(0).
C11, D12, A12, B12 [2] [3]	RXCLAVU (3:0)	I	Cell available signal from PHY side. C11 corresponds to RXCLAVU(3) ... B12 corresponds to RXCLAVU(0).
B11 [2] [3]	RXSOCU	I	Start of cell signal from PHY side.

Table 1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
UTOPIA Transmit Interface, downstream (30 pins)			
D8, C7, A7, B7, D9, A8, C8, B8, A9, C9, D10, B9, A10, C10, D11, B10 3)	TXDATD (15:0)	O	Transmit data to PHY side. D8 corresponds to TXDATD(15) ... B10 corresponds to TXDATD(0).
B5, C6, A6, B6 3)	TXADRD (3:0)	O	Address to PHY side. B5 corresponds to TXADRD(3) ... B6 corresponds to TXADRD(0).
D7 3)	TXPRTYD	O	Odd parity to PHY side.
D6, B4, A5, C5 3)	$\overline{\text{TXENBD}}$ (3:0)	O	Enable signal to PHY side. D6 corresponds to $\overline{\text{TXENBD}}$(3) ... C5 corresponds to $\overline{\text{TXENBD}}$(0).
D5, B3, A4, C4 2) 3)	TXCLAVD (3:0)	I	Cell available signal from PHY side. D5 corresponds to TXCLAVD(3) ... C4 corresponds to TXCLAVD(0).
A3 3)	TXSOCD	O	Start of cell signal to PHY side.
UTOPIA Receive Interface, downstream (31 pins)			
V24, V25, U23, W26, W24, W25, V23, Y26, Y24, Y25, W23, AA26, AA24, AA25, Y23, AB26 2) 3)	RXDATD (15:0)	I	Receive data from ATM side. V24 corresponds to RXDATD(15) ... AB26 corresponds to RXDATD(0).
U26, U24, U25, T23 3)	RXADRD (3:0)	I/O	Address from ATM side. U26 corresponds to RXADRD(3) ... T23 corresponds to RXADRD(0).
V26 1) 3)	RXPRTYD	I	Odd parity of RXDATD(15:0) from ATM side.
T26, T24, T25, R23 3)	$\overline{\text{RXENBD}}$ (3:0)	I/O	Enable signals from ATM side. T26 corresponds to $\overline{\text{RXENBD}}$(3) ... R23 corresponds to $\overline{\text{RXENBD}}$(0).
AB24, AB25, AA23, AC26 3) 4)	RXCLAVD (3:0)	I/O	Cell available signal to ATM side. AB24 corresponds to RXCLAVD(3) ... AC26 corresponds to RXCLAVD(0).
R25 2) 3)	RXSOCD	I	Start of cell signal from ATM side.

Table 1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
R24	RXMS	I	Selects Master (high) or Slave (low) mode for UTOPIA Rx downstream.
UTOPIA Transmit Interface, upstream (31 pins)			
K24, L23, K25, L26, L25, L24, M23, M26, M25, M24, N23, N26, N25, N24, P24, P26 3) 4)	TXDATU (15:0)	O	Transmit data to ATM side. K24 corresponds to TXDATU(15) ... P26 corresponds to TXDATU(0).
G25, J23, H26, H24 3)	TXADRU (3:0)	I/O	Address from ATM side. G25 corresponds to TXADRU(3) ... H24 corresponds to TXADRU(0).
K26 3) 4)	TXPRTYU	O	Odd parity of TXDATU(15:0) to ATM side.
F25, H23, G24, G26 3)	$\overline{\text{TXENBU}}$ (3:0)	I/O	Enable signal from ATM side. F25 corresponds to $\overline{\text{TXENBU}}$(3) ... G26 corresponds to $\overline{\text{TXENBU}}$(0).
J26, J24, K23, J25 3) 4)	TXCLAVU (3:0)	I/O	Cell available signal to ATM side. J26 corresponds to TXCLAVU(3) ... J25 corresponds to TXCLAVU(0).
H25 3) 4)	TXSOCU	O	Start of cell signal from ATM side.
P23	TXMS	I	Selects Master (high) or Slave (low) mode for UTOPIA Tx upstream.
Microprocessor Interface (31 pins)			
C19, B19, D18, A20, C20, B20, D19, A21, C21, B21, D20, A22, C22, B22, D21, A23 3) 4)	MPDAT (15:0)	I/O	Data to/ from microprocessor. C19 corresponds to MPDAT(15) ... A23 corresponds to MPDAT(0).
F23, D25, E26, E24, G23, E25, F24, F26 3)	MPADR (7:0)	I	Address to microprocessor. F23 corresponds to MPADR(7) ... F26 corresponds to MPADR(0).
D24 3)	$\overline{\text{MPWR}}$	I	Write enable from microprocessor.
D26 3)	$\overline{\text{MPRD}}$	I	Read enable from microprocessor.
B24 3)	$\overline{\text{MPCS}}$	I	Chip select from microprocessor.
A24 3) 5)	$\overline{\text{MPINT}}$	O	Interrupt request to microprocessor.

Table 1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
B23 [3) 4)]	$\overline{\text{MPDREQ}}$	O	DMA request to microprocessor.
C23 [3) 4)]	MPRDY	O	Ready output signal for MPDAT write/ read to microprocessor.
D22 [3)]	$\overline{\text{MPDACK}}$	I	µP DMA acknowledge
RAM Interface (SSRAM) (18 pins)			
AF6, AD6, AE6, AC7, AF5, AD5, AE5, AC6, AF4, AD4, AE4, AC5, AF3, AE3, AF2, AD1, AB4, AD2	RAMADR (17:0)	O	Common address to all external RAMs. AF6 corresponds to RAMADR(17) ... AD2 corresponds to RAMADR(0).
Upstream Connection RAM Interface (39 pins)			
AB2, AA3, AA1, AA2, W4, Y3, Y1, Y2, V4, W1, W3, W2, V1, V3, U4, V2, U1, U3, T4, U2, T1, T2, T3, R4, R1, R2, R3, P4, P1, P2, P3, N3	RDATU (31:0)	I/O	Data to/ from connection RAM upstream incl. parity bit. AB2 corresponds to RDATU(31) ... N3 corresponds to RDATU(0).
AB3, Y4	$\overline{\text{RSCU}}$ (1:0)	O	Upstream RAM address status control. AB3 corresponds to $\overline{\text{RSCU}}$(1) and Y4 corresponds to $\overline{\text{RSCU}}$(0).
AB1	$\overline{\text{RADVU}}$	O	Upstream RAM advance input.
AA4, AC2	$\overline{\text{RCEU}}$ (1:0)	O	Upstream RAM chip enable. AA4 corresponds to $\overline{\text{RCEU}}$(1) and AC2 corresponds to $\overline{\text{RCEU}}$(0).
AC3	$\overline{\text{RGWU}}$	O	Upstream RAM global write.
AC1	$\overline{\text{ROEU}}$	O	Upstream RAM output enable.

Table 1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
Policing RAM Interface (41 pins)			
M4, K1, K3, K2, L4, J1, J3, J2, K4, H1, H3, H2, J4, G1, G3, G2, H4, F1, F3, F2, G4, E1, E3, E2, F4, D1, D3, D2, E4, C1, C2, B1	POLDAT (31:0)	I/O	Multiplexed data to/ from Policing-RAM/ testbus incl. parity bit. M4 corresponds to POLDAT(31) ... B1 corresponds to POLDAT(0).
L1, L3, L2	$\overline{\text{POLADSC}}$ (2:0)	O	Address status control to Policing RAM. L1 corresponds to $\overline{\text{POLADSC}}$(2) ... L2 corresponds to $\overline{\text{POLADSC}}$(0).
M2	$\overline{\text{POLADV}}$	O	Advance input to Policing RAM.
M1, M3, N4	$\overline{\text{POLCE}}$ (2:0)	O	Chip enable to Policing RAM. M1 corresponds to $\overline{\text{POLCE}}$(2) ... N4 corresponds to $\overline{\text{POLCE}}$(0).
N2	$\overline{\text{POLGW}}$	O	Global write to Policing RAM.
N1	$\overline{\text{POLOE}}$	O	Output enable to Policing RAM.
Downstream Connection RAM Interface (39 pins)			
AD15, AC14, AF14, AE14, AD14, AD13, AF13, AE13, AF12, AD12, AC13, AE12, AF11, AD11, AE11, AC12, AF10, AD10, AE10, AC11, AF9, AD9, AE9, AC10, AF8, AD8, AE8, AC9, AF7, AD7, AE7, AC8	RDATD (31:0)	I/O	Data to/ from connection RAM downstream incl. parity bit. AD15 corresponds to RDATD(31) ... AC8 corresponds to RDATD(0).

Table 1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
AF15, AE15	$\overline{\text{RSCD}}$ (1:0)	O	Downstream RAM address status control. AF15 corresponds to $\overline{\text{RSCD}}$(1) and AE15 corresponds to $\overline{\text{RSCD}}$(0).
AC15	$\overline{\text{RADVD}}$	O	Downstream RAM advance input.
AE16, AD16	$\overline{\text{RCED}}$ (1:0)	O	Downstream RAM chip enable. AE16 corresponds to $\overline{\text{RCED}}$(1) and AD16 corresponds to $\overline{\text{RCED}}$(0).
AF16	$\overline{\text{RGWD}}$	O	Downstream RAM global write.
AE17	$\overline{\text{ROED}}$	O	Downstream RAM output enable.
Address Reduction Circuit Interface, CAME (26 pins)			
AE22, AD21, AF21, AE21, AC19, AD20, AF20, AE20, AC18, AF19, AD19, AE19, AF18, AD18, AC17, AE18, AF17 [2) 4)]	ARCDAT (16:0)	I/O	Data from/to CAME incl. parity bit. AE22 corresponds to ARCDAT(16) ... AF17 corresponds to ARCDAT(0).
AE23, AF22, AD22, AC20	ARCADR (3:0)	O	Address to CAME. AE23 corresponds to ARCADR(3) ... AC20 corresponds to ARCADR(0).
AC21	$\overline{\text{ARCRES}}$	O	Reset to CAME.
AD23	$\overline{\text{ARCCS}}$	O	Chip select to CAME.
AF23	$\overline{\text{ARCWE}}$	O	Write enable to CAME.
AE24	$\overline{\text{ARCOE}}$	O	Output enable to CAME.
AC22	ARCCLK	O	Clock to CAME is half of the ATM-LP core frequency given by SYSCLK.
JTAG Interface (5 pins)			
C25 [1)]	$\overline{\text{TRST}}$	I	Boundary scan reset
C26 [1)]	TDI	I	Test data input
P25 [1)]	TCK	I	Test clock
E23 [1)]	TMS	I	Test mode select
A25 [4)]	TDO	O	Test data output

Table 1 Pin Definitions and Functions (cont'd)

Pin No.	Symbol	Input (I) Output (O)	Function
Test Interface (6 pins)			
AC25 [1]	$\overline{\text{OUTTRI}}$	I	Puts all outputs except TDO into tristate mode.
AC24	$\overline{\text{UTTRI}}$	I	Puts all UTOPIA outputs into tristate mode.
AF24 [2]	SMODE	I	Has to be connected to ground.
AE26 [2]	SENAB	I	Has to be connected to ground.
AD26	ALPIIDD	I	Has to be connected to ground.
AB23	NDTRO	O	

Pin No.	Function
Supply (124 pins)	
E7, E9, E11, E13, E14, E16, E18, E20, G5, G22, J5, J22, L5, L22, N5, N22, P5, P22, T5, T22, V5, V22, Y5, Y22, AB7, AB9, AB11, AB13, AB14, AB16, AB18, AB20	VDD
A1, A2, A26, B2, B25, B26, C3, C24, D4, D23, E5, E6, E8, E10, E12, E15, E17, E19, E21, E22, F5, F22, H5, H22, K5, K22, L11, L12, L13, L14, L15, L16, M5, M11, M12, M13, M14, M15, M16, M22, N11, N12, N13, N14, N15, N16, P11, P12, P13, P14, P15, P16, R5, R11, R12, R13, R14, R15, R16, R22, T11, T12, T13, T14, T15, T16, U5, U22, W5, W22, AA5, AA22, AB5, AB6, AB8, AB10, AB12, AB15, AB17, AB19, AB21, AB22, AC4, AC23, AD3, AD24, AE1, AE2, AE25, AF1, AF25, AF26	VSS
Unconnected pins (0 pins)	
-	unconnected pins

2 Functional Description

2.1 Core Functions and Interfaces of the ATM-LP

The ATM Layer Processor (ATM-LP) is a device which has a bidirectional data transfer throughput of 687 Mbit/s for up to 16384 connections. The ATM-LP performs Header Translation, Traffic Measurement and a simple OAM Fault Management Function in both directions. Additionally a Policing unit is implemented in upstream and a logical Multicast and Buffer Management Unit is implemented in downstream direction. The UTOPIA Interface at the ingress and engress side transfers the standardized ATM cell format.

The connection specific data for Policing, Traffic Measurement and OAM can be stored in external RAMs. If these functions are not needed the related RAMs can be omitted. For Header Translation in downstream direction an external RAM is mandatory. In upstream direction either an external Address Reduction Circuit like the Infineon Technologies Chip CAME PXB 4360 E or an internal Address Reduction Circuit (ARC) can be used for the conversion of the PN/VPI/VCI into a Local Connection Identifier (LCI). The internal ARC is limited in the arbitrary usage of the VPI and VCI range.

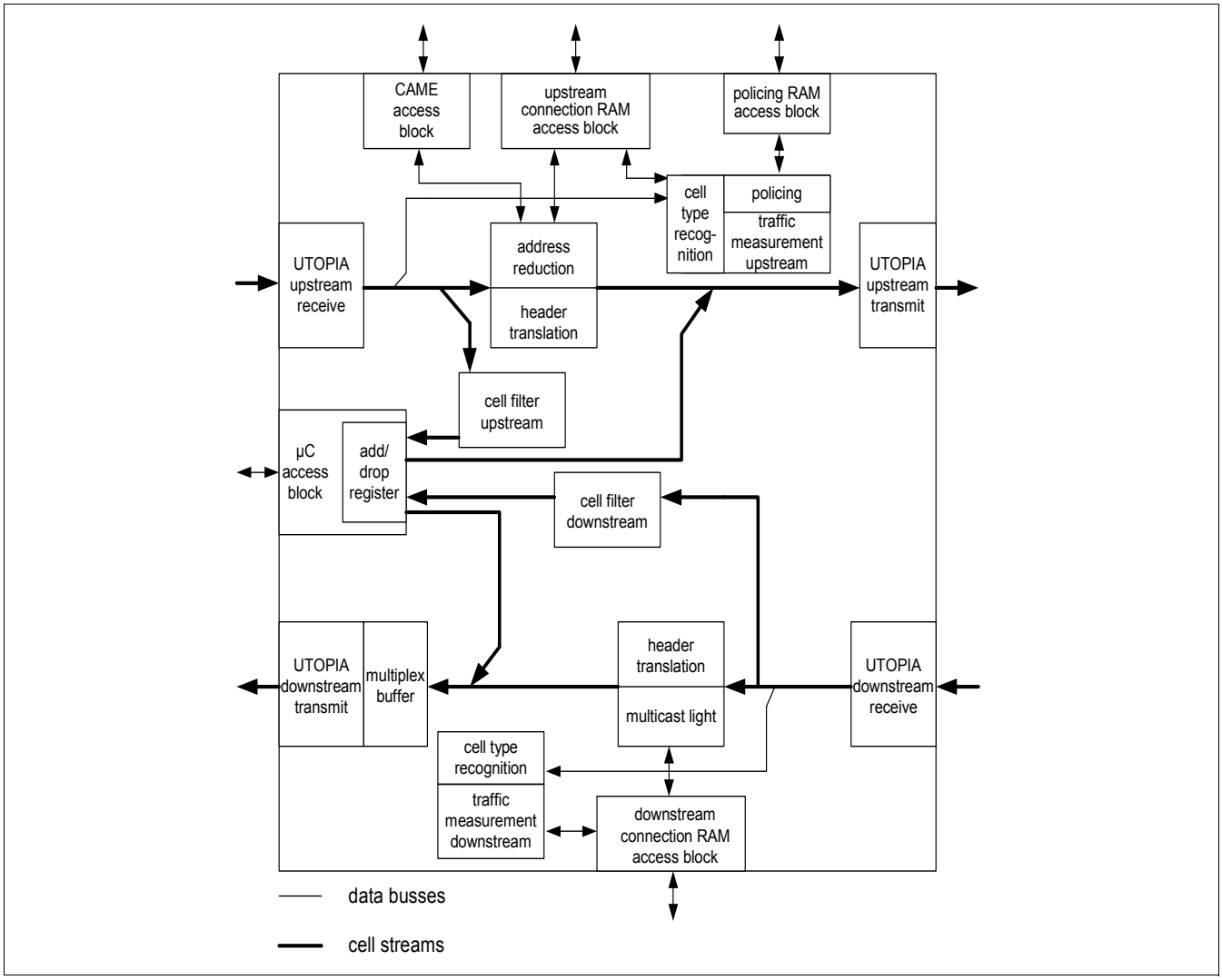


Figure 8 ATM-LP Block Diagram

2.2 Functional Description of user data flow in up- and downstream direction

Throughout this specification the term ‘port’ is used in the meaning given by the UTOPIA specification [1]. ‘Upstream’ means the direction towards the switching network, ‘Downstream’ towards the physical layer device (PHY).

Upstream:

In the upstream direction the cells are taken from the PHY-devices into the input UTOPIA buffer, which performs the speed adaptation between the UTOPIA clock and the internal ATM-LP clock. Subsequently the header of the cell is extracted and used for address reduction together with the port number. The resulting reduced address is called Local Connection Identifier (LCI). It uniquely identifies the connection during processing in the ATM Layer. In order to make the LCI accessible to the following ATM Layer devices (e.g. AOP, ABM) it is mapped into the header of the cell. Additionally the so-called housekeeping (HK) bits are mapped into the cell header (UDF1 byte), which carry Infineon Technologies proprietary cell identification (e.g.: Cross Office Check) evaluated by the ATM Layer devices within the system. The mapping of new contents into the header is called Header Translation (HT). In the ATM-LP the LCI is used as address for accessing the external RAMs containing the connection specific data.

Two other functions performed upon the upstream cell flow are traffic measurement and policing. In case of traffic measurement the various traffic counters are read from the external connection RAM (CONNRAMUP), updated and stored back. The policing unit (POLU) reads the variables, constants and flags needed by the UPC/NPC algorithm, performs it and stores the updated state variables back into the policing RAM (POLURAM). If an overflow of the contracted bit rate happens, cells will be discarded or tagged depending on the chosen configuration. Both, policing and traffic measurement, require a preliminary cell type recognition, which uses the cell header and the connection configuration flags read from CONNRAMUP. If not discarded, the cell with the new header (including LCI and HK) exits ATM-LP through the output UTOPIA interface.

Downstream:

After the cell has passed the input UTOPIA buffer the LCI is extracted from the header and used to address the external connection RAM (CONNRAMDO), which contains the new VPI,VCI and PN as well as the traffic counters for downstream direction. In case of the header translation the restored VPI, VCI and PN are mapped into the header as defined by the external ATM UTOPIA cell format. For special ‘low end’ applications there is a possibility to perform a so-called ‘Multicast-light’ function, which means broadcasting the incoming cell to different ports and/or connections, in exchange for lower performance. The traffic measurements downstream are performed in a similar way as in upstream direction. The outgoing cell is intermediately stored in the UTOPIA output buffer until the addressed PHY device is able to receive it.´

2.3 Address Reduction

The ATM-LP and the other members of the Infineon Technologies 622MBit ATM chip set use an internal address identifier beside the switching element for all ATM related functions. The internal address identifier is named LCI and has an address width of 14 bits which supports up to 16k connections for the STM-4 link. Two modes are supported by the ATM-LP to reduce the address range. The first mode needs an external Address Reduction Circuit (CAME device PXB 4360 E) which translates any arbitrary address, inside the address range from 0 to 2^{32}-1, into another arbitrary address inside the address range from 0 to 2^{14}-1. The configuration of the

external ARC (CAME device) has to be done for each established connection separately. Herewith the PN, VPI and VCI of an incoming cell are converted into an LCI. This mode is the most flexible translation mechanism which is not always needed if the VPI and VCI is in a predefined address range as used e.g. in the Access Network area or in a LAN environment. For such applications an internal Address Reduction Circuit was built in which can be used in a second mode. The internal ARC can be configured with only three parameters for all connections which determine the range of the PN, VPI and VCI for the calculation of the LCI. The cell header structure used by the Infineon Technologies ATM chip set is shown in **Figure 9**.

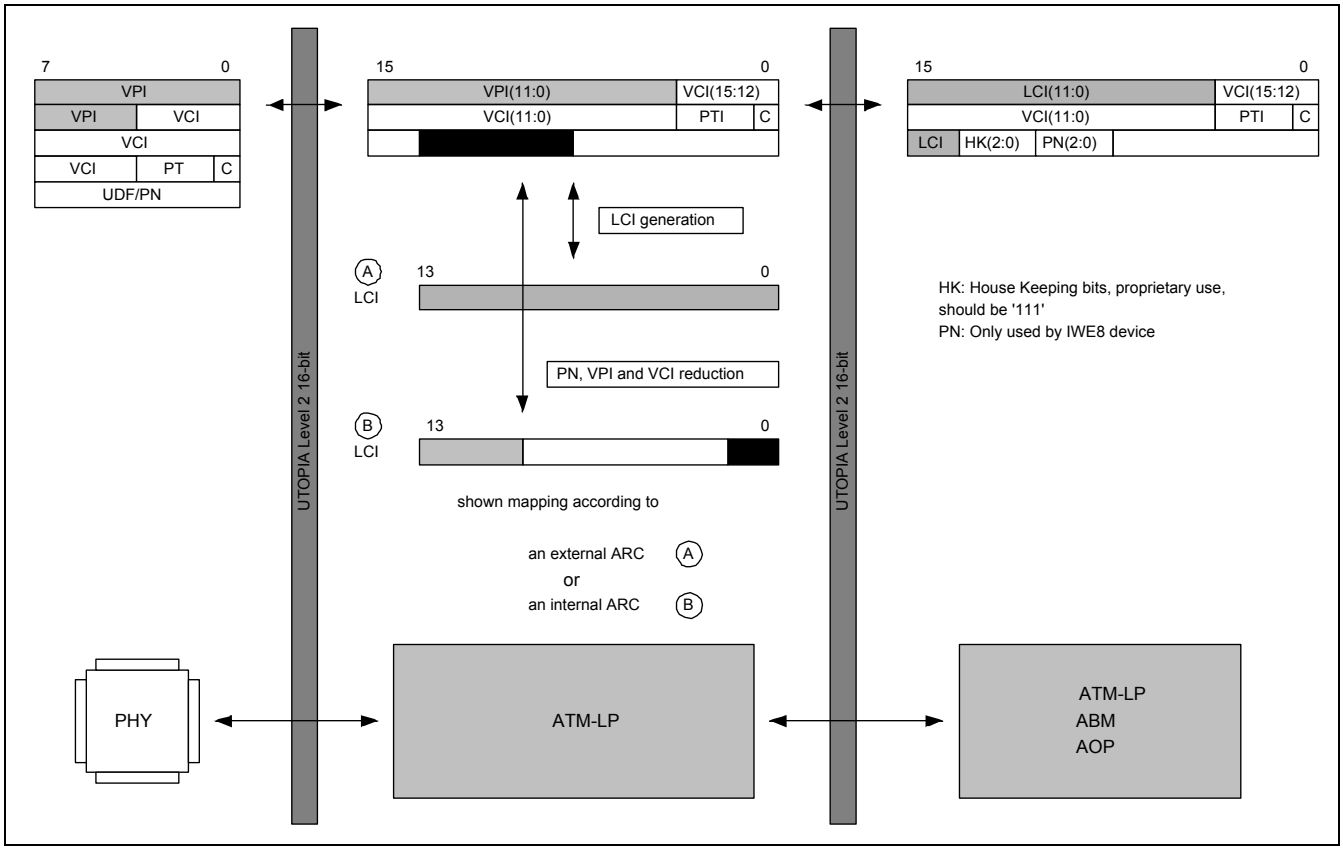


Figure 9 Cell Header Structure used by the ATM Chip Set

The LCI is used by the ATM-LP to address the connection specific entries stored in the external CONNRAMUP and POLURAM in upstream direction and CONNRAMDO in downstream direction. CONNRAMUP stores information for OAM, Traffic Measurement and Header Translation for each connection. It is also SW configurable (see **section 3.3.2.1,** page 77) whether the connection is valid (see VCON_UP) or not which is a useful feature for both set up and release procedure. Herewith an established connection can be configured and tested before it is valid for the user. The release of a connection can be done immediately and afterwards all connection specific data can be read out for billing purposes. The cell arrival of an invalid connection can cause two actions. Either an interrupt is generated (see VLD_ERR_U/D, **section 3.21.2,** page 119) and the cell is discarded or the cell is transmitted (see VLDERREN_U/D, **section 3.29,** page 135) without interrupt generation.

2.3.1 Internal Address Reduction Circuit

The usage and configuration of the internal ARC is SW-controlled via the MODE and ADRED_VPIM register (see **section 3.18,** page 112). The CAM Flag in register MODE selects the usage of the internal or external ARC (CAME device). For the internal ARC the range of the PN, VPI and VCI for the calculation of the LCI is determined by the three parameters P_NUMB, M_NUMB and VPIMIN. The source of the PN, which can be derived either from the UTOPIA Address or the PN inside the UDF1 of a cell, is selected by the flag PN_SOURCE_U. Using internal ARC requires an assignement of VPI and VCI to a logical connection in an order which accommodates the mapping scheme of the ATM-LP (see **figure 12**). The mapping rule has the following concept.

The VPCs are divided into two groups. The first group contains the terminated VPCs and the second group the transparent VPCs. The VPI values of the terminated VPCs are lower than the value of the parameter VPIMIN. The VPI values of the transparent VPCs are greater than or equal to the value of the parameter VPIMIN. The number of VCCs from each terminated VPC is determined by the ratio of the Blocksize (BLS) to maximum PN_{max}. The number of transparent VPCs is equal to the number of VCCs of each terminated VPC minus VPIMIN. The SW is responsible for the correct selection of the parameters P_NUMB, M_NUMB and VPIMIN. The meaning of parameters is the following:

- The Blocksize BLS = number of ports * number of VCCs within a terminated VPC = 2^{M_NUMB}.
- The maximum number of ports $PN_{max} = 2^{P\_NUMB}$.
- The maximum of VCCs in a terminated VPC = $VCC_{max} = 2^{(M\_NUMB - P\_NUMB)} = BLS/PN_{max}$

Please note that,

- since a VPC block size is equal to a VCC block size, $VPC_{max} = VCC_{max}$.
- the terminated VPIs < VPIMIN, the transparent VPIs >= VPIMIN.

The principle of the internal ARC is explained on an example where 4 ports are supported by the ATM-LP. Each port transports 128 VPCs and 128 VCCs per VPC. 20 VPCs are terminated at the ATM switch. The calculation of the three parameters and the mapping rules for the calculation of the LCI is shown in **table 2**, **figure 10** and **11**.

Table 2 Relationship between Network Requirements and Configuration Parameters

Network Requirements	Configuration Parameter
4 Ports	P_NUMB = 2
128 VCCs per terminated VPC	BLS = 4ports * 128 VCCs = 512 -> M_NUMB = 9
128 VPCs split into 20 terminated and 108 transparent VPCs	VPIMIN = 21

According to the requirement of 20 terminated VPCs the value of VPIMIN is 21. The external RAM can store 32 blocks of the given block size (16k / BLS). These blocks should be divided in up to 31 blocks with terminated VPCs (0..30) and one block with transparent VPCs. However for the most efficient usage of the external RAM the value of VPIMIN should be 31. The example is continued with these new parameters. Two mapping rules exist for the mapping of transparent and terminated VPCs.

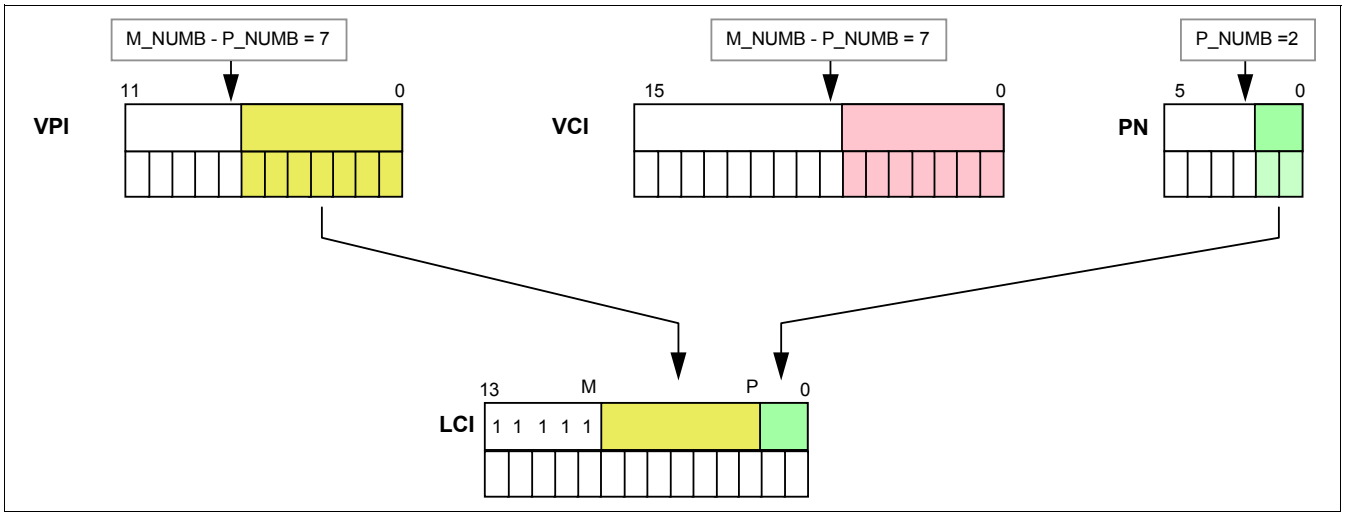


Figure 10 Mapping Rule for Transparent VPCs (VPI ≥ VPIMIN)

Figure 10 shows that the LCI value of the transparent VPCs is gathered only from the VPI and the PN range. The LCI range is in the interval between LCI_{max} and LCI_{max}-2^{M_NUMB} (maximum number of transparent VPC over all ports). Inside the LCI range only the LCIs from the VPCs with a VPI value greater than or equal to VPIMIN are generated. The LCI value from the transparent VPCs with a VPI value between 0 and VPMIN-1 is not generated because the internal ACR mechanism switches to the other mapping rule depicted in **figure 11**. In this case the LCI value of the terminated VPCs is gathered from the PN, VPI and VCI range.

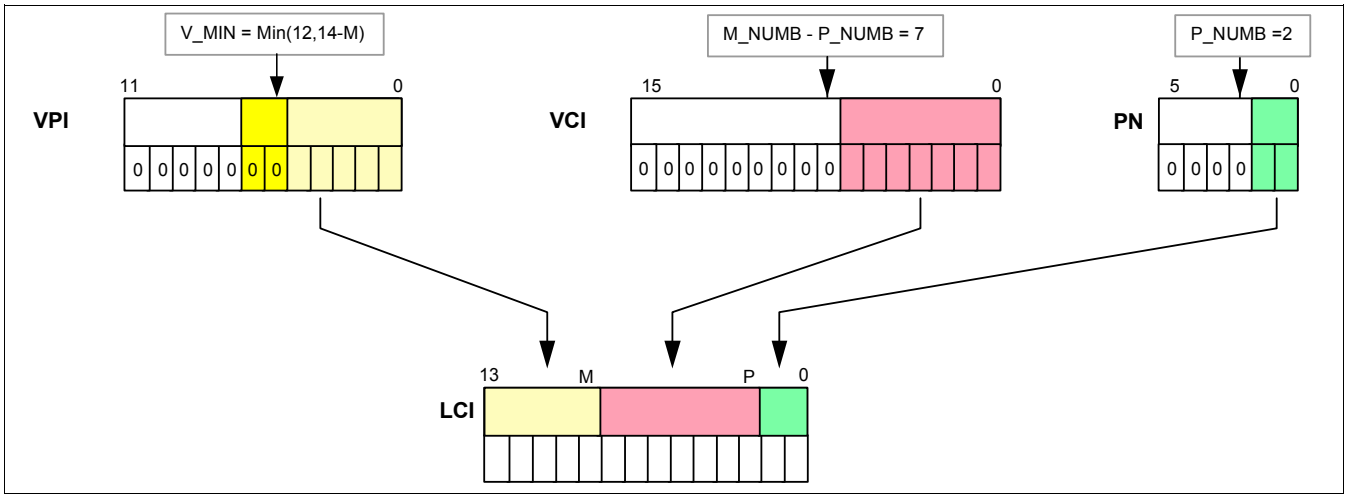


Figure 11 Mapping Rule for Terminated VPCs (VPI < VPIMIN)

The bit field of the PN and VPI not mapped into the LCI must be zero in the header of the incoming cell. Otherwise the cell will be discarded. The same is true for the not mapped bit fields of the VCI of the cell with VPI < VPIMIN.

The mapping rule gives the following LCI structure. The LCI address range is divided into two sections. The upper section contains the LCI which corresponds to the VPI of the transparent Virtual Path Connections. In this section the LCIs for the VPI interval between 0 and 30 are not generated (VPIs ≥ VPIMIN).

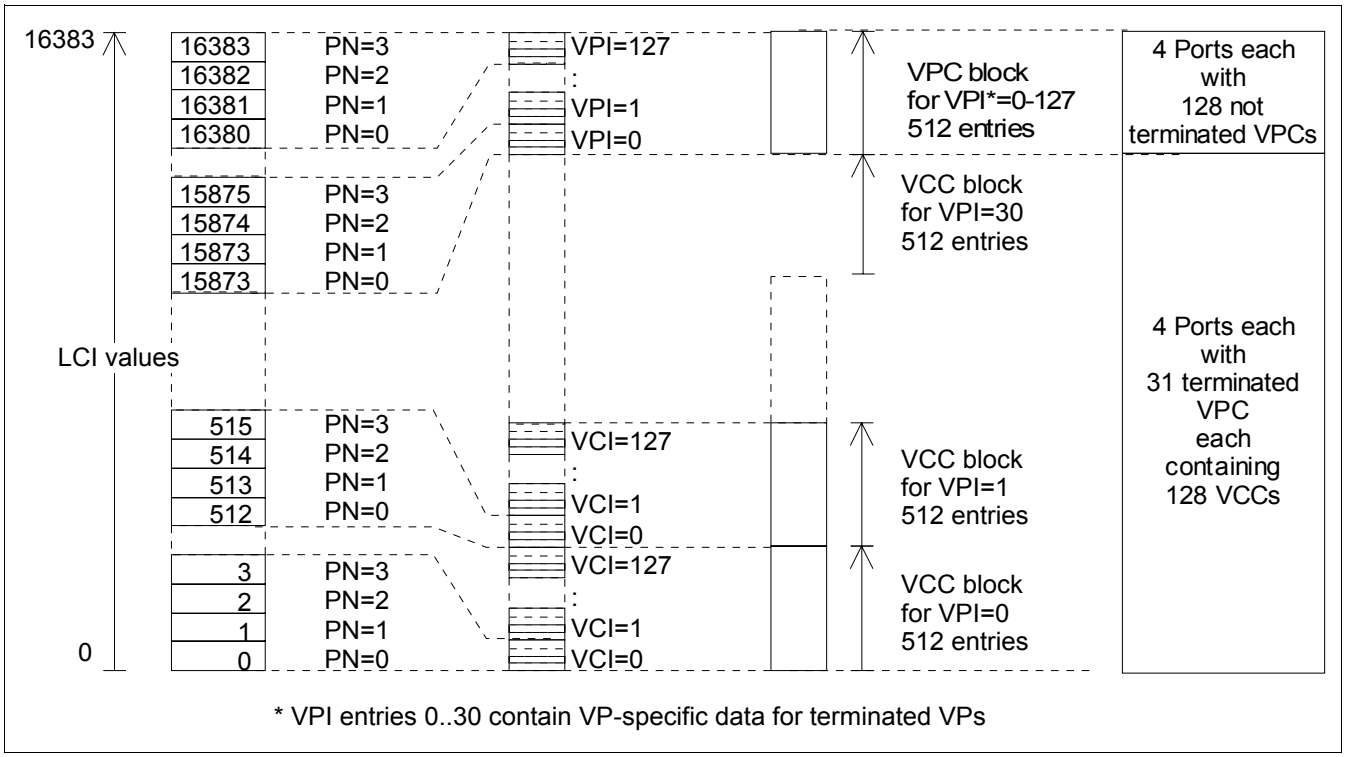


Figure 12 LCI Structure for 4 Ports with a VCI- and VPI Bundle Size of 128

This LCI range can be used to store the connection specific traffic measurement data for the terminated VPCs which are addressed by the LCI2_UP pointer. For detailed explanation see **section 2.5,** page 47. The lower section contains the LCI corresponding to the VPI and VCI values of the terminated Virtual Path Connections. The LSBs of the LCI contain the PHY numbers PN so the ascending LCI-values are cyclically associated with the PHYs. Details of the LCI structure are depicted in **figure 12**.

In the following a second example is shown to explain the difference between the usage of the external ARC (CAME device) and the internal ARC. It is shown that it only depends on the VPI and VCI range whether the internal or external ARC (CAME device) is selected. The scenario is that 2 physical lines are connected to the ATM-LP via the UTOPIA interface at port 1 and 2.

a) At port 1: There are transmitted 10 terminated and 205 not terminated VPCs.
VPI = 0 contains 73 VCCs (VCI = 0...72),.... and VPI = 9 contains 40 VCCs (VCI = 0...39).
b) At port 2: There are transmitted 1 terminated and 180 not terminated VPCs.
VPI = 0 contains 86 VCCs (VCI = 0...85).

For the selected VPI and VCI values the external ARC (CAME device) has to be used. The internal ARC can be used if different VPI/VCI values are chosen for the same number of transmitted VPCs and VCCs. The steps for the selection of the right VPI and VCI values are depicted in **figure 13**. In this example the VPI values for the first not terminated VPC have to be shifted to VPIMIN = 16. Additionally the number of all VCCs of each terminated VPC has to be the same as the number of all transmitted VPCs.

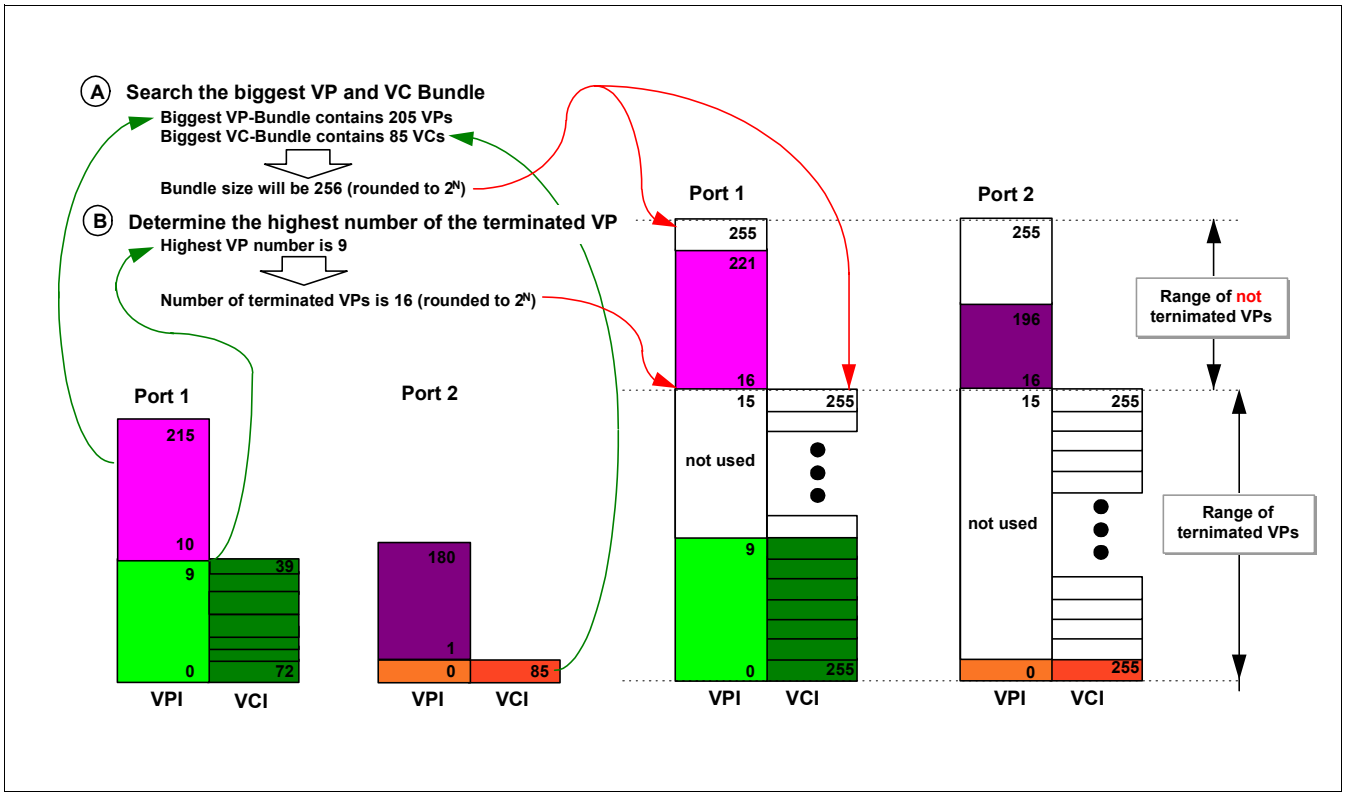


Figure 13 VPI/VCI Range needed for Usage of Internal ARC

The number of VPCs being equal to the number of VCCs is 256. Using such VPI/VCI values we can serve up to 4 ports each transmitting 4096 connections. The difference between the two scenarios is that the internal ARC has predefined ranges of VPI and VCI which are not completely used.

2.3.2 External Address Reduction Circuit (CAME device)

The Address Reduction Circuit can be a Content Addressable Memory or a Pointer Look-up Circuit which reads the PN, VPI and VCI and delivers the corresponding LCI as a search result. Infineon Technologies provides a Content Addressable Memory Element CAME PXB 4360 E. The ATM-LP supports the configuration, test and search in the external ARC operation mode (CAME device, see **figure 14**).

The configuration of the external ARC (CAME device) is SW controlled. The CAM Flag of the MODE register (see **section 3.18.2,** page 112) selects the usage of the external ARC (CAME device). For the setup of each connection the corresponding LCI, PN, VPI and VCI are written from the microprocessor into the ADR (see **section 3.26,** page 130), CAMADRL register (see **section 3.6.1,** page 92) and CAMADRH register (see **section 3.6.2,** page 92). Furthermore it can be defined whether this entry belongs to a connection of a terminated VPC and whether the entry is valid which is indicated by the P_IP and VCON bits respectively in the ADR register. Subsequently the CAME-Write command of the CMR (see **section 3.19,** page 113) register invokes the writing of the ADR, CAMADRL and CAMADRH register successively to the external ARC (CAME device). After a number of cycles needed for the command execution of the CAME the ATM-LP reads the status information from the CAME and writes it into the CSTATR register (see **section 3.20.2,** page 116). An indication for the execution of the CAME-Write command is delivered to the CMR register. In the CSTATR register two alarm

indications are foreseen for the CAME-Write mode. First alarm is generated by the CAME if a PN, VPI, VCI and LCI iswritten into the CAME which already exists. Such an entry is refused by the CAME. The second alarm is generated by the CAME if a valid connection (VCON in the CAME) is overwritten. This means the PN, VPI and VCI for an active LCI is changed without switching down the VCON of the LCI in the previous step. This has to be prevented because the connection has to be released before an new connection with the same LCI is set up. In this case the CAME has to refuse the entry.

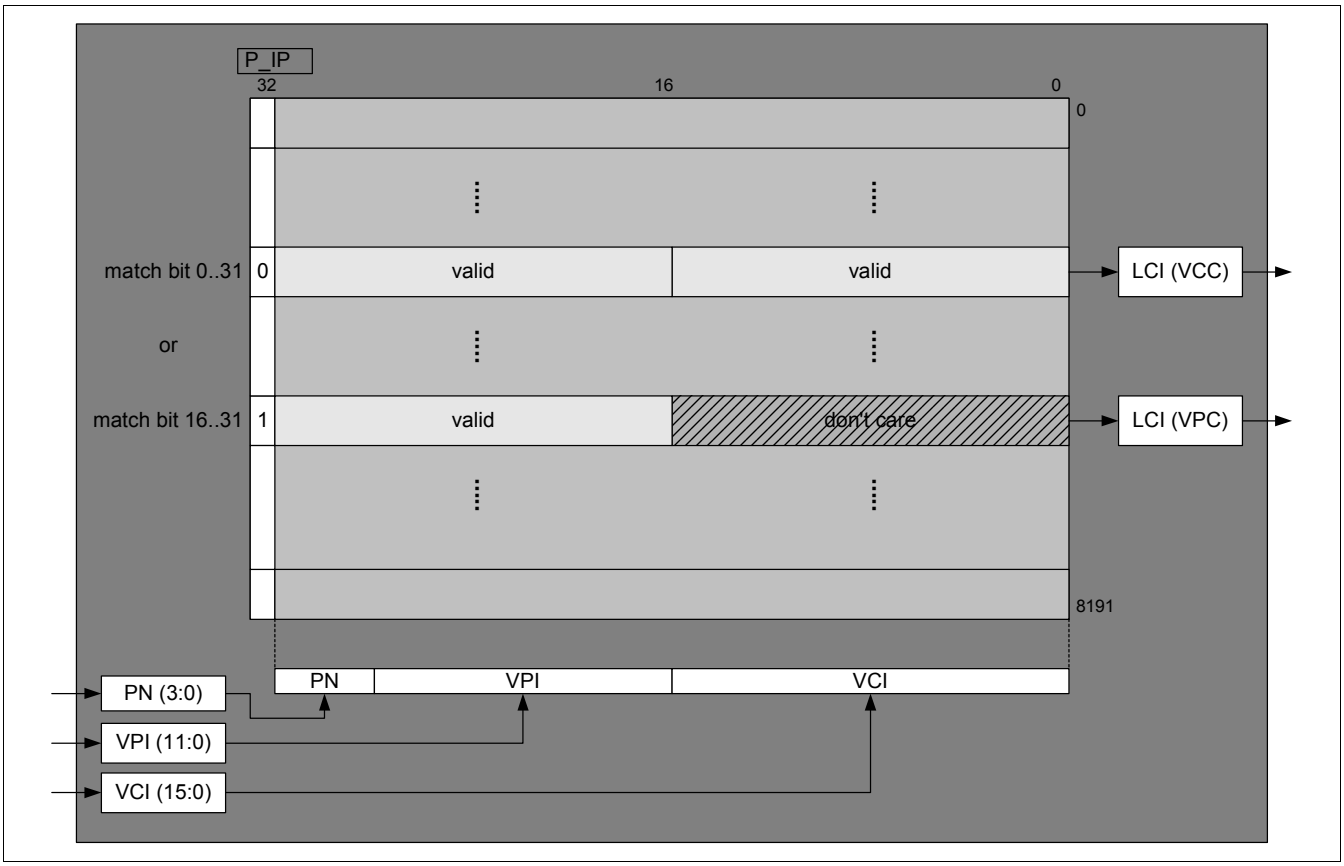


Figure 14 Address Reduction with CAME

The ATM-LP supports a CAME-Read mode into the CMR register to verify the values of the PN, VPI, VCI, P_IP and VCON for each LCI defined in the ADR register, which are written into the CAMADRL and CAMADRH registers.

To test the external ARC (CAME device) a test mode is supported by the ATM-LP. In this mode the test commands are written into the ADR register and transferred to the CAME with the test command in the CMR register. After test command execution the ATM-LP reads the status information and writes it into the CSTATR register. Two test cases are foreseen to identify failures in the internal memory of the CAME. After the configuration of the memory banks with a predefined value the contents of the memory banks are read and compared. In case of a difference an alarm indication TEST READ FAULT is activated in the CSTATR register. The same can be done using a search command which detects memory locations with different contents. For this case the alarm indication TEST SEARCH FAULT is activated in the CSTATR register.

Upon cell arrival the ATM-LP invokes the CAME search command either for the user cells or for the OAM F4 Flow cells of a terminated VPC. The PN, VPI and VCI are written to the external

ARC (CAME device). After the execution of the search command which needs a number of cycles the ATM-LP reads the LCI, VCON, P_IP and status information. The status information is written into the CSIR register and the LCI is written into the cell header. The source of the PN which can be either the UTOPIA Address or the PN in the UDF1 of the cell is determined by the PN_SOURCE_U in the MODE register. The number of PN(5:0) bits used for the CAME is defined by P_NUMB in the MODE register and has to be in the interval between 4 and 6. For P_NUMB equal to 4 the contents of CAMADRH(16:0) are gathered from PN (3:0) and VPI (11:0) which is used for NNI application. If the number of PN bits is increased then

(16 - (number of PN bits))

least significant VPI bits are mapped into the CAMADRH register. In case of a failure all internal errors in the CAME during the address reduction are signalled by the CAM_ERR interrupt in the ISR1 register (see **section 3.21.2,** page 119). The status information is written into the CSIR register (see **section 3.22,** page 123). Information on parity errors at the CAME interface, mismatch or multimatch as a response of the CAME search command and other failure cases are given. The VCON bit in the CAME defines whether the connection is valid or not. For not valid LCIs the ATM-LP will discard or forward the cell depending on the NODIS_CAM flag in the TESTR (see **section 3.29,** page 135) register. For OAM F4 cells the CAME delivers an LCI of any of the VCC's contained in the VPC.

A short summary of all SW related control, interrupt and status registers is given below for orientation. The detailed description can be founded in **section 3,** page 66.

Control bits of the internal register **MODE**:

- The usage of the internal or external Address reduction circuit is determined by the **CAM** bit.
- The **P_NUMB** bits define how many bits of the port number are used to derive the LCI. The port number is used by both the internal and external ACR.
- The **M_NUMB** bits define the block size used by the internal ACR to derive the LCI. The **PN_SOURCE_U** bit selects whether the UTOPIA address or the PN in the UDF1 of the cell header is used as the source of the port number.

Control bits of the internal register **ADRED_VPIM**:

- **VPIMIN** bits define the lowest VPI value of all transparent VPCs. This parameter is only used by the internal ARC. The value of VPIs above the value of the lowest VPI belong to the group of transparent VPCs (not terminated VPC).

Control bits of the register **ADR**:

- **ADR** bits correspond to the value of the LCI for the operation of the external ARC (CAME device).
- **P_IP** bit indicates whether the connection point is a path intermediate point of a transparent VPC or an termination point of the VPC.
- **VCON** bit indicates whether the connection is valid or not.

Control bits of the registers **CAMADRL** and **CAMADRH**:

- **VCI** bits correspond to the value of the VCI for the operation of the external ARC (CAME device).
- **PN** bits correspond to the value of the PN for the operation of the external ARC (CAME device).
- **VPI** bits correspond to the value of the VPI for the operation of the external ARC (CAME device).

Control bits of the internal register **CMR**:

- **MPREQDEF** bits control both the reading from and the writing to the external ARC (CAME device) and CONNRAMUP. The data transfer to the external ARC (CAME device) occurs via the internal registers ADR, CAMADRL and CAMADRH. The data transfer to the external CONNRAMUP occurs via the internal registers ADR, WDRxL/H and RDRxL/H. Besides the separate transfer to the ADR and CONNRAMUP it is also possible to write the data to both units simultaneously. The addressing of the WDRxL/H occurs via the LCI in the internal ADR register which is also used for programming, testing and operation of the external ADR.
- **STREQ** bit invokes the command and indicates the finishing of the command which is defined by the **MPREQDEF** bits.

Status bits of the internal register **CSTATR**:

- **STATUS** bits give a detailed status report of the external ARC (CAME device) after the microprocessor request.

Alarm Indication bits of the internal register **ISR1**:

- **CAM_ERR** bit gives an interrupt if errors occur during the address reduction in the external ARC (CAME device).

Status bits of the internal register **CSIR**:

- **STATUS** bits give a detailed failure report of the external ARC (CAME device) whenever the interrupt CAM_ERR is generated.

Configuration bit of the Test register **TESTR**:

- The bit **NODIS_CAM** determines whether a cell is discarded or not if the connection is not configured in the external ARC (CAME device) for this cell.

Test bits of the Test register **CAMVILCI**:

- The bits **LCI** are the response to the LCI value from the external ARC (CAME device) in the test mode.
- The bit **P_IP** is the response to the P-IP value from the external ARC (CAME device) in the test mode.
- The bit **VCON** is the response to the VCON value from the external ARC (CAME device) in the test mode.

2.3.3 Processing of the Header Structure by the ATM-LP

The header format of the ATM cells which are received and transmitted at the 16 bit UTOPIA Interface at the PHY side is depicted in **figure 15**. According to the standardized cell format [1], the ATM-LP optionally supports a second proprietary port number information in the UDF1 (word2(8:15)). In upstream direction the ATM-LP can extract the port number either from the UTOPIA Address or from the UDF1 in the cell header. In downstream direction the ATM-LP can provide two port numbers simultaneously. The first port number is transmitted via the UTOPIA Address and the second via the PN in the UDF1. This is a useful feature especially for low bit rate lines were up to 64 ports can be supported with one queue and a single UTOPIA address. However it is necessary that the PHY device translates the second PN in the UDF1 into the corresponding PN of the physical line. The Infineon Technologies chip IWE8 (PXB4220) supports this feature. The contents of the new generated cell in downstream direction come from the external RAM (CONNRAMDOWN).

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	VPI(11:0) or GFC(3:0) and VPI(7:0)												VCI(15:12)			
1	VCI(11:0)												PT(2:0)			CLP
2			PN(5:0)						UDF2							
word																

Figure 15 Cell Header Format at the PHY-ATM-LP UTOPIA Interface

The header format of the ATM cells which are received and transmitted at the 16 bit UTOPIA Interface at the ATM side is depicted in **figure 16**. The contents of the new generated cell in upstream direction come from the internal or external Address Reduction Circuit (LCI), the external RAM CONNRAMUP (HK) and the policing unit (CLP) depending on the nonconformance test.

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	LCI(11:0)												VCI(15:12)			
1	VCI(11:0)												PT(2:0)			CLP
2	LCI(13:12)		HK(2:0)			PN(2:0)			UDF2							
word																

Figure 16 Cell Header Format at the ATM-ATM-LP UTOPIA Interface

2.3.3.1 House Keeping (HK) Bits

Within the Infineon ATM Chip Set the use of House Keeping (HK) bits is possible. These three bits are included in the cell header in upstream direction and evaluated only in downstream direction. These bits are used to perform a kind of node internal OAM processing which is Infineon proprietary. The ATM-LP only supports three combinations. With HK = "111" the incoming cell is a user cell, i.e. all cells without special HK functions. When a user cells arrives at the ATM-LP, it is forwarded to the UTOPIA interface. Cells with HK = "010" are Dynamic Bandwith Allocation (DBA) cells, which are needed for traffic management. These cells are dropped to the microprocessor. The last supported HK = "100" defines Cross Office Check (COC) cells. These cells are used to verify the functionality of the network node. They are dropped to the microprocessor when arriving at the ATM-LP. Because the HK is only defined in the Infineon ATM Chip Set, all cells with HKs should not leave the network node. Therefore all cells with not supported HKs are discarded. The HK function can be disabled using bit HK_DIS in register DCT_CONFIG (see **section 3.24.2,** page 127).

2.4 Policing in Upstream Direction

At the announcement of a connection request, an acceptance algorithm checks in ATM networks if enough capacity is available on the transmission line in order to transmit the user data at the desired bit rate assuring quality of services objectives. The connection acceptance algorithm usually requires separate policing of Sustainable Cell Rate (SCR, ATM-Forum) and Peak Cell Rate (PCR, ITU). The policing function checks if the cells of the incoming cell stream are conforming to the negotiated connection parameters in order to guarantee the transmission quality for each network user. If the contracted cell rate is exceeded the cell is either discarded or tagged (changing the CLP bit from 0 for high priority cells to 1 for low priority cells, i.e. increasing the cell loss probability.). Policing at the entrance of the public network is called Usage Parameter Control (UPC); policing between two networks is called Network Parameter Control (NPC).

The UPC/NPC algorithm implemented in the ATM-LP is functionally equivalent to the Generic Cell Rate Algorithm (i.e. Leaky Bucket or Virtual Scheduling Algorithm, abbreviated GCRA, LB or VSA) as defined in the ATM Forum, UNI specification and the ITU-T recommendation I.371.

The Policing Unit of the ATM-LP has a UPC/NPC function capability on a per connection basis for up to 16384 connections. The general configuration and the alarm indication of the policing unit is determined by the internal registers of the ATM-LP (P_CONRL [**section 3.7.1,** page 93], P_CONRH [**section 3.7.2,** page 94], SC_CONR1 [**section 3.27.1,** page 131], SC_CONR2 [**section 3.27.2,** page 131], ISR1 [**section 3.21.2,** page 119] and TESTR [**section 3.29,** page 135]). The connection specific configuration of the Leacky Bucket (LB) units and the corresponding policing parameters are stored in the external POLURAM (Dword 0-10 [**section** 3.3.1.1 - 3.3.1.11, page 73 - page 75]). The counter values of the nonconforming cells are stored in the external SSRAM (CONNRAMUP) [**section 3.3.2,** page 77] for traffic measurement.

2.4.1 The Leaky Bucket (LB) Algorithm

The principle of the Leaky Bucket can be viewed as a finite capacity bucket whose real-valued content drains out at a continuous rate of one unit of content per time unit and whose content is increased by the increment T for each conforming cell. Equivalently, it can be viewed as the work load in a finite capacity queue or as a real-valued counter. If at a cell arrival the counter of the bucket is less than or equal to the limit value τ, then the cell is conforming; otherwise, the cell is non-conforming. The capacity of the bucket (the upper bound of the counter) is $(T+\tau)$.

Tracing the steps of the continuous-state leaky bucket algorithm (see **figure 17**), at the arrival time of the first cell $t_a(1)$, the content of the bucket is set to zero and the last conformance time LCT is set to $t_a(1)$. At the next arrival time of the k^{th} cell $t_a(k)$, first the content of the bucket is provisionally updated to the value X', which equals the content of the bucket after the arrival of the last conforming cell X minus the amount the bucket has drained since the arrival, $[t_a(k)\text{-LCT}]$. If X' is less than or equal to the limit value τ, then the cell is conforming and the bucket content X is set to X' (or to 0 if X' is negative) plus the increment T, and the last conformance time LCT is set to the current time $t_a(k)$. If X' is greater than the limit value τ, then the cell is non-conforming and the values of X and LCT are unchanged.

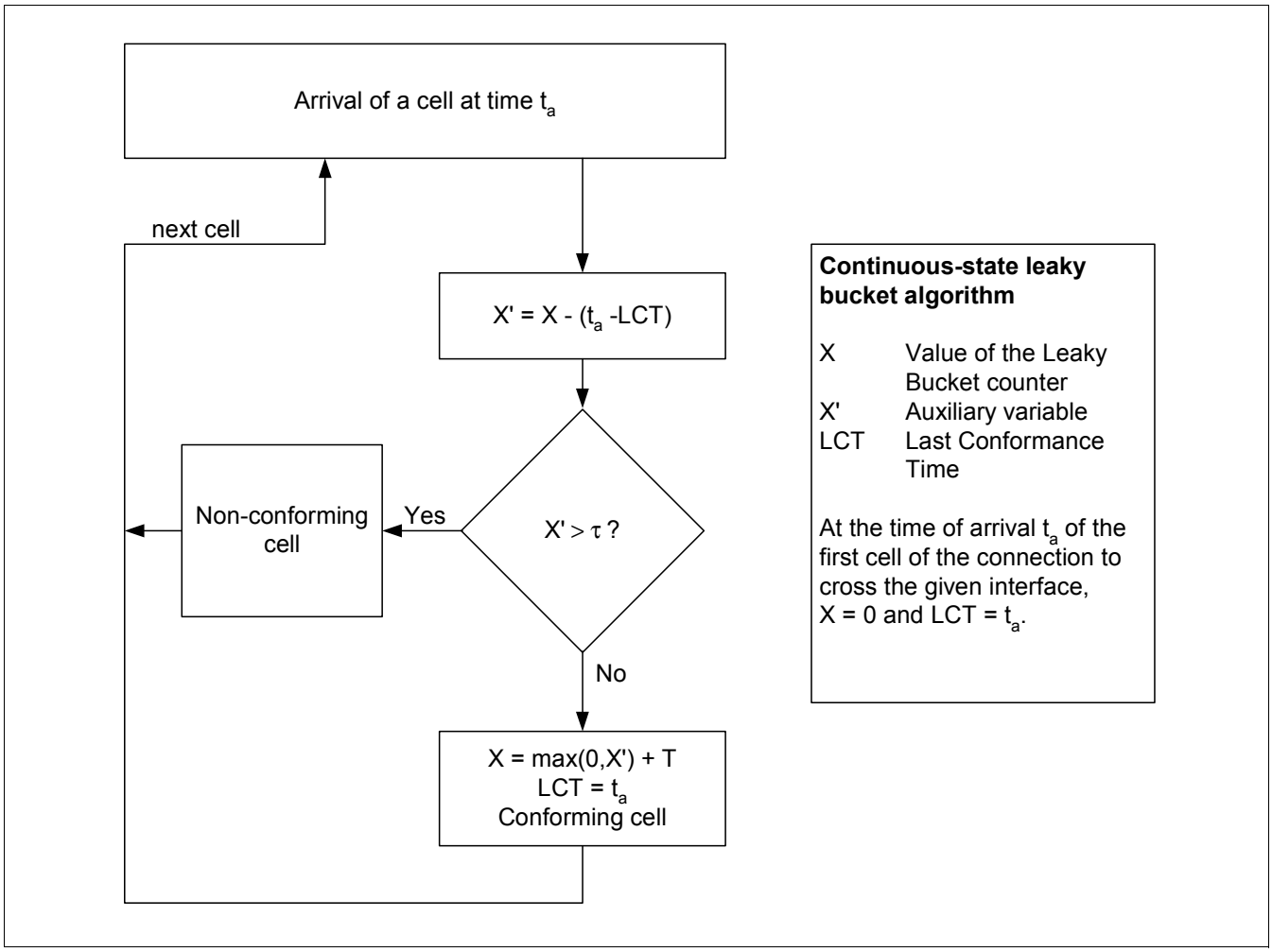


Figure 17 Leaky Bucket Algorithm (according to ITU-T I.371)

To realize a number of different sevices defined by ATM-Forum and ITU, the ATM-LP provides a set of three Leaky Buckets, organized in two parallel branches. The first upper branch contains an LB1 and optionally an LB2 in serial. Herewith the parameters of the services can be realized. The second down branch contains the LB3. The lower branch is not necessary for the realisation of ATM-Forum and ITU-T services. Therefore LB3 can be disabled and is provide for additional parameters. For each connection the Leaky Bucket configuration and the policing parameters, containing the three parameters W_{min}, Delta and Y (see **section 2.4.3,** page 44), are stored in the external policing RAM (POLURAM, see **section 3.3.1,** page 73). The POLURAM entry for a connection contains 11 Dwords. The Dwords 0 to 9 contain the policing parameters, Dword10 the configuration parameters. Up to four different modes are selectable per connection via the MODE bits. The policing configuration modes are summarized in **table 3**, page 41 and are depicted in the **section 2.4.2.1,** page 42 (mode 0), **section 2.4.2.2,** page 43 (mode 1), **section 2.4.2.3,** page 43 (mode 2) and **section 2.4.2.4,** page 44 (mode 3). The context between policing modes and the services of ATM-Forum and ITU is shown in **table 4**.

Table 3 Policing Operation Modes

Mode	Tagging	LB1	LB2	LB3
0	Yes	SCR (0)	PCR (0+1)	PCR (0+1)
1	No	SCR (0)	PCR (0+1)	PCR (0+1)
2	No	SCR (0+1)	PCR (0+1)	PCR (0+1)
3	No	PCR (0+1)	disabled	PCR (0+1)

Table 4 Definition of Services (ITU-T and ATM-Forum)

ITU-T		ATM-Forum		Mode
Service	Parameters	Service	Parameters	
DBR	PCR (0+1) PCR (OAM)	CBR	PCR (0+1) PCR (OAM)	3
SBR1	PCR (0+1) SCR (0+1)	VBR1	PCR (0+1) SCR (0+1)	2
SBR2	PCR (0+1) SCR (0)	VBR2	PCR (0+1) SCR (0)	1
SBR3	PCR (0+1) SCR (0) tagging optional	VBR3	PCR (0+1) SCR (0) tagging optional	0
ABT/DT ABT/IT	PCR (0+1) SCR (0+1) PCR (RM) PCR (OAM)			2
		UBR1	PCR (0+1)	3
		UBR2	PCR (0+1) tagging optional	not supported
ABR	PCR (0+1) MCR (0+1)	ABR	PCR (0) MCR (0) ICR (0) ACR (0)	for ITU : 3 for ATM : not supported

For each connection the microprocessor can configure which cells should be policed. Therefore register MODE consists a set of 2-bit flags for seven different cell types. Using these flags it is choosen, if the according cell type is policed (and in which branch) or not. If all cell types in a connection are not policed by setting the flag bits to ’00’, the connection is defined as not configured. In this case an interrupt is generated if a cell for this connection is detected by the POLU. Using bits DIS_U/D the microprocessor is able to select, which branch for the Leaky Bucket is used.

2.4.2 General Configuration of the POLU

The operation of the POLU is controlled by the microprocessor via the P_CONRL and P_CONRH registers. The VALID_CONF bit is used to indicate that the data has been changed by the microprocessor and that the POLU has accepted and executed the command. Two operation modes, namely Test Operation Mode (TOM) and Normal Operation Mode, are

implemented. A reset of the ATM-LP puts the POLU in TOM with no policing is enabled. After initializing the POLURAM (all ’0’) and the establishment of a connection the POLU can be operated in the Normal Operation Mode by setting the TOM bit in register P_CONRL. For all connections the tagging and discarding of cells can be suppressed resprectively via the bits TAGINH and DISINH.

Using the scan registers SC_CONR1 and SC_CONR2 the range of policed LCIs is defined. The POLU can only be operated after the activation of the POLU refresh mechanism which is activated with the POLU_REFR_EN bit.

The TESTR register provides two bits for the handling of incorrect cells. The selection whether a cell is discarded or not if the cell generates a parity error at the POLURAM interface is done using bit PARERREN_POLU. Such an error is indicated via the interrupt status register bit POLU_PARERR_U. It doesn’t matter if discarded or not, for these cells no policing occurs. The second bit, POVLDERREN, determines whether a cell is discarded or not if the connection is not configured for this cell. This error generates an interrupt which is indicated by the interrupt status register bit POLVLD_ERR. A connection is not configured if all values of the cell policing option flags are ’00’. A connection is defined as configured if all values of the cell policing option flags are ’11’. For both cases the policing is not active.

2.4.2.1 Operation Mode 0

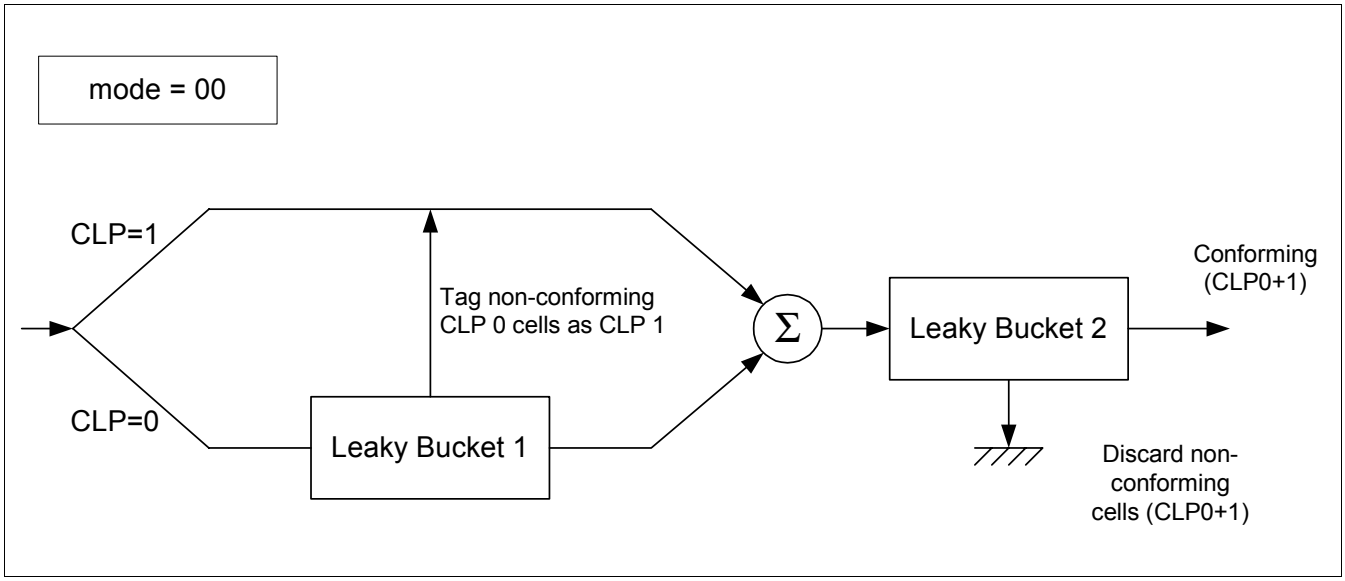


Figure 18 POLU Operation Mode 0

This mode is the only one in which the priority of non-conforming cells is changed to lower priority (cell is tagged). When this mode is configured, e.g. for SBR.3 (ITU) or VBR.3 (ATM-Forum) services, the values for the LB1 are calculated with the SCR(0)-parameter and the values for LB2 with the PCR(0+1)-parameter. Cells with CLP=1 bypass the LB1. Only cells with CLP=0 are policed by the LB1. The resulting cell stream, consists of the conforming CLP(0) cells and the not policed cells with CLP(1), run through the policing with LB2.

2.4.2.2 Operation Mode 1

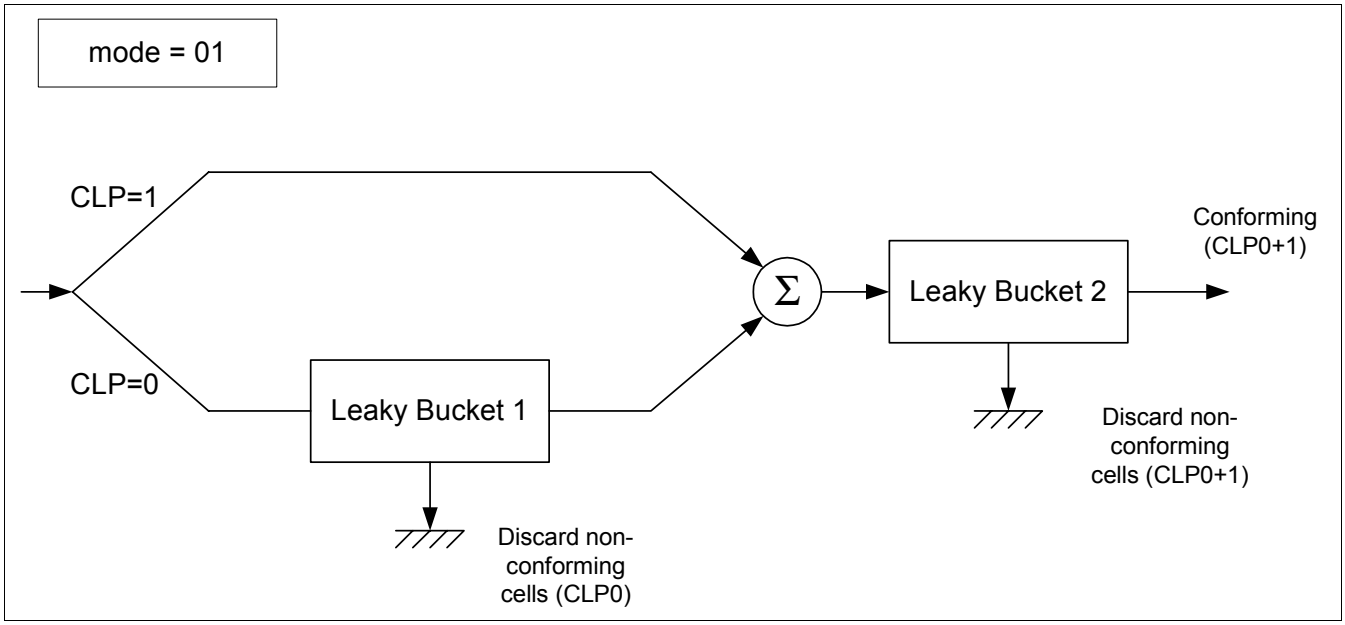


Figure 19 POLU Operation Mode 1

This mode is configured for e.g. SBR.2 (ITU) or VBR.2 (ATM-Forum) services. The values for the LB1 are calculated with the SCR(0)-parameter and the values for LB2 with the PCR(0+1)-parameter. Cells with CLP=1 bypass the LB1. Only cells with CLP=0 are policed by the LB1. In this mode, no tagging is available. So the non-conforming cells are discarded. The resulting cell stream, consists of the conforming CLP(0) cells and the not policed cells with CLP(1), run through the policing with LB2.

2.4.2.3 Operation Mode 2

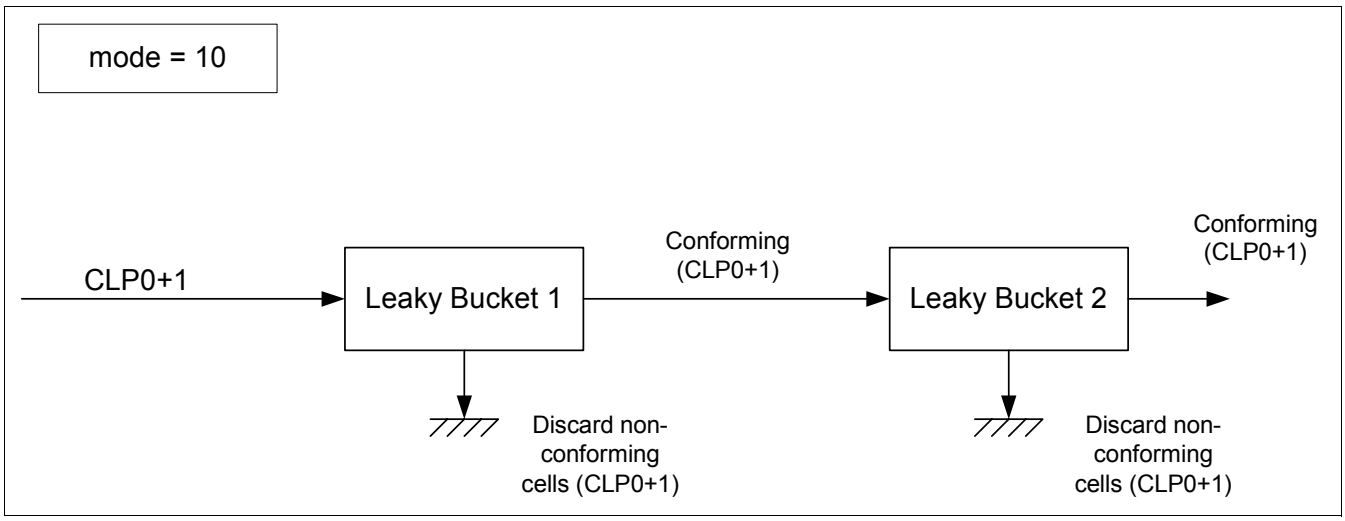


Figure 20 POLU Operation Mode 2

In mode 2 the values for the LB1 are calculated with the SCR(0+1)-parameter and the values for LB2 with the PCR(0+1)-parameter. This mode is selected e.g. for SBR.1 (ITU) or VBR.1 (ATM-Forum) service. The complete cell stream (cells with CLP=0 and CLP=1) is policed by the LB1. The resulting cell stream is conforming to the SCR(0+1) and is afterwards policed by LB2.

Now, the resulting cell stream is conforming to the PCR(0+1). Additionally the LB3 can be declared for PCR(OAM) policing (for ABT services by ITU).

2.4.2.4 Operation Mode 3

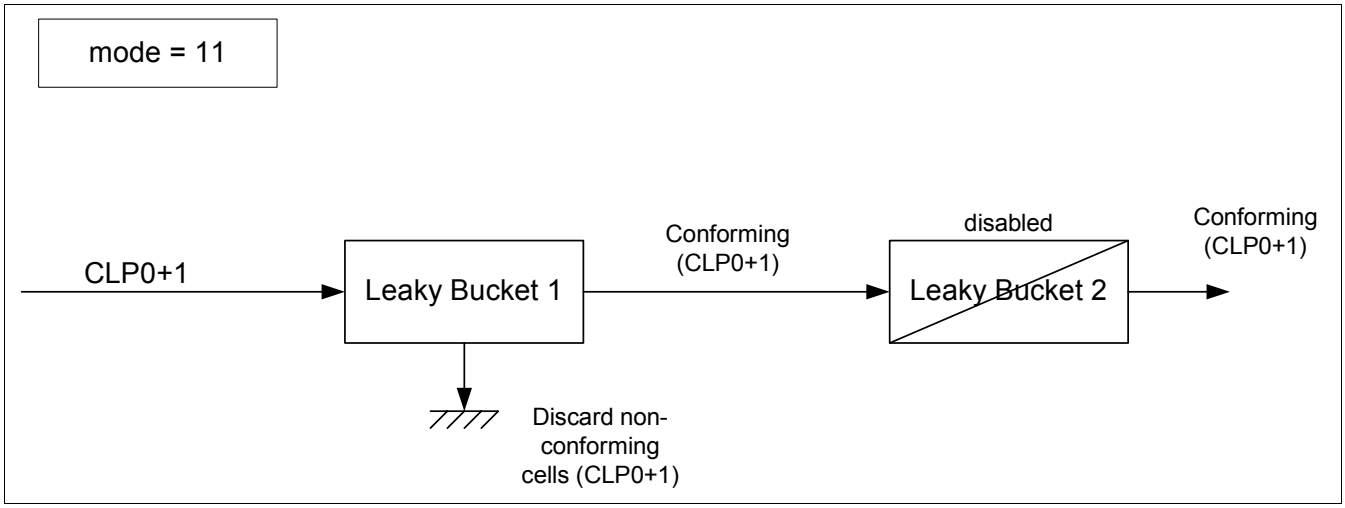


Figure 21 POLU Operation Mode 3

This mode is used e.g. for DBR (ITU), CBR or UBR1 (ATM-Forum) services. The values for the LB1 are calculated with the PCR(0+1)-parameter. The LB2 is disabled in this mode, the cell stream passes it without policing actions. The complete cell stream is policed by the LB1. The non-conforming cells are discarded. For DBR and CBR the LB3 can be configured for policing the PCR (OAM).

2.4.3 Calculation of POLU Parameters

The policing parameters for the leaky bucket are derived from the PCR, SCR, MBS and tagging indication provided from the signalling message. The CDVT is provided by the network operator via mutual agreements between network operator and user or via signalling message. The Λ_x and T_x parameters for SCR and PCR are calculated with the same formula. Therefore the index in the formula is named xCR, where x stands for Peak (P) or Sustainable (S).

According to ITU up to 16384 xCR values Λ_{xCR} are defined which range from 1cell/s to 4.29077Gcell/s. The relative difference between any pair of successive Λ_{xCR} value is smaller than 2^{-9}.

$$m_{xCR} = \left\lceil \log_2\left(\frac{xCR_{sig}}{1023}\right) + 9 \right\rceil$$

$$k_{xCR} = \left\lceil \frac{xCR_{sig}}{2^{m_{xCR}-9}} - 512 \right\rceil$$

Note : $\lceil x \rceil$ stands for rounding up to the nearest integer value.

$$\Lambda_{xCR} = 2^{m_{xCR}}(1+k_{xCR}/512) \text{ [cells/second]}$$
$$0 \le m_{xCR} \le 31$$
$$0 \le k_{xCR} \le 511$$

The reciprocal value of Λ_{xCR} gives the corresponding peak emission interval value $T_{xCR.}$ Due to the non-linearity an extra bit is needed for the exponent. T_{xCR} is calculated as:

$$T_{xCR} = 2^{-(m_{xCR}+1)} \cdot \left(1 + \frac{1023 - k'_{xCR}}{1024}\right) \text{seconds}$$

$$k'_{PCR} = \left[\frac{2047 \cdot k_{xCR} - 512}{k_{xCR} + 512}\right] + 1$$

$$0 \le m_{xCR} \le 31$$

$$0 \le k_{xCR} \le 511$$

This gives 16384 peak emission interval values T_{xCR} ranging between 0.9995 and $2.33*10^{-10}$ seconds. The relative difference between any pair of Λ_{xCR} and T_{xCR} is smaller than 0.0997%. For the non-conformance test of a connection two policing parameters are needed by the POLU for configuration of the Leaky Buckets. These are the value of **Delta**, the decrement parameter, and $\mathbf{W_{min}}$, comparable to the limit value of the Leaky Bucket. The two parameters are stored between Word3 [**section 3.3.1.4,** page 74] and Word10 [**section 3.3.1.11,** page 75] in the external RAM (POLURAM) and are calculated as:

$$\text{Delta} = T/T_z = xCR_Z/xCR$$
$$W_{min} = \tau/T_z$$

T_z is the peak emission interval for the cell processing of the ATM-LP. For a SYSCLK with 51.84MHz and 32 cycles for one cell, the peak emission interval T_z for one cell is 617.28ns. The corresponding xCR is 1,620,000 cells per second. Delta is the cell emission interval normalized to the cell processing period. It has 2^{32} values and a granularity of 2^{-11}. As a result a granularity of 2^{-10} cells/s of the PCR or SCR can be adjusted.

W_{min} is the ratio between the CDV parameter τ and the emission interval for one cell T_z. τ can also be derived from the signalling parameters MBS, T_{SCR} and T_{PCR} as:

$$\tau_{IBT} = [(MBS - 1)(T_{SCR} - T_{PCR})] \text{seconds}$$

2.4.4 Example for POLU configuration

This example is according to to the specification for Unstructured Circuit Emulation Service of the ATM Forum and ITU. This service e.g. handles CBR traffic using AAL1 with 47 bytes per cell at a data rate of 2.048Mbit/s for E1, which results in a peak cell rate of 5446.8cell/s (= PCR_{sig}). According to I.371 the m and k parameters are calculated according:

$$m_{PCR} = \left\lceil \log_2\left(\frac{PCR_{sig}}{1023}\right) + 9 \right\rceil$$

$$k_{PCR} = \left\lceil \frac{PCR_{sig}}{2^{m_{PCR}-9}} - 512 \right\rceil$$

The value of both parameters has to be round up. As a result m_{PCR}=12 and k_{PCR}=169. With the formula given in **section 2.4.3** the parameters are: k'_{PCR}=508 (rounding down), T_{PCR} = 183.463µs and Λ_{PCR} =5448cells/s. Be aware that the inverse value of T_{PCR} (which is 5450.68cells/s) is higher than the value of Λ_{PCR}.

The POLU parameter Delta (T_{PCR}/T_Z) is 297.21006. The cell cycle time T_z is 617.28ns.

The value of the LSB of Delta is 2^{-11}. Herewith Delta is encoded as $949AE_H$ (= Delta*2^{11}, round down). The POLU parameter W_{min} (τ_{PCR}/T_z) is 1215 if the CDVT is 750µs at the UNI. The encoding of the W_{min} is $25F800_H$ (= W_{min}*2^{11}). The Configuration and parameter values for POLU are as follow:

Table 5 Example for Configuration

Service & Parameters for E1 Circuit Emulation with 750µs CDVT at the UNI		**POLU Configuration Parameters**			
DBR	$PCR_{(0+1)}$ $\tau_{PCR(0+1)}$	MODE = 3	$Delta_1$ = $949AE_H$ W_{min1} = $25F800_H$	$Delta_2$ = 0 W_{min2} = 0	$Delta_3$ = 0 W_{min3} = 0
		USER_U/D = 10 F4RM_U/D = 00 F5RM_U/D = 00 F4SEG_U/D = 00 F4E2E_U/D = 00 F5SEG_U/D = 00 F5E2E_U/D = 00 DIS_U/D = 01			

The user cells are policed in the upper branch at LB1. Discarding is enabled. The LB2 is disabled. The OAM and RM cell types are not policed (transparent bypass). The LB3 can be optionally used for a separate OAM policing. $Delta_3$ and W_{min3} is derived from the $PCR_{(OAM)}$ and $\tau_{PCR(OAM)}$ values as shown above. The FxSEG_U/D and/or FxE2E_U/D has to be set to 01 and the DIS_U/D to 00.

2.5 Traffic Measurement Unit for up- and downstream direction

The ATM-LP provides several traffic counters which can be used for accounting management (i.e. billing), for observation of the ATM cell traffic behavior as well as for protocol monitoring measurement. Traffic measurement is implemented at VCC, VPC and port level and fulfills the Bellcore requirements GR-1248-core. The ATM-LP supports a minimum measurement interval of at least 44 minutes.

The connection specific data as well as the traffic measurement data of the VCCs, transparent and terminated VPCs are stored in the external CONNRAMUP and CONNRAMDO RAMs. The port specific traffic measurement data are stored in the internal Port table of the ATM-LP. After the address reduction the connection specific data and traffic measurement counter values are read from the external connection RAM which is addressed via the LCI value of the cell. For the upstream direction 8 dwords and for the downstream direction 7 dwords are read. The data structure is depicted in **figure 22**.

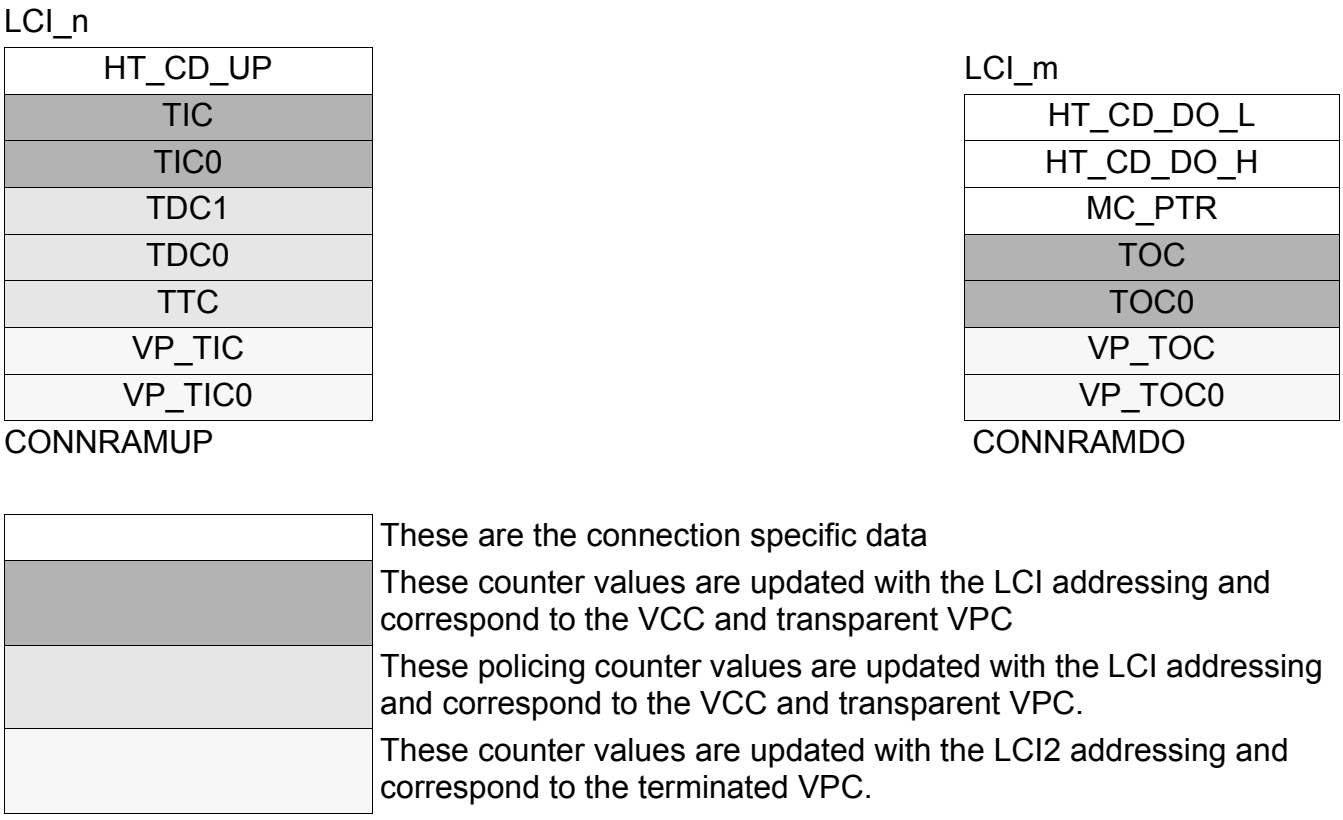


Figure 22 Data Structure in the External CONNRAMUP and CONNRAMDO RAM for each LCI Value

Subsequently both the Traffic Measurement (TIC, TIC0 in upstream and TOC, TOC0 in downstream) and Policing (TDC0, TDC1 and TTC) counter values are updated with respect to the identified cell type for VCC and transparent VPC. Additionally the ATM-LP reads from a second LCI2 address the Traffic Measurement (VP_TIC, VP_TIC0 in upstream and VP_TOC, VP_TOC0 in downstream) counter values for the terminated VPCs. The LCI2 is stored in the connection specific data addressed by the LCI. The value of the LCI2 is identical for all VCCs which are transported in a common terminated VPC. After counter update all counter values are stored back in the external CONNRAMUP and CONNRAMDO. For transparent VPCs it is possible to set LCI2 to the value of LCI. Herewith the counter values TI/OCs and VP_TI/OC are

identical and the memory usage is reduced. The cell types and the corresponding name of counters are given in **table 6** for the VCC level and in **table 6** for the VPC level.

Table 6 Traffic Measurement at VCC Level

Cell Type	Counter and RAM
Total incoming cells	TIC in CONNRAMUP
Total outgoing cells	TOC in CONNRAMDO
Total incoming cells with CLP=0	TIC0 in CONNRAMUP
Total outgoing cells with CLP=0	TOC0 in CONNRAMDO
Total discarded incoming cells due to UPC/ NPC with CLP=1	TDC1 in CONNRAMUP
Total discarded incoming cells due to UPC/ NPC with CLP=0	TDC0 in CONNRAMUP
Total tagged incoming cells due to UPC/NPC	TTC in CONNRAMUP

Table 7 Traffic Measurement at VPC Level

Cell Type	Counter and RAM
Total incoming cells	VP_TIC in CONNRAMUP
Total outgoing cells	VP_TOC in CONNRAMDO
Total incoming cells with CLP=0	VP_TIC0 in CONNRAMUP
Total outgoing cells with CLP=0	VP_TOC0 in CONNRAMDO

Two kind of traffic measurement counters are implemented for the port level. The first group of counters is fixedly allocated to the UTOPIA ports 0..15 and counts the total number of incoming cells in upstream direction (POTIC, see **section 3.3.4.1,** page 81) and the total number of outgoing cells in downstream direction (POTOC, see **section 3.3.4.2,** page 84). The fixed counters can be enabled or disabled via register ENDPOTC (see **section 3.14.2,** page 105) for upstream direction and register ENPOTOC (see **section 3.15.2,** page 107) for downstream direction. The second group consists of eight countersets for each direction, which can be flexibly allocated to the ports 0..23. In upstream direction the countersets contain four counters, named POTI_Ci, PDC_Ci, POTICN_Ci and POTICOR_Ci. POTIC_Ci counts the total number of incoming cells at port i. PDC_Ci summarizes the total number of discarded cells due to unallocated PN/VPI/VCI at port i. The total number of incoming cells with a non-zero GFC field at port i is counted by POTICN_Ci. And POTICOR_Ci shows the number of total incoming OAM/ RM cells at port i. These counters are stored in the traffic measurement RAM, which is also called port table. The structure of the port table is shown in **section 3.3.4.1,** page 81. The PN allocation to the counterset and their configuration is controlled by registers PORTCONFn_U (**section 3.14.1,** page 104) for upstream direction. In downstream direction, the countersets include two counters, which are POTOC_Ci and POTOCOR_Ci. Using POTOC_Ci the total number of outgoing cells at port i is available and POTOCOR_Ci counts the total number of outgoing OAM/RM cells at port i. The PN allocation in downstream direction and the configuration of the countersets is done via registers PORTCONFn_D (**section 3.15.1,** page 106). It is selectable for each counterset, which counter should be enabled or disabled. If two or more countersets are allocated to one port, only the counterset with the lowest number is active. This case is given after reset, because at this event all eight countersets are assigned to port

number 0. The cell types and the corresponding name of counters are given in **table 6** for the Port level. An overview of the traffic measurement capability is depicted in **figure 23**.

Table 8 Traffic Measurement Counters at Port Level

Cell Type n [0..7] for each counterset	Counter of the Port table
Total incoming cells due to unallocated PN/VPI/VCI at port number defined in CNT_PORTn_U	PDC_Cn
Total incoming cells with non-zero GFC-field at port number defined in CNT_PORTn_U	POTICN_Cn
Total incoming cells at port number defined in CNT_PORTn_U	POTIC_Cn
Total incoming OAM or RM cells enabled per connection at port number defined in CNT_PORTn_U	POTICOR_Cn
Total outgoing cells at port number defined in CNT_PORTn_U	POTOC_Cn
Total outgoing OAM, RM or discarded F5RM cells enabled per connection at port number defined in CNT_PORTn_U	POTOCOR_Cn

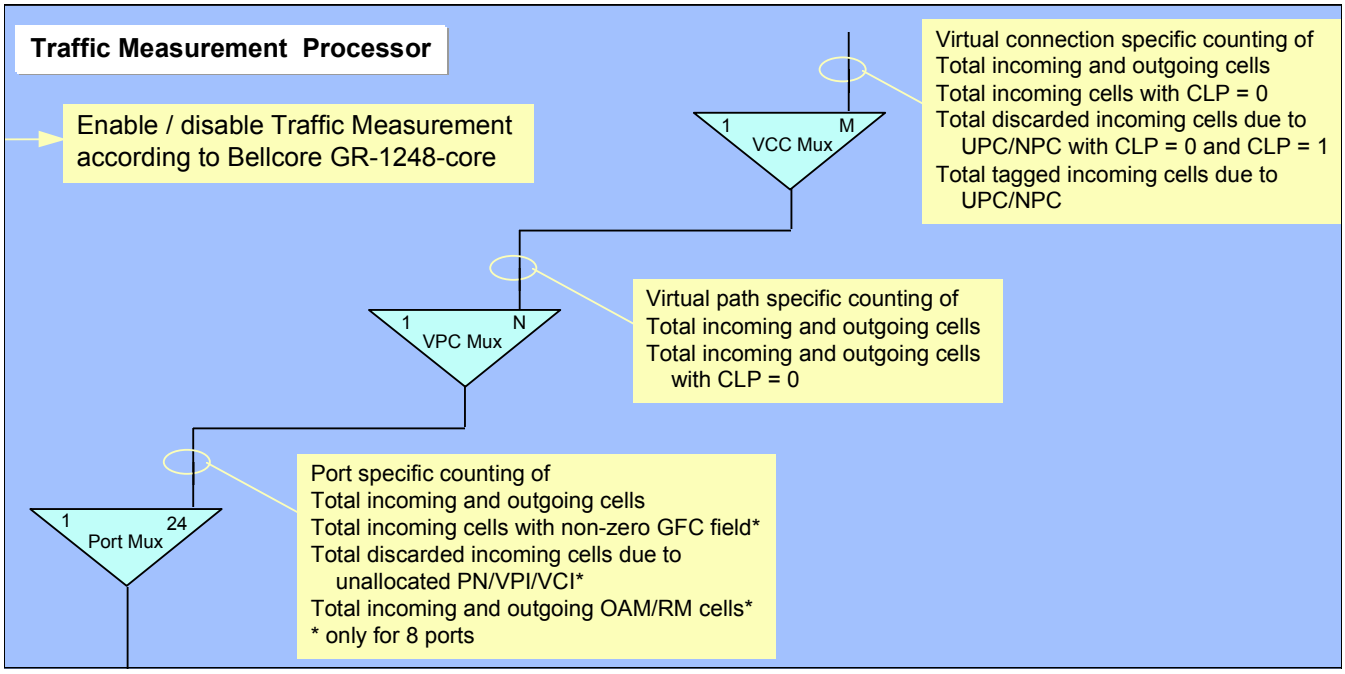


Figure 23 Traffic Measurement at the Port, VPC and VCC Level

The Traffic Measurement can be activated by a SW flag EN_TRAF_MEAS_UP/DO in the external CONNRAMUP/DO for each connection at the VCC and VPC level.

At the port level it is configurable with the SW flag OAM_CNT_U (**section 3.14.1,** page 104) in the ATM-LP register whether the TM counter POTICOR counts the OAM or RM cells in upstream direction. Furthermore the SW flag INC_TIMC_SSD (**section 3.3.2.1,** page 77) in the CONNRAMUP define per connection whether this specific connection is counted. For the downstream direction the SW flag OAM_CNT_D (**section 3.15.1,** page 106) in the ATM-LP register selects whether the TM counter POTOCOR_Ci counts the OAM, RM or both discarded F5RM and PTI (111) cells. The SW flags INC_TOMC_SSD and INC_TOF5RMC_SSD (**section 3.3.3.1,** page 79) in the CONNRAMDO define per connection whether this specific connection

is counted in the POTOC_Ci and POTOCOR_Ci. Herewith it is possible that one, some or all connections running on this port are counted.

2.5.1 Traffic Measurement data transfer via DMA

The ATM-LP supports a DMA mechanism for fast data transfer of the connection specific counters at VCC and VPC level from CONNRAMUP and CONNRAMDO to the microprocessor RAM. The ATM-LP internal condition for a DMA access is the occurence of an empty cycle that means no cell is available at the UTOPIA receive interface. This has to be considered for system design (amount of user cells, UTOPIA frequency, core frequency of ATM-LP). In downstream direction it is possible to force empty cycles by setting bit FORCE_EC_D in register CONUT3 to generate backpressure to the preceding ASIC that stores the cells in its buffer queues (see **section 3.16.5,** page 110).

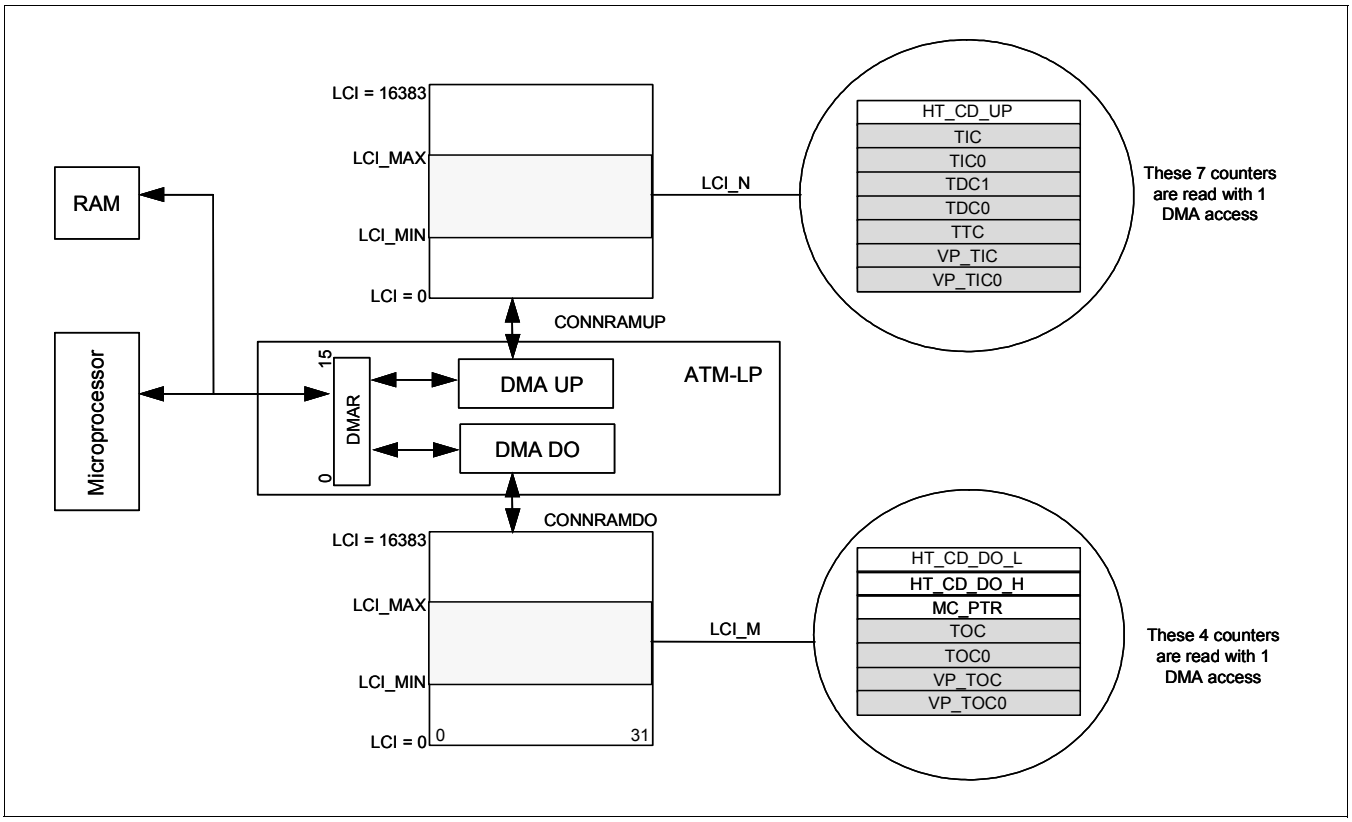


Figure 24 DMA for Fast Traffic Measurement Data Transfer

In upstream direction it has to be considered in the system design (UTOPIA frequency, ATM-LP frequency and ATM user cell rate) that there is a trade off between switch port usage and microprocessor access time to CONNRAMUP and CONNRAMDO. For PHY devices up to STM-4 equivalent there is no restriction for the ATM-LP as each 10th cell will be an empty cell. For the ATM-LP this means no cell at the UTOPIA interface. Due to the fact that idle cells can also be transmitted in the STM-4 signal but not via the UTOPIA interface the number of empty cells will be higher. The empty cell will be used for configuration and DMA access. Problems will occur only if the UTOPIA Interface is overbooken. The relationship between link rate, switch port rate and user cell rate is shown in **figure 25**.

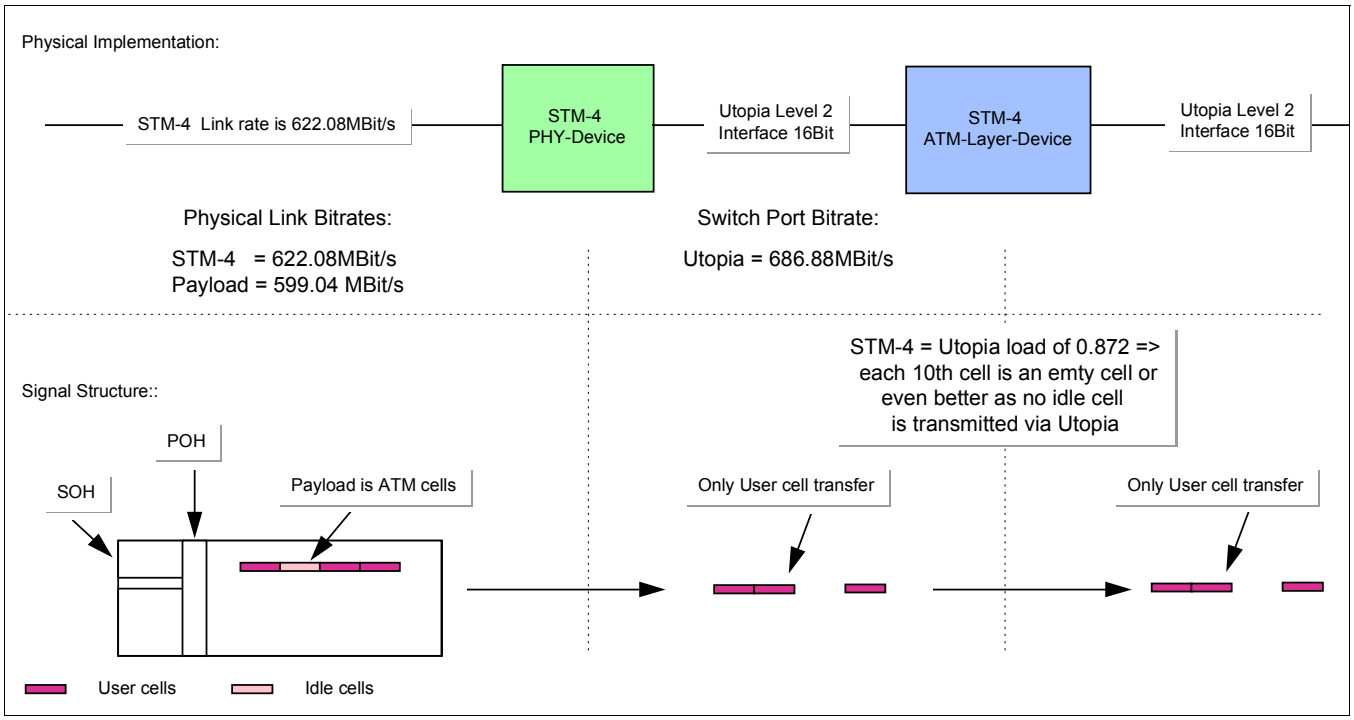


Figure 25 Relationship between Link Rate, Switch Port Rate and ATM User Cell Rate

The DMA is controlled by three registers called DMA_MIN (**section 3.32.1,** page 138), DMA_MAX (**section 3.32.2,** page 138) and DCONR (**section 3.28.1,** page 132) . DMAMIN and DMAMAX determine the range of LCIs which counters are read to the microprocessor RAM via DMA. The DMA is performed LCI-wise with one DMA access transferring all counters of one LCI. The order of the DMA accesses is from LCI_MIN to LCI_MAX. Using bit DMA_UD in register DCONR the direction (up- or downstream) can be selected. By setting bit DMA_START in the same register the mircoprocessor can start the DMA. This bit is reset by the ATM-LP when the DMA process has finished, therefore the microprocessor has to poll this bit until it is reset. After the DMA access is done the microprocessor can get the counter values by reading the DMAR register (**section 3.28.2,** page 134). After the bit DMA_START of the DCONR register is set, the write access to DMAMIN, DMAMAX and DCONR except the DMA_START bit is blocked. This guarantees that the configuration of DMA cannot be changed during the complete DMA cycle. The microprocessor can stop the DMA by clearing DMA_START. As a result the DMA is finished and the DMA processor of the ATM-LP is reset. The DMA for a single LCI_n occures during an empty cell cycle. The transfer between ATM-LP and microprocessor is controlled by the HW pins MPDREQ and MPDACK. MPDREQ is active after all connection specific traffic measurement counters are written into the DMA buffer of the ATM-LP and becomes inactive after the contents of the DMA buffer are read out by the microprocessor via the DMAR register. The next DMA cycle for LCI_n+1 is initiated either by the MPDACK signal from the microprocessor or by the ATM-LP. The delay time between two consecutive DMA depends on the occurrence of the next suitable empty cell cycle. This can lead to a large load on the microprocessor bus if enough empty cycles are available so that the processes with lower priority than the DMA are blocked. Therefore the minimum delay between two DMA accesses can be configured by the DMA_WAIT bit in register TESTR (**section 3.29,** page 135) and by the DMA_DELAY variable in the DCONR register. Using the reset bits CTRn_RES in the CONR register the microprocessor can reset each counter value separately for the specified LCIs.

When the values are read to the DMA buffer, the counters are reset. A guide line for DMA is given in chapter 4.

2.6 UTOPIA Functionality

The ATM-LP provides an UTOPIA Level 2 interface with multiplexed status polling according to [2] at the PHY and the ATM side. At the PHY side the receive and transmit UTOPIA Interface has master capability. At the ATM side the hardware pins RXMS and TXMS select for the receive and transmit direction of the UTOPIA interface whether it acts as an UTOPIA master or slave (see **figure 26**).

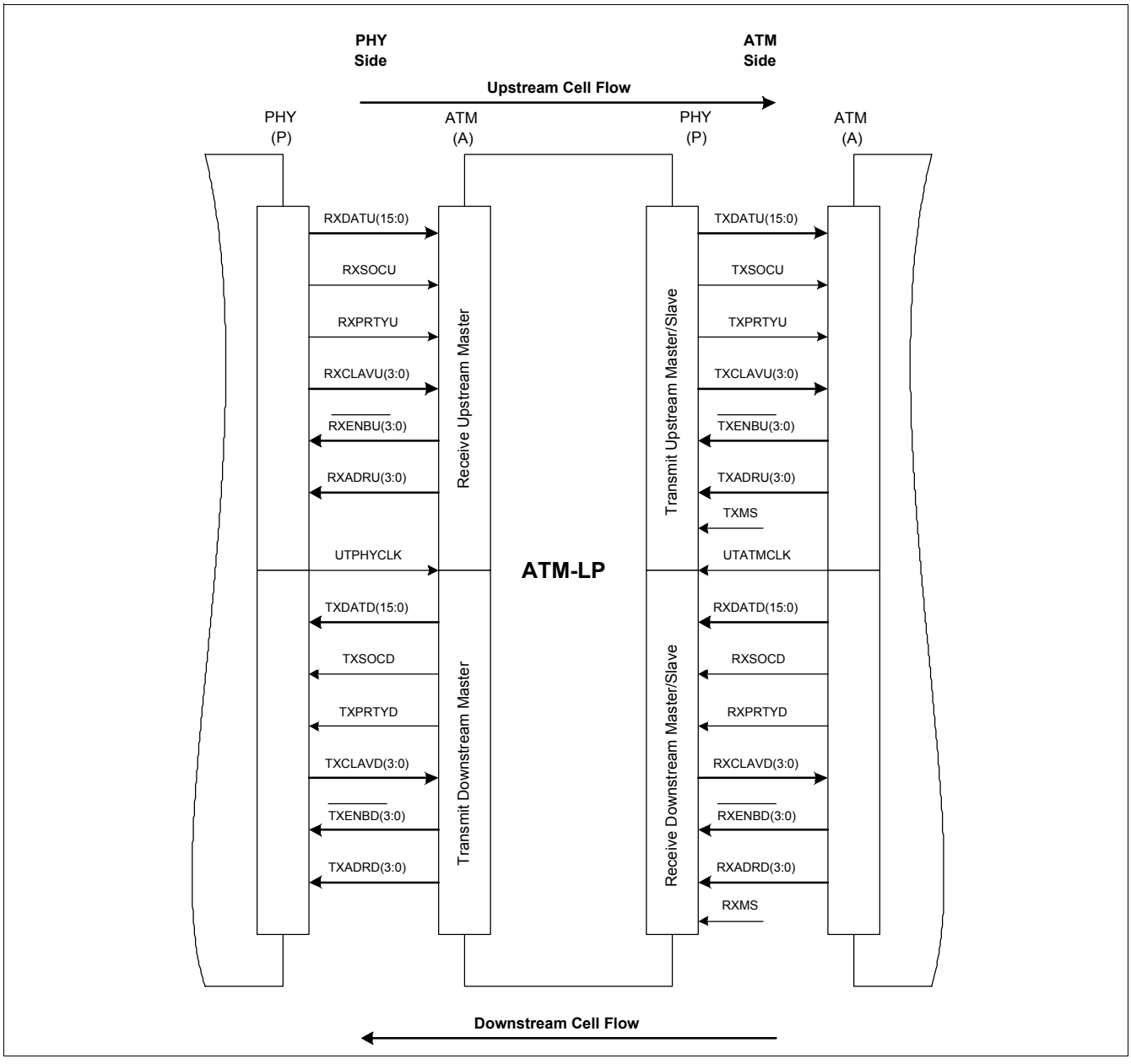


Figure 26 UTOPIA Interface

The multiplexed status polling of the ATM-LP supports up to 4 independent Clav/Enable line pairs. This has the advantage that all PHYs can be polled during one cell cycle. Additionally 4 UTOPIA Level 1 devices with a tristate Rx-Data bus can be supported by the ATM-LP. During one cell cycle up to 12 UTOPIA Addresses are scanned which gives a maximum capacitance of 48 ports with the 4 Clav/Enable line pairs. The ATM-LP supports 24 ports. An example for the ATM-LP configuration with 4 PHY-devices connected with the 4 Clav/Enable line pairs is given

in **figure 27**. In this example 24 lines, each with a data transfer rate of 25.6 MBit/s result in a total throughput of 614.4 MBit/s, are supported by the ATM-LP.

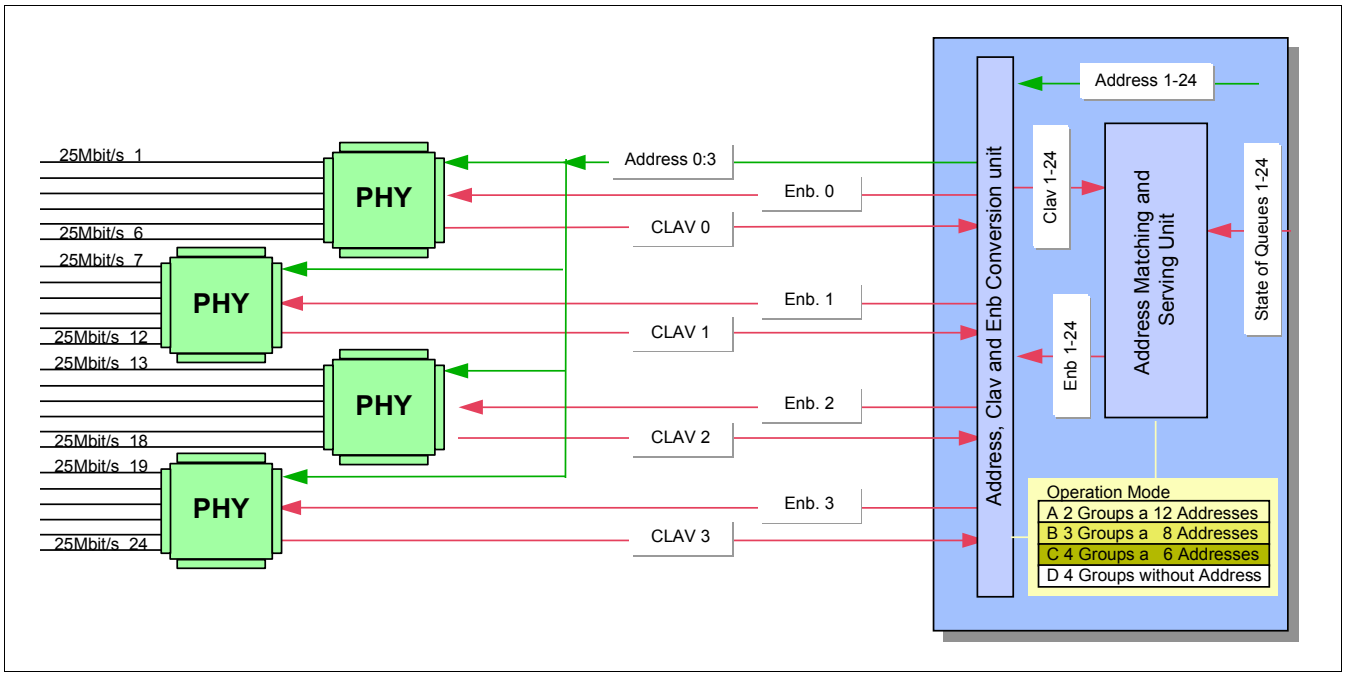


Figure 27 UTOPIA Interface Configuration for 4*6 PHYs at the PHY Side

For both PHY and ATM sides the parity protection and the data bus width of 8 or 16 bit is selectable via the configuration bits UTP_PAR, UTA_PAR, UTP_16BIT and UTA_16BIT in the CONUT2 register (see **page 108**). The ATM-LP supports cell level handshake without paused transfer. The frequencies of the UTOPIA clocks UTPHYCLK and UTATMCLK at the PHY and ATM side are independent from each other and should be lower than or equal to the SYSCLK of the ATM-LP. The bidirectional data throughput of the UTOPIA interface is up to 686.88MBit/s for a 16 bit data bus and an UTOPIA clock of 51.84MHz. According to [2] the UTOPIA interface supports a minimum of up to 8 PHY-devices for an STM-1 throughput and up to 4 PHY-devices for an STM-4 throughput at the PHY and the ATM side.

For up- and downstream each of the 24 ports can be enabled via SW configuration bits UT_PORT_U and UT_PORT_D in registers CONUT1A-C (see **page 108**). In upstream direction the cells in the UTOPIA transmit interface buffer are discarded in the ATM-LP and the cells at the UTOPIA receive interface are not accepted by the ATM-LP if the port is disabled during the operation. In downstream direction the acceptance and transmission of cells is locked but the cells in the port specific queue are not discarded. As the cells remain in the port specific queue of the ATM-LP the port disabling should be done at the switch element which locks the acceptance but transmit the rest of cells in the port specific queue.

The ATM-LP converts the 24 ports into an UTOPIA Address and 4 Clav/Enable line pairs. Four Address Group configurations are selectable for the PHY and ATM side via the SW configuration bits UTP_CONFIG and UTA_CONFIG in the register CONUT2. The possible configurations are shown in **figure 28**.

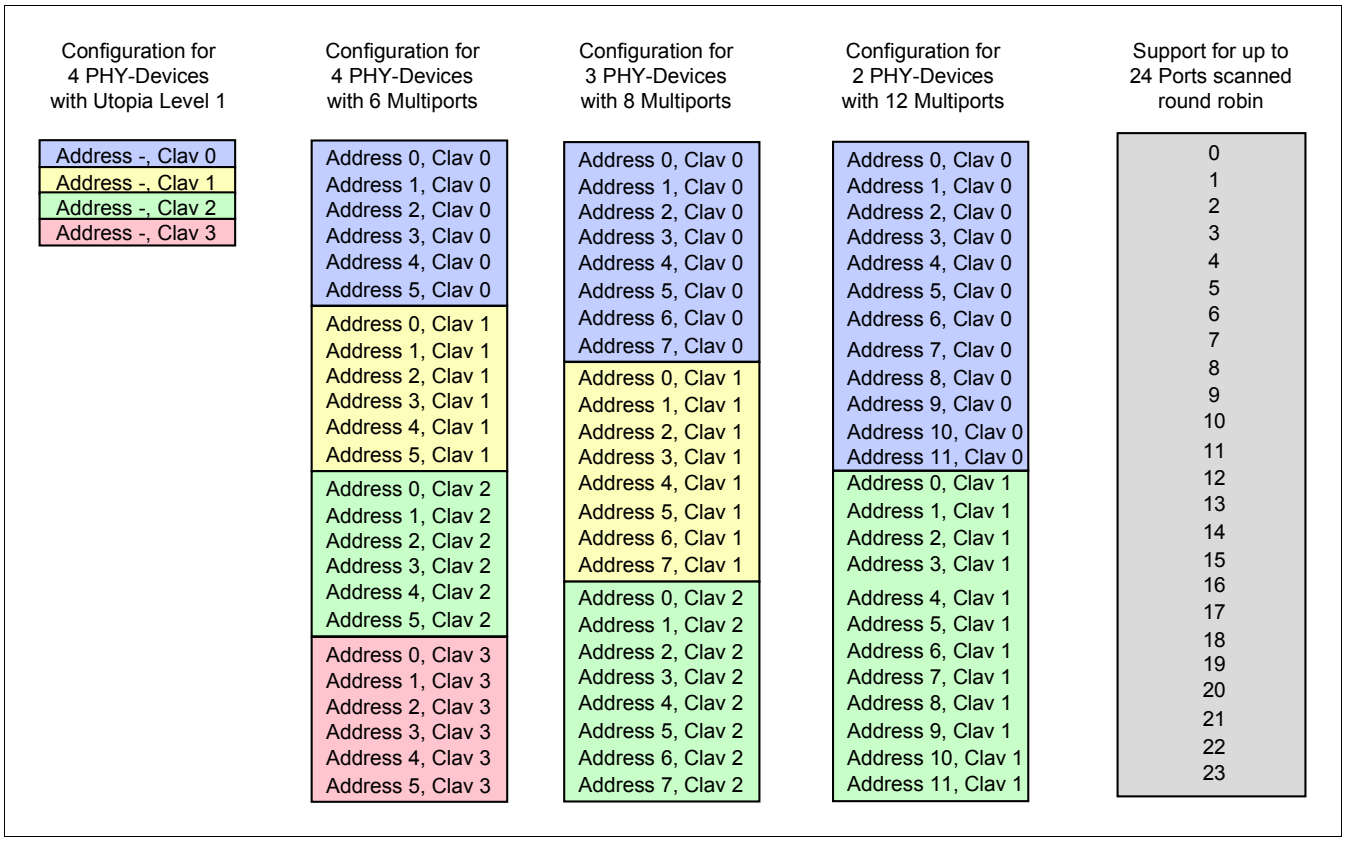


Figure 28 Possible Address Group Configurations

Herewith the ATM-LP supports:

- 4 PHY devices without UTOPIA Address (UTOPIA level 1) or with up to 6 Port Addresses
- 3 PHY devices with up to 8 Port Addresses
- 2 PHY devices with up to 12 Port Addresses

The poll cycle is identical in all modes, i.e. the address lines output all addresses from 0 to 11 in ascending order during one cell cycle. For each address output at the address lines all PHYs are polled. The polling order is shown in **table 9**. If the address is greater than the number of Multiports at the device, the associated CLAVx is set to 0. The real Multiport number depends on the selected mode. The polling sequence of the next polling cycle depends on the current transmitting PHY, e.g. if port 5 is the current transmitter the next polling sequence starts in 4x6 mode with port 11.

Table 9 Polling Order of Port Numbers

Mode	Polling Order of Port numbers																							
4x6	0	6	12	18	1	7	13	19	2	8	14	20	3	9	15	21	4	10	16	22	5	11	17	23
3x8	0	8	16	1	9	17	2	10	18	3	11	19	4	12	20	5	13	21	6	14	22	7	15	23
2x12	0	12	1	13	2	14	3	15	4	16	5	17	6	18	7	19	8	20	9	21	10	22	11	23
1x4	0	1	2	3	4																			

Depending on the selected mode different Clav/Enable lines and addresses are associated to a special port. As an example for port number 9, the following table shows that 3 different addresses and Clav/Enable lines are activated for 4 different address group configurations. The

configuration of 4 UTOPIA level 1 interfaces is not possible as the port number 9 is not in the port address range 0 to 3.:

Table 10 Example for Port Number 9

Configuration of the UTOPIA Interface	4*6	3*8	2*12	4*1
UTOPIA Address	3	1	9	-
Clav/Enable line	1	1	0	-

Figure 29 depicts the address group configuration at the PHY and ATM side of two ATM-LPs connected to one AOP. This is a possible scenario for Access Network System architecture. As it can be seen it is not necessary that the Address Group Configuration is identical at the PHY and the ATM side of the ATM-LP, AOP or ABM. However it is required that the port number range from 0 to 23 is shared by the number of ATM-LPs and each port number is used only once. The SW is responsible that the used port number range is covered by the Address group configuration.

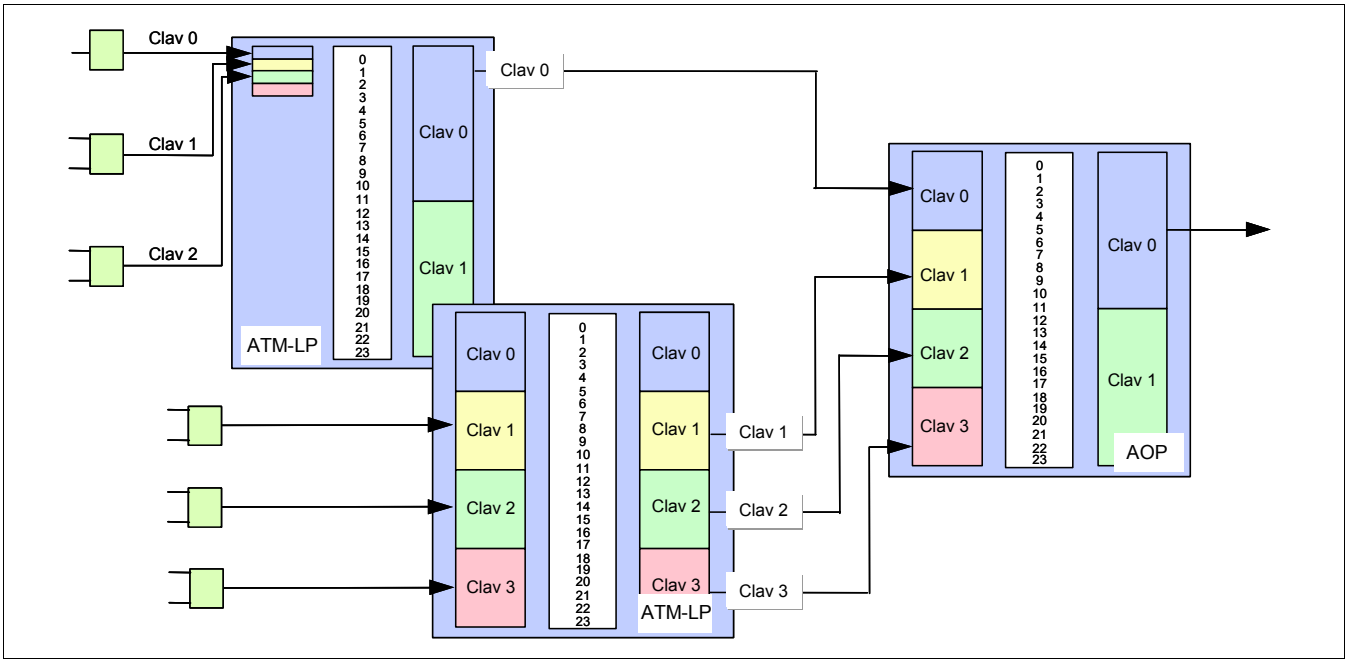


Figure 29 Example of an Address Group Configuration

The ATM-LP has a shared memory buffer of 64 cells for the downstream direction. Up to 24 queues share the memory buffer. The queue number range of 0 to 23 corresponds to the port number range. The addressing of the ports or queues occurs via the UTOPIA address and the Clav/Enable pairs which are converted into the port number depending on the address group configuration. One threshold which is identical for all queues can be adjusted via the SW configuration bits UT_THRESH in register CONUT3. Herewith a port specific backpressure signal can be given to the UTOPIA receive interface in downstream direction if the filling level of the queue is greater than or equal to the queue threshold. The error indication which is related to the UTOPIA interface is given in register ISR0. An interrupt indication BOV is generated if the 63rd cell is stored in the shared buffer and an interrupt indication QOV is generated if one or more queues have an overflow status. A detailed queue overflow indication is provided in the register UT_QO1/2 (see **page 111**) by the indication bits QOV_i. Parity errors at the PHY side of the receive and transmit UTOPIA interface generate an interrupt UT_PARERR_U/D. The

occurrence of a start of cell error or cell length error at the receive UTOPIA interface in up- and downstream direction generates an interrupt UT_CELLERR_U/D. An overflow at the UTOPIA receive FIFO in upstream direction is detected via the interrupt flag UTRXFIFO_OV_U.

For diagnosis the ATM-LP has 4 protocol monitoring register sets PRMONR0..3x_U for upstream direction and one protocol monitoring register set PRMONRx_D for downstream direction to buffer the last discarded cell due to ATM cell header error. An ATM cell header error occurs if either an error in the external address reduction circuit CAME is indicated or if a parity error appears at the CONNRAMDO interface. For both cases an interrupt CAM_ERR and RAM_PARERR_D indication is given in register ISR1. Each register set can be enabled by SW flags EN0_U, EN1_U, EN2_U, EN3_U and EN_D in the register HEADCAPEN (see **page 103**). The 4 registers for upstream direction are related to the 4 CLAV Groups. In downstream direction only one register set is related to all CLAV groups. An indication is given by the interrupt bit PMO_HLOG in register ISR0 if one or more cells are stored in the PRMONR registers. A detailed status indication for each PRMONR register is given by the SW flags PMO_HLOH0_U, PMO_HLOH1_U, PMO_HLOH2_U, PMO_HLOH3_U and PMO_HLOH_D in register STATR (see **page 115**). The indication bit is reset after the complete read out of the cell header by the microprocessor.

2.7 OAM Functionality

The ATM-LP supports together with the external microprocessor an OAM light function for low cost applications where no AOP is used. The OAM light function covers the AIS, RDI, CC, CCA and LB handling for F4 and F5 flow according ITU [7] and Bellcore [8]. Not supported are the OAM functions for Connections Quality Measurement (PM). The OAM light function can be disabled by the SW flag OAM_EN in the register DCT/UCT_CONFIG (see page 125) for up- and downstream direction if the AOP is used. In this mode all OAM cells are forwarded to the AOP without CRC-10 checking. In the OAM light mode the type of the connection point and the consequent OAM cell processing can be defined and the CRC-10 checking and generation is performed for the extracted and inserted OAM cells. For the F4 and F5 OAM flow the connection point can be configurated via SW Bits F4/F5PT_CFG in the CONNRAMUP/DO RAM as intermediate point IP, originating segment point OSP, originating end-to-end point OEP, terminating segment point TSP and terminating end-to-end point TEP for each connection. Additionally a connection point can be also defined as not existing. The following **Figure 30** depicts the different types of connection points and the corresponding possible segment and end-to-end flows for F4 and F5 OAM flow.

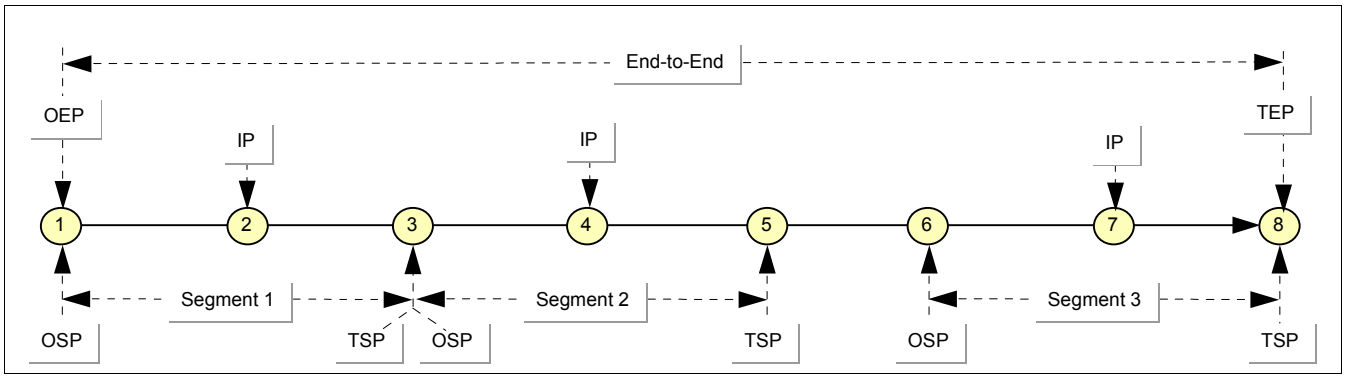


Figure 30 Types of Connection Points for F4 and F5 OAM Flow

The consequent actions for the OAM cells at the connection points can be configurated via SW. At the termination points it is configurable for each defined and undefined OAM cell type whether it is discarded or dropped. The corresponding SW flags AR/CC/LB_DISC in the ATM-LP register DCT/UCT_CONFIG has an influence on all connections.

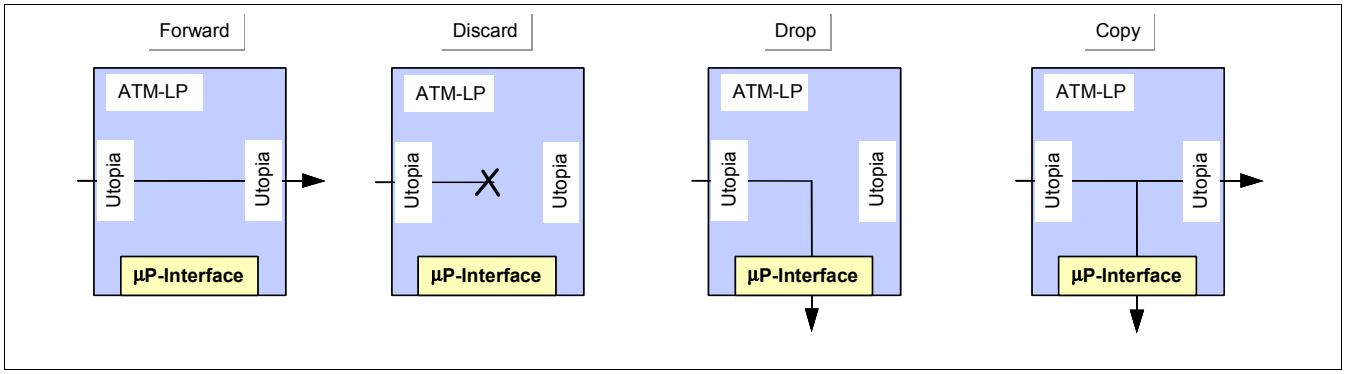


Figure 31 Consequent Actions on OAM Cells

At the intermediate points it is configurable whether the AIS, RDI, CC and CCA cells are copied or forwarded and whether the LB cells are dropped or forwarded. The corresponding SW flags AR/CC_IP_COPY and LB_IP_DROP in the CONNRAMUP/DO are connection specific.

For each connection point only one F4 and one F5 connection point can be defined by the F4PT_CFG and F5PT_CFG Bits. This has an influence to the ATM-LP configuration if two adjacent segment boarders are located at the same Network Node. This case is illustrated in the following **Figure 32** and **33** where in network Node 3 a segment is terminated and the next is originated. For a transparent and terminated VP the termination point VP-TSP/EP is configured at the ingress and the originating point VP-OSP/EP is configured at the engress side of the Node. A configuration of a termination and origination for the same F4 or F5 flow at one node side is not possible. **Figure 32** shows a Network Node with a Switching fabric and several ATM-LPs at the ingress and engress side of the Network node. **Figure 33** shows a low cost Network Node with a single ATM-LP and no additional Switching fabric which is used as an ATM-Multiplexors for up to 622MBit/s Throughput in Access Networks.

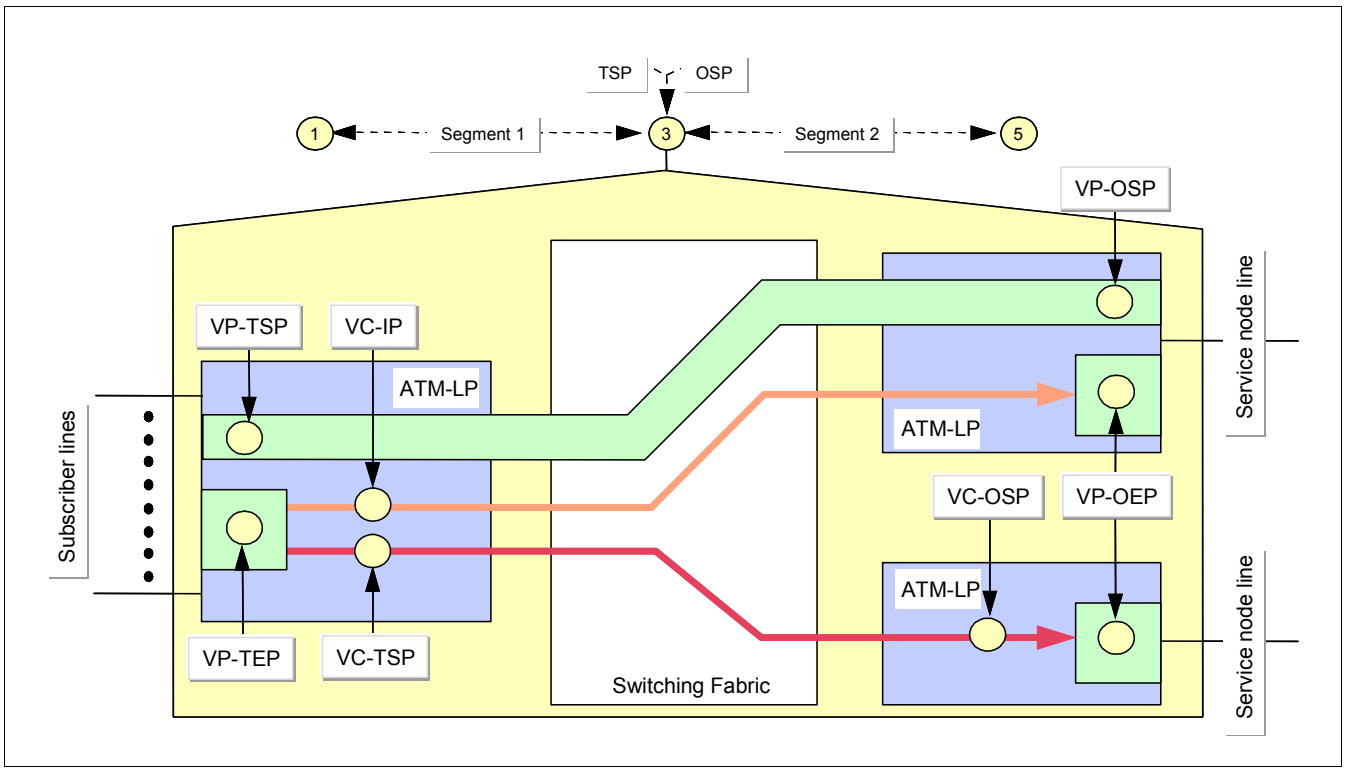


Figure 32 Configuration of the Connection Points for Nodes with Switching Fabric

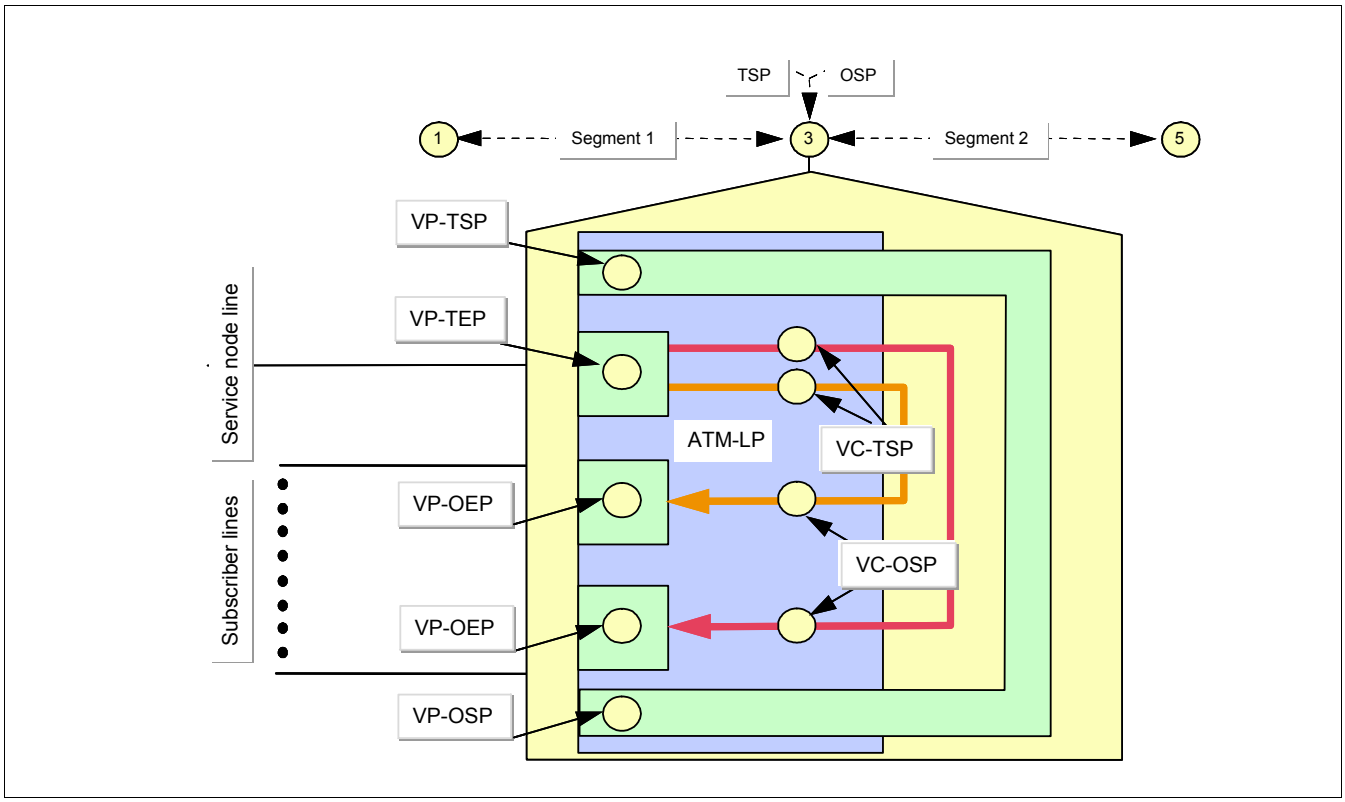


Figure 33 Configuration of the Connection Points for Nodes without Switching Fabric

The normal OAM processing of the ATM-LP is the insertion of OAM cells via the insertion buffer by the microprocessor at the OEP and OSP. At the IP the OAM cell is forwarded without any processing and is automatically dropped via the extraction buffer to the microprocessor at the TEP and TSP. With the connection specific flags AR_IP_COPY and CC_IP_COPY the AIS, RDI, CC and CCA cells are copied to the microprocessor for monitoring purpose at the IP. The OAM flow is depicted in **Figure 34**. With the connection specific flags LB_IP_DROP the LB cells are dropped to the microprocessor. After the LB processing the LB cell is reinserted. The dropping is necessary as the microprocessor has to check the LB-Identification number which is located at the payload of the LB cell.

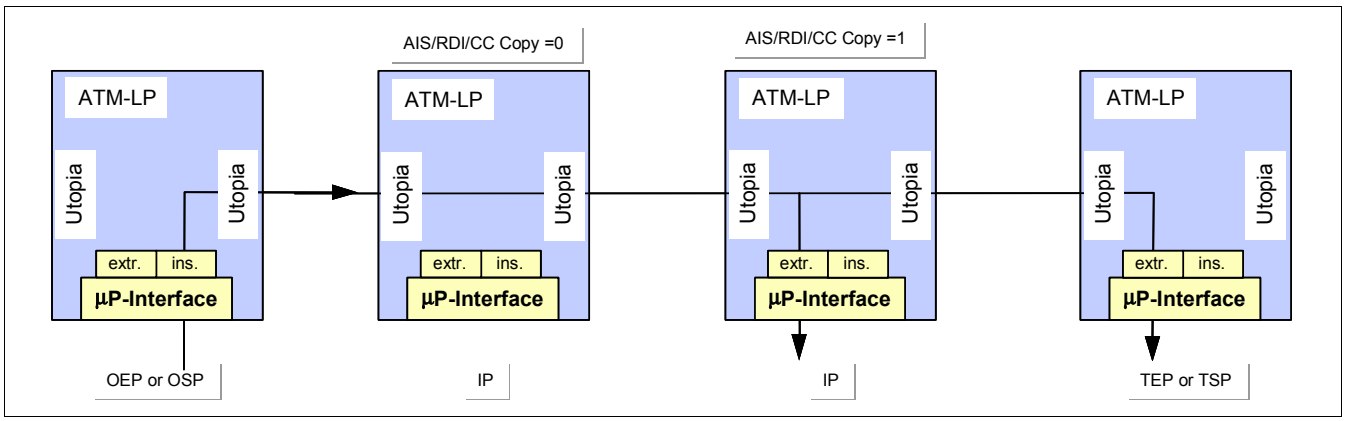


Figure 34 Processing for AIS, RDI, CC and CCA OAM Cells

The **Figure 35** depicts the OAM flow processing for LB cells. With the cell type specific flags AR_DISC, CC_DISC, LB_DISC and UNDEF_DISC in the register DCT/UCT_CONFIG the AIS, RDI, CC, CCA, LB and undefined OAM cells can be discarded at the TEP and TSP in order to minimize the processor load in failure case.

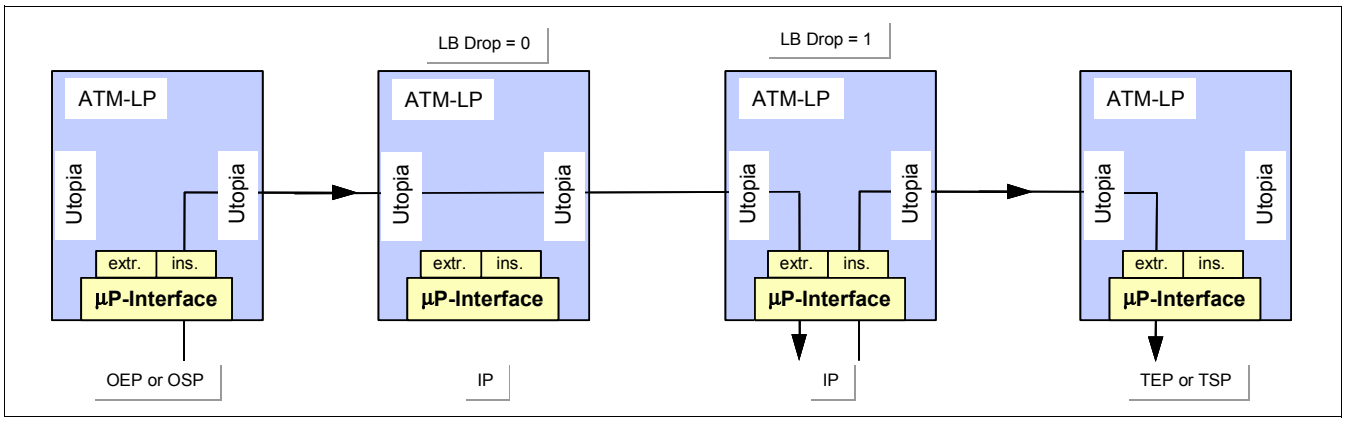


Figure 35 Processing for LB OAM Cells

A check of error detection code (CRC-10) is performed by the UTOPIA receive interface in up- and downstream direction for every OAM cell and an EDC error is indicated by the EDC_ERR_U/D bits in the ISR1 register. The false OAM cells are discarded or forwarded according to the configuration by the CRC_NODISC bit in the DCT/UCT_CONFIG register. The OAM cells and the information on the identified cell type is extracted via the receive cell buffer register RXR (see page 99) to the microprocessor. The OAM cell has a 56Byte format which includes the cell type information in word 27 Bit(15:10) as depicted in **Figure 36**. The receive cell buffer stores up to 12 cells and an indication bit RXR_USTR in ISR1 register is set until all cells are read out by the microprocessor and is afterwards reset automatically by the ATM-LP.

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Header_1								Header_2							
1	Header_3								Header_4							
2	UDF1								UDF2							
3	Payload_1								Payload_2							
4	Payload_3								Payload_4							
:	:								:							
26	Payload_47								Payload_48							
27	Celltype(5:0)						unused									
word																

Figure 36 Cell Format extracted from ATM-LP to Microprocessor

The insertion of OAM cells is performed via the Transmit cell registers 0 to 26 (see page 96) by the microprocessor. The cell format is 56 Bytes as in receive direction however the cell type field in word 28 is not used. An E Bit in UDF2 (5) controls the generation of the CRC-10 for outgoing OAM cells at the UTOPIA transmit interface. For inserted Non-OAM cells the CRC-10 generation can be disabled. For OAM/RM cells passing the ATM-LP no further CRC-10 is generated. The cell structure is depicted in **Figure 37** for the ATM-LP upstream direction without Header translation. The other scenario are described in the TXR2 register description (see page 97). The insertion of the cell from the transmit cell buffer into the cell stream is initiated

by the START_TR bit in TXR_CONFIG register (see page 99).

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	Header_1								Header_2							
1	Header_3								Header_4							
2	LCI		HK			unused					E	PNUT				
3	Payload_1								Payload_2							
4	Payload_3								Payload_4							
:	:								:							
26	Payload_47								Payload_48							
27	unused								unused							
word																

Figure 37 Cell Format inserted from Microprocessor into the ATM-LP Upstream Direction without Header Translation

The following table gives an overview of the consequent actions on the OAM and RM cells in dependence on the configuration of the connection points at the F4 and F5 flow. If no connection point is defined (F4-no and F5-no) no useful action is guaranteed. In this case the F4 configuration has a higher priority than the F5 configuration.

Table 11 Recommended F4 and F5 Configuration and Consequent Action on OAM and RM cells

Connection Point		Consequent Actions	
F4	F5	OAM	RM, F5RES
F4-no	F5-no	no action	no action
F4-no	F5-OEP	dis-F4 & dis-F5	no action
F4-no	F5-OSP	dis-F4 & dis-F5S	no action
F4-no	F5-IP	dis-F4	no action
F4-no	F5-TSP	dis-F4 & dro-F5S	no action
F4-no	F5-TEP	dis-F4 & dro-F5	no action
F4-OEP	no	dis-F5	no action
F4-OEP	F5-OEP	dis-F4 & dis-F5	no action
F4-OEP	F5-OSP	dis-F4 & dis-F5S	no action
F4-OEP	F5-IP	dis-F4	no action
F4-OEP	F5-TSP	dis-F4 & dro-F5	no action
F4-OSP	don’t care	dis-F4S & F5=User	F5=User
F4-IP	don’t care	F5=User	F5=User
F4-TSP	don’t care	dro-F4S & F5=User	F5=User
F4-TEP	F5-no	dro-F4 & dis-F5	no action
F4-TEP	F5-OSP	dro-F4 & dis-F5S	no action
F4-TEP	F5-IP	dro-F4	no action
F4-TEP	F5-TSP	dro-F4 & dro-F5S	no action
F4-TEP	F5-TEP	dro-F4 & dro-F5	no action

dro: dropping; dis: discarding; F4/F5: F4/F5 End-to-End cell; F4S/F5S: F4/F5 Segment cell;

In downstream direction the discarding of the House Keeping cells for proprietary OAM functions and of both the F5RM and F5RES (PTI=111) at TEP can be enabled or disabled by the HK_DIS and F5RM_DISC flags in the DCT/UCT_CONFIG register. The F5RM and F5RES discard function is needed if the PHY device cannot handle these cell types.

2.8 Programmable Cell Filter Functionality

The ATM-LP has two fully programmable and maskable cell type filters for up- and downstream direction that can be configurated to forward, discard, drop or copy the filtered cell. Each programmable cell filter can be enabled or disabled via the SW flag PCF1/2_EN and the corresponding actions on the filtered cell are configurated via SW bits PCF1/2_ACT in the DCT/UCT_CONFIG register respectively. The data format of the cell filter and the cell mask structure is written from the microprocessor via the WDR0-3 (see page 71) write registers to the cell filter. The cell filter compares bit by bit the first seven Bytes of each cell with the seven Bytes of the unmasked cell filter. Masked bits of the cell filter are not compared. The following **Table 12** shows the matching conditions for the cell filter.

Table 12 Truth Table for Cell Filter

Comparison of Cell Header Bit (x,y) with Programmable Cell Filter Bit (x,y)	Programmable Cell Mask Bit (x,y)	Match for Bit (x,y)
don't care	0	yes
cell header bit(x,y) = cell filter bit(x,y)	1	yes
cell header bit(x,y) ≠ cell filter bit(x,y)	1	no

The Cell filter match if the comparison of all bits of the extended cell header matches. After the matching the corresponding action on the filtered cell (forward, discard, drop or copy) depends on the status of the CRC-10 check and the SW flag CRC_1/2_NODISC in register DCT/UCT_CONFIG. The action on the filtered cell is performed if no CRC-10 failure occur or if the discarding of cells with CRC-10 failure is disabled by the SW flag CRC_1/2_NODISC which is recommended for all user cells extracted by the cell filter. The reason is that user cells have normally no CRC-10.

The programmable cell filter 1 and 2 as well as the cell type filter for OAM light has different priorities which influence the cell processing if all three cell filters match for the same incoming cell. The priority is as follow:

- Programmable and maskable cell filter 1 has highest priority if matching (Prio 1)
- Programmable and maskable cell filter 2 has medium priority if matching (Prio 2)
- Cell filter for other cells as OAM cell has lowest priority if matching (Prio 3)

The filter with the highest priority determines the cell processing. The SW is responsible for the reasonable programming of the cell filters because the priority mechanism can lead to misinserted cells in case of OAM light.

Caution

At a F4 TEP the OAM filter will drop the F4 End-to-End OAM cell if OAM light is enabled. A programmable cell filter configurated for the same F4 End-to-End OAM cell with the cell action „forward“ has a higher priority than the OAM cell filter so that this cell is forwarded. This leads to a misinserted OAM cell.

The extended cell header format checked by the programmable cell filter is depicted in **Figure 38**. The Payload_1 contains informations on the OAM type (AIS, RDI, CC, CCA, LB or undefined).

bit:	7	6	5	4	3	2	1	0
1	Up: GFC/VPI; Down: LCI				Up: VPI; Down: LCI			
2	Up: VPI; Down: LCI				VCI			
3	VCI							
4	VCI				PTI			CLP
5	UDF1							
6	UDF2							
7	Payload_1							

Figure 38 Cell Format checked for Programmable Cell Filter

2.9 Configuration of ATM-LP via Microprocessor

The ATM-LP is configurated via the write and read registers WDR and RDR (see page 71) by the microprocessor. The WDR and RDR registers consist of 11 dwords (32Bit) which are connected with the 16 Bit Data bus of the microprocessor interface. The CMR register (see page 113) controls the access of the microprocessor to the external RAMs (POLURAM, CONNRAMUP and CONNRAMDO), the external Address Reduction Circuit CAME, the internal Port Tables for Traffic Measurement and the internal programmable Cell Filters 1 and 2. The address of the RAMs, CAME and Port Table is transferred via the ADR register (see page 130). For the programming of the POLURAM all 11 dwords of the WDR and RDR registers are used. For the CONNRAMUP only 8 dwords, for the CONNRAMDO only 7 dwords, for the Port Tables only 8 dwords and for the programmable Cell Filter only 4 dwords are used. The LCI address of all RAMs and the Port Table Address is written into the ADR register. The addressing of the programmable Cell Filters is controlled directly by the CMR. The CAME contents is transferred via the CAMADR register and the LCI address via the ADR register. Additionally a read modify write mask register RMW (see page 124) is implemented for the case that only parts of the dwords shall be changed. The start of the specific request is initiated by the SW flag STREQ which is reset by the ATM-LP when the command is finished. The ATM-LP registers are programmed as usual. The structure of register and the address and data flow for the access to the internal and external RAMs is depicted in **Figure 39**.

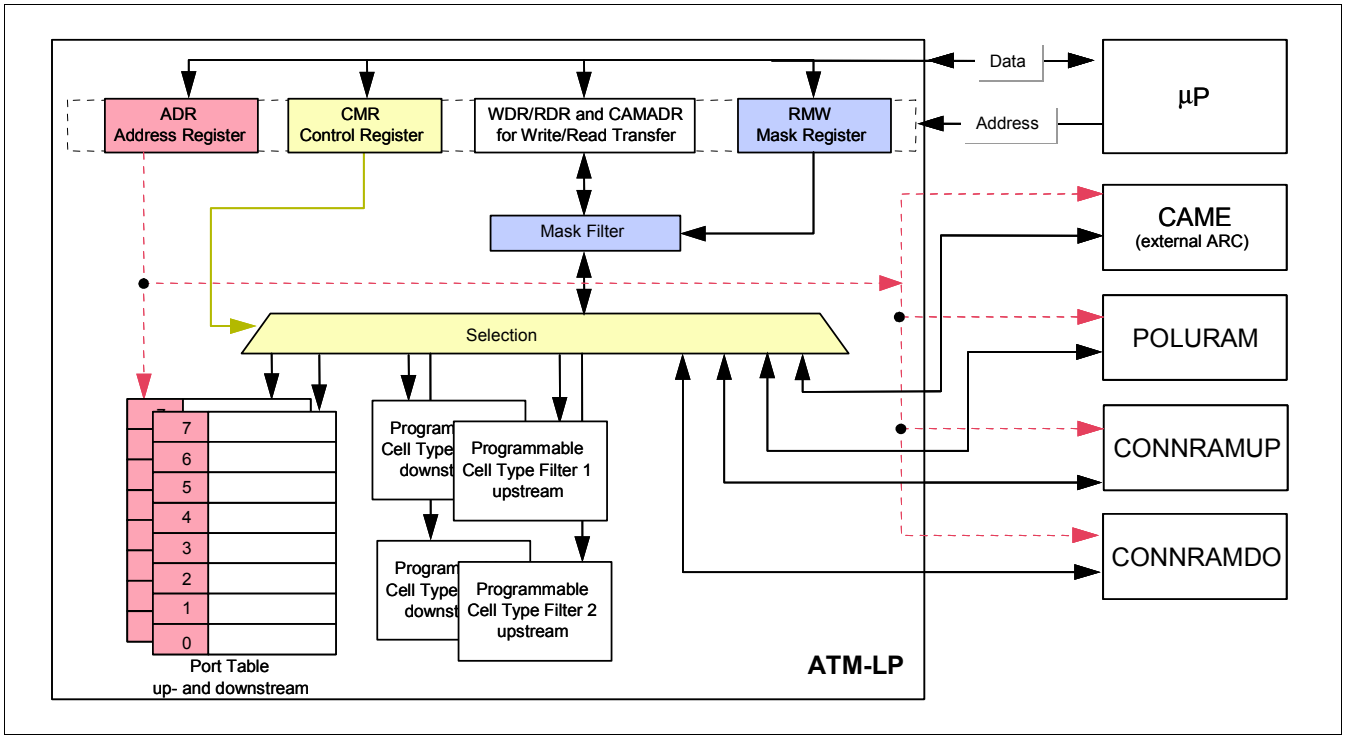


Figure 39 Access to the Internal and External RAMs

3 Register Description

3.1 Overview of the ATM-LP Register

Table 13 ATM-LP Registers Overview

addr (hex)	register	description	reset value	µP	see page
Read/Write Registers					
00	WDR0L	write register 0	undef.	r/w	71
01	WDR0H	write register 0	undef.	r/w	71
...	...	...			
14	WDRAL	write register A	undef.	r/w	71
15	WDRAH	write register A	undef.	r/w	71
16	RDR0L	read register 0	undef.	r/w	72
17	RDR0H	read register 0	undef.	r/w	72
...	...	...			
2A	RDRAL	read register A	undef.	r/w	72
2B	RDRAH	read register A	undef.	r/w	72
Port Configuration Registers					
2E	UNIPORTL	port configuration (UNI)	0000	r/w	91
2F	UNIPORTH	port configuration (UNI)	0000	r/w	91
CAME Data Registers					
32	CAMADRL	data which is to store into the CAME	0000	r/w	92
33	CAMADRH	data which is to store into the CAME	0000	r/w	92
POLU Configuration Register					
36	P_CONRL	POLU configuration register	00FF	r/w	93
37	P_CONRH	POLU configuration register	0000	r/w	94
Version Register					
40	VERL	Low/High Word of Version numberv	9063	r	95
41	VERH	Low/High Word of Version numberv	523B	r	95

Table 13 ATM-LP Registers Overview (cont'd)

addr (hex)	register	description	reset value	µP	see page
Transmit Registers (Cell Insertion Buffer)/TXR Configuration Register					
50	TXR0	transmit cell register 0	0000	r/w	96
51	TXR1	transmit cell register 1	0000	r/w	96
52	TXR2	transmit cell register 2	0000	r/w	97
53	TXR3	transmit cell register 3: payload 0/ payload 1	0000	r/w	98
...	...	...		...	
6A	TXR26	transmit cell register 26: payload 46/ payload 47	0000	r/w	98
6B	TXR_CONFIG	configuration of transmit cell buffer	0000	r/w	99
Receive Register/Receive Cell Buffer					
70	RXR	receive cell buffer access	undef.	r	99
Header Capture/Protocol Monitoring Register Set 0 .. 3 Upstream					
72	PRMONR0A_U	protocol monitoring buffer 0 upstream	0000	r	101
73	PRMONR0B_U	protocol monitoring buffer 0 upstream	0000	r	101
74	PRMONR0C_U	protocol monitoring buffer 0 upstream	0000	r	102
...	...	...			
7B	PRMONR3A_U	protocol monitoring buffer 3 upstream	0000	r	101
7C	PRMONR3B_U	protocol monitoring buffer 3 upstream	0000	r	101
7D	PRMONR3C_U	protocol monitoring buffer 3 upstream	0000	r	102
Header Capture/Protocol Monitoring Register Set Downstream					
7E	PRMONRA_D	protocol monitoring buffer downstream	0000	r	102
7F	PRMONRB_D	protocol monitoring buffer downstream	0000	r	103
80	PRMONRC_D	protocol monitoring buffer downstream	0000	r	103
Protocol Monitoring Configuration Register					
81	HEADCAPEN	enables header capturing	0000	r/w	103

Table 13 ATM-LP Registers Overview (cont'd)

addr (hex)	register	description	reset value	µP	see page
Configuration of Portspecific Counters Upstream					
84	PORTCONF0_U	port specific counter configuration upstream	0000	r/w	104
...	...	...			
8B	PORTCONF7_U	port specific counter configuration upstream	0000	r/w	104
8C	ENPOTIC	enables port specific counter POTIC	0000	r/w	105
Configuration of Portspecific Counters Downstream					
8D	PORTCONF0_D	port specific counter configuration down-stream	0000	r/w	106
...	...	...			
94	PORTCONF7_D	port specific counter configuration downstream	0000	r/w	106
95	ENPOTOC	enables port specific counter POTOC	0000	r/w	107
UTOPIA Configuration Registers					
96	CONUT1A	UTOPIA configuration	0000	r/w	107
97	CONUT1B	UTOPIA configuration	0000	r/w	108
98	CONUT1C	UTOPIA configuration	0000	r/w	108
99	CONUT2	UTOPIA configuration	0000	r/w	108
9A	CONUT3	UTOPIA configuration	003F	r/w	110
UTOPIA Downstream Queue Overflow Indication Registers					
9B	UT_QOV1	UTOPIA queue overflow (downstream)	0000	r*)	111
9C	UT_QOV2	UTOPIA queue overflow; buffer overflow (downstream)	0000	r*)	111
Configuration Of Header Translation/Special Enable Bits					
9E	ADRED_VPIM	minimal VPI used in ARC without CAME	0000	r/w	112
9F	MODE	configuration of address reduction, header translation and traffic measurement; enable writing of TESTR and BISTMODE	0000	r/w	112

Table 13 ATM-LP Registers Overview (cont'd)

addr (hex)	register	description	reset value	µP	see page
Command Register					
A0	CMR	µP-request definition	0000	r/w	113
Status Registers For Header Capture/CAME					
A1	STATR	status of protocol monitoring	0000	r	115
A2	CSTATR	status of CAME after µP request	0000	r	116
Interrupt Status Registers/Interrupt Mask Registers					
A3	ISR0	interrupt status register	0000	r*)	117
A4	ISR1	interrupt status register	0000	r*)	119
A5	IMR0	interrupt mask register	0000	r/w	120
A6	IMR1	interrupt mask register	0000	r/w	122
CAME Interrupt Status Register					
A7	CSIR	status of CAME after interrupt; port number after interrupts	0000	r*)	123
RWR MASK REGISTER					
A9	RMW_MASK	mask of single words at read/write accesses	0000	r/w	124
Cell Type Recognition Configuration Registers					
AA	UCT_CONFIG	action on receiving OAM-cells upstream	0000	r/w	125
AB	DCT_CONFIG	action on receiving OAM-cells downstream	0000	r/w	127
RMW Reset Configuration Register					
AC	RMW_CONF	reset of single words in the read/modify/ write block	0000	r/w	129
Address Register For CMR Commands					
AD	ADR	address of a µP request	0000	r/w	130

Table 13 ATM-LP Registers Overview (cont'd)

addr (hex)	register	description	reset value	µP	see page
Scan Configuration Registers					
AE	SC_CONR1	configuration of POLU refresh	0000	r/w	131
AF	SC_CONR2	configuration of POLU refresh	0000	r/w	131
DMA Configuration/Read Register					
B0	DCONR	configuration of DMA	0000	r/w	132
B1	DMAR	DMA FIFO access	undef.	r	134
Test Register/Special Modes					
B2	TESTR	test configuration	0000	r/w	135
POLU Status Registers					
B3	P_STATR0	POLU status register 0	0000	r	137
B4	P_STATR1	POLU status register 1	0000	r	137
B5	P_STATR2	POLU status register 2	0000	r	137
CAME Valid Intermediate LCI					
B6	CAMVILCI	response from address reduction test	0000	r	138
DMA Range Registers					
B8	DMA_MIN	lower LCI of DMA	0000	r/w	138
B9	DMA_MAX	upper LCI of DMA	0000	r/w	138
BIST Registers					
BA	BISTMODE1	BIST mode register 1	0000	r/w	139
BB	BISTMODE2	BIST mode register 2	0000	r/w	140
BC	BISTDONE	BIST active register	0000	r	141
BD	BISTERROR	BIST result register	0FFF	r/w**)	142

*Note: *) Single bits of this register are resettable by writing a '1' to them.*
***) Register is reset at each write access.*

3.2 Transfer Register General Mapping to Dwords

3.2.1 Read/Write Registers

Register set used for all read/write µP-requests (see CMR-register **Section 3.19,** page 113). They are used as an shadow image of the specified data block.

WDR (Write Data Register): contents of WDR registers are transferred to the destination selected in register CMR.

RDR (Read Data Register): contents of the source selected in register CMR are transferred to RDR registers.

Note: At write accesses to an external RAM bit 31 of the corresponding WDR-register is used to control the parity generation as follows:
bit31=0 : generate right parity for this word
bit31=1 : generate wrong parity for this word.
At read accesses from an external RAM the result of the parity check is written into bit 31 of the corresponding RDR-register. The coding is as follows:
bit31=0 : parity check is okay for this word
bit31=1 : parity check failed for this word.

3.2.1.1 Write Transfer Registers (WDR0L/WDR0H..WDRAL/WDRAH)

Read/write Address $00_H..15_H$
Value after reset undefined

Dword	31 23	15 7 0
10	Register WDRAH / Address 15_H	Register WDRAL / Address 14_H
9	Register WDR9H / Address 13_H	Register WDR9L / Address 12_H
8	Register WDR8H / Address 11_H	Register WDR8L / Address 10_H
7	Register WDR7H / Address $0F_H$	Register WDR7L / Address $0E_H$
6	Register WDR6H / Address $0D_H$	Register WDR6L / Address $0C_H$
5	Register WDR5H / Address $0B_H$	Register WDR5L / Address $0A_H$
4	Register WDR4H / Address 09_H	Register WDR4L / Address 08_H
3	Register WDR3H / Address 07_H	Register WDR3L / Address 06_H
2	Register WDR2H / Address 05_H	Register WDR2L / Address 04_H
1	Register WDR1H / Address 03_H	Register WDR1L / Address 02_H
0	Register WDR0H / Address 01_H	Register WDR0L / Address 00_H

3.2.1.2 Read Transfer Registers (RDR0L/RDR0H..RDRAL/RDRAH)

Read/write Address $16_H..2B_H$
Value after reset undefined

Dword	31 23	15 7 0
10	Register RDRAH / Address $2B_H$	Register RDRAL / Address $2A_H$
9	Register RDR9H / Address 29_H	Register RDR9L / Address 28_H
8	Register RDR8H / Address 27_H	Register RDR8L / Address 26_H
7	Register RDR7H / Address 25_H	Register RDR7L / Address 24_H
6	Register RDR6H / Address 23_H	Register RDR6L / Address 22_H
5	Register RDR5H / Address 21_H	Register RDR5L / Address 20_H
4	Register RDR4H / Address $1F_H$	Register RDR4L / Address $1E_H$
3	Register RDR3H / Address $1D_H$	Register RDR3L / Address $1C_H$
2	Register RDR2H / Address $1B_H$	Register RDR2L / Address $1A_H$
1	Register RDR1H / Address 19_H	Register RDR1L / Address 18_H
0	Register RDR0H / Address 17_H	Register RDR0L / Address 16_H

3.3 Mapping of Transfer Register to Internal / External RAMs

3.3.1 Policing RAM (POLURAM)

Note: The 31-st bit is always a parity over address and data.

Dword	31	23	15	7	0
10	31	27	F5E2E_U/D(1:0)	F4E2E_U/D(1:0)	F5SEG_U/D(1:0)	F4SEG_U/D(1:0)	F5RM_U/D(1:0)	F4RM_U/D(1:0)	USER_U/D(1:0)	MODE(1:0)	DIS_U/D(1:0)	DELTA3(31:23)
9	31	DELTA3(22:0)	DELTA2(31:24)
8	31	DELTA2(23:0)	DELTA1(31:25)
7	31	DELTA1(24:0)	WMIN3(33:28)
6	31	WMIN3(27:0)	WMIN2(33:31)
5	31	WMIN2(30:0)
4	31	WMIN1(41:11)
3	31	WMIN1(10:0)	Y3(34:15)
2	31	Y3(14:0)	Y2(34:19)
1	31	Y2(18:0)	Y1(42:31)
0	31	Y1(30:0)
CMR(4:0) = 00000												

3.3.1.1 Policing RAM : Dword0

Bit 31 Parity Bit of Dword0
Odd Parity over address and data.

Y1(30:0) Policing variable of LB1.

Note: Initialized with all '0' at the establishment of a connection. Don't change the value during normal policing operation.

3.3.1.2 Policing RAM : Dword1

Bit 31 Parity Bit of Dword1
Odd Parity over address and data.

Y2(18:0) Policing variable of LB2.

Note: Initialized with all '0' at the establishment of a connection. Don't change the value during normal policing operation.

Y1(42:31) Policing variable of LB1.

Note: Initialized with all '0' at the establishment of a connection. Don't change the value during normal policing operation.

3.3.1.3 Policing RAM : Dword2

Bit 31 Parity Bit of Dword2
Odd Parity over address and data.

Y3(14:0) Policing variable of LB3.

Note: Initialized with all '0' at the establishment of a connection. Don't change the value during normal policing operation.

Y2(34:19) Policing variable of LB2.

Note: Initialized with all '0' at the establishment of a connection. Don't change the value during normal policing operation.

3.3.1.4 Policing RAM : Dword3

Bit 31 Parity Bit of Dword3
Odd Parity over address and data.

WMIN1(10:0) Policing parameter w_{min1} of LB1
WMIN1(10:0) is fractional value of w_{min1}. LSB of w_{min1} (WMIN1(0)) is 2^{-11}.

Y3(34:15) Policing variable of LB3.

Note: Initialized with all '0' at the establishment of a connection. Don't change the value during normal policing operation.

3.3.1.5 Policing RAM : Dword4

Bit 31 Parity Bit of Dword4
Odd Parity over address and data.

WMIN1(41:11) Policing parameter w_{min1} of LB1
WMIN1(41:11) is integer value of w_{min1}. MSB of w_{min1} (WMIN1(41)) is 2^{31}.

3.3.1.6 Policing RAM : Dword5

Bit 31 Parity Bit of Dword5
Odd Parity over address and data.

WMIN2(30:0) Policing parameter w_{min2} of LB2
WMIN2(10:0) is fractional value of w_{min2}. LSB of w_{min2} (WMIN2(0)) is 2^{-11}.
WMIN2(30:11) is integer value of w_{min2}.

3.3.1.7 Policing RAM : Dword6

Bit 31 Parity Bit of Dword6
Odd Parity over address and data.

WMIN3(27:0) Policing parameter w_{min3} of LB3
WNIM3(10:0) is fractional value of w_{min3}. LSB of w_{min3} (WMIN3(0)) is 2^{-11}.
WMIN3(27:11) is integer value of w_{min3}.

WMIN2(33:31) MSB of w_{min2} (WMIN2(33)) is 2^{23}.

3.3.1.8 Policing RAM : Dword7

Bit 31 — Parity Bit of Dword7
Odd Parity over address and data.

DELTA1(24:0) — Policing parameter $Delta_1$ of LB1
DELTA1(10:0) is fractional value of $Delta_1$. LSB of $Delta_1$ (DELTA1(0)) is 2^{-11}.
DELTA1(24:11) is integer value of $Delta_1$.

WMIN3(33:28) — MSB of w_{min3} (WMIN3(33)) is 2^{23}.

3.3.1.9 Policing RAM : Dword8

Bit 31 — Parity Bit of Dword8
Odd Parity over address and data.

DELTA2(23:0) — Policing parameter Delta2 of LB2
DELTA2(10:0) is fractional value of $Delta_2$. LSB of $Delta_2$ (DELTA2(0)) is 2^{-11}.
DELTA2(23:11) is integer value of $Delta_2$.

DELTA1(31:25) — Policing parameter $Delta_1$ of LB1
MSB of $Delta_1$ (DELTA1(31)) is 2^{21}.

3.3.1.10 Policing RAM : Dword9

Bit 31 — Parity Bit of Dword9
Odd Parity over address and data.

DELTA3(22:0) — Policing parameter $Delta_3$ of LB3
DELTA3(10:0) is fractional value of $Delta_3$. LSB of $Delta_3$ (DELTA3(0)) is 2^{-11}.
DELTA3(22:11) is integer value of $Delta_3$.

DELTA2(31:24) — Policing parameter $Delta_2$ of LB2
MSB of $Delta_2$ (DELTA2(31)) is 2^{21}.

3.3.1.11 Policing RAM : Dword10

Bit 31 — Parity Bit of Dword10
Odd Parity over address and data.

Bit 30:28 — Not used.

Bit 27 — SHOW_PARAM used only for testing. Don’t change the contents.

F5E2E_U/D(1:0) — Coding of F5 end to end cell policing option flags:

- 00 No policing.
- 01 Down path (LB3).
- 10 Upper path (LB1 and LB2)
- 11 No policing.

F4E2E_U/D(1:0) — Coding of F4 end to end cell policing option flags:

- 00 No policing.
- 01 Down path (LB3).
- 10 Upper path (LB1 and LB2)
- 11 No policing.

F5SEG_U/D(1:0) Coding of F5 segment cell policing option flags:
- 00 No policing.
- 01 Down path (LB3).
- 10 Upper path (LB1 and LB2)
- 11 No policing.

F4SEG_U/D(1:0) Coding of F4 segment cell policing option flags:
- 00 No policing.
- 01 Down path (LB3).
- 10 Upper path (LB1 and LB2)
- 11 No policing.

F5RM_U/D(1:0) Coding of F5RM cell policing option flags:
- 00 No policing.
- 01 Down path (LB3).
- 10 Upper path (LB1 and LB2)
- 11 No policing.

F4RM_U/D(1:0) Coding of F4RM cell policing option flags:
- 00 No policing.
- 01 Down path (LB3).
- 10 Upper path (LB1 and LB2)
- 11 No policing.

USER_U/D(1:0) Coding of User cell policing option flags:
- 00 No policing.
- 01 Down path (LB3).
- 10 Upper path (LB1 and LB2)
- 11 No policing.

MODE(1:0) POLU operating mode.
- 00 Tagging option is on
  - Parameters of LB1 are: SCR_0 and MBS_0
  - Parameter of LB2 is: PCR_{0+1}
  - Parameter of LB3 is: PCR_{0+1}
- 01 Tagging option is off
  - Parameters of LB1 are: SCR_0 and MBS_0
  - Parameter of LB2 is: PCR_{0+1}
  - Parameter of LB3 is: PCR_{0+1}
- 10 Tagging option is off
  - Parameters of LB1 are: SCR_{0+1} and MBS_{0+1}
  - Parameter of LB2 is: PCR_{0+1}
  - Parameter of LB3 is: PCR_{0+1}
- 11 Tagging option is off
  - Parameters of LB1 are: PCR_{0+1}
  - Parameter of LB2 is: disabled
  - Parameter of LB3 is: PCR_{0+1}

DIS_U/D(1:0) Disable connection flag for upper/down path.

00	normal policing
01	down path disabled
10	upper path disabled
11	down and upper path disabled

Note: Disabling means: The state variables and the counters of the nonconforming cells are updated, but the cells are neither discarded or tagged.

DELTA3(31:23) Policing parameter $Delta_3$ of LB3
MSB of $Delta_3$ (DELTA3(31)) is 2^{21}.

3.3.2 Connection RAM Upstream

Dword	31				23							15							7							0
7	P	VPC specific total incoming cells with CLP=0 (= P_TIC0)																								
6	P	VPC specific total incoming cells (= P_TIC)																								
5	P	Counter (Total tagged cells) (= TTC)																								
4	P	Counter (Total discarded cells with CLP=0) (= TDC0)																								
3	P	Counter (Total discarded cells with CLP=1) (= TDC1)																								
2	P	Total incoming cells with CLP=0 (= TIC0)																								
1	P	Total incoming cells (= TIC)																								
0	P	30		28	F5PT_CFG(2:0)			F4PT_CFG(2:0)			21	20	19	HK(2:0)			15	14	LCI2_UP(13:0)							
CMR(4:0) = 00001																										

3.3.2.1 Connection RAM Upstream: Dword0

Header translation connection data up.

P Parity
Odd Parity over address and data (look at remarks for Read/Write registers in ATM-LP Registers Detailed Description).

Bit 30 P_IP
Reserved for future functions.

Bit 29 Not used.

Bit 28 CC_IP_COPY

0	Forward cells
1	Continuity Check (CC) OAM cells are copied at intermediate points (IP) (used for OAM Light).

F5PT_CFG(2:0) F5 (channel specific) point configuration (used for OAM Light). The subsequent layer point codings are possible :

000 No F5 layer point
010 F5 OEP (originating end point)
011 F5 OSP (originating segment point)
100 F5 IP (intermediate point)
110 F5 TSP (terminating segment point)
111 F5 TEP (terminating end point)

F4PT_CFG(2:0) F4 (path specific) point configuration (used for OAM Light). The subsequent layer point codings are possible :

000 No F4 layer point
010 F4 OEP (originating end point)
011 F4 OSP (originating segment point)
100 F4 IP (intermediate point)
110 F4 TSP (terminating segment point)
111 F4 TEP (terminating end point)

Bit 21 LB_IP_DROP
Default LB action on IP points (used by cell type recognition) :

0 Forward cells.
1 Drop OAM cells of type LB at intermediate points.

Bit 20 AR_IP_COPY
Default OAM action on IP points (used by cell type recognition) :

0 Forward cells.
1 Copy OAM cells of type AIS/RDI at intermediate points.

Bit 19 VCON_UP

0 Invalid connection.
1 Valid connection indicated.

HK(2:0) House Keeping bits.

Bit 15 INC_TIMC_SSD

1 Increment the Total Incoming Management Cells special studies counter upstream at cell emission on this VC.

Bit 14 EN_TRAF_MEAS_UP

1 Enable traffic measurements (independently of VCON).

LCI2_UP(13:0) F4 data pointer.

3.3.3 Connection RAM downstream

Dword	31								23								15								7								0
6	P	VP specific total outgoing cells with CLP=0 (= P_TOC0)																														
5	P	VPC specific total outgoing cells (= P_TOC)																														
4	P	Total outgoing cells with CLP=0 (= TOC0)																														
3	P	Total outgoing cells (= TOC)																														
2	P																PN_UT_DO (4:0)									14	NEXT_LCI(13:0)						
1	P	30	29	28	VPI_DO(11:0)																VCI_DO(15:0)												
0	P	30	F5CFG (2:0)			F4CFG (2:0)			23	22	PNUDF(5:0)								15	14	LCI2_DO(13:0)												
CMR(4:0) = 00010																																

3.3.3.1 Connection RAM downstream : Dword0

Header translation connection data down (Flags, LCI2, PN).

P — Parity
Odd Parity over address and data (look at remarks for Read/Write registers in ATM-LP Registers Detailed Description).

Bit 30 — P_IP
- 0 Path End Point.
- 1 Path Intermediate Point. At Path Intermediate Points only a VPI header translation takes place.

F5CFG(2:0) — F5 (channel specific) point configuration (used for OAM Light). The subsequent layer point codings are possible :
- 000 No F5 layer point
- 010 F5 OEP (originating end point)
- 011 F5 OSP (originating segment point)
- 100 F5 IP (intermediate point)
- 110 F5 TSP (terminating segment point)
- 111 F5 TEP (terminating end point)

F4CFG(2:0) — F4 (path specific) point configuration (used for OAM Light). The subsequent layer point codings are possible :
- 000 No F4 layer point
- 010 F4 OEP (originating end point)
- 011 F4 OSP (originating segment point)
- 100 F4 IP (intermediate point)
- 110 F4 TSP (terminating segment point)
- 111 F4 TEP (terminating end point)

Bit 23 EN_TRAF_MEAS_DO
1 Enable traffic measurements of all connection specific counters of this specific connection (independently of VCON-bit).

Bit 22 VCON_DO
1 Indicates that this connection is valid.

PNUDF(5:0) New portnumber (PN) that is mapped into the UDF1 field of the outgoing cell header (mapping will be always done independently of selected portnumber mode).

Bit 15 INC_TOF5RMC_SSD
Increment the Total Outgoing Resource Management Cells special studies counter downstream (counter POTOCOR) at F5 RM cell emission on this VC.

Bit 14 INC_TOMC_SSD
Increment the Total Outgoing Cells special studies counter downstream (counter POTOCOR) at cell emission on this VC.

LCI2_DO(13:0) The LCI2 is a F4 data pointer which addresses the path specific counters.

3.3.3.2 Connection RAM downstream : Dword 1

Header translation connection data down (VPI,VCI).

Bit 31 Parity
Odd Parity over address and data.

Bit 30 CC_IP_COPY
0 Forward cells.
1 Copy OAM cells of type CCA/CC at intermediate points.

Bit 29 LB_IP_DROP
Default LB action on IP points (used by cell type recognition) :
0 Forward cells.
1 Drop OAM cells of type LB at intermediate points.

Bit 28 AR_IP_COPY
Default OAM action on IP points (used by cell type recognition) :
0 Forward cells.
1 Copy OAM cells of type AIS/RDI at intermediate points.

VPI_DO(11:0) New VPI for Header Translation.

VCI_DO(15:0) New VCI for Header Translation.

3.3.3.3 Connection RAM downstream : Dword2

LCI of the following connection in the multicast chain.

Bit 31 Parity
Odd Parity over address and data.

Bit 30:21 Not used.

PN_UT_DO(4:0) UT-PN, used if MODE(11) = ’0’.

Bit 15 Not used.

Bit 14 MC_ANCHOR
0 Indicates the end of the linked list in MC.
1 The NEXT_LCI pointer (b.13..0) is valid.

NEXT_LCI(13:0) LCI of the following connection in the multicast chain.

3.3.4 Traffic Measurement RAM (Port Table)

3.3.4.1 Port Table Upstream

Dword	31 23 15 7 0
47	Counter POTIC_F for : Total incoming cells at port number 15
...	...
32	Counter POTIC_0 for : Total incoming cells at port number 0
31	Counter POTICOR_C7 for : Total incoming OAM or RM cells enabled per connection at port number CNTPORT7_U
30	Counter POTIC_C7 for : Total incoming cells at port number CNTPORT7_U
29	Counter POTICN_C7 for : Total incoming cells with non-zero GFC-field at port number CNTPORT7_U
28	Counter PDC_C7 for : Total discarded cells due to unallocated PN/VPI/VCI at port number CNTPORT7_U
...	...
3	Counter POTICOR_C0 for : Total incoming OAM or RM cells enabled per connection at port number CNTPORT0_U
2	Counter POTIC_C0 for : Total incoming cells at port number CNTPORT0_U
1	Counter POTICN_C0 for : Total incoming cells with non-zero GFC-field at port number CNTPORT0_U
0	Counter PDC_C0 for : Total discarded cells due to unallocated PN/VPI/VCI at port number CNTPORT0_U

CMR(4:0) = 00011;

Addressing via LCI of ADR register

Address	Dword
0_H	0 - 7
1_H	8 - 15
2_H	16 - 23
3_H	24 - 31
4_H	32 - 39
5_H	40 - 47
6_H - $3FFF_H$	no action

Data to/from RDR/WDR register at address 0_H in ADR register

Dword(0..7)	Counter
0	PDC_C0
1	POTICN_C0
2	POTIC_C0
3	POTICOR_C0
4	PDC_C1
5	POTICN_C1
6	POTIC_C1
7	POTICOR_C1
8 - A	not used

Data to/from RDR/WDR register at address 1_H in ADR register

Dword(8..15)	Counter
0	PDC_C2
1	POTICN_C2
2	POTIC_C2
3	POTICOR_C2
4	PDC_C3
5	POTICN_C3
6	POTIC_C3
7	POTICOR_C3
8 - A	not used

Data to/from RDR/WDR register at address 2_H in ADR register

Dword(16..23)	Counter
0	PDC_C4
1	POTICN_C4
2	POTIC_C4
3	POTICOR_C4
4	PDC_C5
5	POTICN_C5
6	POTIC_C5
7	POTICOR_C5
8 - A	not used

Data to/from RDR/WDR register at address 3_H in ADR register

Dword(24..31)	Counter
0	PDC_C6
1	POTICN_C6
2	POTIC_C6
3	POTICOR_C6
4	PDC_C7
5	POTICN_C7
6	POTIC_C7
7	POTICOR_C7
8 - A	not used

Data to/from RDR/WDR register at address 4_H in ADR register

Dword(32..39)	Counter
0	POTIC_0
1	POTIC_1
2	POTIC_2
3	POTIC_3
4	POTIC_4
5	POTIC_5
6	POTIC_6
7	POTIC_7
8 - A	not used

Data to/from RDR/WDR register at address 5_H in ADR register

Dword(40..47)	Counter
0	POTIC_8
1	POTIC_9
2	POTIC_A
3	POTIC_B
4	POTIC_C
5	POTIC_D
6	POTIC_E
7	POTIC_F
8 - A	not used

3.3.4.2 Port Table Downstream

Dword	31 23 15 7 0
31	Counter POTOC_F for : Total outgoing cells at port number 15
...	...
16	Counter POTOC_0 for : Total outgoing cells at port number 0
15	Counter POTOCOR_C7 for : Total outgoing OAM or RM cells or discarded F5RM cells enabled per connection at port number CNTPORT7_D
14	Counter POTOC_C7 for : Total outgoing cells at port number CNTPORT7_D
...	...
1	Counter POTOCOR_C0 for : Total outgoing OAM or RM cells or discarded F5RM cells enabled per connection at port number CNTPORT0_D
0	Counter POTOC_C0 for : Total outgoing cells at port number CNTPORT0_D

CMR(4:0) = 00100;

Addressing via LCI of ADR register

Address	Dword
0_H	0 - 7
1_H	8 - 15
2_H	16 - 23
3_H	24 - 31
4_H - $3FFF_H$	no action

Read out with CMR register. TM counters addressed by LCI value of ADR register.

Data to/from RDR/WDR register at address 0_H in ADR register

Dword(0..7)	Counter
0	POTOC_C0
1	POTOCOR_C0
2	POTOC_C1
3	POTOCOR_C1
4	POTOC_C2
5	POTOCOR_C2
6	POTOC_C3
7	POTOCOR_C3
8 - A	not used

Data to/from RDR/WDR register at address 1_H in ADR register

Dword(8..15)	Counter
0	POTOC_C4
1	POTOCOR_C4
2	POTOC_C5
3	POTOCOR_C5
4	POTOC_C6
5	POTOCOR_C6
6	POTOC_C7
7	POTOCOR_C7
8 - A	not used

Data to/from RDR/WDR register at address 2_H in ADR register

Dword(16..23)	Counter
0	POTOC_0
1	POTOC_1
2	POTOC_2
3	POTOC_3
4	POTOC_4
5	POTOC_5
6	POTOC_6
7	POTOC_7
8 - A	not used

Data to/from RDR/WDR register at address 3_H in ADR register

Dword(24..31)	Counter
0	POTOC_8
1	POTOC_9
2	POTOC_A
3	POTOC_B
4	POTOC_C
5	POTOC_D
6	POTOC_E
7	POTOC_F
8 - A	not used

3.4 Cell Type Filter Registers

Read/write Address controlled by CMR command
Value after reset occur via µP initialization

Data structure of extended cell header...

up/down celltype	11	015	02	0	7	07	07	0
	VPI	VCI	PT	C	UDF1	UDF2	1st payload	

...is compared with data structure of masked cell filter :

U 1	CT_FILTH1_U1(7:0)	CT_FILTH2_U1(7:0)	CT_FILTH3_U1(7:0)	CT_FILTH4_U1(7:0)	CT_FILTU1_U1(7:0)	CT_FILTU2_U1(7:0)	CT_FILTP1_U1(7:0)
U 1	CT_FILTH1_U1(15:8)	CT_FILTH2_U1(15:8)	CT_FILTH3_U1(15:8)	CT_FILTH4_U1(15:8)	CT_FILTU1_U1(15:8)	CT_FILTU2_U1(15:8)	CT_FILTP1_U1(15:8)
U 2	CT_FILTH1_U2(7:0)	CT_FILTH2_U2(7:0)	CT_FILTH3_U2(7:0)	CT_FILTH4_U2(7:0)	CT_FILTU2_U2(7:0)	CT_FILTU2_U2(7:0)	CT_FILTP1_U2(7:0)
U 2	CT_FILTH1_U2(15:8)	CT_FILTH2_U2(15:8)	CT_FILTH3_U2(15:8)	CT_FILTH4_U2(15:8)	CT_FILTU2_U2(15:8)	CT_FILTU2_U2(15:8)	CT_FILTP1_U2(15:8)
D 1	CT_FILTH1_D1(7:0)	CT_FILTH2_D1(7:0)	CT_FILTH3_D1(7:0)	CT_FILTH4_D1(7:0)	CT_FILTD1_D1(7:0)	CT_FILTU2_D1(7:0)	CT_FILTP1_D1(7:0)
D 1	CT_FILTH1_D1(15:8)	CT_FILTH2_D1(15:8)	CT_FILTH3_D1(15:8)	CT_FILTH4_D1(15:8)	CT_FILTD1_D1(15:8)	CT_FILTU2_D1(15:8)	CT_FILTP1_D1(15:8)
D 2	CT_FILTH1_D2(7:0)	CT_FILTH2_D2(7:0)	CT_FILTH3_D2(7:0)	CT_FILTH4_D2(7:0)	CT_FILTD2_D2(7:0)	CT_FILTU2_D2(7:0)	CT_FILTP1_D2(7:0)
D 2	CT_FILTH1_D2(15:8)	CT_FILTH2_D2(15:8)	CT_FILTH3_D2(15:8)	CT_FILTH4_D2(15:8)	CT_FILTD2_D2(15:8)	CT_FILTU2_D2(15:8)	CT_FILTP1_D2(15:8)
	7 07	07	07	07	07	07	0	

3.4.1 Register for Programmable Cell Type Filter 1 in Upstream

Dword	31 23	15 7 0
3	CT_FILTP1_U1(15:0)	
2	CT_FILTU1_U1(15:0)	CT_FILTU2_U1(15:0)
1	CT_FILTH3_U1(15:0)	CT_FILTH4_U1(15:0)
0	CT_FILTH1_U1(15:0)	C T_FILTH2_U1(15:0)

CMR(4:0) = 00101; write/read depicted data format to/from WDR0..3/RDR0..3 registers.

Note: Mask-bit:
'0' is don't care
'1' use Filter-bit for comparison.

3.4.1.1 Byte 1 and 2 of Cell Type Filter 1 : Dword 0

CT_FILTH2_U1(15:8) Filter1 for header byte 2.
CT_FILTH2_U1(7:0) Mask for filter 1 for header byte 2.
CT_FILTH1_U1(15:8) Filter1 for header byte 1.
CT_FILTH1_U1(7:0) Mask for filter 1 for header byte 1.

3.4.1.2 Byte 3 and 4 of Cell Type Filter 1 : Dword 1

CT_FILTH4_U1(15:8) Filter1 for header byte 4.
CT_FILTH4_U1(7:0) Mask for filter 1 for header byte 4.
CT_FILTH3_U1(15:8) Filter1 for header byte 3.
CT_FILTH3_U1(7:0) Mask for filter 1 for header byte 3.

3.4.1.3 Byte 5 and 6 of Cell Type Filter 1 : Dword 2

CT_FILTU2_U1(15:8) Filter1 for UDF2.
CT_FILTU2_U1(7:0) Mask for filter UDF2.
CT_FILTU1_U1(15:8) Filter1 for UDF1.
CT_FILTU1_U1(7:0) Mask for filter 1 UDF1.

3.4.1.4 Byte 7 of Cell Type Filter 1 : Dword 3

Bit (15:0) Not used.
CT_FILTP1_U1(15:8) Filter1 for payload byte 1.
CT_FILTP1_U1(7:0) Mask for filter 1 for payload byte 1.

3.4.2 Register for Programmable Cell Type Filter 2 in Upstream

Dword	31 23	15 7 0
3	CT_FILTP1_U2(15:0)	
2	CT_FILTU1_U2(15:0)	CT_FILTU2_U2(15:0)
1	CT_FILTH3_U2(15:0)	CT_FILTH4_U2(15:0)
0	CT_FILTH1_U2(15:0)	C T_FILTH2_U2(15:0)

CMR(4:0) = 00110; write/read depicted data format to/from WDR0..3/RDR0..3 registers.

Note: Mask-bit:
'0' is don't care
'1' use Filter-bit for comparison.

3.4.2.1 Byte 1 and 2 of Cell Type Filter 2 : Dword 0

CT_FILTH2_U2(15:8) Filter2 for header byte 2.
CT_FILTH2_U2(7:0) Mask for filter 2 for header byte 2.
CT_FILTH1_U2(15:8) Filter2 for header byte 1.
CT_FILTH1_U2(7:0) Mask for filter 2 for header byte 1.

3.4.2.2 Byte 3 and 4 of Cell Type Filter 2 : Dword 1

CT_FILTH4_U2(15:8) Filter2 for header byte 4.
CT_FILTH4_U2(7:0) Mask for filter 2 for header byte 4.
CT_FILTH3_U2(15:8) Filter2 for header byte 3.
CT_FILTH3_U2(7:0) Mask for filter 2 for header byte 3.

3.4.2.3 Byte 5 and 6 of Cell Type Filter 2 : Dword 2

CT_FILTU2_U2(15:8) Filter2 for UDF2.
CT_FILTU2_U2(7:0) Mask for filter UDF2.
CT_FILTU1_U2(15:8) Filter2 for UDF1.
CT_FILTU1_U2(7:0) Mask for filter 2 UDF1.

3.4.2.4 Byte 7 of Cell Type Filter 2 : Dword 3

Bit (15:0) Not used.
CT_FILTP1_U2(15:8) Filter2 for payload byte 1.
CT_FILTP1_U2(7:0) Mask for filter 2 for payload byte 1.

3.4.3 Register for Programmable Cell Type Filter 1 in Downstream

Dword	31 23	15 7 0
3	CT_FILTP1_D1(15:0)	
2	CT_FILTU1_D1(15:0)	CT_FILTU2_D1(15:0)
1	CT_FILTH3_D1(15:0)	CT_FILTH4_D1(15:0)
0	CT_FILTH1_D1(15:0)	C T_FILTH2_D1(15:0)

CMR(4:0) = 01110; write/read depicted data format to/from WDR0..3/RDR0..3 registers.

Note: Mask-bit:
'0' is don't care
'1' use Filter-bit for comparison.

3.4.3.1 Byte 1 and 2 of Cell Type Filter 1 : Dword 0

CT_FILTH2_D1(15:8) Filter1 for header byte 2.
CT_FILTH2_D1(7:0) Mask for filter 1 for header byte 2.
CT_FILTH1_D1(15:8) Filter1 for header byte 1.
CT_FILTH1_D1(7:0) Mask for filter 1 for header byte 1.

3.4.3.2 Byte 3 and 4 of Cell Type Filter 1 : Dword 1

CT_FILTH4_D1(15:8) Filter1 for header byte 4.
CT_FILTH4_D1(7:0) Mask for filter 1 for header byte 4.
CT_FILTH3_D1(15:8) Filter1 for header byte 3.
CT_FILTH3_D1(7:0) Mask for filter 1 for header byte 3.

3.4.3.3 Byte 5 and 6 of Cell Type Filter 1 : Dword 2

CT_FILTU2_D1(15:8) Filter1 for UDF2.
CT_FILTU2_D1(7:0) Mask for filter UDF2.
CT_FILTU1_D1(15:8) Filter1 for UDF1.
CT_FILTU1_D1(7:0) Mask for filter 1 UDF1.

3.4.3.4 Byte 7 of Cell Type Filter 1 : Dword 3

Bit (15:0) Not used.
CT_FILTP1_D1(15:8) Filter1 for payload byte 1.
CT_FILTP1_D1(7:0) Mask for filter 1 for payload byte 1.

3.4.4 Register for Programmable Cell Type Filter 2 in Downstream

Dword	31 23	15 7 0
3	CT_FILTP1_D2(15:0)	
2	CT_FILTU1_D2(15:0)	CT_FILTU2_D2(15:0)
1	CT_FILTH3_D2(15:0)	CT_FILTH4_D2(15:0)
0	CT_FILTH1_D2(15:0)	C T_FILTH2_D2(15:0)

CMR(4:0) = 01111; write/read depicted data format to/from WDR0..3/RDR0..3 registers.

Note: Mask-bit:
'0' is don't care
'1' use Filter-bit for comparison.

3.4.4.1 Byte 1 and 2 of Cell Type Filter 2 : Dword 0

CT_FILTH2_D2(15:8) Filter2 for header byte 2.
CT_FILTH2_D2(7:0) Mask for filter 2 for header byte 2.
CT_FILTH1_D2(15:8) Filter2 for header byte 1.
CT_FILTH1_D2(7:0) Mask for filter 2 for header byte 1.

3.4.4.2 Byte 3 and 4 of Cell Type Filter 2 : Dword 1

CT_FILTH4_D2(15:8) Filter2 for header byte 4.
CT_FILTH4_D2(7:0) Mask for filter 2 for header byte 4.
CT_FILTH3_D2(15:8) Filter2 for header byte 3.
CT_FILTH3_D2(7:0) Mask for filter 2 for header byte 3.

3.4.4.3 Byte 5 and 6 of Cell Type Filter 2 : Dword 2

CT_FILTU2_D2(15:8) Filter2 for UDF2.
CT_FILTU2_D2(7:0) Mask for filter UDF2.
CT_FILTU1_D2(15:8) Filter2 for UDF1.
CT_FILTU1_D2(7:0) Mask for filter 2 UDF1.

3.4.4.4 Byte 7 of Cell Type Filter 2 : Dword 3

Bit (15:0) Not used.
CT_FILTP1_D2(15:8) Filter2 for payload byte 1.
CT_FILTP1_D2(7:0) Mask for filter 2 for payload byte 1.

3.5 Port Configuration Registers

With these registers every port can be configured individually as UNI (User to Network Interface) with reduced 8 bit address range or NNI (Network to Network Interface) with full address range of up to 12 bit.

3.5.1 Port Configuration UNI (UNIPORTL)

Read/write Address $2E_H$
Value after reset 0000_H

15							8
UNI(15:8)							
7							**0**
UNI(7:0)							

UNI(15:0)

0 NNI-Port (i.e. up to 12 bits of VPI will be used for address reduction depending on the number of port number bits ⇒ see MODE register **Section 3.18.2,** page 112)

1 UNI-port (i.e. only 8 bit of VPI will be used for address reduction)

3.5.2 Port Configuration UNI (UNIPORTH)

Read/write Address $2F_H$
Value after reset 0000_H

15							8
unused							
7							**0**
UNI(23:16)							

unused(15:8) Fixed to zero.

UNI(23:16)

0 NNI-Port (i.e. up to 12 bits of VPI will be used for dress reduction depending on the number of port number bits ⇒ see MODE register **Section 3.18.2,** page 112)

1 UNI-port (i.e. only 8 bit of VPI will be used at address reduction)

3.6 CAME Data Registers

These registers are programmed with the full-length input address (PN / VPI / VCI) of 32 bit length which shall be assigned to the reduced LCI (Local Connection Identifier) of 14 bit length in the CAME.

3.6.1 CAMADRL

Read/write Address 32_H
Value after reset 0000_H

15	8
CAMADRL(15:8)	
7	**0**
CAMADRL(7:0)	

CAMADRL(15:0) Data (i.e. VCI) which is stored in the CAME under the address LCI specified in the ADR register. Responds of the CAME for the following CAME commands defined in CMR register (see **page 113**) :

00111 'read a line from the CAME ...'
01000 'write a line into the CAME ...'
01001 'write a line into the CAME and one entry to Connection ...'
01011 'CAME test ...'

3.6.2 CAMADRH

Read/write Address 33_H
Value after reset 0000_H

15	8
CAMADRH(15:8)	
7	**0**
CAMADRH(7:0)	

CAMADRH(15:0) Data (i.e. PN / VPI) which is stored in the CAME under the address LCI specified in the ADR register. Responds of the CAME for the following CAME commands defined in CMR register (see **page 113**) :

00111 'read a line from the CAME ...'
01000 'write a line into the CAME ...'
01001 'write a line into the CAME and one entry to Connection ...'

3.7 POLU Configuration Register

With P_CONR_L and P_CONR_H the POLU (Policing Unit) is configured for normal mode as well as for test modes. In the test mode 'Show selected policing values ...' the results are loaded in the registers P_STATR0 ... P_STATR2.

3.7.1 POLU Configuration Register (P_CONRL)

Read/write Address 36_H
Value after reset $00FF_H$

15				8
COM(9:2)				
7				**0**
COM(1:0)	TOM	INC COUNT INH(2:0)	DISC INH	TAG INH

Note: The contents of P_CONRL and P_CONRH will be transferred together to the POLU only if bit VALID_CONF in P_CONRH is set to 1!

COM(9:0) Only for Test. Don't change the contents for normal policing operation.

TOM

0 Normal Operation Mode.
1 Test Operation Mode (only for Testing).

INC COUNT INH(2:0)

0 The corresponding PH_INCR_COUNTER-pulse is suppressed for all connections.
1 The pulse is transmitted.

DISC INH

0 'Cell discard' indication is suppressed for all connections.
1 Cell discard enabled.

TAG INH

0 'Tag cell' indication is suppressed for all connections.
1 Tagging is enabled.

3.7.2 POLU Configuration Register (P_CONRH)

Read/write Address 37_H
Value after reset 0000_H

15							8
VALID_ CONF	COM(24:18)						
7							**0**
COM(17:10)							

Note: The contents of P_CONRL and P_CONRH will be transferred together to the POLU only if bit VALID_CONF in P_CONRH is set to 1!

VALID_CONF

0 The content of the register has already been transferred to the POLU.
1 The register has been written into by the µP, but it has *not* been synchronized by the POLU yet.

COM(24:10) Only for Test. Don't change the contents for normal policing operation.

3.8 Version Register

The Version register provides a Version number for system management purposes. The Version number is identical with the boundary scan ID code.

3.8.1 VERL

Read Address 40_H
Value after reset 9069_H

15	8
VERL(15:8)	
7	**0**
VERL(7:0)	

VERL(15:0) Version of the ATM-LP (low part): 1001 0000 0110 1001

3.8.2 VERH

Read Address 41_H
Value after reset $523B_H$

15	8
VERH(15:8)	
7	**0**
VERH(7:0)	

VERH(15:0) Version of the ATM-LP (high part): 0101 0010 0011 1011

3.9 Transmit Cell Registers 0..26 (TXR0..26)

These are registers used by µP to insert a cell into the cell flow upstream or downstream.

3.9.1 Transmit Cell Register 0 (TXR0)

Read/write Address 50_H
Value after reset 0000_H

15	8
word0(15:8)	
7	**0**
word0(7:0)	

word0(15:0) Upstream with header translation:
UNI: GFC[3:0] / VPI[7:0] / VCI[15:12]
NNI: VPI[11:0] / VCI[15:12]
Upstream without header translation:
LCI[11:0] / VCI[15:12]
Downstream with header translation:
LCI[11:0] / VCI[15:12]
Downstream without header translation:
UNI: GFC[3:0] / VPI[7:0] / VCI[15:12]
NNI: VPI[11:0] / VCI[15:12]

3.9.2 Transmit Cell Register 1 (TXR1)

Read/write Address 51_H
Value after reset 0000_H

15	8
word1(15:8)	
7	**0**
word1(7:0)	

word1(15:0) VCI[11:0] / PTI[2:0] / CLP

3.9.3 Transmit Cell Register 2 (TXR2)

Read/write Address 52_H
Value after reset 0000_H

15							8
word2(15:8)							
7							**0**
word2(7:0)							

word2(15:0) Upstream without header translation:
LCI[13:12] / HK[2:0] / unused[4:0] / E / PNUT[4:0]
Upstream with header translation:
unused[1:0] / PNPHY[5:0](*) / unused[1:0] / E / PNUT[4:0](*)
Downstream without header translation:
unused[1:0] / PNPHY[5:0] / unused[1:0] / E / PNUT[4:0]
Downstream with header translation:
LCI[13:12] / unused[7:0] / E / PNUT[4:0] :

E
Error Detection Code (CRC10):
0 No action.
1 Perform EDC.

PNUT[4:0]
Absolute port number UTOPIA.

PNPHY[5:0]
Port number of PHY-device:
0..63 For AN applications.
0..7 For PADACK applications.

Note: (*) PN-source as programmed in MODE-register.

3.9.4 Transmit Cell Registers 3..26 (TXR3..TXR26)

Read/write Address 53_H...$6A_H$
Value after reset 0000_H (for all)

Addr.	Name	15 8	7 0
53	TXR3	Payload byte 0	Payload byte 1
54	TXR4	Payload byte 2	Payload byte 3
55	TXR5	Payload byte 4	Payload byte 5
56	TXR6	Payload byte 6	Payload byte 7
57	TXR7	Payload byte 8	Payload byte 9
55	TXR8	Payload byte 10	Payload byte 11
59	TXR9	Payload byte 12	Payload byte 13
5A	TXR10	Payload byte 14	Payload byte 15
5B	TXR11	Payload byte 16	Payload byte 17
5C	TXR12	Payload byte 18	Payload byte 19
5D	TXR13	Payload byte 20	Payload byte 21
5E	TXR14	Payload byte 22	Payload byte 23
5F	TXR15	Payload byte 24	Payload byte 25
60	TXR16	Payload byte 26	Payload byte 27
61	TXR17	Payload byte 28	Payload byte 29
62	TXR18	Payload byte 30	Payload byte 31
63	TXR19	Payload byte 32	Payload byte 33
64	TXR20	Payload byte 34	Payload byte 35
65	TXR21	Payload byte 36	Payload byte 37
66	TXR22	Payload byte 38	Payload byte 39
67	TXR23	Payload byte 40	Payload byte 41
68	TXR24	Payload byte 42	Payload byte 43
66	TXR25	Payload byte 44	Payload byte 45
6A	TXR26	Payload byte 46	Payload byte 47

3.9.5 Configuration of Transmit Cell Buffer (TXR_CONFIG)

Read/write Address $6B_H$
Value after reset 0000_H

15							8
unused							
7							**0**
unused					TRANSM_ DIR	HTON	START _TR

unused(15:3) Fixed to zero.

TRANSM_DIR

0 Transmit a cell upstream.
1 Transmit a cell downstream.

HTON

0 Without header translation.
1 Header translation on.

START_TR

0 No action.
1 Start transmission from transmit cell buffer TXR (this bit is reset by the ASIC after transmission).

Note: It is strongly recommended not to start the transmission upstream while the UTRXFIFO_OV_U-bit is set to 1 (input queue overflow of UTOPIA receive upstream interface)!
It is strongly recommended not to start the transmission downstream while the BOV-bit of ISR0 or the UT_QOV-bit of the corresponding port is set to 1 (buffer/queue overflow of statistical demultiplexing buffer in UTOPIA transmit downstream interface)!

3.10 Receive Register/Receive Cell Buffer (RXR)

Read Address 70_H
Value after reset undefined

15							8
word n(15:8)							
7							**0**
word n(7:0)							

This 16 bit read-only register is used for access to the Receive Cell Buffer. There is one common Receive Cell Buffer for up- and downstream direction that can store 12 cells at maximum. With RXR the Receive Cell Buffer is read in the order octet number 0 to octet number 55.

Note: Cells with header translation, inserted by the µP via Transmit Cell Buffer, can directly be dropped to Receive Cell Buffer.
Cells without header translation, inserted by the µP via Transmit Cell Buffer, cannot be dropped to Receive Cell Buffer. However for test purposes this can be achieved by directly forwarding a cell from TXR to RXR using bit 13 of register TESTR (LOOP_TXRX).

word 0(15:8) Upstream:
UNI: GFC[3:0] / VPI[7:4]
NNI: VPI[11:4]
Downstream:
LCI[11:4]

word 0(7:0) Upstream:
VPI[3:0] / VCI[15:12]
Downstream:
LCI[3:0] / VCI[15:12]

word 1(15:8) VCI[11:4]

word 1(7:0) VCI[3:0] / PTI[2:0] / CLP

word 2(15:8) Upstream:
Unused[1:0] / PNPHY[5:0].
Downstream:
LCI[13:12] / HK[2:0] / unused[2:0].
PNPHY[5:0]
Port number of PHY-device:
0..63 For AN applications.

Note: PNPHY[2:0] represents the port number of IWE8 in upstream direction.

word 2(7:0) Unused[1:0] / D / PNUT[4:0]
D
Direction:
0 Downstream
1 Upstream
PNUT[4:0]
Absolute port number UTOPIA.

word 3(15:8) Payload byte 0.

word 3(7:0) Payload byte 1.

... ...

word 26(15:8) Payload byte 46.

word 26(7:0) Payload byte 47.

word 27(15:8) CELLTYPE[5:0] / unused[1:0]
CELLTYPE[5:2]

0000	User cell.
0001	RM (Resource Management) cell.
0010	PCF1 (extracted by Programmable Cell Filter 1) cell.
0011	PCF2 (extracted by Programmable Cell Filter 2) cell.
0100	F5RES (F5 reserved for future functions with PTI=111) cell (only downstream).
0101	COC (cross office check) cell (only downstream).
0111	DBA (dynamic bandwidth allocation) cell.
1000	AIS (alarm indication signal) cell.
1001	RDI (remote defect indication) cell.
1010	CCA (continuity check activation) cell.

	1011	CC (continuity check) cell.
	1100	LB (loop back) cell.
	1111	Undef (undefined oamtype) cell.
	CELLTYPE[1]	
	0	Seg (segment) cell
	1	Ete (end_to_end) cell
	CELLTYPE[0]	
	0	F4 (virtual path) cell
	1	F5 (virtual channel) cell
word 27(7:0)	Unused[7:0]	

3.11 Header Capture/Protocol Monitoring Register Set 0 ... 3 Upstream

For the upstream direction 4 Protocol Monitoring Register sets are provided, one for each CLAV/ ENABLE-group.
At the ports specified in the HEADCAPEN-register always the header of the last cell discarded due to 'ATM cell header error' is logged in the corresponding PRMONR-buffer. Additionally the flag HLOG in the STATR-register is set. During readout of one PRMONR-buffer the buffer is locked. So every readout of a PRMONR-buffer has to be completed!

3.11.1 Protocol Monitoring Buffer 0...3 Upstream (PRMONR0A_U..3A_U)

Read Address $72_{H,}$ 75_{H}, 78_{H}, $7B_{H}$
Value after reset 0000_{H}

15							8
UDF1(7:0)							
7							**0**
UDF2(7:0)							

UDF1(7:0)	User Defined Byte1 (unused[1:0] / PNPHY[5:0]).
UDF2(7:0)	User Defined Byte2 (CLAV-group[1:0] / 1 / PNUT[4:0]).

3.11.2 Protocol Monitoring Buffer 0...3 Upstream (PRMONR0B_U..3B_U)

Read Address $73_{H,}$ 76_{H}, 79_{H}, $7C_{H}$
Value after reset 0000_{H}

15							8
VCI(11:4)							
7							**0**
VCI(3:0)				PTI(2:0)			CLP

VCI(11:0)	Virtual Channel Identifier
PTI(2:0)	Payload Type Identifier
CLP	Cell Loss Priority

3.11.3 Protocol Monitoring Buffer 0...3 Upstream (PRMONR0C_U..3C_U)

Read Address $74_{H,}$ 77_{H}, $7A_{H}$, $7D_{H}$
Value after reset 0000_{H}

15	8
GFC(3:0) / VPI(11:8)	VPI(7:4)
7	**0**
VPI(3:0)	VCI(15:12)

GFC(3:0)/VPI(11:8) At UNI: Generic Flow Control (GFC)
At NNI: Virtual Path Identifier (VPI)

VPI(7:0) Virtual Path Identifier

VCI(15:12) Virtual Channel Identifier

3.12 Header Capture/Protocol Monitoring Register Set Downstream

For the downstream direction only 1 Protocol Monitoring Register set is provided for all CLAV/ ENABLE-groups.
The header of cells discarded due to 'internal cell header error' is logged in the PRMONR-buffer. Additionally the flag HLOG in the STATR-register is set. During readout of one PRMONR-buffer the buffer is locked. So every readout of the PRMONR-buffer has to be completed!

3.12.1 Protocol Monitoring Buffer 0 Downstream (PRMONRA_D)

Read Address $7E_{H}$
Value after reset 0000_{H}

15	8
UDF1(7:0)	
7	**0**
UDF2(7:0)	

UDF1(7:0) User defined field 1:
7:6 Two MSBits of Local Connection Identifier (LCI (13:12)).
5:3 HK Bits.

UDF2(7:0) Port number from UTOPIA Rx downstream:
4:0 PN_UT_DN(4:0).

3.12.2 Protocol Monitoring Buffer Downstream (PRMONRB_D)

Read Address $7F_H$
Value after reset 0000_H

15							8
VCI(11:4)							
7							**0**
VCI(3:0)				PTI(2:0)			CLP

VCI(11:0) Virtual Channel Identifier.
PTI(2:0) Payload Type Identifier.
CLP Cell Loss Priority.

3.12.3 Protocol Monitoring Buffer Downstream (PRMONRC_D)

Read Address 80_H
Value after reset 0000_H

15							8
LCI(11:4)							
7							**0**
LCI(3:0)				VCI(15:12)			

LCI(11:0) Local Connection Identifier.
VCI(15:12) Virtual Channel Identifier.

3.13 Protocol Monitoring Configuration Register (HEADCAPEN)

Read/write Address 81_H
Value after reset 0000_H

15							8
unused							
7							**0**
unused			EN_D	EN3_U	EN2_U	EN1_U	EN0_U

This register enables/disables the Protocol Monitoring Sets upstream and downstream.

unused(10:0) Fixed to zero.

EN_D

0 Disables capturing of cells from Clav-group 0-3 in register PRMONR_D.

1 Enables capturing of cells from Clav-group 0-3 in register PRMONR_D.

EN3_U

0 Disables capturing of cells from CLAV-group3 in register PRMONR3_U.

1 Enables capturing of cells from CLAV-group3 in register PRMONR3_U.

EN2_U .

0 Disables capturing of cells from CLAV-group2 in register PRMONR2_U.

1 Enables capturing of cells from CLAV-group2 in register PRMONR2_U.

EN1_U

0 Disables capturing of cells from CLAV-group1 in register PRMONR1_U.

1 Enables capturing of cells from CLAV-group1 in register PRMONR1_U.

EN0_U

0 Disables capturing of cells from CLAV-group0 in register PRMONR0_U.

1 Enables capturing of cells from CLAV-group0 in register PRMONR0_U.

3.14 Configuration of Portspecific Counters Upstream

The portspecific counters are stored in an ASIC internal RAM. The contents of this RAM are not affected by a SW-reset. Every counter has 32 bit length. In case of an overflow the counters remain on the maximum count value of ‘FFFF’.

For each port0 .. 15 a ‘total incoming cell (POTIC)’-counter is provided, while port16 .. 23 don’t have a ‘total incoming cell’-counter.

Additionally eight port specific countersets with special counters are provided which can be assigned to any port by the registers PORTCONF0 .. 7_U.

If two of these eight countersets are configured to count cells from the same port only the counterset with the lower number will be active.

3.14.1 Port Specific Counter Configuration Upstream (PORTCONF0_U..7_U)

Read/write Address 84...8B$_H$
Value after reset 0000$_H$

15				8
unused		CNT_POTICOR_ALL	CNT_POTIC	OAM_CNT_U

7			0
CNT_POTICOR	CNT_PORTENi_U	CNT_PORTi_U(5:0)	

Note: PDC_Ci: Total discarded cells due to unallocated PN / VPI / VCI at port i.
POTICN_Ci: Total incoming cells with non-zero-GFC-field at port i.
POTIC_Ci: Total incoming cells at port i.
POTICOR_Ci: Total incoming OAM/RM cells at port i. By the flag INC_TIMC_SSD (word0, bit15 of Connection RAM upstream) this counter can be connection specifically enabled.

unused(4:0) Fixed to zero.

CNT_POTICOR_ALL Define the number of connections which are counted:

0 Counts cells in POTICOR_Ci for specific connections enabled by the flag INC_TIMC_SSD in the connection RAM.

1 Counts cells in POTICOR_Ci for all connections independently of flag INC_TIMC_SSD in the connection RAM.

CNT_POTIC

0 Disables the POTIC_Ci counter.

1 Enables the POTIC_Ci counter.

OAM_CNT_U Configures the POTICOR counter:

0 Count RM cells in POTICOR_Ci.

1 Count OAM cells in POTICOR_Ci.

CNT_POTICOR

0 Disables the POTICOR_Ci counter.

1 Enables the POTICOR_Ci counter.

CNT_PORTENi_U

0 Disables the counters PDC_Ci and POTICN_Ci.

1 Enables the counters PDC_Ci and POTICN_Ci.

CNT_PORTi_U(5:0)

Upstream portnumber of the port at which cells will be counted in the counters: PDC_Ci, POTICN_Ci, POTIC_Ci, POTICOR_Ci.

3.14.2 ENPOTIC

Read/write Address $8C_H$
Value after reset 0000_H

15							8
ENPOTIC(15:8)							
7							**0**
ENPOTIC(7:0)							

Note: POTIC: Total incoming cells.

ENPOTIC(15:0) Enables counter POTIC at port 0-15.

3.15 Configuration of Portspecific Counters Downstream

The portspecific counters are stored in an ASIC internal RAM. The contents of this RAM are not affected by a SW-reset. Every counter has 32 bit length. In case of an overflow the counters remain on the maximum count value of ‘FFFF’.

For each port0 .. 15 a ‘total incoming cell’-counter is provided, while port16 .. 23 have no ‘total incoming cell’-counter.

Additionally eight port specific countersets with special counters are provided which can be assigned to any port by the registers PORTCONF0 .. 7_D.

If two of these eight countersets are configured to count cells from the same port only the counterset with the lower number will be active.

3.15.1 PORTCONF0_D ... 7_D

Read/write Address $8D_H...94_H$
Value after reset 0000_H

15							8
unused					CNT_POTOCOR_ALL	CNT_POTOC	OAM_CNT_D(1)

7							0
OAM_CNT_D(0)	unused						CNT_PORTi_D(5:0)

Note: POTOC_Ci: Total outgoing cells at port i.
POTOCOR_Ci: Total outgoing OAM/RM/discarded F5RM cells at port i. By the flag INC_TOF5RMC_SSD (word0, bit15 of Connection Ram downstream) this counter can be connection specifically enabled.

unused(5:1) Fixed to zero.

CNT_POTOCOR_ALL

0 Counts cells in POTOCOR_Ci counter for specific connections enabled by the flag INC_TOF5RMC_SSD or INC_TOMC_SSD in the connection RAM. INC_TOF5RMC_SSD is evaluated if discarded F5RM and PTI (111) cells are counted in the POTOCOR_Ci counter. INC_TOMC_SSD is evaluated if OAM or RM cells are counted in the POTOCOR_Ci counter

1 Counts cells in POTOCOR_Ci counter for all connections independently of flag INC_TOF5RMC_SSD or INC_TOMC_SSD in the connection RAM.

CNT_POTOC

0 Disables the POTOC_Ci counter.

1 Enables the POTOC_Ci counter.

OAM_CNT_D(1:0) Configures and enables the POTICOR counter:

00	Disables the POTOCOR_Ci counter.
01	Counts OAM cells and enables the POTOCOR_Ci counter.
10	Counts RM cells and enables the POTOCOR_Ci counter.
11	Counts discarded F5RM and PTI(111) cells and enables the POTOCOR_Ci counter.

unused(0) Not fixed.

CNT_PORTi_D(5:0)

Downstream portnumber of the port at which cells will be counted in the counters: POTOC_Ci, POTOCOR_Ci.

3.15.2 ENPOTOC

Read/write Address 95_H
Value after reset 0000_H

15							8
ENPOTOC(15:8)							
7							**0**
ENPOTOC(7:0)							

ENPOTOC(15:0) Enables counter POTOC at port 15..0.

3.16 UTOPIA Configuration Registers

With these registers the enabling/disabling and the mode of all ATM-LP UTOPIA interfaces (UTRXU, UTTXU, UTRXD, UTTXD) is configured.

3.16.1 UTOPIA Configuration (CONUT1A)

Read/write Address 96_H
Value after reset 0000_H

15							8
UT_PORT_U(15:8)							
7							**0**
UT_PORT_U (7:0)							

UT_PORT_U(15:0)

0	Disables UTOPIA port 15..0 upstream.
1	Enables UTOPIA port 15..0 upstream.

3.16.2 UTOPIA Configuration (CONUT1B)

Read/write Address 97_H
Value after reset 0000_H

15							8
UT_PORT_D (23:16)							
7							**0**
UT_PORT_U (23:16)							

UT_PORT_D(23:16)

0	Disables UTOPIA port 23..16 downstream.
1	Enables UTOPIA port 23..16 downstream.

UT_PORT_U(23:16)

0	Disables UTOPIA port 23..16 upstream.
1	Enables UTOPIA port 23..16 upstream.

3.16.3 UTOPIA Configuration (CONUT1C)

Read/write Address 98_H
Value after reset 0000_H

15							8
UT_PORT_D(15:8)							
7							**0**
UT_PORT_D (7:0)							

UT_PORT_D(15:0)

0	Disables UTOPIA port 15..0 downstream.
1	Enables UTOPIA port 15..0 downstream.

3.16.4 UTOPIA Configuration (CONUT2)

Read/write Address 99_H
Value after reset 0000_H

15					8
UTP_ 16BIT	UTP_ PAR	UTP_CONFIG(1:0)	UTA_ 16BIT	UTA_ PAR	UTA_CONFIG(1:0)
7					**0**
unused					

UTP_16BIT

0	8bit data bus at PHY side.
1	16bit data bus at PHY side.

UTP_PAR

0	Don’t check parity of PHY receive data.
1	Check parity of PHY receive data.

UTP_CONFIG(1:0)

Configuration of mode at PHY side:

00	4 x 6 port
01	3 x 8 port
10	2 x 12 port
11	UTOPIA Level 1 (4 x 1 port)

UTA_16BIT

0	8bit data bus at ATM side.
1	16bit data bus at ATM side.

UTA_PAR

0	Don’t check parity of ATM receive data.
1	Check parity of ATM receive data.

UTA_CONFIG(1:0)

Configuration of mode at ATM side:

00	4 x 6 port
01	3 x 8 port
10	2 x 12 port
11	UTOPIA Level 1 (4 x 1 port)

unused(7:0) Fixed to zero.

3.16.5 UTOPIA Configuration (CONUT3)

Read/write Address $9A_H$
Value after reset $003F_H$

15		8
FORCE_ EC_D	EC_MININT_D(6:0)	

7		0
UT_VPN	unused	UT_THRESH(5:0)

FORCE_EC_D

0 No forcing of Empty Cycles downstream.
1 Force Empty Cycles downstream.

EC_MININT_D(6:0)

Minimal interval (in cell cycles) between 2 Empty Cycles downstream. This bit is only valid if FORCE_EC_D is equal one.

UT_VPN

0 Don’t change incoming port number.
1 Change incoming port number 0 to1 (can be used to switch between two LCI ranges for redundancy purposes).

unused Fixed to zero.

UT_THRESH(5:0)

Queue threshold of UTOPIA demultiplexing buffer (each queue has the same threshold).

3.17 UTOPIA Downstream Queue Overflow Indication Registers

If a queue overflow occurs in the statistical demultiplexing buffer downstream, an UTOPIA backpressure is generated for the preceding ASIC so that no further cells will be accepted. Cells for this queue that are already inside the ATM-LP (UTOPIA input buffer or workbench) will be still added to the queue so that blocking will be avoided.

3.17.1 UT_QOV1

Read Address $9B_H$
Value after reset 0000_H

Note: Single bits of this register are resettable by writing a '1' to them.

15							8
QOV(15:8)							
7							**0**
QOV (7:0)							

QOV(15:0)

0	No queue overflow of port 15..0 at UTOPIA downstream PHY-side.
1	Queue overflow of port 15..0 at UTOPIA downstream PHY-side.

3.17.2 UT_QOV2

Read Address $9C_H$
Value after reset 0000_H

Note: Single bits of this register are resettable by writing a '1' to them.

15							8
unused							
7							**0**
QOV (23:16)							

unused(7:0) Fixed to zero.

QOV(23:16)

0	No queue overflow of port 23..16 at UTOPIA downstream PHY-side.
1	Queue overflow of port 23..16 at UTOPIA downstream PHY-side.

3.18 Configuration of Header Translation/Special Enable Bits

These registers configure the header translation (CAME or internal address reduction, number of portnumber bits), select the port number source and provide two special Enable bits, one to enable all traffic measurement counters and the other to enable write access to the registers TESTR and BISTMODE1/2.

3.18.1 ADRED_VPIM

Read/write Address $9E_H$
Value after reset 0000_H

15							8
unused							VPIMIN(11:8)
7							**0**
VPIMIN(7:0)							

unused(3:0) Fixed to zero.

VPIMIN(11:0) Minimal VPI used in address reduction algorithm without CAME (only valid if bit CAM in MODE register is set to 1).

3.18.2 MODE

Read/write Address $9F_H$
Value after reset 0000_H

15							8
unused		TESTR_EN	COUNTEN	PN_SOURCE_D	PN_SOURCE_U	unused	
7							**0**
M_NUMB(3:0)				P_NUMB(2:0)			CAM

unused(3:2) Fixed to zero.

TESTR_EN

0 The write access to TESTR-register and BIST-register is disabled.
1 The TESTR-register and the BIST-register are writable.

COUNTEN

0 All traffic measurement counters will be stopped.
1 All traffic measurement counters will be enabled.

PN_SOURCE_D Source of the portnumber downstream:

0 Connection RAM (CONNRAMDO)
1 UTOPIA

PN_SOURCE_U Source of the portnumber upstream:

0 UTOPIA
1 UDF1(5:0)

unused(1:0) Fixed to zero.

M_NUMB(3:0) Block size parameter (only valid if bit CAM=1).

Note: In case of address reduction without CAME P_NUMB=M_NUMB or M_NUMB=0 leads to a CAM_ERR interrupt and all cells (upstream) will be discarded!

P_NUMB(2:0) Number of portnumber bits which are mapped into the LCI (if bit CAM=1) or PN / VPI / VCI supplied to CAME (if CAM=0;
Remark: P_NUMB = 7, 6, 5 leads to CAM_ERR interrupt, only P_NUMB = 6, 5, 4, 3, 2, 1, 0 is allowed !).

CAM

0 Address reduction with external Address Reduction Circuit (CAME device PXB 4360 E).
1 Address reduction with internal Address Reduction Circuit.

3.19 Command Register (CMR)

Read/write Address $A0_H$
Value after reset 0000_H

15			8
SWRESET(3:0)			unused
7			**0**
unused	STREQ	READONLY	MPREQDEF(4:0)

The command register provides and controls all kinds of possible µP requests.

SWRESET(3:0)

0110 Software reset (leads to an internal active low reset pulse).

Note: The whole ASIC (including registers and UTOPIA interfaces) is reset. Only the contents of the internal RAMs (portspecific counters, RWR-buffer, RXR-buffer) are not affected.

unused(3:0) Fixed to zero.

STREQ

0 Unspecified.
1 Start of the specified request (the STREQ bit is reset by the ASIC when the command is finished).

READONLY

0 Write the specified data.
1 Read the specified data.

MPREQDEF(4:0) MP-request definition:

00000 Read or write one entry from/to POLU RAM using the LCI in the ADR register.
00001 Read or write one entry from/to connection RAM upstream using the LCI in the ADR register. (**Remark:** at write accesses the new LCI2 (defined in WDR0) is used to address VP specific data).
00010 Read or write one entry from/to connection RAM downstream using the LCI in the ADR register (**Remark:** at write accesses the new LCI2 (defined in WDR0) is used to address VP specific data).

00011	Read or write one entry from/to port table upstream using the ADR register (see Appendix 1: Addressing of Port Table counters upstream).
00100	Read or write one entry from/to port table downstream using the ADR register (see Appendix 1: Addressing of Port Table counters downstream).
00101	Read or write cell type filter 1 upstream (see Appendix 2: Structure/ Transmission Order of Cell Type Filters (x=U, y=1)).
00110	Read or write cell type filter 2 upstream (see Appendix 2: Structure/ Transmission Order of Cell Type Filters (x=U, y=2)).
00111	Read a line from the CAME using the LCI in the ADR register, the VCI in CAMADRL and the PN/VPI in CAMADRH (not VCON and P_IP, see page 3-77, <HLink>79, <HLink>130 and <HLink>138).
01000	Write a line in the CAME using the LCI in the ADR register, the VCI in CAMADRL and the PN/VPI in CAMADRH.
01001	Write a line into the CAME and one entry to connection RAM upstream using the LCI in the ADR register, the VCI in CAMADRL and the PN/VPI in CAMADRH.
01010	Not used.
01011	CAME test using ADR register for CAME test configuration and CAMADRL register for CAME test result (see [9]).
01100	Transfer UPC/NPC parameters from the POLURAM to the POLU Register File using the LCI in the ADR register. Only for test purpose.
01101	Transfer updated UPC/NPC parameters from the POLU Register File to the POLURAM using the LCI in the ADR register. Only for test purpose.
01110	Read or write cell type filter 1 downstream (see Appendix 2: Structure/Transmission Order of Cell Type Filters (x=D, y=1)).
01111	Read or write cell type filter 2 downstream (see Appendix 2: Structure/Transmission Order of Cell Type Filters (x=D, y=2)).

3.20 Status Registers for Header Capture/CAME

3.20.1 Status Register for Header Capture (STATR)

Read Address $A1_H$
Value after reset 0000_H

15					8
unused					
7					**0**
unused	PMO_ HLOG_D	PMO_ HLOG3_U	PMO_ HLOG2_U	PMO_ HLOG1_U	PMO_ HLOG0_U

The STATR register provides the status of all Protocol Monitoring Sets upstream and downstream.

unused(10:0) Fixed to zero.

PMO_HLOG_D

0 No external header has been written to PRMONR_D.
1 Indication that downstream an external header has been written to PRMONR_D. The bit is reset by the ATM-LP after the completion of µP read access to PRMONR_D.

PMO_HLOG3_U

0 No external header has been written to PRMONR3_U.
1 Indication that for a cell from CLAV-group 3 upstream an external header has been written to PRMONR3_U. The bit is reset by the ATM-LP after the completion of µP read access to PRMONR3_U.

PMO_HLOG2_U

0 No external header has been written to PRMONR2_U.
1 Indication that for a cell from CLAV-group 2 upstream an external header has been written to PRMONR2_U. The bit is reset by the ATM-LP after the completion of µP read access to PRMONR2_U.

PMO_HLOG1_U

0 No external header has been written to PRMONR1_U.
1 Indication that for a cell from CLAV-group 1 upstream an external header has been written to PRMONR1_U. The bit is reset by the ATM-LP after the completion of µP read access to PRMONR1_U.

PMO_HLOG0_U

0 No external header has been written to PRMONR0_U.
1 Indication that for a cell from CLAV-group 0 upstream an external header has been written to PRMONR0_U. The bit is reset by the ATM-LP after the completion of µP read access to PRMONR0_U.

3.20.2 Status Register for CAME (CSTATR)

Read Address $A2_H$
Value after reset 0000_H

15	8
unused	

7	0
unused	STATUS(3:0)

The CSTATR register provides the CAME status after configuration by µP via CMR register.

unused(11:0) Fixed to zero.

STATUS(3:0) Status delivered from the CAME after µP requests:
STATUS[3:2] =
- 00 Ok (STATUS[1:0]=00)
- 01 Busy (STATUS[1:0]=00)
- 10 Alarm:
  STATUS[1:0] =
  - 00 Mismatch (at search requests).
  - 01 Multimatch (at search requests).
  - 10 Test search fault (at search requests).
  - 00 Refused entry (at write request).
  - 01 Refused line (at write request).
  - 00 Test read fault (at read request).
- 11 Error:
  STATUS[1:0] =
  - 00 Address/data bus parity error.
  - 01 Cascade error.
  - 10 Command cycle error.

3.21 Interrupt Status Registers/Interrupt Mask Registers

The interrupt status registers store potential interrupt causes that occurred. The coding is as follows:

0: no interrupt cause

1: interrupt cause occurred.

Each interrupt status bit can be reset individually by writing a logical 1 to it. The only exception is the interrupt status bit RXR_USTR (ISR1, bit9) which is reset automatically. A microprocessor interrupt is only generated if the corresponding interrupt mask bit is set to 1.

3.21.1 Interrupt Status Register (ISR0)

Read Address $A3_H$
Value after reset 0000_H

Note: Single bits of this register are resettable by writing a '1' to them.

15							8
unused				UTRXFIFO_OV_U	CTY_DIS_D	CTY_DIS_U	QOV
7							**0**
BOV	PMO_HLOG	unused	UT_CELL ERR_D	UT_PAR ERR_D	RXR_OV	UT_CELL ERR_U	UT_PAR ERR_U

unused(4:1) Fixed to zero.

UTRXFIFO_OV_U

1 Overflow of UTOPIA receive interface cell buffer upstream.
This interrupt is generated when the 4 cell deep UTOPIA receive interface FIFO is full and a backpressure to the PHY device is generated.

CTY_DIS_D

1 Any cell discarded due to cell type recognition downstream.

CTY_DIS_U

1 Any cell discarded due to cell type recognition upstream.

QOV

1 Overflow of one or more UTOPIA cell queues downstream (demultiplexing buffer) at PHY-side.
This interrupt is generated for any port when the queue threshold (UT_THRESH[5:0] in register CONUT3) is reached. After the interrupt a backpressure signal is generated for the affected port. All cells for this port that are already inside the ASIC will still be stored in the queue so that blocking of the ASIC is avoided.
There is no queuespecific backpressure to the microprocessor TXR-buffer. The SW is responsible that cells are not written to a queue in overflow state.

BOV

1 Overflow of UTOPIA cell buffer downstream (demultiplexing buffer) at PHY-side.
This interrupt is generated when the 63rd cell is stored in the demultiplexing buffer (capacity 64 cells). For subsequent cells a backpressure signal will be generated so that no cells will be lost inside the ASIC.

PMO_HLOG

1 Indication that one or more cell header have been logged in the PRMONR-register sets (see STATR-register **Section 3.20.1,** page 115).

unused(0) Fixed to zero.

UT_CELLERR_D

1 Start of cell error or cell length error at UTOPIA receive interface downstream.
Start of cell error: the SOC-pulse is not generated although the partner device has reported to send a cell and the Enable signal has been asserted by the ASIC.
Cell length error: an additional SOC-pulse is generated during the running cell transfer.

UT_PARERR_D

1 Data parity error at UTOPIA receive interface downstream.

RXR_OV

1 Receive cell buffer overflow.
This interrupt is generated after the 1st RXR-cell is discarded because the RXR-buffer is full (capacity 12 cells).

UT_CELLERR_U

1 Start of cell or cell length error at UTOPIA receive interface upstream.
Start of cell error: the SOC-pulse is not generated although the PHY device has reported to send a cell and has been enabled by the ASIC.
Cell length error: an additional SOC-pulse is generated during the running cell transfer.

UT_PARERR_U

1 Data parity error at UTOPIA receive interface upstream.

3.21.2 Interrupt Status Register (ISR1)

Read Address $A4_H$
Value after reset 0000_H

Note: Single bits of this register are resettable by writing a '1' to them.

15							8
unused			POLVLD_ERR	VLD_ERR_D	VLD_ERR_U	RXR_USTR	unused
7							**0**
EDC_ERR_D	EDC_ERR_U	CAM_ERR	unused	POLU_PARERR_U	RAM_PARERR_D	RAM_PARERR_U	unused

unused(5:3) Fixed to zero.

POLVLD_ERR

1 Connection not valid in POLU-RAM upstream.The cell header will not be written to PRMONR0..3_U.

VLD_ERR_D

1 Connection not valid in connection RAM downstream.
This interrupt is generated if the VCON_DO flag of a connection (bit22 of word0 of a connection entry in connection RAM downstream) is not set.
The cell header will be written to PRMONR_D if possible (see PRMONR **Section 3.12.1,** page 102) and the interrupt PMO_HLOG is set.

VLD_ERR_U

1 Connection not valid in connection RAM upstream.
This interrupt is generated if the VCON_UP flag of a connection (bit19 of word0 of a connection entry in connection RAM upstream) is not set.

RXR_USTR

1 Cell stored in RXR-buffer.
This bit is set until all cells (12 cells maximum) are read out by the mP and is afterwards reset automatically.

unused(2) Fixed to zero.

EDC_ERR_D

1 EDC (CRC10) error in an OAM cell from UTOPIA receive interface downstream.
The interrupt is only generated if OAM cell processing is enabled (see bit0 OAM_EN of register DCT_CONFIG **Section 3.24.2,** page 127).

EDC_ERR_U

1 EDC (CRC10) error in an OAM cell from UTOPIA receive interface upstream.
The interrupt is only generated if OAM cell processing is enabled (see bit0 OAM_EN of register UCT_CONFIG **Section 3.24.1,** page 125).

CAM_ERR

1 Error during address reduction in CAME.
The affected cell is discarded. All internal errors in the CAME are reported by this interrupt flag. Additionally the status flags from the CAME are written to CSIR register.
The cell header will be written to PRMONR0..3_U if possible (see PRMONR **Section 3.11.1,** page 101) and the interrupt PMO_HLOG is generated.

unused(1) Fixed to zero.

POLU_PARERR_U

1 Error at the RAM interface upstream during a read access from the external POLU RAM. The cell header will not be written to PRMONR0 .. 3_U.

RAM_PARERR_D

1 Error at the RAM interface downstream during a read access from the external Connection RAM downstream. During a cell cycle the corresponding cell is discarded.
The cell header will be written to PRMONR_D if possible (see PRMONR **Section 3.12.1,** page 102) and the interrupt PMO_HLOG is generated.

RAM_PARERR_U

1 Error at the RAM interface upstream during a read access from the external Connection RAM upstream. During a cell cycle the corresponding cell is discarded.
The cell header will not be written to PRMONR0 .. 3_U.

unused(0) Fixed to zero.

3.21.3 Interrupt Mask Register (IMR0)

Read/write Address $A5_H$
Value after reset 0000_H

15							8
unused				MUTRXFIFO_OV_U	MCTY_DIS_D	MCTY_DIS_U	MQOV
7							**0**
MBOV	MPMO_HLOG	unused	MUT_CELLERR_D	MUT_PARERR_D	MRXR_OV	MUT_CELERR_U	MUT_PARERR_U

For every interrupt status bit the corresponding interrupt mask bit is provided (IMR0 for ISR0). The interrupt mask bit controls whether the setting of an interrupt status bit leads to a microprocessor interrupt (activation of the interrupt line MPINT_N).

unused(4:1) Fixed to zero.

MUTRXFIFO_OV_U
- 0 Microprocessor interrupt is disabled.
- 1 Microprocessor interrupt is enabled.

MCTY_DIS_D
- 0 Microprocessor interrupt is disabled.
- 1 Microprocessor interrupt is enabled.

MCTY_DIS_U
- 0 Microprocessor interrupt is disabled.
- 1 Microprocessor interrupt is enabled.

MQOV
- 0 Microprocessor interrupt is disabled.
- 1 Microprocessor interrupt is enabled.

MBOV
- 0 Microprocessor interrupt is disabled.
- 1 Microprocessor interrupt is enabled.

MPMO_HLOG
- 0 Microprocessor interrupt is disabled.
- 1 Microprocessor interrupt is enabled.

unused(0) Fixed to zero.

MUT_CELLERR_D
- 0 Microprocessor interrupt is disabled.
- 1 Microprocessor interrupt is enabled.

MUT_PARERR_D
- 0 Microprocessor interrupt is disabled.
- 1 Microprocessor interrupt is enabled.

MRXR_OV
- 0 Microprocessor interrupt is disabled.
- 1 Microprocessor interrupt is enabled.

MUT_CELLERR_U
- 0 Microprocessor interrupt is disabled.
- 1 Microprocessor interrupt is enabled.

MUT_PARERR_U
- 0 Microprocessor interrupt is disabled.
- 1 Microprocessor interrupt is enabled.

3.21.4 Interrupt Mask Register (IMR1)

Read/write Address $A6_H$
Value after reset 0000_H

15							8
unused			MPOLVLD_ERR	MVLD_ERR_D	MVLD_ERR_U	MRXR_USTR	unused
7							**0**
MEDC_ERR_D	MEDC_ERR_U	MCAM_ERR	unused	MPOLU_PARERR_U	MRAM_PARERR_D	MRAM_PARERR_U	unused

For every interrupt status bit the corresponding interrupt mask bit is provided (IMR1 for ISR1). The interrupt mask bit controls whether the setting of an interrupt status bit leads to a microprocessor interrupt (activation of the interrupt line MPINT_N).

unused(5:3) Fixed to zero.

MPOLVLD_ERR

0 Microprocessor interrupt is disabled.
1 Microprocessor interrupt is enabled.

MVLD_ERR_D

0 Microprocessor interrupt is disabled.
1 Microprocessor interrupt is enabled.

MVLD_ERR_U

0 Microprocessor interrupt is disabled.
1 Microprocessor interrupt is enabled.

MRXR_USTR

0 Microprocessor interrupt is disabled.
1 Microprocessor interrupt is enabled.

unused(2) Fixed to zero.

MEDC_ERR_D

0 Microprocessor interrupt is disabled.
1 Microprocessor interrupt is enabled.

MEDC_ERR_U

0 Microprocessor interrupt is disabled.
1 Microprocessor interrupt is enabled.

MCAM_ERR

0 Microprocessor interrupt is disabled.
1 Microprocessor interrupt is enabled.

unused(1) Fixed to zero.

MPOLU_PARERR_U

0 Microprocessor interrupt is disabled.
1 Microprocessor interrupt is enabled.

MRAM_PARERR_D
- 0 Microprocessor interrupt is disabled.
- 1 Microprocessor interrupt is enabled.

MRAM_PARERR_U
- 0 Microprocessor interrupt is disabled.
- 1 Microprocessor interrupt is enabled.

unused(0) Fixed to zero.

3.22 CAME Interrupt Status Register (CSIR)

Read Address $A7_H$
Value after reset 0000_H

Note: Single bits of this register are resettable by writing a '1' to them.

15							8
unused							
7							**0**
unused							STATUS(3:0)

This register gives detailed information about the cause of a CAME interrupt during normal operation (cell transfer).

unused(11:0) Fixed to zero.

STATUS(3:0) Status delivered by the CAME for PN / VPI / VCI specific interrupts in ISR1.
STATUS[3:2] =
- 00 Ok (STATUS[1:0]=00)
- 01 Busy (STATUS[1:0]=00)
- 10 Alarm:
  STATUS[1:0] =
  - 00 Mismatch (at search requests).
  - 01 Multimatch (at search requests).
  - 10 Test search fault (at search requests).
  - 00 Refused entry (at write request).
  - 01 Refused line (at write request).
  - 00 Test read fault (at read request).
- 11 Error:
  STATUS[1:0] =
  - 00 Address/data bus parity error.
  - 01 Cascade error.
  - 10 Command cycle error.

3.23 RWR Mask Register (RMW_MASK)

Read/write Address $A9_H$
Value after reset 0000_H

15							8
unused					RMW_ MASKA	RMW_ MASK9	RMW_ MASK8

7							0
RMW_ MASK7	RMW_ MASK6	RMW_ MASK5	RMW_ MASK4	RMW_ MASK3	RMW_ MASK2	RMW_ MASK1	RMW_ MASK0

unused(4:0) Fixed to zero.

RMW_MASK_i i=[0..A]
In both cases the old RAM value is available after the execution in the RDR register:

0 Source is WDR-register (new Dword is written into the RAM).
1 Source is RDR-buffer (no change, old Dword is written back).

Note: READONLY flag in register CMR (see page 113) has higher priority then the RMW_MASK bits.

3.24 Cell Type Recognition Configuration Registers

The registers UCT_CONFIG and DCT_CONFIG configure the celltype recognition upstream and downstream:

– enabling of OAM Light with provision of some global OAM cell discard functions
– enabling and configuration of programmable cell type filters
– treatment of CRC errors
– enabling of housekeeping processing (only downstream)
– provision of F5RM/F5RES cell discard function for PADACK applications (only downstream).

3.24.1 UCT_CONFIG

Read/write Address AA_H
Value after reset 0000_H

15						8
unused	CRC_2_ NODISC	CRC_1_ NODISC	CRC_ NODISC	PCF2_ACT(1:0)		PCF2_ EN

7						0
PCF1_ACT(1:0)	PCF1_ EN	UNDEF_ NODISC	LB_ DISC	CC_ DISC	AR_ DISC	OAM_ EN

unused(1:0) Set to zero.

CRC_2_NODISC

0 Discard cells due to CRC errors if matching PCF2.
1 Discard no cells due to CRC errors if matching PCF2.

Note: This flag is only valid if PCF2_EN is set to '1'.

CRC_1_NODISC

0 Discard cells due to CRC errors if matching PCF1.
1 Discard no cells due to CRC errors if matching PCF1.

Note: This flag is only valid if PCF1_EN is set to '1'.

CRC_NODISC

0 Discard OAM cells due to CRC errors.
1 Discard no OAM cells due to CRC errors.

Note: This flag is only valid if OAM_EN is set to '1'.

PCF2_ACT(1:0) Selected action for cell types that match PCF2:

00 Forward
01 Discard
10 Drop
11 Copy

Note: The filters do not work at cells which are discarded due to policing!

PCF2_EN

0 Disables PCF2 (Programmable Cell Filter 2).
1 Enables PCF2 (Programmable Cell Filter 2).

PCF1_ACT(1:0) Selected action for cell types that match PCF1:

00	Forward
01	Discard
10	Drop
11	Copy

Note: The filters do not work at cells which are discarded due to policing!

PCF1_EN

0	Disables PCF1 (Programmable Cell Filter 1).
1	Enables PCF1 (Programmable Cell Filter 1).

UNDEF_NODISC

0	Discards cells with undefined oamtype at end points (TSP,TEP).
1	Drops cells with undefined oamtype at end points (TSP,TEP).

LB_DISC

0	Drops LB cells at end points (TSP,TEP).
1	Discards LB cells at end points (TSP,TEP).

CC_DISC

0	Drops CC/CCA cells at end points (TSP,TEP).
1	Discards CC/CCA cells at end points (TSP,TEP).

AR_DISC

0	Drops AIS/RDI cells at end points (TSP,TEP).
1	Discards AIS/RDI cells at end points (TSP,TEP).

OAM_EN

0	Disables OAM cell processing.
1	Enables OAM cell processing (OAM Light).

Note: For more details look at description of 'OAM Light'.

3.24.2 DCT_CONFIG

Read/write Address AB_H
Value after reset 0000_H

15						8
F5RM_ DISC	HK_DIS	CRC_2_ NODISC	CRC_1_ NODISC	CRC_ NODISC	PCF2_ACT(1:0)	PCF2_ EN

7						0
PCF1_ACT(1:0)	PCF1_EN	UNDEF_ NODISC	LB_ DISC	CC_ DISC	AR_ DISC	OAM_ EN

F5RM_DISC

0 Discard no F5RM and F5_PTI=’111’ (F5RES) cells.
1 Discard F5RM and F5_PTI=’111’ (F5RES) cells.

Note: Special PADACK application. F5RM and F5_PTI=’111’ (F5RES) cells are only discarded at F5 end points (TEP).

HK_DIS

0 Enables House Keeping (HK) processing.
1 Disables House Keeping (HK) processing.

Note: House Keeping is a Siemens proprietary inside-node maintenance procedure.

CRC_2_NODISC

0 Discard cells due to CRC errors if matching PCF2.
1 Discard no cells due to CRC errors if matching PCF2.

Note: This flag is only valid if PCF2_EN is set to ’1’.

CRC_1_NODISC

0 Discard cells due to CRC errors if matching PCF1.
1 Discard no cells due to CRC errors if matching PCF1.

Note: This flag is only valid if PCF1_EN is set to ’1’.

CRC_NODISC

0 Discard OAM cells due to CRC errors.
1 Discard no OAM cells due to CRC errors.

Note: This flag is only valid if OAM_EN is set to ’1’.

PCF2_ACT(1:0) Selected action for cell types that match PCF2:

00 Forward
01 Discard
10 Drop
11 Copy

PCF2_EN

0 Disables PCF2 (Programmable Cell Filter 2).
1 Enables PCF2 (Programmable Cell Filter 2).

PCF1_ACT(1:0) Selected action for cell types that match PCF1:

00	Forward
01	Discard
10	Drop
11	Copy

PCF1_EN

0	Disables PCF1 (Programmable Cell Filter 1).
1	Enables PCF1 (Programmable Cell Filter 1).

UNDEF_NODISC

0	Discards cells with undefined oamtype at end points (TSP,TEP).
1	Drops cells with undefined oamtype at end points (TSP,TEP).

LB_DISC

0	Drops LB cells at end points (TSP,TEP).
1	Discards LB cells at end points (TSP,TEP).

CC_DISC

0	Drops CC/CCA cells at end points (TSP,TEP).
1	Discards CC/CCA cells at end points (TSP,TEP).

AR_DISC

0	Drops AIS/RDI cells at end points (TSP,TEP).
1	Discards AIS/RDI cells at end points (TSP,TEP).

OAM_EN

0	Disables OAM cell processing.
1	Enables OAM cell processing (OAM Light).

Note: For more details look at description of 'OAM Light'.

3.25 Reset Configuration Register (RMW_CONF)

Read/write Address AC_H
Value after reset 0000_H

15							8
unused					RMW_ RES_A	RMW_ RES_9	RMW_ RES_8

7							0
RMW_ RES_7	RMW_ RES_6	RMW_ RES_5	RMW_ RES_4	RMW_ RES_3	RMW_ RES_2	RMW_ RES_1	RMW_ RES_0

The RWR reset register is useful to reset a RAM entry or parts of a RAM entry to ‘0’, because it is not required to write the ‘0’ into all WDR registers. Additionally in the RMW_MASK register the source for the next write access has to be selected, that is:

0: for the words that shall be reset

1: for the words, that shall not be changed, the source is the RDR-buffer (no change, old word is written back).

unused(4:0) Fixed to zero.

RMW_RES_i i=[0..A]:

0 Normal write access without reset.

1 Reset (to ’0’) word i of the read/write data at a write access.

3.26 Address Register for CMR Commands (ADR)

Read/write Address AD_H
Value after reset 0000_H

15			8
VCON	P_IP	ADR(13:8)	
7			**0**
ADR(7:0)			

The ADR register is programmed with the source/destination of several µP commands of the CMR register.

The P_IP and the VCON bit are only valid for CAME entries. P_IP is used for a reduced search request (only PN / VPI) at path intermediate points. VCON indicates whether a CAME entry presents a valid connection. In case that for a incoming cell the VCON bit of the CAME entry is ‘0’, in normal mode (no programming of bit NODIS_CAM in register TESTR) the cell will be discarded and a interrupt is generated.

VCON — Valid connection flag (used at write accesses to CAME):
- 0 Connection not valid.
- 1 Connection valid.

P_IP — Path intermediate point flag (used at write accesses to CAME):
- 0 Address reduction is performed over PN / VPI / VCI.
- 1 Path intermediate point; address reduction is performed only over PN / VPI.

ADR(13:0) — Address of a µP request (see CMR-register **Section 3.19,** page 113). It may contain LCI, port table-address or cell filter number.

3.27 Scan Configuration Registers

The scan configuration registers define the Range of LCIs (from LCI_min to LCI_max) that is refreshed by the POLU.

Starting of the POLU refresh has to be done in the following order:

1. write SC_CONR1 with LCIMIN and POLU_REFR_EN=0
2. write SC_CONR2 with LCIMAX
3. write SC_CONR1 with LCIMIN and with POLU_REFR_EN=1.

3.27.1 SC_CONR1

Read/write Address AE_H
Value after reset 0000_H

15		8
unused	POLU_ REFR_EN	LCI_MIN(13:8)

7	0
LCI_MIN(7:0)	

unused Fixed to zero.

POLU_REFR_EN

0 No policing refresh.
1 Policing refresh in the range between LCI_MIN and LCI_MAX.

LCI_MIN(13:0) Lower limit of LCIs processed by POLU refresh.

3.27.2 SC_CONR2

Read/write Address AF_H
Value after reset 0000_H

15	8
unused	LCI_MAX(13:8)

7	0
LCI_MAX(7:0)	

unused Fixed to zero.

LCI_MAX(13:0) Upper limit of LCIs processed by POLU refresh.

3.28 DMA Configuration/Read Register

The DMA can be performed either for CONNRAMUP or for CONNRAMDO controlled by DMA_UD (bit 0 of DCONR). To read the counters from CONNRAMUP and CONNRAMDO the following steps are necessary:

– Load register DMA_MIN with LCIMIN
– Load register DMA_MAX with LCIMAX
– Load register DCONR with bit DMA_UD=0 and DMA_START=1 ⇒ starts DMA upstream
– Wait until DMA upstream is complete (bit DMA_START=0)
– Load register DMA_MIN with LCIMIN (only if LCIMIN is different for DMA downstream)
– Load register DMA_MAX with LCIMAX (only if LCIMAX is different for DMA downstream)
– Load register DCONR with bit DMA_UD=1 and DMA_START=1 ⇒ starts DMA downstream
– wait until DMA downstream is complete (bit DMA_START=0).

3.28.1 DCONR

Read/write Address $B0_H$
Value after reset 0000_H

15							8
CTR7_ RES	CTR6_ RES	CTR5_ RES	CTR4_ RES	CTR3_ RES	CTR2_ RES	CTR1_ RES	DMA_ DELAY(6)

7							0
DMA_DELAY(5:0)						DMA_ START	DMA_ UD

CTR7_RES

0	Don’t reset counter.
1	Reset counter P_TIC0 (upstream) after DMA read.

CTR6_RES

0	Don’t reset counter.
1	Reset counter P_TIC (upstream) after DMA read.

CTR5_RES

0	Don’t reset counter.
1	Reset counter TTC (upstream) after DMA read.

CTR4_RES

0	Don’t reset counter.
1	Reset counter TDC0 (upstream) or P_TOC0 (downstream) after DMA read.

CTR3_RES

0	Don’t reset counter.
1	Reset counter TDC1 (upstream) or P_TOC (downstream) after DMA read.

CTR2_RES

0 Don’t reset counter.
1 Reset counter TIC0 (upstream) or TOC0 (downstream) after DMA read.

CTR1_RES

0 Don’t reset counter.
1 Reset counter TIC (upstream) or TOC (downstream) after DMA read.

DMA_DELAY(6:0) Delay between two DMA requests.
Delay = (0,1,2,...,127) * 2 * cellcycle.

Note: These bits can be used to avoid DMA bursts on the µP bus.

DMA_START This bit is reset by the ASIC after completion of the DMA; i.e. after the last one of the connections between LCIMIN (in register DMA_MIN) and LCIMAX (in register DMA_MAX) has been read out by µP.
While DMA_START=1 it is not possible to write the registers DCONR, DMA_MIN and DMA_MAX with the exception of bit DMA_START. Writing a ‘0’ to DMA_START resets the running DMA.

0 DMA complete.
1 Start DMA.

DMA_UD

0 DMA in upstream direction.
1 DMA in downstream direction.

Note: A complete DMA must be split in a DMA upstream and a DMA downstream.

3.28.2 DMAR

Read Address $B1_H$
Value after reset undefined

15	8
dword n(15:8/31:24)	
7	**0**
dword n(7:0/23:16)	

This 16 bit register is used to read from the DMA FIFO. There the words are stored with 32 bit length (= dword). To read one dword from the DMA FIFO requires two read accesses to the register DMAR.

For the upstream direction the DMA FIFO is read in the following order :

dword 1(15:0)	Connection RAM upstream (TIC counter).
dword 1(31:16)	Connection RAM upstream (TIC counter).
dword 2(15:0)	Connection RAM upstream (TIC0 counter).
dword 2(31:16)	Connection RAM upstream (TIC0 counter).
dword 3(15:0)	Connection RAM upstream (TDC1 counter).
dword 3(31:16)	Connection RAM upstream (TDC1 counter).
dword 4(15:0)	Connection RAM upstream (TDC0 counter).
dword 4(31:16)	Connection RAM upstream (TDC0 counter).
dword 5(15:0)	Connection RAM upstream (TTC counter).
dword 5(31:16)	Connection RAM upstream (TTC counter).
dword 6(15:0)	Connection RAM upstream (P_TIC counter).
dword 6(31:16)	Connection RAM upstream (P_TIC counter).
dword 7(15:0)	Connection RAM upstream (P_TIC0 counter).
dword 7(31:16)	Connection RAM upstream (P_TIC0 counter).

For the downstream direction the DMA FIFO is read in the following order :

dword 3(15:0)	Connection RAM downstream (TOC counter).
dword 3(31:16)	Connection RAM downstream (TOC counter).
dword 4(15:0)	Connection RAM downstream (TOC0 counter).
dword 4(31:16)	Connection RAM downstream (TOC0 counter).
dword 5(15:0)	Connection RAM downstream (P_TOC counter).
dword 5(31:16)	Connection RAM downstream (P_TOC counter).
dword 6(15:0)	Connection RAM downstream (P_TOC0 counter).
dword 6(31:16)	Connection RAM downstream (P_TOC0 counter).

3.29 Test Register/Special Modes (TESTR)

Read/write Address $B2_H$
Value after reset 0000_H

15							8
unused			LOOP_ TXRX	HW_LOOP _TRANS	TESTINT	NODIS_ CAM	POVLD ERREN	VLDERR EN_D
7							**0**
PARERR EN_D	PARERR EN_U	VLDERR EN_U	PARERR EN_POLU	DMA_ WAIT	MC_DIS	LOOPDU	LOOPUD

The register TESTR provides special modes like loops, the disabling of cell discard functions and multicast. To prevent disturbing of normal mode operation by chance, the write access to the TESTR-register is only possible if bit TESTR_EN in the MODE-register is set to ‘1’!

unused Fixed to zero.

LOOP_TXRX Every change from 0 to 1 starts the transmission of the contents of the TXR-registers to the RXR-registers. In case of RXR-overflow no interrupt is generated and the contents of RXR is overwritten!

HW_LOOP_TRANS
- 0 The HW-loops are not transparent, i.e. the cell stream is only looped back.
- 1 The HW-loops are transparent, i.e. the cell stream is not only looped back but also forwarded to transmit UTOPIA.

TESTINT
- 0 All interrupt sources are enabled.
- 1 All interrupt sources are disabled: every new write access to the RXR-register will generate a new interrupt with a different interrupt flag (gives the opportunity to test interrupts regardless whether interrupts occur).

NODIS_CAM Cells not valid in CAME:
- 0 Cells will not leave UTOPIA.
- 1 Discard no cells (and no interrupt generated).

POVLDERREN Cells not valid in POLU-RAM:
- 0 Discard no cells.
- 1 Discard cells.

VLDERREN_D Cells not valid in connection RAM downstream:
- 0 Cells will not leave UTOPIA.
- 1 Discard no cells (and no interrupt generated).

PARERREN_D Cells generating a parity error at connection RAM downstream:
- 0 Cells will not leave UTOPIA.
- 1 Discard no cells (and no interrupt generated).

PARERREN_U Cells generating a parity error at connection RAM upstream:
- 0 Cells will not leave UTOPIA.
- 1 Discard no cells (and no interrupt generated).

VLDERREN_U Cells not valid in connection RAM upstream:

0 Cells will not leave UTOPIA.

1 Discard no cells (and no interrupt generated).

PARERREN_POLU Cells generating a parity error at POLU RAM:

0 No POLU action.

1 Cells will be discarded, no policing.

DMA_WAIT

0 No DMA-request inactive time.

1 Min. 32 cycles DMA-request inactive time between two active phases on the MPDREQ_N pin.

Note: This bit allows adaptation to Intel 386EX DMA timing.

MC_DIS

0 Enables multicast (downstream).

1 Disables/interrupts multicast (downstream).

LOOPDU

0 No loop.

1 Insert test loop downstream to upstream (during loop in downstream direction only the functionality cell transfer with header translation is possible; other functions like cell insertion, multicast, etc. are not available).

Note: With the bit HW_LOOP_TRANS the loop can be configured as transparent or not transparent.

LOOPUD

0 No loop.

1 Insert test loop upstream to downstream (during loop in downstream direction only the functionality cell transfer with header translation is possible; other functions like cell insertion, multicast, etc. are not available).

Note: With the bit HW_LOOP_TRANS the loop can be configured as transparent or not transparent.

3.30 POLU Status Registers (P_STATR0..2)

3.30.1 P_STATR0

Read Address $B3_H$
Value after reset 0000_H

15	8
word(15:8)	
7	**0**
word(7:0)	

word(15:0) Only for Test. Don't change the contents for normal policing operation.

3.30.2 P_STATR1

Read Address $B4_H$
Value after reset 0000_H

15	8
word(15:8)	
7	**0**
word(7:0)	

word(15:0) Only for Test. Don't change the contents for normal policing operation.

3.30.3 P_STATR2

Read Address $B5_H$
Value after reset 0000_H

15	8
word(15:8)	
7	**0**
word(7:0)	

word(15:0) Only for Test. Don't change the contents for normal policing operation.

3.31 CAME Valid Intermediate LCI (CAMVILCI)

Read Address $B6_H$
Value after reset 0000_H

15			8
VCON	P_IP	LCI(13:8)	

7	0
LCI(7:0)	

The address reduction test is only started via the command ‘read a line in the CAME’ in the CMR register.

Note: Response of CAME is written to CAMVILCI.

VCON	Valid connection flag (also in read mode).
P_IP	Path intermediate point flag (also in read mode).
LCI(13:0)	LCI

3.32 DMA Range Registers

DMA_MIN and DMA_MAX define the range of LCI’s that is processed by DMA according to the settings in the register DCONR.

3.32.1 DMA_MIN

Read/write Address $B8_H$
Value after reset 0000_H

15	8
unused	LCI_MIN(13:8)

7	0
LCI_MIN(7:0)	

unused	Fixed to zero.
LCI_MIN(13:0)	Lowest LCI (LCIMIN) of LCI range processed by DMA.

3.32.2 DMA_MAX

Read/write Address $B9_H$
Value after reset 0000_H

15	8
unused	LCI_MAX(13:8)

7	0
LCI_MAX(7:0)	

unused	Fixed to zero.
LCI_MAX(13:0)	Highest LCI (LCIMAX) of LCI range processed by DMA.

3.33 BIST Registers

The BIST is normally used for test purposes of the ASIC vendor. Inside the ATM-LP the signals ‘BISTDONE’ and ‘BISTERROR’ are stored in registers so that the BIST can be used for an initial RAM test (only ASIC internal RAMs). With the BIST signals stored in registers the BIST test is only a ‘go/no go’ test. It is not possible to determine which RAM parts are faulty.

A BIST test of all internal RAMs is performed in the following order:

– set bit ‘TESTR_EN’ in the MODE register to ‘1’
– check the reset values of the BIST registers (BISTMODE1/2=BISTDONE=0000hex; BISTERROR=0FFFhex)
– BIST self test: set the mode bits of all RAMs to ‘01’ (The BIST self test starts toggling of the BISTERROR signals. The first ‘0’-state on these signals is captured by the BISTERROR register to indicate that a BIST error has occurred.)
– wait for about 100 clock cycles
– control the BISTERROR register (BISTERROR=0000hex); that means a BIST error has occurred and has been recognized for every internal RAM ⇒ the control logic is able to detect BIST errors
– reset the Bist self test for all internal RAMs (BISTMODE1/2=0000hex)
– reset the BISTERROR register (this register is reset with any write access)
– check reset of BISTERROR register (BISTERROR=0FFFhex)
– BIST test: set the mode bits of all RAMs to ‘10’
– wait until the BISTDONE bit of every internal RAM is set (BISTDONE=0FFFhex)
– check whether Bist errors occurred (BISTERROR /= 0FFFhex).

To prevent disturbing of normal mode operation by chance, the write access to the BISTMODE1/2-register is only possible if bit TESTR_EN in the MODE-register is set to ‘1’!

After completion of BIST test a software-Reset (see CMR-register **Section 3.19,** page 113) has to be started because the BIST affects also the control RAM (NCP RAM) of the demultiplexing buffer in the UTOPIA transmit downstream interface which leads to a malfunction.

3.33.1 BIST Mode Register 1 (BISTMODE1)

Read/write Address BA_H
Value after reset 0000_H

15			8
BIST_TRM(1:0)	BIST_RXR(1:0)	BIST_NCP(1:0)	BIST_UTTXD1(1:0)
7			**0**
BIST_UTTXD0(1:0)	BIST_UTRXD(1:0)	BIST_UTTXU(1:0)	BIST_UTRXU(1:0)

Note: Actions for Bistmode:

00 Inactive
01 Test of BIST.
10 Start BIST.
11 Diagnosis (not used).

BIST_TRM(1:0)

Bistmode for TRM RAM. Traffic Measurement Port Table not modified at SW reset.

BIST_RXR(1:0)

Bistmode for RXR RAM. Rx 12 cell extraction Buffer not modified at SW reset.

BIST_NCP(1:0)

Bistmode for UTTXD NCP RAM (UTOPIA-Address-RAM). Set to ’0’ with SW reset.

BIST_UTTXD1(1:0)

Bistmode for UTTXD Buffer RAM 1. UTOPIA Tx-downstream shared memory Buffer of 64 cells. Set to ’0’ with SW reset.

BIST_UTTXD0(1:0)

Bistmode for UTTXD Buffer RAM 0. UTOPIA Tx-downstream shared memory Buffer of 64 cells. Set to ’0’ with SW reset.

BIST_UTRXD(1:0)

Bistmode for UTRXD Buffer RAM. UTOPIA Rx-downstream cell FIFO. Set to ’0’ with SW reset.

BIST_UTTXU(1:0)

Bistmode for UTTXU Buffer RAM. UTOPIA Tx-upstream cell FIFO. Set to ’0’ with SW reset.

BIST_UTRXU(1:0)

Bistmode for UTRXU Buffer RAM. UTOPIA Rx-upstream cell FIFO. Set to ’0’ with SW reset.

3.33.2 BIST Mode Register 2 (BISTMODE2)

Read/write Address BB_H
Value after reset 0000_H

15			8
unused			
7			**0**
BIST_RWR1(1:0)	BIST_RWR0(1:0)	BIST_UCW1(1:0)	BIST_UCW0(1:0)

Note: Actions for Bistmode:

00 Inactive
01 Test of BIST.
10 Start BIST.
11 Diagnosis (not used).

unused Fixed to zero.

BIST_RWR1(1:0)
Bistmode for RWR RAM 1. µP Read/Write not modified at SW reset.
BIST_RWR0(1:0)
Bistmode for RWR RAM 0. µP Read/Write not modified at SW reset.
BIST_UCW1(1:0)
Bistmode for UCW RAM 1. Upstream workbench not modified at SW reset.
BIST_UCW0(1:0)
Bistmode for UCW RAM 0. Upstream workbench not modified at SW reset.

3.33.3 BIST Active Register (BISTDONE)

Read Address BC_H
Value after reset 0000_H

15							8
unused				BISTDONE_RWR1	BISTDONE_RWR0	BISTDONE_UCW1	BISTDONE_UCW0
7							**0**
BISTDONE_TRM	BISTDONE_RXR	BISTDONE_NCP	BISTDONE_UTTXD1	BISTDONE_UTTXD0	BISTDONE_UTRXD	BISTDONE_UTTXU	BISTDONE_UTRXU

unused Fixed to zero.
BISTDONE_RWR1
0 Bistmode for RWR RAM 1 is busy.
1 Bistmode for RWR RAM 1 is done.
BISTDONE_RWR0
0 Bistmode for RWR RAM 0 is busy.
1 Bistmode for RWR RAM 0 is done.
BISTDONE_UCW1
0 Bistmode for UCW RAM 1 is busy.
1 Bistmode for UCW RAM 1 is done.
BISTDONE_UCW0
0 Bistmode for UCW RAM 0 is busy.
1 Bistmode for UCW RAM 0 is done.
BISTDONE_TRM
0 Bistmode for TRM RAM is busy.
1 Bistmode for TRM RAM is done.
BISTDONE_RXR
0 Bistmode for RXR RAM is busy.
1 Bistmode for RXR RAM is done.
BISTDONE_NCP
0 Bistmode for UTTXD NCP RAM is busy.
1 Bistmode for UTTXD NCP RAM is done.

BISTDONE_UTTXD1

0 Bistmode for UTTXD Buffer RAM is busy.
1 Bistmode for UTTXD Buffer RAM is done.

BISTDONE_UTTXD0

0 Bistmode for UTTXD Buffer RAM 0 is busy.
1 Bistmode for UTTXD Buffer RAM 0 is done.

BISTDONE_UTRXD

0 Bistmode for UTRXD Buffer RAM is busy.
1 Bistmode for UTRXD Buffer RAM is done.

BISTDONE_UTTXU

0 Bistmode for UTTXU Buffer RAM is busy.
1 Bistmode for UTTXU Buffer RAM is done.

BISTDONE_UTRXU

0 Bistmode for UTRXU Buffer RAM is busy.
1 Bistmode for UTRXU Buffer RAM is done.

3.33.4 BIST Result Register (BISTERROR)

Read/write Address BD_H
Value after reset $0FFF_H$

15							8
unused				BISTERR_RWR1	BISTERR_RWR0	BISTERR_UCW1	BISTERR_UCW0
7							**0**
BISTERR_TRM	BISTERR_RXR	BISTERR_NCP	BISTERR_UTTXD1	BISTERR_UTTXD0	BISTERR_UTRXD	BISTERR_UTTXU	BISTERR_UTRXU

Note: The register is resetted at every write access (if bit TESTR_EN in MODE-register is equal 1)!

unused Fixed to zero.

BISTERR_RWR1

0 Bisterror for RWR RAM 1 occurred.
1 No Bisterror.

BISTERR_RWR0

0 Bisterror for RWR RAM 0 occurred.
1 No Bisterror.

BISTERR_UCW1

0 Bisterror for UCW RAM 1 occurred.
1 No Bisterror.

BISTERR_UCW0

0	Bisterror for UCW RAM 0 occurred.
1	No Bisterror.

BISTERR_TRM

0	Bisterror for TRM RAM occurred.
1	No Bisterror.

BISTERR_RXR

0	Bisterror for RXR RAM occurred.
1	No Bisterror.

BISTERR_NCP

0	Bisterror for UTTXD NCP RAM occurred.
1	No Bisterror.

BISTERR_UTTXD1

0	Bisterror for UTTXD Buffer RAM 1 occurred.
1	No Bisterror.

BISTERR_UTTXD0

0	Bisterror for UTTXD Buffer RAM 0 occurred.
1	No Bisterror.

BISTERR_UTRXD

0	Bisterror for UTRXD Buffer RAM occurred.
1	No Bisterror.

BISTERR_UTTXU

0	Bisterror for UTTXU Buffer RAM occurred.
1	No Bisterror.

BISTERR_UTRXU

0	Bisterror for UTRXU Buffer RAM occurred.
1	No Bisterror.

4 Operation

4.1 Multicast

The Multicast light functionality is a sequential multicast. A multicast cell, arrived at the input cell queue of the UTOPIA transmit interface downstream, is hold in the first entry of the input queue and copied to the output shared buffer queues given by the linked list structure in CONNRAMDO. The indication for a multicast cell is bit MC_ANCHOR in Dword2 of CONNRAMDO (see **section 3.3.3.3,** page 80). The cell is copied to the queues/ports given by the PN of each LCI included in the linked list. The ATM-LP supports spatial and logical multicast. When the selected LCIs include different ports/queues it is a spatial multicast. If the selected LCIs are defined for the same port/queue it is a logical multicast. The example in **figure 40** describes a spatial multicast into three queues.

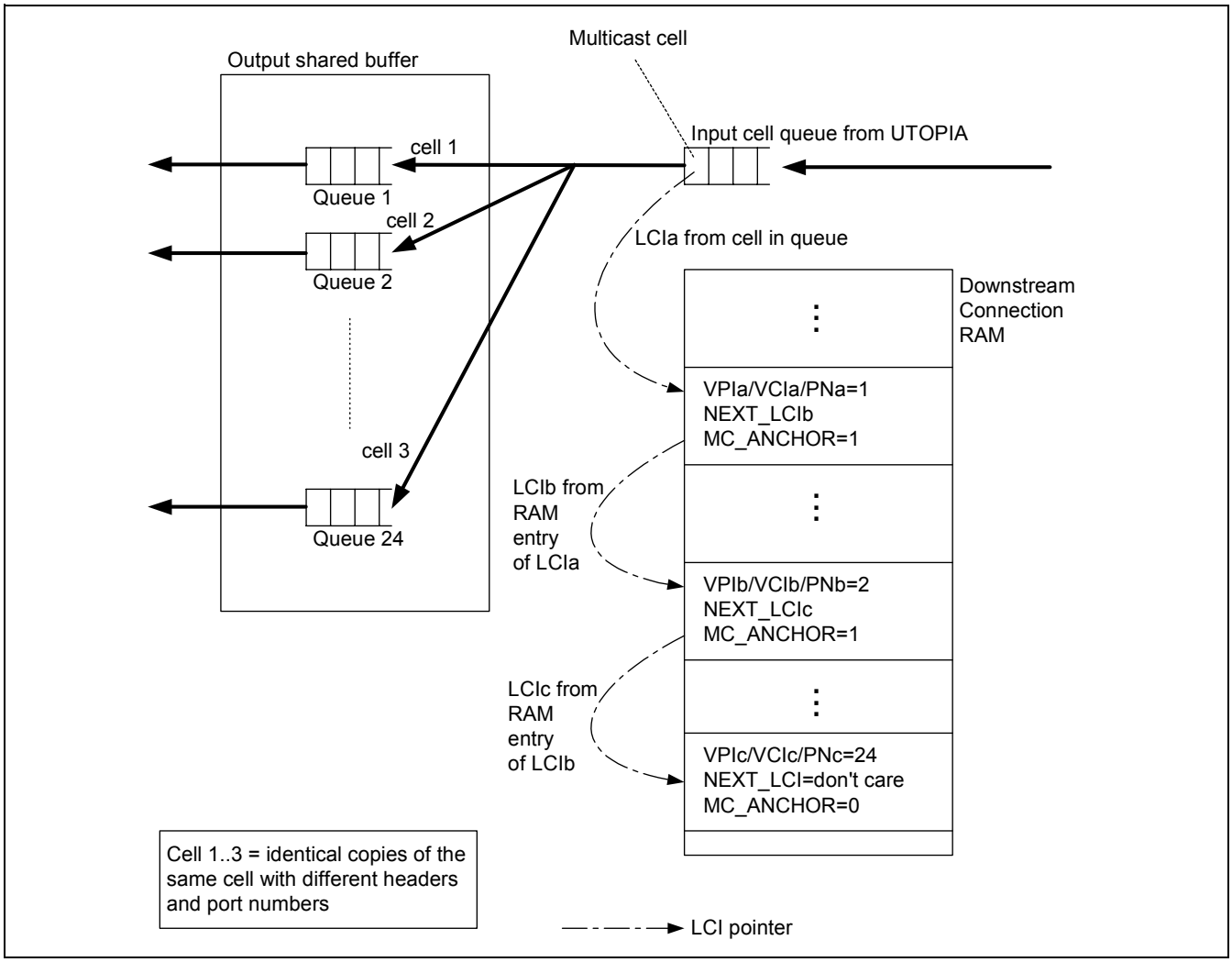


Figure 40 Example for Spatial Multicast

To initiate a multicast, the microprocessor has to set the MC_ANCHOR bit in Dword2 of the connection entry in CONNRAMUP. The NEXT_LCI entry in Dword2 defines the LCI of the following connection in the multicast chain. This LCI has to be valid if the MC_ANCHOR bit is set. Otherwise this entry is "don't care".

4.2 UTOPIA Configuration

The ATM-LP provides five registers for UTOPIA interface configuration. The registers CONUT1A-C (see **section 3.16.1,** page 107, **section 3.16.2,** page 108 and **section 3.16.3,** page 108) are used to enable/disable each of the 24 UTOPIA ports in both upstream and downstream direction. The register CONUT2 (see **section 3.16.4,** page 108) is used to set the data bus width (8 or 16 bit) and the UTOPIA mode (Level 1 or 2) on the PHY and the ATM side. To enable the forced inserting of empty cell cycles in downstream direction and to set the queue threshold of the UTOPIA buffer the register CONUT3 (see **section 3.16.5,** page 110) is used. The microprocessor can monitor the status of the UTOPIA interface via the two UTOPIA status registers UT_QOV1 and UT_QOV2 (see **section 3.17.1,** page 111 and **section 3.17.2,** page 111). These registers indicate on which queue an overflow occured.

4.3 RAM Access

The microprocessor cannot access the external RAMs (POLURAM and CONNRAM) directly. It has to use the read and write transfer registers of the ATM-LP. The ATM-LP uses a read-modify-write type access.

Read-Modify-Write-Access :

First write the LCI to register ADR (see **section 3.26,** page 130) and the new contents for this LCI to the write registers from WDR0L to WDRAH (see **section 3.2.1,** page 71). To select the Dwords of the selected entry which should not be changed (read-only) set the associated mask bits in the mask register RMW_MASK (see **section 3.23,** page 124). Using bits MPREQDEF in the command register CMR (see **section 3.19,** page 113) the source RAM must be selected. Set bit READONLY to ’0’ and the start bit STREQ to ’1’. Setting the last mentioned bit starts the read-modify-write process. The microprocessor now has to poll the STREQ bit. When the ATM-LP finished the RAM access, this bit will be reset. After that, the microprocessor can read the old RAM entries via the read registers from RDR0L to RDRAH (see **section 3.2.1,** page 71).

Read-Only-Access :

First write the LCI to register ADR (see **section 3.26,** page 130). The source RAM must be selected by using bits MPREQDEF in the command register CMR (see **section 3.19,** page 113). Set the bit READONLY to ’1’ and the start bit STREQ to ’1’. Note, that the bit READONLY has a higher priority than the mask register bits. Therefore the mask register has no effect during a read-only-access. The setting of the last bit starts the read-modify-write process. The microprocessor now has to poll the STREQ bit. When the ATM-LP has finished the RAM access, this bit will be reset. After that, the microprocessor can read the old RAM entries via the read registers from RDR0L to RDRAH (see **section 3.2.1,** page 71).

4.4 CAME Access

The microprocessor is responsible for the configuration of the external address reduction circuit CAME. Therefore a write access to the CAME is necessary and can be done via a set of five registers which are provided by the ATM-LP. First the microprocessor writes the LCI of the connection to the address register ADR (see **section 3.26,** page 130). The VCI of the connection is written to register CAMADRL (see **section 3.6.1,** page 92). The VPI and the PN are written to register CAMADRH (see **section 3.6.2,** page 92). After this the microprocessor has to set register CMR (see **section 3.19,** page 113) to value 0x0048 (write line to CAME and start transfer). The transfer is finished after bit STREQ is reset by the ATM-LP. By reading

register CSTATR (see **section 3.20.2,** page 116) status information about the CAME after a microprocessor access are available.

4.5 Policing Configuration

To configurate the policing unit and to start the policing process execute the following steps. The policing unit has the capability of policing 16384 connections independently. Because of that, the Leaky Bucket algorithm has to be defined for each policed connection. This has to be done via the entries in the POLURAM, which consists of 11 Dwords (see **section 3.3.1,** page 73). With the Dwords 0 to 10 the variables of the Leaky Buckets algorithm are defined. Dword 10 is used for setting F4/F5 policing options, POLU operation mode and policing path definition. The POLURAM access is done as described in **section 4.3,** page 145. Set the POLU to normal mode via bit TOM in the POLU configuration register P_CONRL (see **section 3.7.1,** page 93). Besides tagging and discarding of cells via the POLU can be disabled with this register (bits DISC_INH and TAG_INH). The contents of the P_CONRL register are transferred to the POLU by setting bit VALID_CONF in register P_CONRH (see **section 3.7.2,** page 94). After this the LCI range of the connections which should policed has to be defined using registers SC_CONR1 and SC_CONR2 (see **section 3.27.1,** page 131 and **section 3.27.2,** page 131). First write the lower LCI (LCImin) to register SC_CONR1 with bit POLU_REFR_EN = ’0’. Then write the upper LCI (LCImax) to register SC_CONR2. To enable the policing write LCImin to register SC_CONR1 with bit POLU_REFR_EN = ’1’. To stop the policing the microprocessor has to reset this bit again.

4.6 Connection Setup

The following steps are required to set up a connection through the ATM-LP using the CAME (here e.g. for upstream direction). Write the LCI for the connection to the address register ADR (see **section 3.26,** page 130). The VCI of the connection is written to the CAME address register CAMADRL (see **section 3.6.1,** page 92). The PN and the VPI of the connection are written to the CAME address register CAMADRH (see **section 3.6.2,** page 92). Write the connection specific parameters to the write registers WDR0L and WDR0H (register see **section 3.2.1,** page 71; for connection specific parameters see **section 3.3.2,** page 77, Dword0). If OAM light functions are not used, set all OAM parameters to ’0’. Set bit VCON_UP to indicate a valid connection and bit EN_TRAF_MEAS_UP when traffic measurement should be enabled for this connection. Set registers from WDR1L to WDR6H to value 0x0000. Herewith the counters are reset. Write the value 0x0049 to the command register CMR (see **section 3.19,** page 113). This has the effect of writing one line into the CAME and one entry to the CONNRAMUP using the LCI in register ADR, the VCI in register CAMADRL and the PN and VCI in register CAMADRH. The CONNRAMUP is written to with the contents of the write transfer registers (WDRxx).

4.7 Cell Insertion and Extraction

To insert user defined cells the ATM-LP provides one set of 27 registers from TXR0 to TXR26 (see **section 3.9,** page 96). These registers can be programmed by the microprocessor. The registers from TXR0 to TXR2 are used to program the cell header and registers from TXR3 to TXR26 are used to insert the payload. After data is written to the transmit cell registers, the microprocessor can control the insertion via the configuration of the transmit cell buffer register TXR_CONFIG (see **section 3.9,** page 96). Using bit TRANSM_DIR it is selectable whether the cell is inserted in up- or in downstream direction. Bit HTON is used to enable header translation.

By setting bit START_TR the insertion starts. After the cell is inserted, the ATM-LP resets bit START_TR. It is strongly recommended not to start the transmission in upstream direction while the bit UTRXFIFO_OV_U in register ISR0 is set to ’1’ (see **section 3.21.1,** page 117). When this bit is set, an input queue overflow of the UTOPIA receive interface upstream occurs. It is also strongly recommended not to start the transmission in downstream direction while bit BOV in the register ISR0 or bit UT_QOV of the corresponding port (see **section 3.17.1,** page 111 and **section 3.17.2,** page 111) are set to ’1’. This indicates a buffer/queue overflow in the UTOPIA transmit interface downstream.

Any cells copied or dropped from the cell stream can be read from the AOP by the processor with 27 reads to the RXR register. The reads do not need to be consecutive. With bit RXR_USTR set to ’1’ the ATM-LP indicates that a cell is stored in the cell receive buffer. After read out the complete set of cells, this bit is reset by ATM-LP automatically.

4.8 DMA Configuration and Access

The ATM-LP supports DMA for a fast transfer of connection counter information from CONNRAMUP and CONNRAMDO to the microprocessor RAM. The microprocessor can control the DMA access via three registers called DMA_MIN, DMA_MAX and DCONR (see **section 3.32.1,** page 138, **section 3.32.2,** page 138 and **section 3.28.1,** page 132). First write the range of LCI values for DMA transfer to the DMA_MIN (lower LCI value) and DMA_MAX (upper LCI value). Then configure the DCONR register, i.e. select the counters which will be reset by the DMA, the delay between two DMA bursts on the microprocessor bus using bits DMA_DELAY and the direction on which the counters should read out by bit DMA_UD (up- or downstream). When the DMA is configurated set bit DMA_START to initiate the DMA transfer. With the external pin MPDREQ = ’0’ the ATM-LP indicates that a new LCI entry has been written into the ATM-LP DMA buffer. The microprocessor response with setting MPACK to ’0’. Than the microprocessor can read out the connection counters by 14 read accesses to DMAR in upstream or 8 read accesses to DMAR in downstream direction. The inactive time between two read accesses (duration of ’high’ on MPRD) must be at least one ATM-LP SYSCLK cycle. With MPDREQ = ’1’ the ATM-LP indicates that the DMA buffer is empty. The microprocessor has to set MPACK to ’1’ for the DMA can performe the next LCI. When the next LCI entry has been written to the ATM-LP DMA buffer, the pin MPDREQ becomes active again. The microprocessor has to repeat the read out procedure until the ATM-LP finished the DMA access and indicates this state by reseting bit DMA_START. Note, that a fast transfer can be accomplished by connecting the external pin MPDACK permanently high.

5 Interface Description

5.1 UTOPIA Interface

UTOPIA Handshaking at the PHY side:

- If one of the ports of the upstream receive line is selected (RXADRU) by the ATM-LP and this port is able to transmit one cell, RXCLAVU is asserted. By asserting RXENBU the ATM-LP forces the transmission of a whole cell. RXSOCU indicates the Start Of Cell.
- In downstream direction the ATM-LP selects one port and if the port is able to receive one cell TXCLAVD is asserted. When the transmission to this port starts, TXENBD and the TXSOCD is set.

UTOPIA Handshaking at the ATM side:

- For the upstream transmit line the ATM-LP represents one of 24 ports. Its valid port address is programmable. If the ATM-LP is selected and TXCLAVU is asserted, then TXENBU is set, if one cell is available for transmission.
- The cells downstream can be received from up to 24 ports. The selected ATM-LP with programmable port address asserts RXCLAVD, if it is able to receive one cell. When the transmission to this port starts, RXENBD and RXSOCD is set.

In the following figures three UTOPIA configurations with the corresponding system architecture are depicted. **Figure 41** depicts the ATM-LP between the PHYs and an other ATM Layer device e.g. AOP, ABM or ASP. For this application the UTOPIA interface at the ATM side is in slave mode. **Figure 42** and **43** depicts an ATM-LP between PHYs used as multiplexor for access networks or backbone applications.

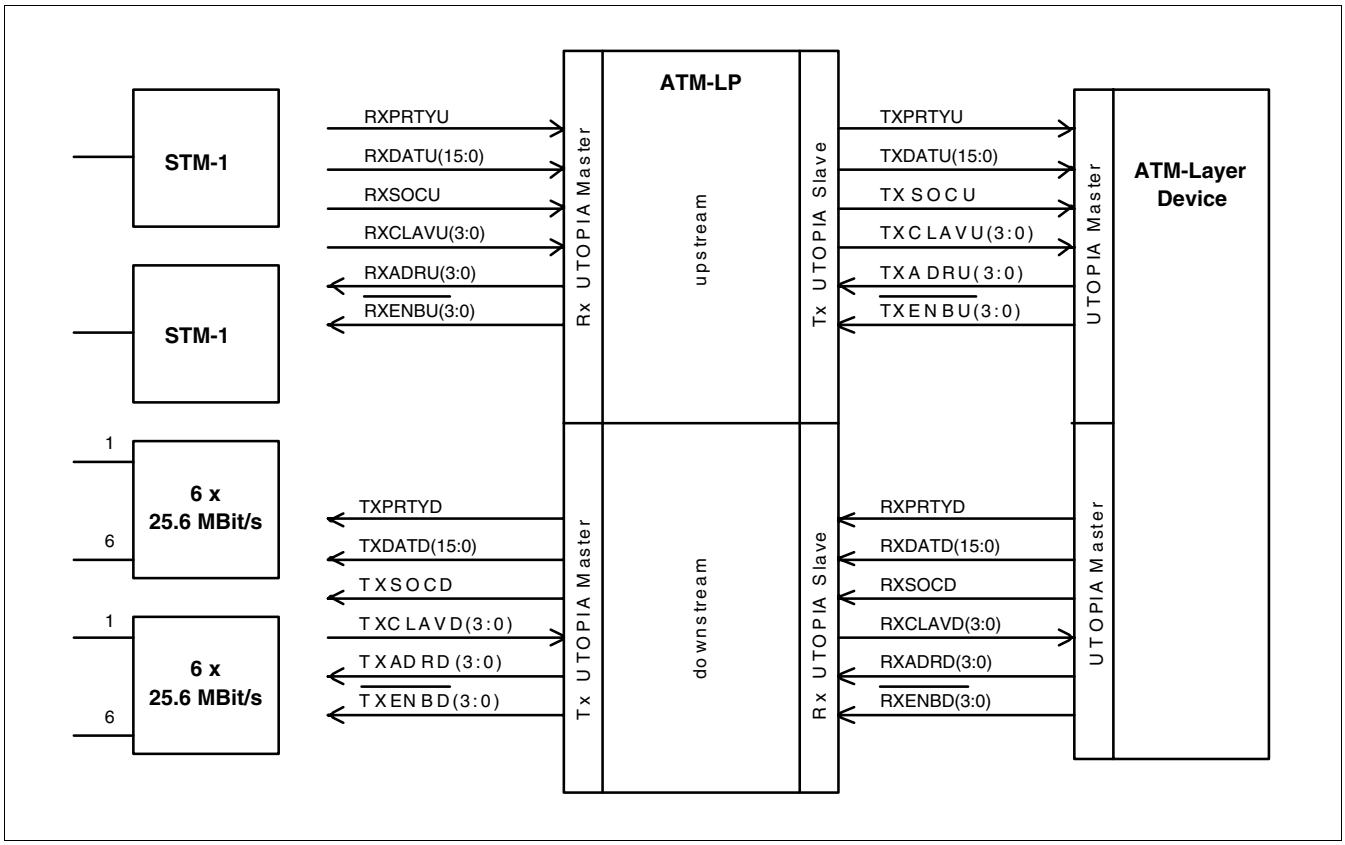


Figure 41 UTOPIA Interface Configuration with Slave Mode at the ATM Side

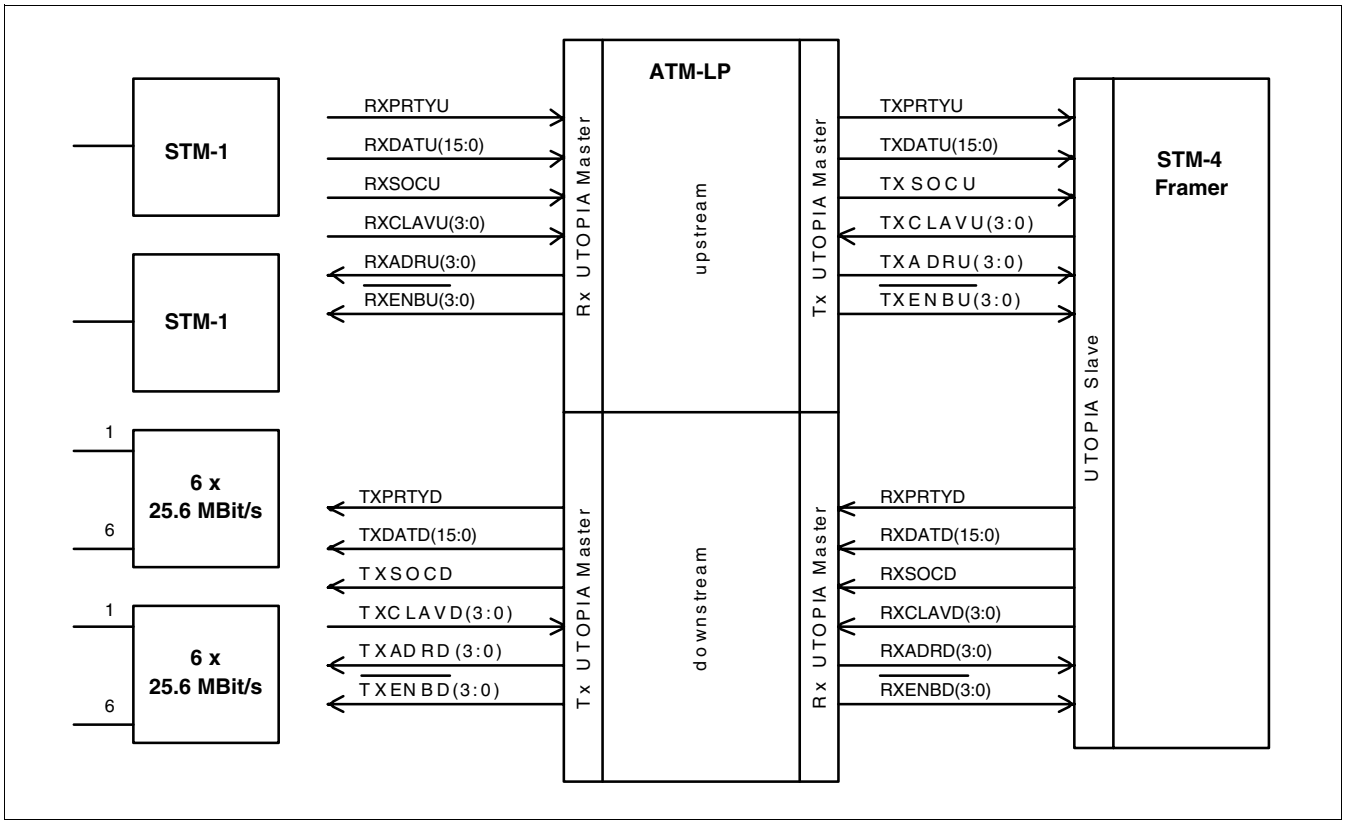


Figure 42 UTOPIA Interface Configuration with Master Mode at the ATM Side

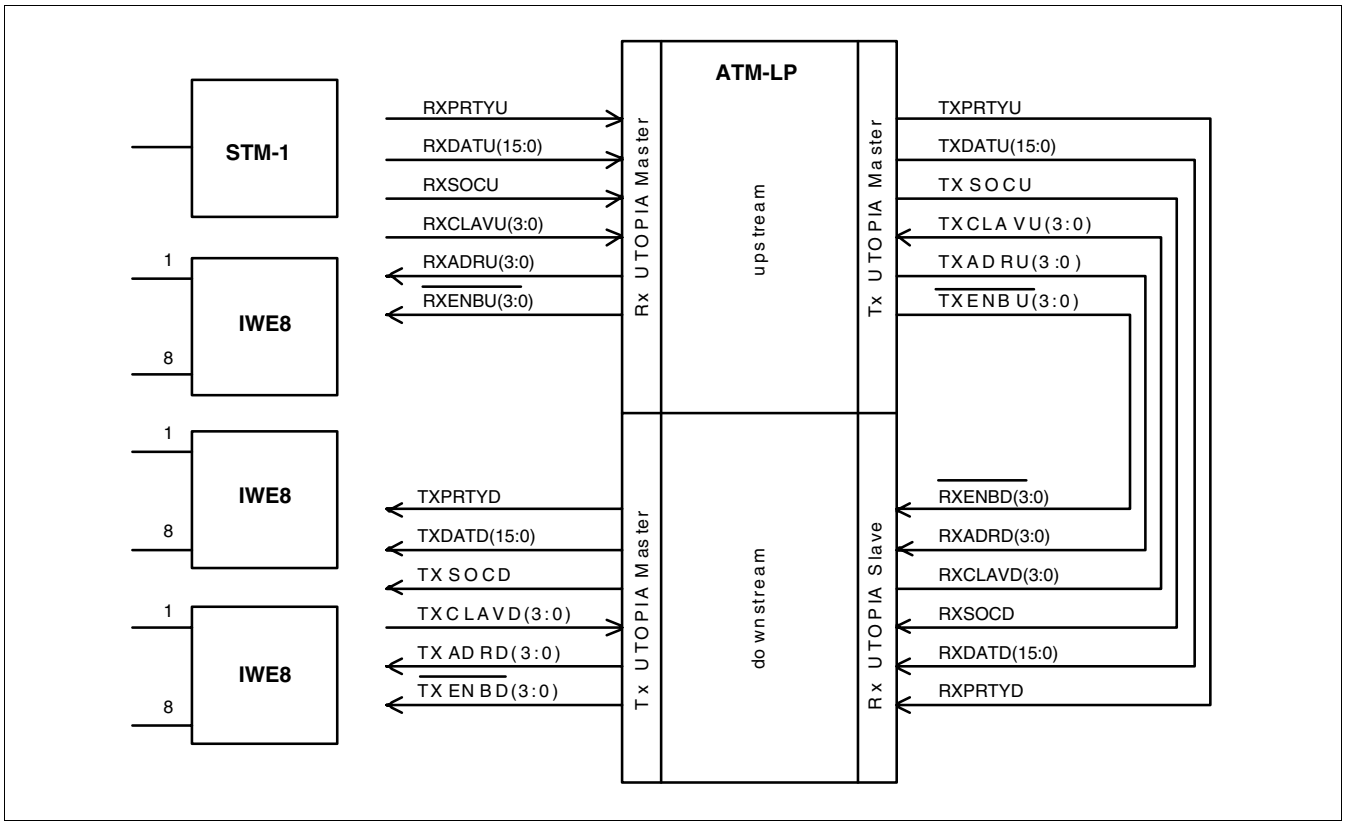


Figure 43 UTOPIA Interface Configuration with Master Mode for Tx and Slave Mode for Rx Direction at the ATM Side

The following table gives an overview over the UTOPIA signals:

Table 14 UTOPIA Interface Signals

xxDATy(15:0)	Data bus
xxADRy(3:0)	Address
xxPRTYy	Data path Parity
$\overline{\text{xxENBy}}$(3:0)	Enable
xxCLAVy(3:0)	Cell available
xxSOCy	Start of Cell
UTzzzCLK	UTOPIA clock

xx=RX: receive line / xx=TX: transmit line

y=U: upstream / y=D: downstream

zzz=PHY: PHY side / zzz=ATM: ATM side

Backpressure Mechanism

Backpressure means that cell transmission is disabled even if cells are available from the transmitting port of the preceding ASIC. In this case no $\overline{\text{RXENBU}}$ / RXCLAVD is set by the ATM-LP in response to an asserted RXCLAVU / $\overline{\text{TXENBD}}$.

Upstream line: A backpressure is only asserted if an adjacent ASIC asserts a backpressure to the ATM-LP.

Downstream line: A backpressure is asserted by the ATM-LP if an empty cell cycle time slot is needed, e.g. for microprocessor request or for cell insertion from the microprocessor add buffer, or in case of queue or buffer overflow of the statistical demultiplexing buffer. A PHY overflow leads only indirectly to a backpressure when the corresponding queue of the statistical multiplexing buffer overflows.

ATM-LP Throughput

Nominally the ATM-LP can cope with an UTOPIA frequency of up to F_{UTOPIA}=51,84 Mhz. However the average net cell rate over UTOPIA interface should be significantly lower due to the limits imposed by the time needed for internal data processing at the chosen ATM-LP core frequency F_{CORE}. The maximal allowed net UTOPIA throughput is given by:

$B_{UTMAX} = F_{CORE} * 53 * 8 / 32$ bit/s

{ATM cell: 53 * 8 bit}

{internal clock cycles per ATM cell: 32}

For F_{CORE} = 51,84 Mhz we get B_{UTMAX} = 686,88 Mbit/s.

However with this throughput no empty cell time slots in the ATM-LP core will occur which are necessary for microprocessor access to external RAMs, insertion of cells from the add buffer as well as the refresh of policing data. The latter one reduces the maximum allowed net throughput by about 1%, while the time needed for completing microprocessor requests is inversely proportional to the frequency of empty cell time slots. In order to be able to read out e.g. the billing counters of 16384 connections within a time interval smaller then 0,5 seconds, the maximal allowed net throughput has to be reduced by a further 3%.

5.2 External RAM Interface

The ATM-LP chip involves three RAM interfaces, CONNRAMUP and POLURAM for the upstream and CONNRAMDO for the downstream part. The RAM interfaces support access to the external synchronous SRAMs using bidirectional 32 bit data bus. The MSB of the data bus is used as parity signal.

Depending on the maximum number of connections supported two RAM types can be configured by the HW Pin AD25 (RAMVER). Connected to ground selects the 1M SSRAM(32k*32) and to high selects the 2M SSRAM (64k*32). The selection is identical for all three RAM Interfaces. The Toshiba RAM types TC55V1325FF-7 for 1M SSRAM and TC55V2325FF-7 for 2M SSRAM are recommended. Other RAM types should fulfil the specification of Toshiba.

CONNRAMUP

CONNRAMUP is used to store:

– Traffic counters.
– Parts of the internal header (namely HK bits).
– Control flags and internal pointers.

The connection data for one LCI requires 8 x 32bit words in the upstream connection RAM, so the whole CONNRAMUP has a capacity of 4Mbit for 16k connections or 2 Mbit for 8k connections. Up to 2 SSRAMs are supported.

POLURAM

The POLURAM is used to store:

– State variables and constant parameters of the policing algorithm.
– Control flags for UPC/NPC configuration.

The policing data for one LCI requires 11 x 32bit words in the policing RAM, so the whole POLURAM has a capacity of 6Mbit for 16k connections or 3 Mbit for 8k connections. The POLURAM can be omitted if no UPC/NPC is required. Up to 3 SSRAMs are supported.

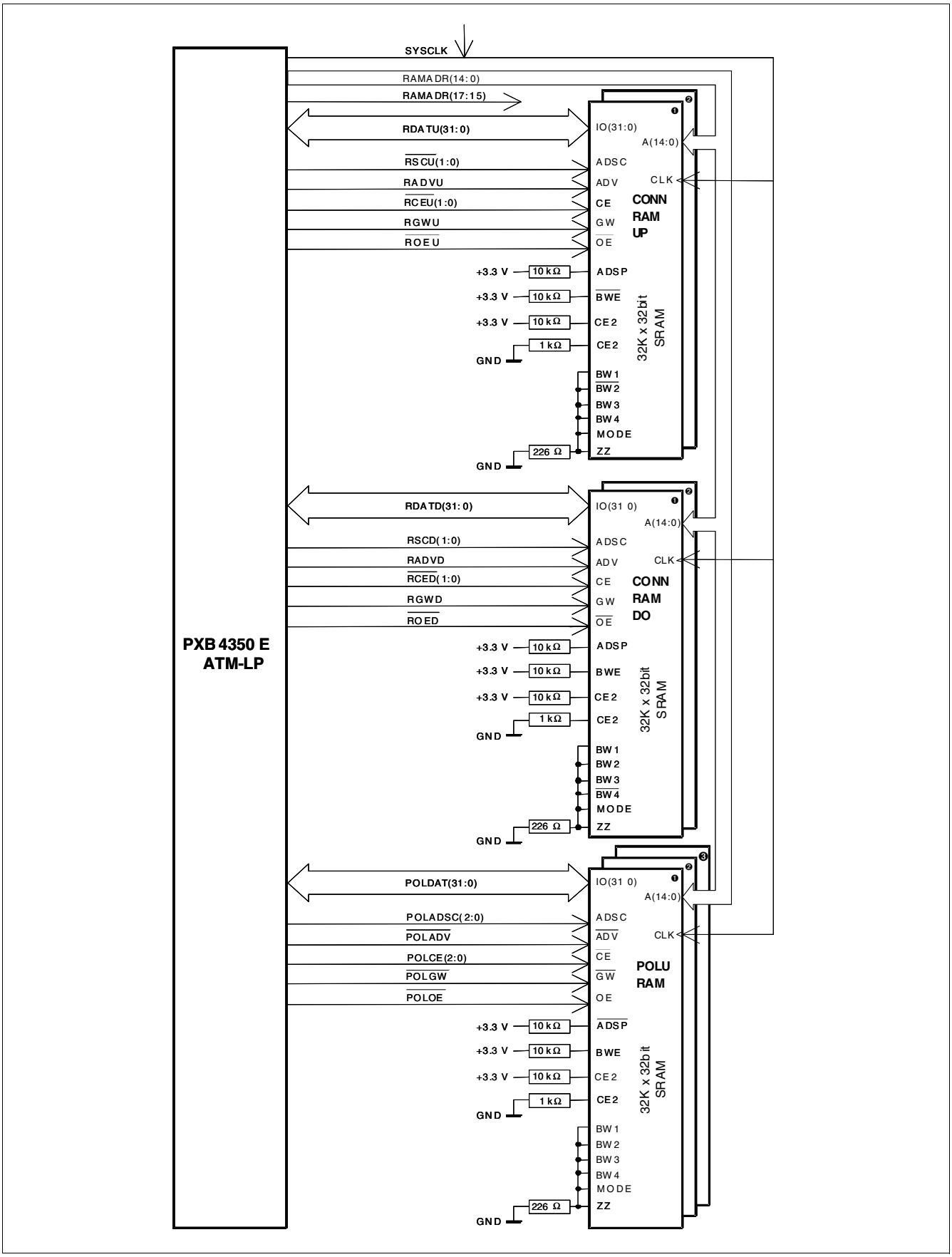


Figure 44 Connection RAM Upstream Interface Signals (using 1 Mbit SRAMs)

CONNRAMDO

The CONNRAMDO is used to store:

– Traffic Counters.
– The external header (i.e PN, VPI and VCI).
– For Multicast light the pointer to the next entry of the linked list.
– Control flags and internal pointers.

The connection data for one LCI requires 7 x 32bit words in the downstream connection RAM, so the whole CONNRAMDO has a capacity of 4Mbit for 16k connections or 2 Mbit for 8k connections. Up to 2 SSRAMs are supported.

The following table shows all possible RAM configurations of the ATM-LP for the usage of the 1M and 2M SSRAMs types depending on the selection of RAM types controlled by the HW-Pin RAMVERS and the number of needed connections. The POLURAM is not fully used for the support of 8k connections with 2M SSRAMs.

Table 15 Possible RAM Configurations of the ATM-LP

Number of supported Connections	16k		8k	
HW-Pin RAMVER (AD25)	0 for 1M	1 for 2M	0 for 1M	1 for 2M
Number of CONNRAMUP	-	2	2	1
Number of CONNRAMDO	-	2	2	1
Number of POLURAM	-	3	3	2

5.3 Microprocessor and Control Interface

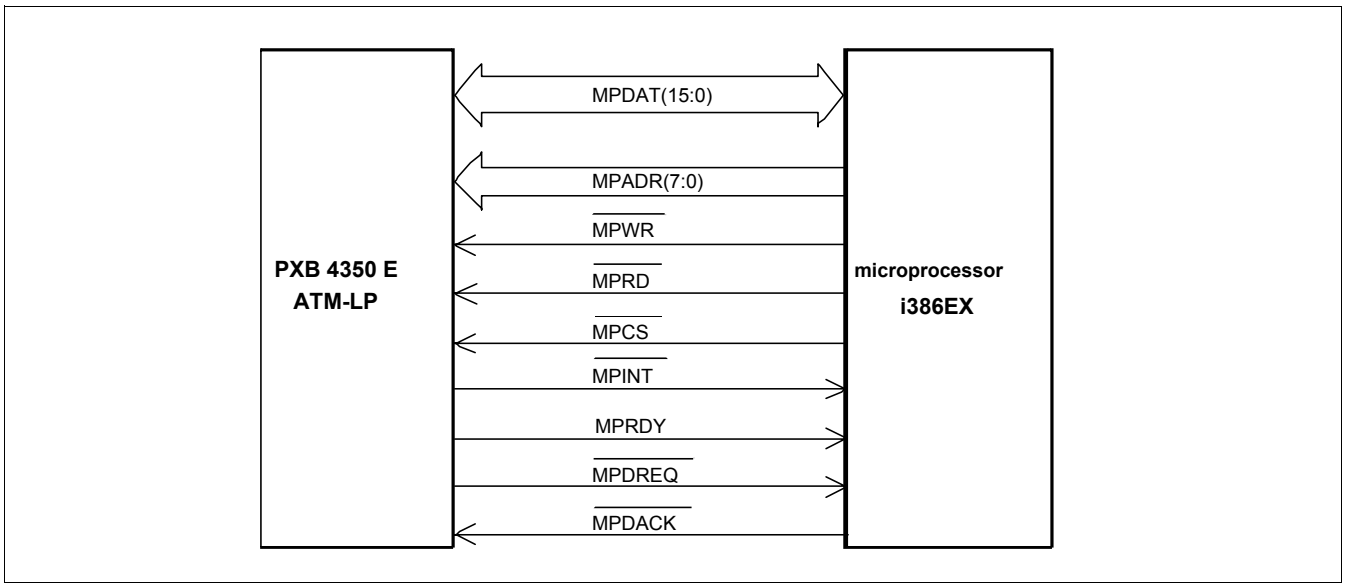


Figure 45 Microprocessor Interface

The ATM-LP chip has an asynchronous microprocessor interface. The interface consists of an 16 bit wide common data bus with 8 address lines as required for interfacing 80x86 processors. Bytewise access is not supported. The asynchronous bus access is working with a handshake mechanism for data flow control. During the inactive state the data bus is switched to high

impedance, it becomes active only when Chip Select is active.The pins MPDREQ and MPDACK are used for DMA access. When DMA buffer is not empty, the ATM-LP set the MPDREQ pin to zero. The microprocessor can now read the DMAR register and give a receipt by setting MPDACK to zero. If DMA buffer is empty, MPDREQ will be one.

Table 16 Microprocessor Interface Signals

Signal	Description
MPDAT(15:0)	Bidirectional common data bus between the microprocessor and the ATM-LP. Its signals will be tristated when MPCS or MPRDY is high.
MPADR(7:0)	Address bus for the interface.
MPWR	Write signal for the interface (active low).
MPRD	Read signal for the interface (active low).
MPCS	Chip Select signal used to address the ATM-LP (active low).
MPINT	Interrupt Request (active low). This pin is an open drain output.
MPDREQ	DMA request signal indicating that data is to be read out from the DMA buffer (active low). After the falling edge of the last possible read access (which empties the receive buffer), the MPDREQ pin becomes inactive within 60ns to avoid an additional read access of the microprocessor.
MPRDY	Ready output signal for microprocessor write and read access (active high). This pin is put low by the ATM-LP immediately after the falling edge of the microprocessor read or write signals MPRD/MPWR and remains inactive until the ATM-LP has put or get the required data via the bus MPDAT(15:0). During the first clock period after the low-high change it is driven high by the ASIC. Afterwards it is held high by a pull-up. During the inactive time of MPRDY the microprocessor performs wait states.

5.4 JTAG/Boundary Scan Interface

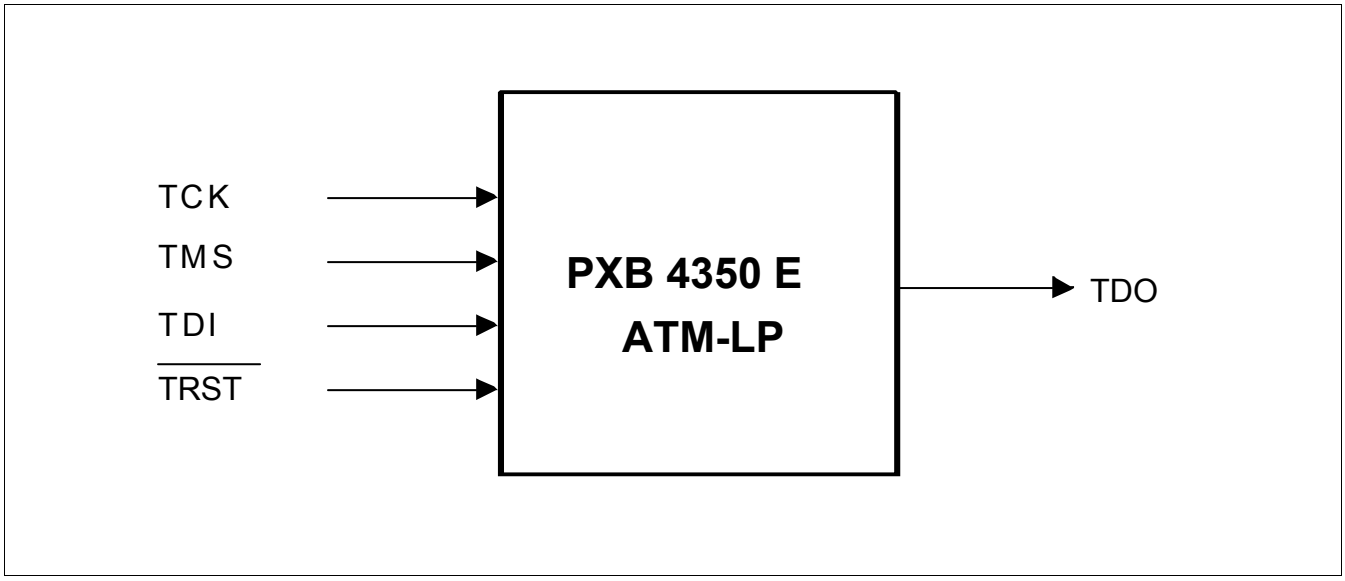


Figure 46 JTAG/Boundary Scan Interface

The JATG/boundary scan pins $\overline{\text{TRST}}$, TDI, TCK, TMS, and TDO are required for board test purposes. The boundary scan is conformal to IEEE 1149.1a (JTAG) serial test bus protocol and the specification [7]. The ID code of the ATM-LP can be read out from the boundary scan identity code register. The boundary scan ID number is 523B9069H. Additionally internal control pads are provided to switch specific output or input/output pins to tristate.

Table 17 Boundary Scan Interface

$\overline{\text{TRST}}$	Asynchronous Reset for the Test-Access-Port-Controller
TDI	Test Data Input with internal pull-up resistor
TCK	Test clock with internal pull-up resistor
TMS	Test Mode Select input with internal pull-up resistor
TDO	Test Data Output

Note: Control pad is active high and switches the corresponding pin or group of pins to tristate.

Table 18 ATM-LP Boundary Scan Table

Boundary Scan Number	PIN-Nr.	Signal-Name	Type
0	B24	$\overline{\text{MPCS}}$	I
1	A24	$\overline{\text{MPINT}}$	O
2	D22	$\overline{\text{MPDACK}}$	I
3	-	Control pad for $\overline{\text{MPDREQ}}$	-
4	B23	$\overline{\text{MPDREQ}}$	O
5	-	Control pad for MPRDY	-
6	C23	MPRDY	O
7	-	Control pad for MPDAT(15:0)	-
8	A23	MPDAT(0)	I/O
10	D21	MPDAT(1)	I/O
12	B22	MPDAT(2)	I/O
14	C22	MPDAT(3)	I/O
16	A22	MPDAT(4)	I/O
18	D20	MPDAT(5)	I/O
20	B21	MPDAT(6)	I/O
22	C21	MPDAT(7)	I/O
24	A21	MPDAT(8)	I/O
26	D19	MPDAT(9)	I/O
28	B20	MPDAT(10)	I/O

Table 18 ATM-LP Boundary Scan Table (cont'd)

Boundary Scan Number	PIN-Nr.	Signal-Name	Type
30	C20	MPDAT(11)	I/O
32	A20	MPDAT(12)	I/O
34	D18	MPDAT(13)	I/O
36	B19	MPDAT(14)	I/O
38	C19	MPDAT(15)	I/O
40	A19	RXDATU(0)	I
41	D17	RXDATU(1)	I
42	B18	RXDATU(2)	I
43	C18	RXDATU(3)	I
44	A18	RXDATU(4)	I
45	D16	RXDATU(5)	I
46	B17	RXDATU(6)	I
47	C17	RXDATU(7)	I
48	A17	RXDATU(8)	I
49	D15	RXDATU(9)	I
50	B16	RXDATU(10)	I
51	C16	RXDATU(11)	I
52	A16	RXDATU(12)	I
53	B15	RXDATU(13)	I
54	D14	RXDATU(14)	I
55	C15	RXDATU(15)	I
56	-	Control pad for RXADRU(3:0), $\overline{\text{RXENBU}}$(3:0), TXDATD(15:0), TXADRD(3:0), TXPRTYD, $\overline{\text{TXENBD}}$(3:0) and TXSOCD	-
57	A15	RXADRU(0)	O
58	B14	RXADRU(1)	O
59	A14	RXADRU(2)	O
60	C14	RXADRU(3)	O
61	C13	RXPRTYU	I
62	B13	$\overline{\text{RXENBU}}$(0)	O
63	A13	$\overline{\text{RXENBU}}$(1)	O

Table 18 ATM-LP Boundary Scan Table (cont'd)

Boundary Scan Number	PIN-Nr.	Signal-Name	Type
64	D13	$\overline{\text{RXENBU}}$(2)	O
65	C12	$\overline{\text{RXENBU}}$(3)	O
66	B12	RXCLAVU(0)	I
67	A12	RXCLAVU(1)	I
68	D12	RXCLAVU(2)	I
69	C11	RXCLAVU(3)	I
70	B11	RXSOCU	I
71	A11	UTPHYCLK	I
72	B10	TXDATD(0)	O
73	D11	TXDATD(1)	O
74	C10	TXDATD(2)	O
75	A10	TXDATD(3)	O
76	B9	TXDATD(4)	O
77	D10	TXDATD(5)	O
78	C9	TXDATD(6)	O
79	A9	TXDATD(7)	O
80	B8	TXDATD(8)	O
81	C8	TXDATD(9)	O
82	A8	TXDATD(10)	O
83	D9	TXDATD(11)	O
84	B7	TXDATD(12)	O
85	A7	TXDATD(13)	O
86	C7	TXDATD(14)	O
87	D8	TXDATD(15)	O
88	B6	TXADRD(0)	O
89	A6	TXADRD(1)	O
90	C6	TXADRD(2)	O
91	B5	TXADRD(3)	O
92	D7	TXPRTYD	O
93	C5	$\overline{\text{TXENBD}}$(0)	O

Table 18 ATM-LP Boundary Scan Table (cont'd)

Boundary Scan Number	PIN-Nr.	Signal-Name	Type
94	A5	$\overline{\text{TXENBD}}$(1)	O
95	B4	$\overline{\text{TXENBD}}$(2)	O
96	D6	$\overline{\text{TXENBD}}$(3)	O
97	C4	TXCLAVD(0)	I
98	A4	TXCLAVD(1)	I
99	B3	TXCLAVD(2)	I
100	D5	TXCLAVD(3)	I
101	A3	TXSOCD	O
102	-	Control pad for POLDAT(31:0)	-
103	B1	POLDAT(0)	I/O
105	C2	POLDAT(1)	I/O
107	C1	POLDAT(2)	I/O
109	E4	POLDAT(3)	I/O
111	D2	POLDAT(4)	I/O
113	D3	POLDAT(5)	I/O
115	D1	POLDAT(6)	I/O
117	F4	POLDAT(7)	I/O
119	E2	POLDAT(8)	I/O
121	E3	POLDAT(9)	I/O
123	E1	POLDAT(10)	I/O
125	G4	POLDAT(11)	I/O
127	F2	POLDAT(12)	I/O
129	F3	POLDAT(13)	I/O
131	F1	POLDAT(14)	I/O
133	H4	POLDAT(15)	I/O
135	G2	POLDAT(16)	I/O
137	G3	POLDAT(17)	I/O
139	G1	POLDAT(18)	I/O
141	J4	POLDAT(19)	I/O
143	H2	POLDAT(20)	I/O

Table 18 ATM-LP Boundary Scan Table (cont'd)

Boundary Scan Number	PIN-Nr.	Signal-Name	Type
145	H3	POLDAT(21)	I/O
147	H1	POLDAT(22)	I/O
149	K4	POLDAT(23)	I/O
151	J2	POLDAT(24)	I/O
153	J3	POLDAT(25)	I/O
155	J1	POLDAT(26)	I/O
157	L4	POLDAT(27)	I/O
159	K2	POLDAT(28)	I/O
161	K3	POLDAT(29)	I/O
163	K1	POLDAT(30)	I/O
165	M4	POLDAT(31)	I/O
167	L2	$\overline{\text{POLADSC}}$(0)	O
168	L3	$\overline{\text{POLADSC}}$(1)	O
169	L1	$\overline{\text{POLADSC}}$(2)	O
170	M2	$\overline{\text{POLADV}}$	O
171	N4	$\overline{\text{POLCE}}$(0)	O
172	M3	$\overline{\text{POLCE}}$(1)	O
173	M1	$\overline{\text{POLCE}}$(2)	O
174	N2	$\overline{\text{POLGW}}$	O
175	N1	$\overline{\text{POLOE}}$	O
176	-	Control pad for RDATU(31:0)	-
177	N3	RDATU(0)	I/O
179	P3	RDATU(1)	I/O
181	P2	RDATU(2)	I/O
183	P1	RDATU(3)	I/O
185	P4	RDATU(4)	I/O
187	R3	RDATU(5)	I/O
189	R2	RDATU(6)	I/O
191	R1	RDATU(7)	I/O
193	R4	RDATU(8)	I/O

Table 18 ATM-LP Boundary Scan Table (cont'd)

Boundary Scan Number	PIN-Nr.	Signal-Name	Type
195	T3	RDATU(9)	I/O
197	T2	RDATU(10)	I/O
199	T1	RDATU(11)	I/O
201	U2	RDATU(12)	I/O
203	T4	RDATU(13)	I/O
205	U3	RDATU(14)	I/O
207	U1	RDATU(15)	I/O
209	V2	RDATU(16)	I/O
211	U4	RDATU(17)	I/O
213	V3	RDATU(18)	I/O
215	V1	RDATU(19)	I/O
217	W2	RDATU(20)	I/O
219	W3	RDATU(21)	I/O
221	W1	RDATU(22)	I/O
223	V4	RDATU(23)	I/O
225	Y2	RDATU(24)	I/O
227	Y1	RDATU(25)	I/O
229	Y3	RDATU(26)	I/O
231	W4	RDATU(27)	I/O
233	AA2	RDATU(28)	I/O
235	AA1	RDATU(29)	I/O
237	AA3	RDATU(30)	I/O
239	AB2	RDATU(31)	I/O
241	Y4	$\overline{\text{RSCU}}$(0)	O
242	AB3	$\overline{\text{RSCU}}$(1)	O
243	AB1	$\overline{\text{RADVU}}$	O
244	AC2	$\overline{\text{RCEU}}$(0)	O
245	AA4	$\overline{\text{RCEU}}$(1)	O
246	AC3	$\overline{\text{RGWU}}$	O
247	AC1	$\overline{\text{ROEU}}$	O

Table 18 ATM-LP Boundary Scan Table (cont'd)

Boundary Scan Number	PIN-Nr.	Signal-Name	Type
248	AD2	RAMADR(0)	O
249	AB4	RAMADR(1)	O
250	AD1	RAMADR(2)	O
251	AF2	RAMADR(3)	O
252	AE3	RAMADR(4)	O
253	AF3	RAMADR(5)	O
254	AC5	RAMADR(6)	O
255	AE4	RAMADR(7)	O
256	AD4	RAMADR(8)	O
257	AF4	RAMADR(9)	O
258	AC6	RAMADR(10)	O
259	AE5	RAMADR(11)	O
260	AD5	RAMADR(12)	O
261	AF5	RAMADR(13)	O
262	AC7	RAMADR(14)	O
263	AE6	RAMADR(15)	O
264	AD6	RAMADR(16)	O
265	AF6	RAMADR(17)	O
266	-	Control pad for RDATD(31:0)	-
267	AC8	RDATD(0)	I/O
269	AE7	RDATD(1)	I/O
271	AD7	RDATD(2)	I/O
273	AF7	RDATD(3)	I/O
275	AC9	RDATD(4)	I/O
277	AE8	RDATD(5)	I/O
279	AD8	RDATD(6)	I/O
281	AF8	RDATD(7)	I/O
283	AC10	RDATD(8)	I/O
285	AE9	RDATD(9)	I/O
287	AD9	RDATD(10)	I/O

Table 18 ATM-LP Boundary Scan Table (cont'd)

Boundary Scan Number	PIN-Nr.	Signal-Name	Type
289	AF9	RDATD(11)	I/O
291	AC11	RDATD(12)	I/O
293	AE10	RDATD(13)	I/O
295	AD10	RDATD(14)	I/O
297	AF10	RDATD(15)	I/O
299	AC12	RDATD(16)	I/O
301	AE11	RDATD(17)	I/O
303	AD11	RDATD(18)	I/O
305	AF11	RDATD(19)	I/O
307	AE12	RDATD(20)	I/O
309	AC13	RDATD(21)	I/O
311	AD12	RDATD(22)	I/O
313	AF12	RDATD(23)	I/O
315	AE13	RDATD(24)	I/O
317	AF13	RDATD(25)	I/O
319	AD13	RDATD(26)	I/O
321	AD14	RDATD(27)	I/O
323	AE14	RDATD(28)	I/O
325	AF14	RDATD(29)	I/O
327	AC14	RDATD(30)	I/O
329	AD15	RDATD(31)	I/O
331	AE15	$\overline{\text{RSCD}}$(0)	O
332	AF15	$\overline{\text{RSCD}}$(1)	O
333	AC15	$\overline{\text{RADVD}}$	O
334	AD16	$\overline{\text{RCED}}$(0)	O
335	AE16	$\overline{\text{RCED}}$(1)	O
336	AF16	$\overline{\text{RGWD}}$	O
337	AE17	$\overline{\text{ROED}}$	O
338	AC16	SYSCLK	I
339	AD17	$\overline{\text{RESET}}$	I

Table 18 ATM-LP Boundary Scan Table (cont'd)

Boundary Scan Number	PIN-Nr.	Signal-Name	Type
340	-	Control pad for ARCDAT(16:0)	-
341	AF17	ARCDAT(0)	I/O
343	AE18	ARCDAT(1)	I/O
345	AC17	ARCDAT(2)	I/O
347	AD18	ARCDAT(3)	I/O
349	AF18	ARCDAT(4)	I/O
351	AE19	ARCDAT(5)	I/O
353	AD19	ARCDAT(6)	I/O
355	AF19	ARCDAT(7)	I/O
357	AC18	ARCDAT(8)	I/O
359	AE20	ARCDAT(9)	I/O
361	AF20	ARCDAT(10)	I/O
363	AD20	ARCDAT(11)	I/O
365	AC19	ARCDAT(12)	I/O
367	AE21	ARCDAT(13)	I/O
369	AF21	ARCDAT(14)	I/O
371	AD21	ARCDAT(15)	I/O
373	AE22	ARCDAT(16)	I/O
375	AC20	ARCADR(0)	O
376	AD22	ARCADR(1)	O
377	AF22	ARCADR(2)	O
378	AE23	ARCADR(3)	O
379	AC21	$\overline{\text{ARCRES}}$	O
380	AD23	$\overline{\text{ARCCS}}$	O
381	AF23	$\overline{\text{ARCWE}}$	O
382	AE24	$\overline{\text{ARCOE}}$	O
383	AC22	ARCCLK	O
384	AF24	SMODE	I
385	AE26	SENAB	I
386	AD25	RAMVERS	I

Table 18 ATM-LP Boundary Scan Table (cont'd)

Boundary Scan Number	PIN-Nr.	Signal-Name	Type
387	-	Control pad for RXCLAVD(0)	-
388	-	Control pad for RXCLAVD(1)	-
389	-	Control pad for RXCLAVD(2)	-
390	-	Control pad for RXCLAVD(3)	-
391	AC26	RXCLAVD(0)	I/O
393	AA23	RXCLAVD(1)	I/O
395	AB25	RXCLAVD(2)	I/O
397	AB24	RXCLAVD(3)	I/O
399	AB26	RXDATD(0)	I
400	Y23	RXDATD(1)	I
401	AA25	RXDATD(2)	I
402	AA24	RXDATD(3)	I
403	AA26	RXDATD(4)	I
404	W23	RXDATD(5)	I
405	Y25	RXDATD(6)	I
406	Y24	RXDATD(7)	I
407	Y26	RXDATD(8)	I
408	V23	RXDATD(9)	I
409	W25	RXDATD(10)	I
410	W24	RXDATD(11)	I
411	W26	RXDATD(12)	I
412	U23	RXDATD(13)	I
413	V25	RXDATD(14)	I
414	V24	RXDATD(15)	I
415	V26	RXPRTYD	I
416	-	Control pad for RXADRD(3:0) and $\overline{\text{RXENBD}}$(3:0)	-
417	T23	RXADRD(0)	I/O
419	U25	RXADRD(1)	I/O
421	U24	RXADRD(2)	I/O
423	U26	RXADRD(3)	I/O

Table 18 ATM-LP Boundary Scan Table (cont'd)

Boundary Scan Number	PIN-Nr.	Signal-Name	Type
425	R23	$\overline{\text{RXENBD}}$(0)	I/O
427	T25	$\overline{\text{RXENBD}}$(1)	I/O
429	T24	$\overline{\text{RXENBD}}$(2)	I/O
431	T26	$\overline{\text{RXENBD}}$(3)	I/O
433	R25	RXSOCD	I
434	P23	TXMS	I
435	R24	RXMS	I
436	R26	UTATMCLK	I
437	-	Control pad for TXDATU(15:0), TXPRTYU and TXSOCU	-
438	P26	TXDATU(0)	O
439	P24	TXDATU(1)	O
440	N24	TXDATU(2)	O
441	N25	TXDATU(3)	O
442	N26	TXDATU(4)	O
443	N23	TXDATU(5)	O
444	M24	TXDATU(6)	O
445	M25	TXDATU(7)	O
446	M26	TXDATU(8)	O
447	M23	TXDATU(9)	O
448	L24	TXDATU(10)	O
449	L25	TXDATU(11)	O
450	L26	TXDATU(12)	O
451	K25	TXDATU(13)	O
452	L23	TXDATU(14)	O
453	K24	TXDATU(15)	O
454	K26	TXPRTYU	O
455	-	Control pad for TXCLAVU(0)	-
456	-	Control pad for TXCLAVU(1)	-
457	-	Control pad for TXCLAVU(2)	-
458	-	Control pad for TXCLAVU(3)	-

Table 18 ATM-LP Boundary Scan Table (cont'd)

Boundary Scan Number	PIN-Nr.	Signal-Name	Type
459	J25	TXCLAVU(0)	I/O
461	K23	TXCLAVU(1)	I/O
463	J24	TXCLAVU(2)	I/O
465	J26	TXCLAVU(3)	I/O
467	H25	TXSOCU	O
468	-	Control pad for TXADRU(3:0) and $\overline{\text{TXENBU}}$(3:0)	-
469	H24	TXADRU(0)	I/O
471	H26	TXADRU(1)	I/O
473	J23	TXADRU(2)	I/O
475	G25	TXADRU(3)	I/O
477	G26	$\overline{\text{TXENBU}}$(0)	I/O
479	G24	$\overline{\text{TXENBU}}$(1)	I/O
481	H23	$\overline{\text{TXENBU}}$(2)	I/O
483	F25	$\overline{\text{TXENBU}}$(3)	I/O
485	F26	MPADR(0)	I
486	F24	MPADR(1)	I
487	E25	MPADR(2)	I
488	G23	MPADR(3)	I
489	E24	MPADR(4)	I
490	E26	MPADR(5)	I
491	D25	MPADR(6)	I
492	F23	MPADR(7)	I
493	D24	$\overline{\text{MPWR}}$	I
494	D26	$\overline{\text{MPRD}}$	I

5.5 Clock And Reset Interface

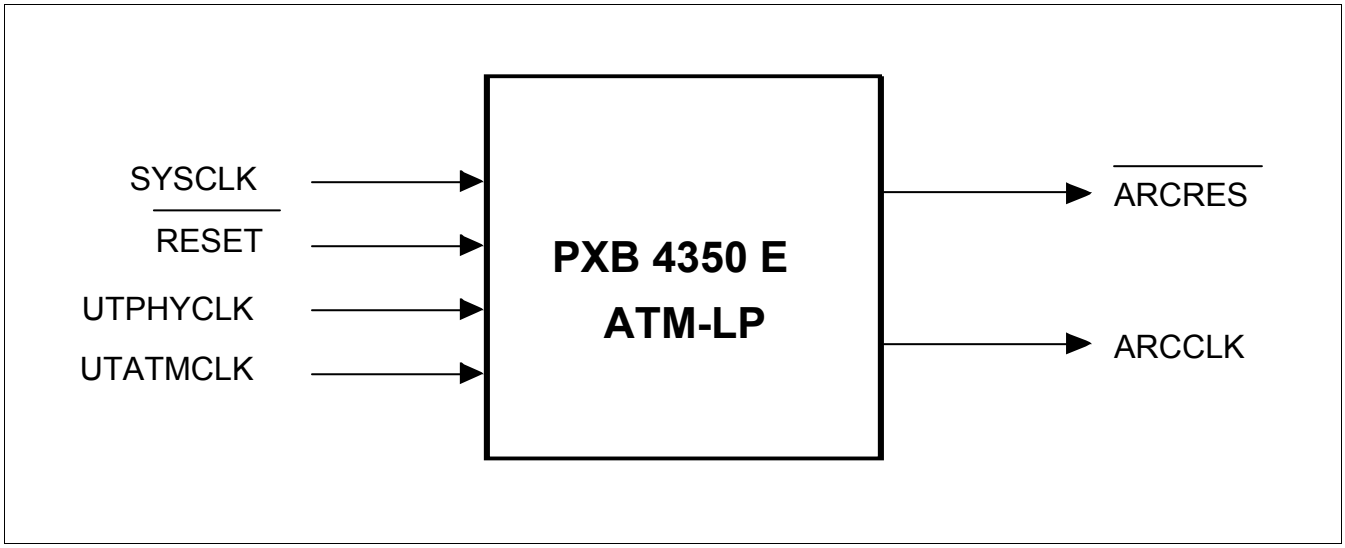


Figure 47 Clock and Reset Interface

ATM-LP System Clock (SYSCLK):

The ATM-LP system (core) clock range is 25 MHz up to 51.84 Mhz.

Reset Input Signal ($\overline{\text{RESET}}$):

The $\overline{\text{RESET}}$ signal is fed in via a LVTTL-compatible input. With low level (GND) it causes an asynchronous reset of the internal circuit. The reset must be asserted for a minimum of four clock cycles. After the reset is accepted the outputs are hold in inactive state and all bidirectional I/Os are switched to tristate until $\overline{\text{RESET}}$ is released. At the low to high transition on the $\overline{\text{RESET}}$ line follows an internal synchronous reset.

UTOPIA clocks (UTPHYCLK, UTATMCLK):

Two UTOPIA clock inputs (one for the PHY- and one for the ATM- side), independent from each other and from SYSCLK, must be provided. The frequency of the UTOPIA clocks must be lower than or equal to SYSCLK.

CAME clock (ARCCLK):

It is derived from SYSCLK by dividing frequency by a factor of two.

CAME Reset Output Signal ($\overline{\text{ARCRES}}$):

It is a LVCMOS low active output. It is asserted by ATM-LP for four SYSCLK periods after the rising edge of $\overline{\text{RESET}}$.

5.6 CAME Interface

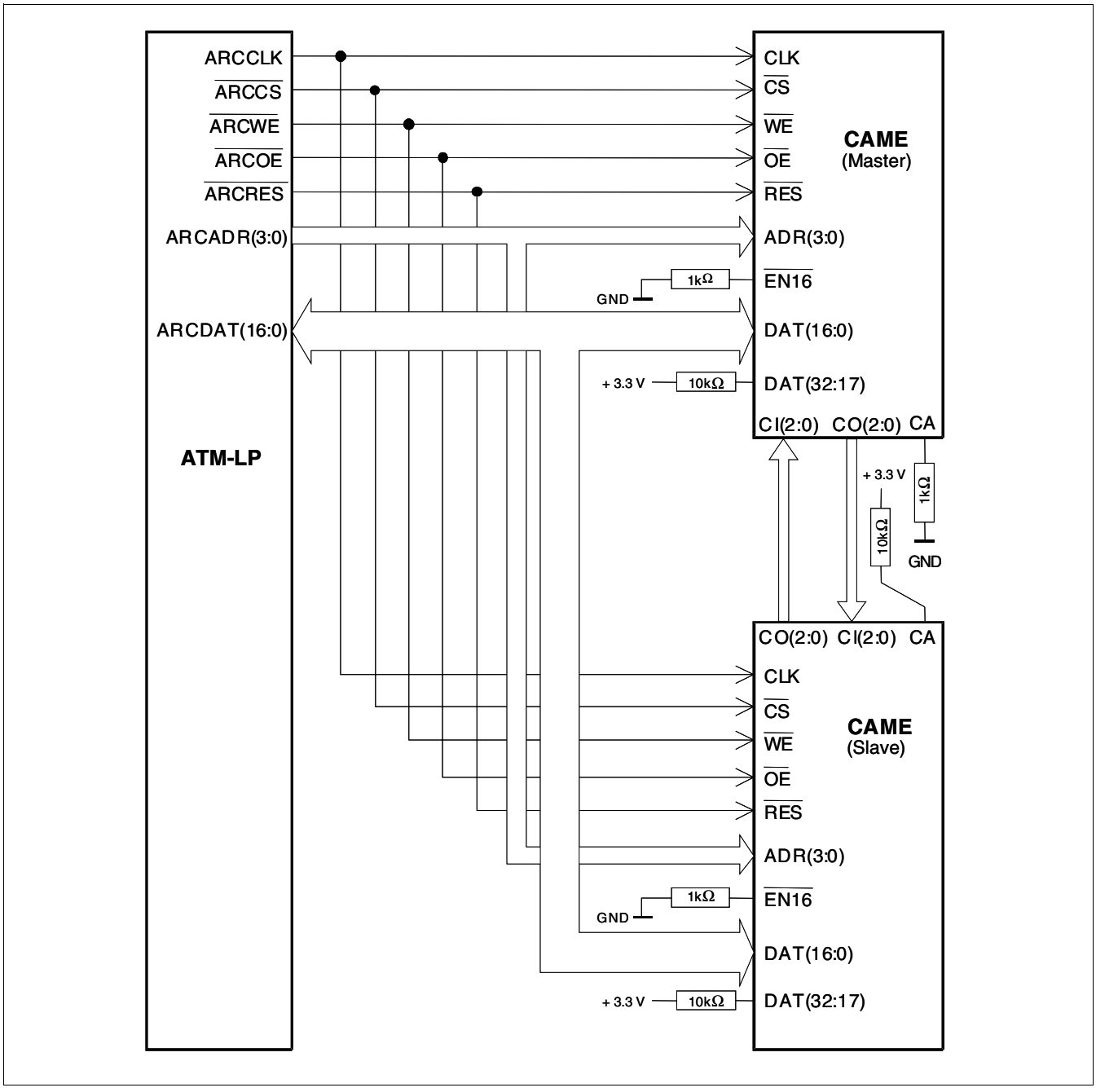


Figure 48 CAME Interface for 16k Connections

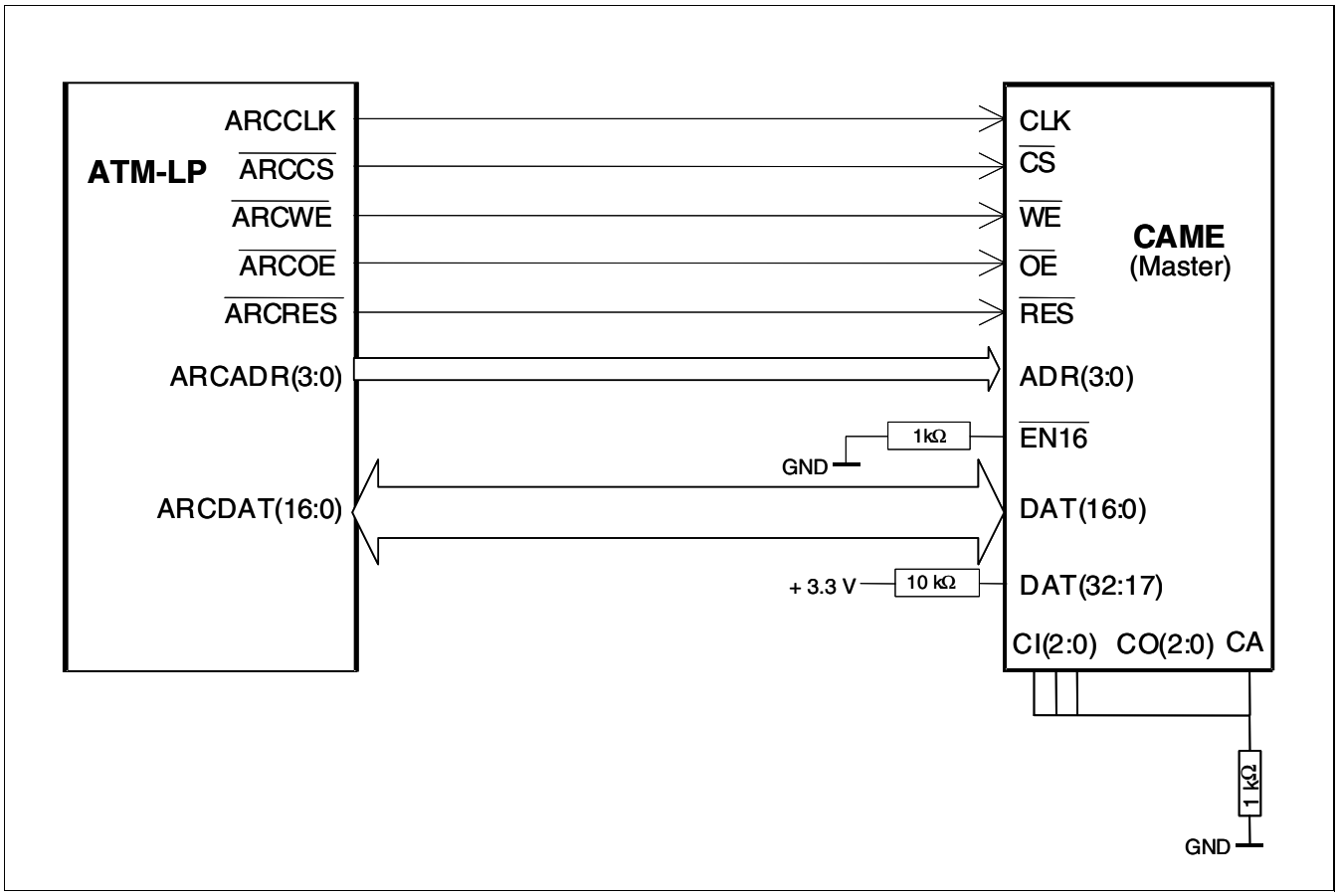


Figure 49 CAME Interface for 8k Connections

For the address reduction of the 32 bit input address consisting of concatenated PN/VPI/VCI values down to the 14 bit LCI up to two parallel cascaded CAME chips are supported. From the ATM-LP's perspective they behave like a single chip.

In NNI mode the sum of the length of PN (up to 6 bit), VPI (12bit) and VCI (16bit) exceed 32bit, which can be maximally processed by CAME.
In this case only the (16 - (number of PN bits)) least significant VPI bits are mapped into the input address.

During the connection setup the CAMEs are initialized by SW, i.e. the input addresses (PN/VPI/VCI) of valid connections are stored at the addresses of the corresponding LCIs. At cell arrival an inverse operation is performed: The PN/VPI/VCI value of the cell is passed to the CAMEs, which search for an corresponding entry and return its LCI.

In some important cases (e.g. the ATM-LP is configurated as an intermediate point of a virtual path, or F4-OAM cells are received at a virtual path terminating point) pure PN/VPI translation takes place and the VCI part is ignored.

ARCCLK is half of the ATM-LP core frequency given by SYSCLK.

5.6.1 Data Structure at CAME Data Bus

CAME Data bit(16) is used as parity line and completes the ARCDAT(1:15) and ACRADR(0:3) to odd parity.

Search processing for OAM F4 Flow

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write to address C_H	PN(3:0)				VPI(11:0)											
Wait for command execution																
Read from address 6_H	V	I	LCI(13:0)													
Read from address E_H													S3	S2	S1	S0

Search processing for user cells

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write to address D_H	PN(3:0)				VPI(11:0)											
Write to address 5_H	VCI(15:0)															
Wait for command execution																
Read from address 6_H	V	I	LCI(13:0)													
Read from address E_H													S3	S2	S1	S0

Search processing activated via the microprocessor

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write to address E_H	PN(3:0)				VPI(11:0)											
Write to address 6_H	VCI(15:0)															
Wait for command execution																
Read from address 6_H	V	I	LCI(13:0)													
Read from address E_H													S3	S2	S1	S0

CAME Write command for configuration of the connection

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write to address 2_H	V	I	LCI(13:0)													
Write to address B_H	PN(3:0)				VPI(11:0)											
Write to address 3_H	VCI(15:0)															
Wait for command execution																
Read from address 6_H																
Read from address E_H													S3	S2	S1	S0

CAME Read command for verification of the connection entry

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write to address 0_H			LCI(13:0)													
Wait for command execution																
Read from address 1_H	PN(3:0)				VPI(11:0)											
Read from address 9_H	VCI(15:0)															
Read from address 6_H	V	I														
Read from address E_H													S3	S2	S1	S0

CAME Test and Configuration command

bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Write to address 7_H			Testmode(13:0)													
Wait for command execution																
Read from address 7_H			Testmode(13:0)													
Read from address F_H													S3	S2	S1	S0

5.7 Test Interface

There are several additional test pins provided for board test. Please let them unconnected or connected to ground as described in section 1.4, part "Additional Testpins".

6 Electrical Characteristics

6.1 Absolute Maximum Ratings

Table 19 Absolute Maximum Ratings

Parameter	Symbol	Limit Values	Unit
Storage Temperature	T_S	-40 to 125	°C
Junction Temperature	T_J	max. 125	°C
Supply Voltage	V_{DD}	-0.3 to 3.9	V
Input Voltage for 3.3V pads	V_{IN}	-1.0 to V_{DD}+0.3	V
Input Voltage for 5V compatible pads	V_{IN}	-1.0 to 6.5	V
Output Voltage	V_{OUT}		V
DC Input Currents	I_{IN}	-10 to 10	µA
Power Dissipation	P_V	1.7	W

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

6.2 Operating Conditions

Table 20 Operating Conditions

Parameter	Symbol	Limit Values	Unit
Supply voltage	V_{DD}	3.14 to 3.47	V
Ground	V_{SS}	0	V
Ambient temperature under bias	T_A	-45 to 85	°C
Junction temperature	T_J	max. 110	°C

6.3 DC Characteristics for all Interfaces

Table 21 DC Characteristics

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Supply Voltage	V_{DD}	3.14	3.3	3.47	V	
Input Low Voltage	V_{IL}	V_{SS} -0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{DD} +0.3	V	LVTTL (3.3V)
		2.0		5.5	V	5-Volt compatible
Switching Threshold	V_T		1.4	2.0	V	
Input Current	I_{IN}	-10	-1..+1	10	µA	V_{IN}=V_{DD} or V_{SS}
		35	115	222	µA	V_{IN}=V_{DD} for Inputs with Pulldown resistors
		-35	-115	-214	µA	V_{IN}=V_{SS} for Inputs with Pullup resistors
Output High Voltage	V_{OH}	2.4		V_{DD}	V	I_{OH}= - 4 mA
Output Low Voltage	V_{OL}		0.2	0.4	V	I_{OH}= 4 mA
Three-state Output Leakage Current	I_{OZ}	-10	-1..+1	10	µA	
Input Capacitance	C_{IN}	2.5		5	pF	
Output Capacitance	C_{OUT}	2		5	pF	

Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at T_A = 25°C and the given supply voltage.

6.4 Capacitances

Table 22 Capacitances

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Input Capacitance	C_{IN}	2.5	5	pF
Output Capacitance	C_{OUT}	2	5	pF
Load Capacitance at:				
UTOPIA PHY side	C_{FO1}		85	pF
RAMADR(17:0)_____	C_{FO2}		85	pF
MPDAT(15:0), MPRD	C_{FO3}		50	pF
POLURAMDAT(31:0)	C_{FO4}		40	pF
other outputs	C_{FO5}		30	pF

6.5 AC Characteristics

T_A = -40 to 85°C , V_{CC} = 3.3 V ± 5 % , V_{SS} = 0 V

All inputs are driven to V_{IH} = 2.4 V for a logical “1”
and to V_{IL} = 0.4 V for a logical “0”

All outputs are measured at V_H = 2.0 V for a logical “1”
and at V_L = 0.8 V for a logical “0”

The AC testing input/output waveforms are shown below.

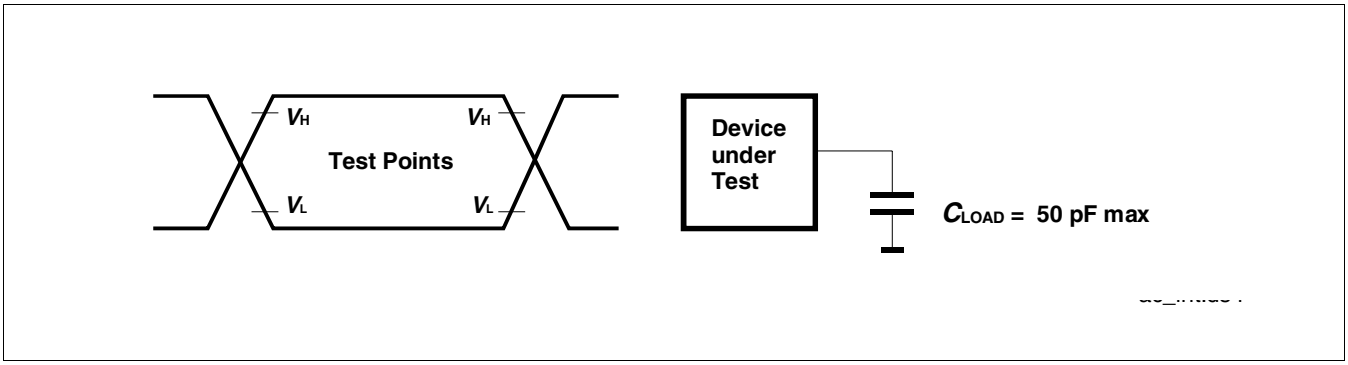


Figure 50 Input/Output Waveform for AC Measurements

6.5.1 Clock and Reset Interface

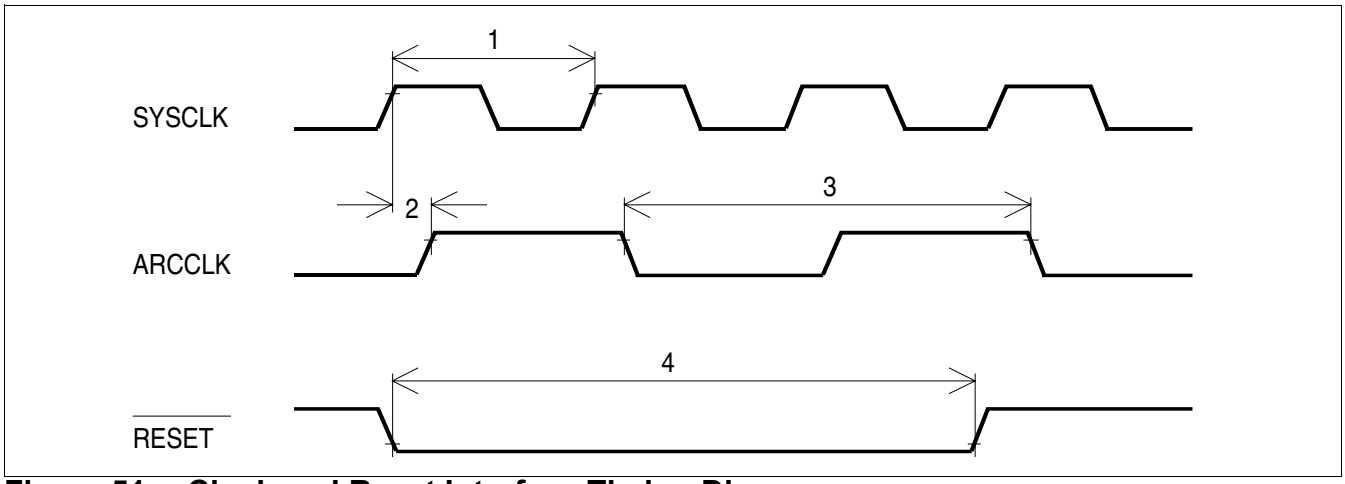


Figure 51 Clock and Reset Interface Timing Diagram

Table 23 Clock and Reset Interface AC Timing Characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	T_{SYSCLK} : Period SYSCLK	19.3			ns
1A	F_{SYSCLK} : Frequency SYSCLK			51.84	MHz
2	Delay SYSCLK to ARCCLK	3		15	ns
3	T_{ARCCLK} : Period ARCCLK	38.6			ns
3A	F_{ARCCLK} : Frequency ARCCLK			25.92	MHz
4	Pulse width $\overline{\text{RESET}}$ low	5			T_{SYSCLK}

Table 24 Clock Frequencies

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Core-clock	SYSCLK	25	51.84	MHz
UTOPIA clock at PHY-side	UTPHYCLK		$<f_{SYSCLK}$	MHz
UTOPIA clock at ATM-side	UTATMCLK		$<f_{SYSCLK}$	MHz
µP clock[1)]			$<f_{SYSCLK}/2$	MHz

[1)] Supplied only to i386EX µP

6.5.2 DMA Interface

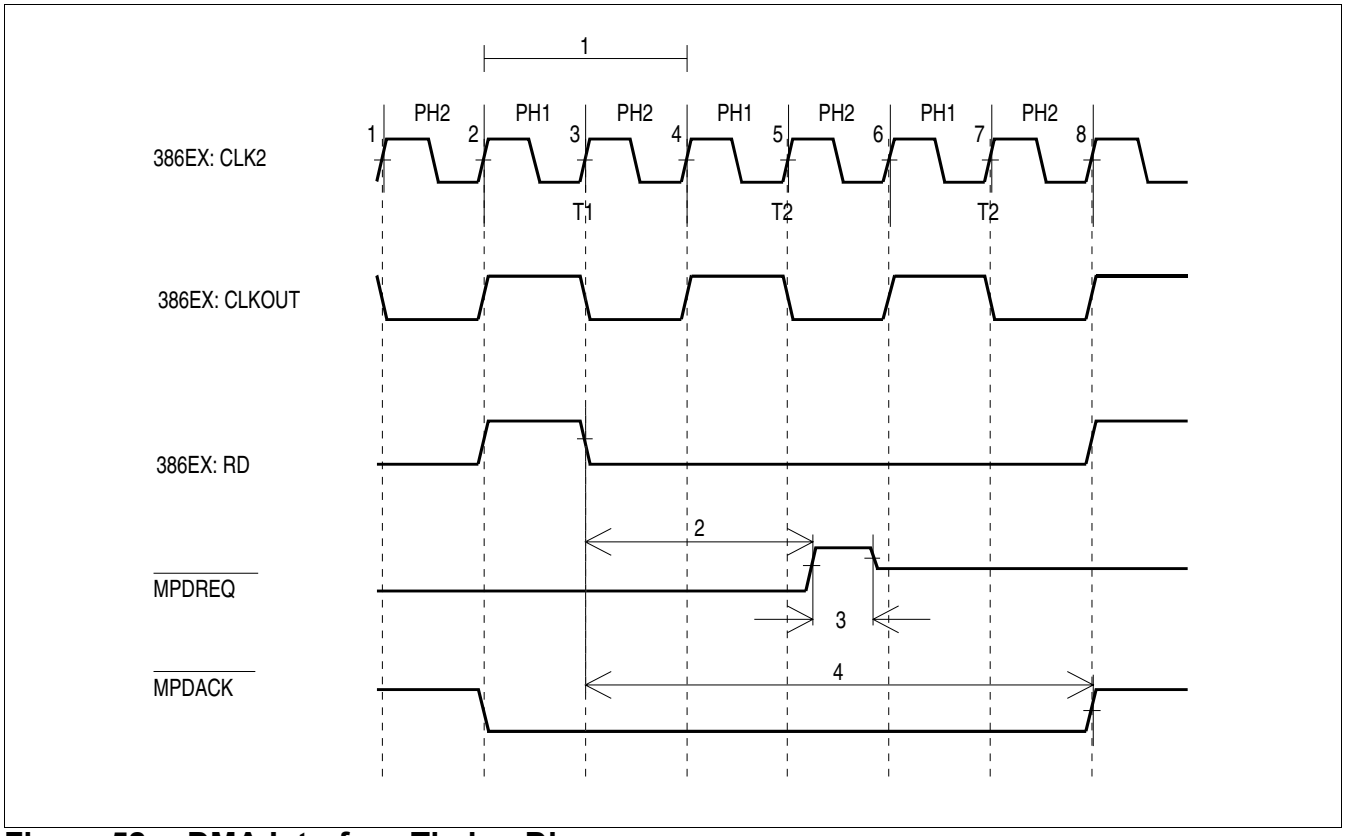


Figure 52 DMA Interface Timing Diagram

Table 25 Clock and Reset Interface AC Timing Characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	T_{CLK2} : Period CLK2		40		ns
1A	F_{CLK2} : Frequency CLK2		25		MHz
2	$T_{RDMPDREQ}$		90		ns
3	T_{SYSCLK} : Period SYSCLK		T_{SYSCLK}		ns
4	$T_{RDMPACK}$		200		ns

6.5.3 UTOPIA Interface

The AC Characteristic of the UTOPIA Interface fulfils the UTOPIA Standard [1 and 2].

6.5.4 SRAM Interface

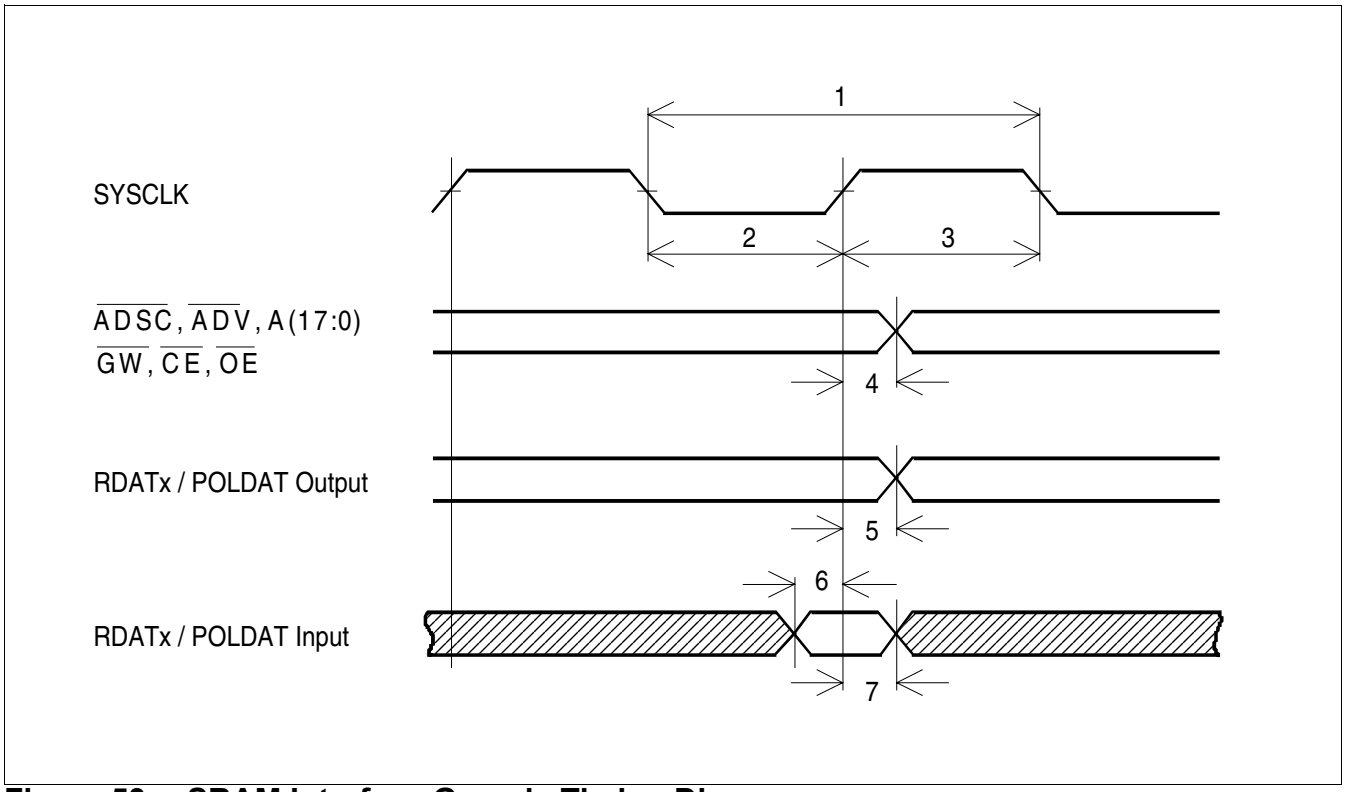


Figure 53 SRAM Interface Generic Timing Diagram

Table 26 SRAM Interface AC Timing Characteristics for 80pF Load

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	T_{SYSCLK} : Period SYSCLK	19.3			ns
1A	F_{SYSCLK} : Frequency SYSCLK			51.84	MHz
2	SYSCLK Low Pulse Width	40		60	%
3	SYSCLK High Pulse Width	40		60	%
4	Delay SYSCLK rising to $\overline{ADSC}$, $\overline{ADV}$, A(14:0), $\overline{GW}$, $\overline{CE}$, $\overline{OE}$	2		15	ns
5	Delay SYSCLK rising to RDATx / POLDAT Output	2		15	ns
6	Setup time RDATx / POLDAT Input before SYSCLK rising (all read cycles)	10			ns
7	Hold time RDATx / POLDAT Input after SYSCLK rising (all read cycles)	2			ns

Note: The SSRAM interface is designed to fulfil the Toshiba SSRAM specification (Type TC55V1325FF-7 (1M SSRAM (32k x 32)) or Type TC55V2325FF-7 (2M SSRAM (64k x 32))). If other SSRAM's are used please check whether these are compliant to Toshiba. The ATM-LP does not use the BWE, ADSP and Snooze mode.

6.5.5 Microprocessor Interface

6.5.5.1 Microprocessor Write Cycle

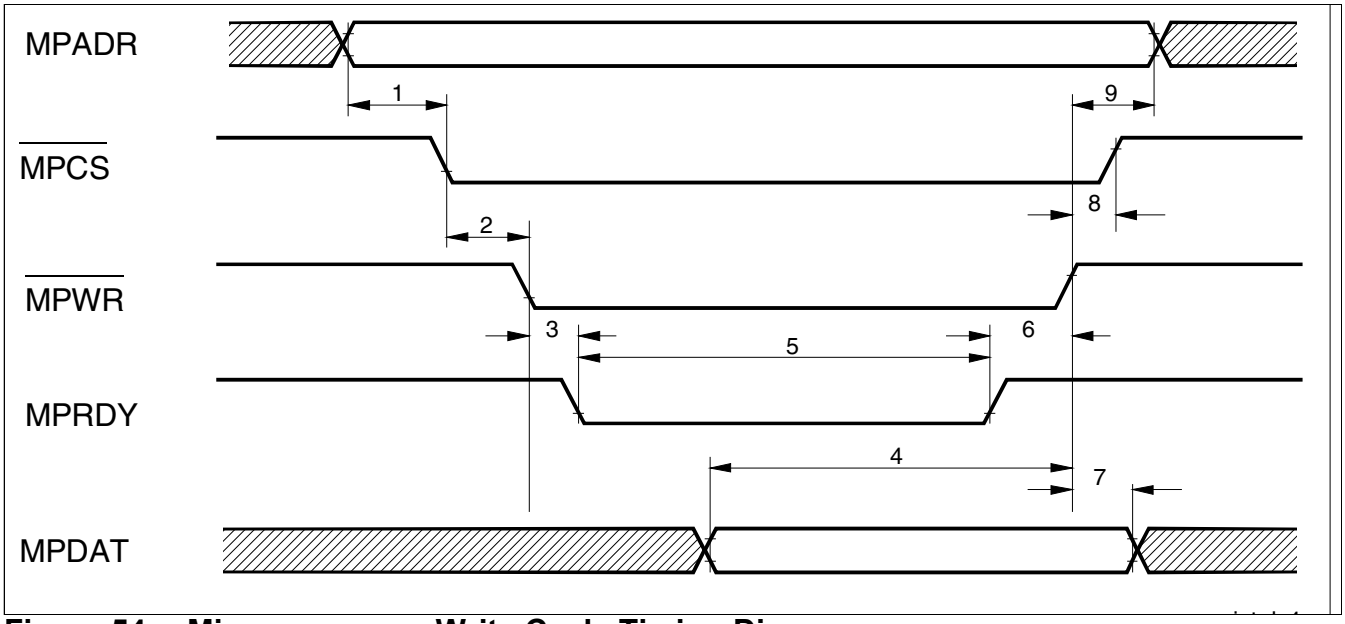


Figure 54 Microprocessor Write Cycle Timing Diagram

Table 27 Microprocessor Write Cycle AC Timing Characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	Setup time MPADR before $\overline{\text{MPCS}}$ low	0			ns
2	Setup time $\overline{\text{MPCS}}$ before $\overline{\text{MPWR}}$ low	0			ns
3	Delay MPRDY low after $\overline{\text{MPWR}}$ low	1		15	ns
4	MPDAT setup time before $\overline{\text{MPWR}}$ high	5			ns
5	Pulse width MPRDY low	3 x T_{clock}		4 x T_{clock}	ns
6	MPRDY high to $\overline{\text{MPWR}}$ high	10			ns
7	Hold time MPDAT after $\overline{\text{MPWR}}$ high	5			ns
8	Hold time $\overline{\text{MPCS}}$ after $\overline{\text{MPWR}}$ high	5			ns
9	Hold time MPADR after $\overline{\text{MPWR}}$ high	5			ns

6.5.5.2 Microprocessor Read Cycle

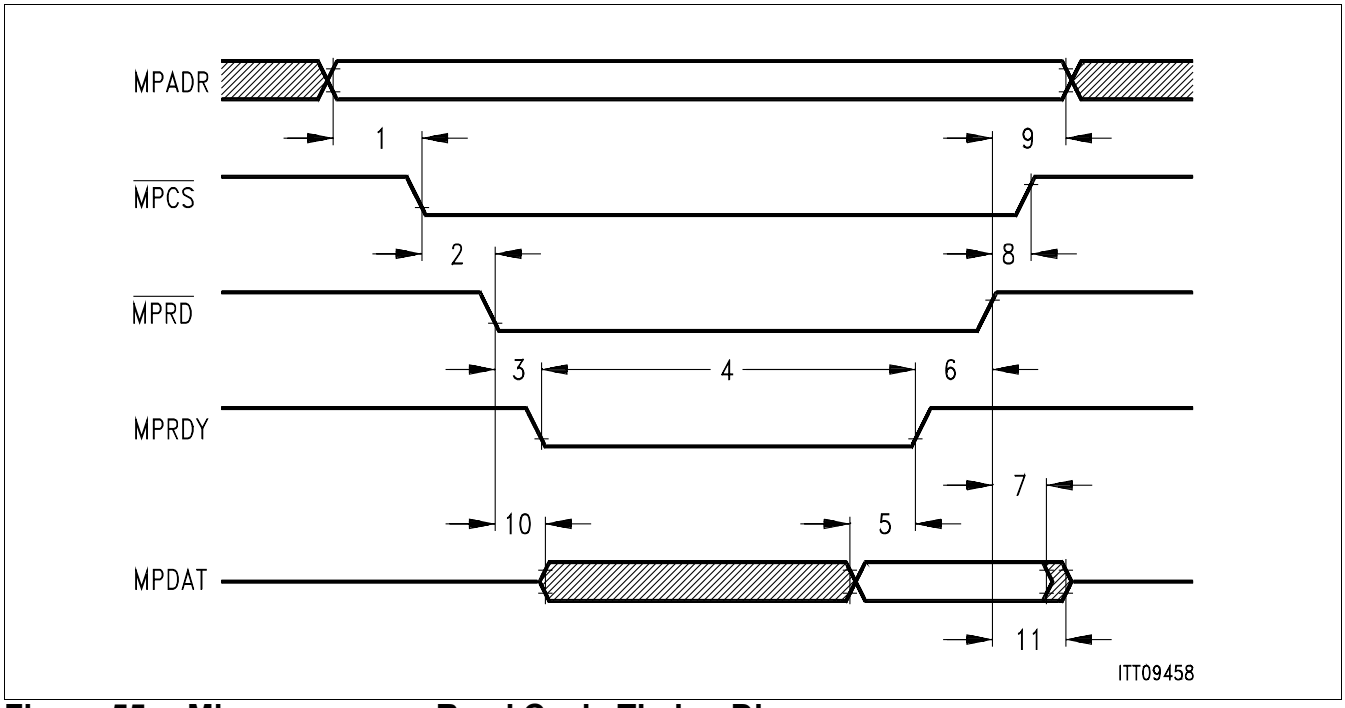


Figure 55 Microprocessor Read Cycle Timing Diagram

Table 28 Microprocessor Read Cycle AC Timing Characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	Setup time MPADR before $\overline{\text{MPCS}}$ low	0			ns
2	Setup time $\overline{\text{MPCS}}$ before $\overline{\text{MPRD}}$ low	0			ns
3	Delay MPRDY low after $\overline{\text{MPRD}}$ low	1		15	ns
4	Pulse width MPRDY low	4 x T_{clock}		5 x T_{clock}	ns
5	MPDAT valid before MPRDY high	5			ns
6	MPRDY high to $\overline{\text{MPRD}}$ high	5			ns
7	Hold time MPDAT after $\overline{\text{MPRD}}$ high	2			ns
8	Hold time $\overline{\text{MPCS}}$ after $\overline{\text{MPRD}}$ high	5			ns
9	Hold time MPADR after $\overline{\text{MPRD}}$ high	5			ns
10	Delay $\overline{\text{MPRD}}$ low to MPDAT low impedance	1		15	ns
11	Delay $\overline{\text{MPRD}}$ high to MPDAT high impedance	1		15	ns

6.5.6 Boundary-Scan Test Interface

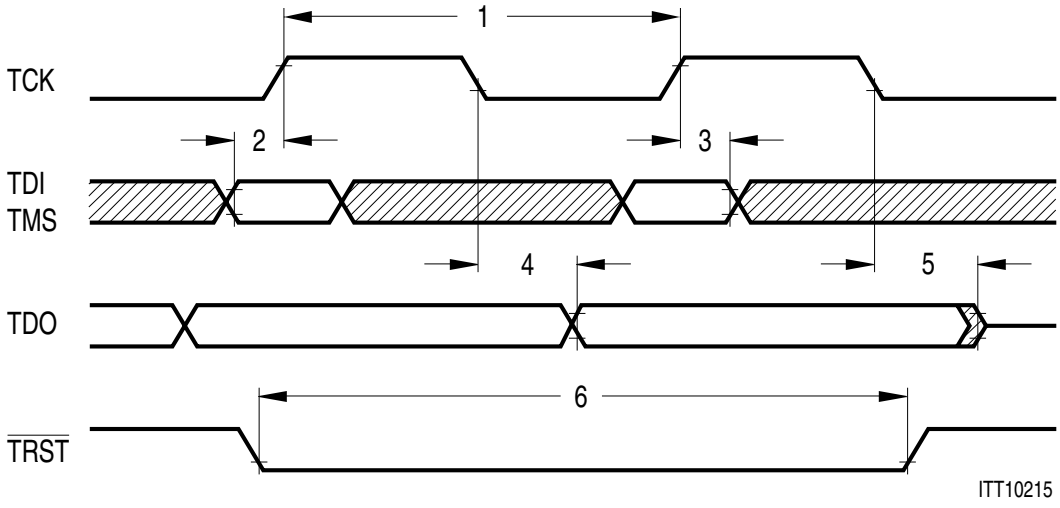


Figure 56 Boundary-Scan Test Interface Timing Diagram

Table 29 Boundary-Scan Test Interface AC Timing Characteristics

No.	Parameter	Limit Values			Unit
		Min	Typ	Max	
1	T_{TCK} : Period TCK	100			ns
1A	F_{TCK} : Frequency TCK			10	MHz
2	Setup time TMS, TDI before TCK rising	10			ns
3	Hold time TMS, TDI after TCK rising	10			ns
4	Delay TCK falling to TDO valid			10	ns
5	Delay TCK falling to TDO high impedance			10	ns
6	Pulse width $\overline{\text{TRST}}$ low	200			ns

6.5.7 AC Characteristics of CAME Interface

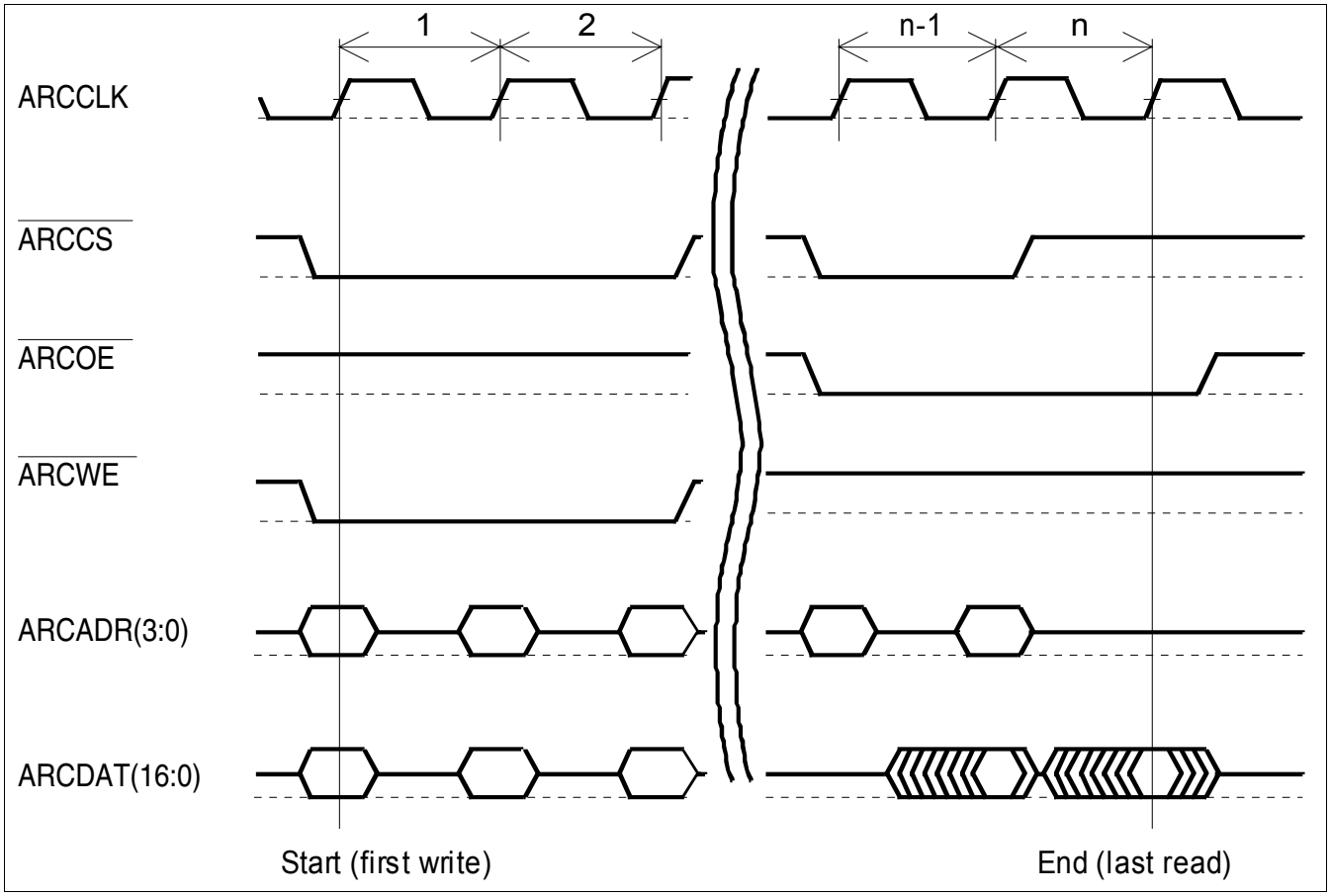


Figure 57 Example of Execution Timing for Write Command (Request #4)

Table 30 Duration of Command Execution

Parameter	Limit Values			Unit
	min.	typ.	max.	
Cell processing search, PN/VPI reduction			13	clock cycles
Cell processing search, PN/VPI/VCI reduction			14	clock cycles
Search request by the microprocessor			14	clock cycles
CAME Write command			10	clock cycles
CAME Read command			13	clock cycles
Test and configuration of the CAME			9	clock cycles

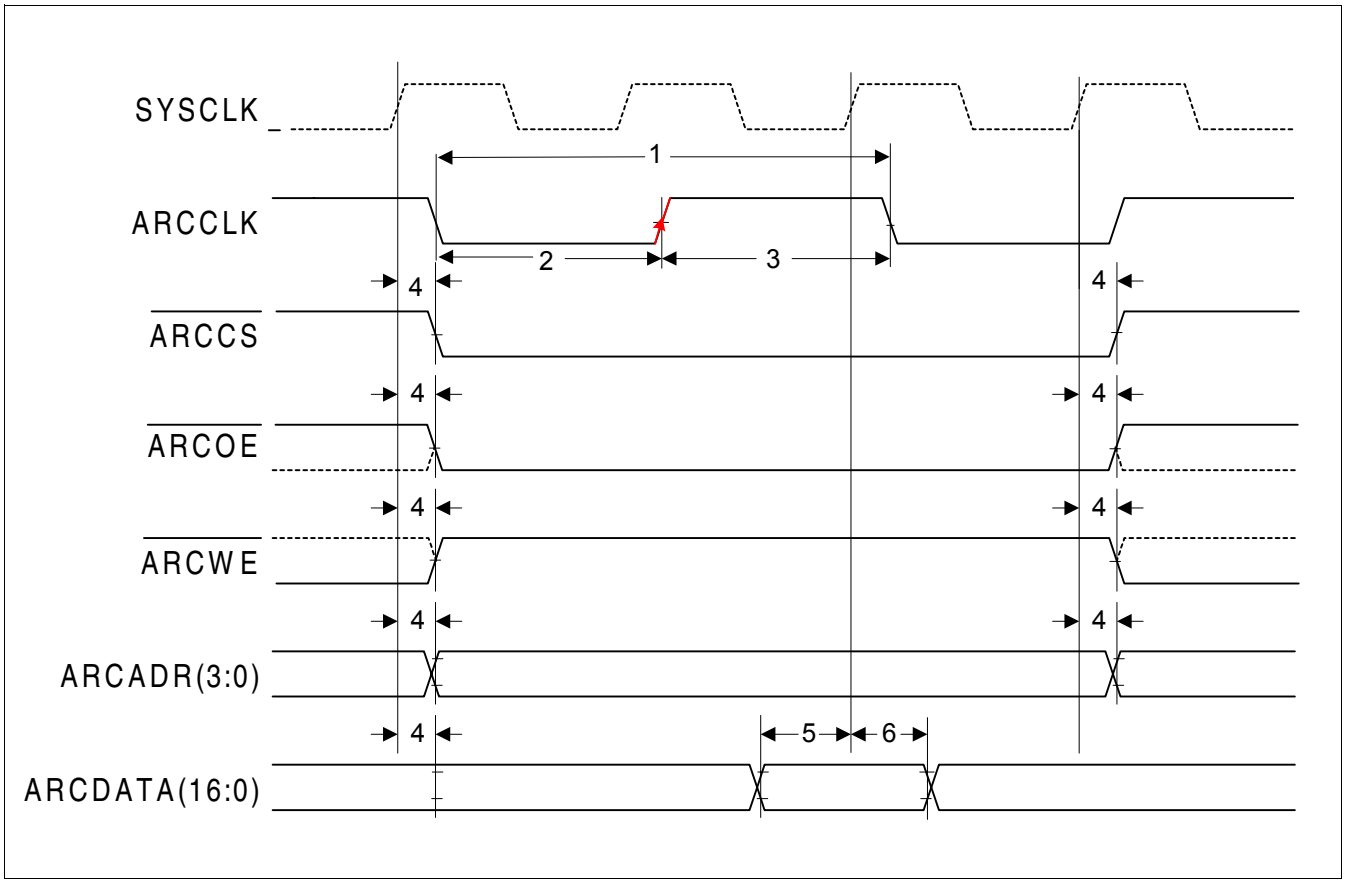


Figure 58 CAME Read Cycle

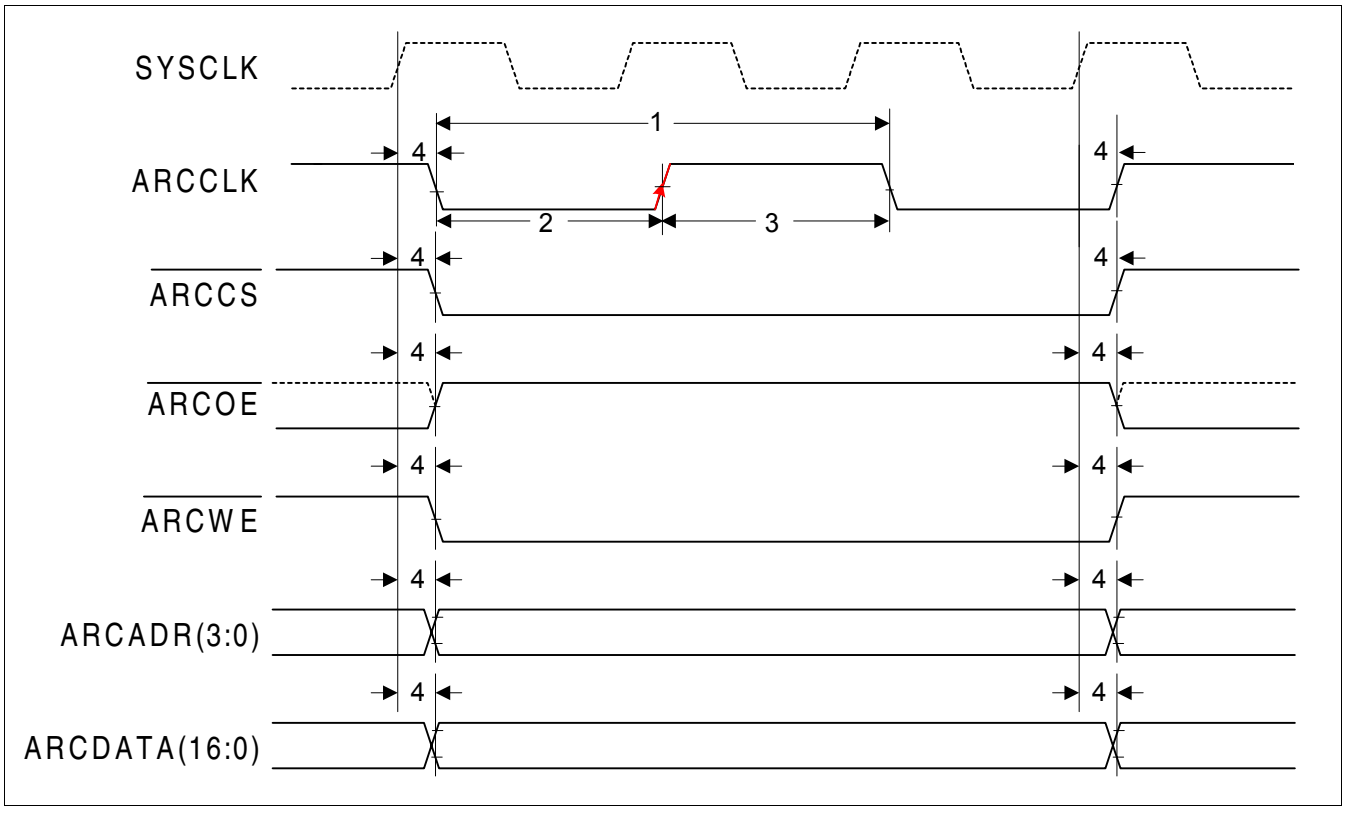


Figure 59 CAME Write Cycle

Table 31 Parameters for Read/Write Access

No.	Parameter	Limit Values			Unit
		min.	typ.	max.	
1	ARCCLK frequency	0.01		25.92	MHz
2	ARCCLK low pulse width	40		60	%
3	ARCCLK high pulse width	40		60	%
4	Path delay SYCLK to ARCCLK, ARCCS, ARCWE, ARCOE, ARCADR, and ARCDAT	3		15	ns
5	Setup time of ARCDAT in read cycle to SYSCLK ↑	5			ns
6	Hold time of ARCDAT in read cycle from SYSCLK ↑	4			ns

7 Package Outlines

BGA-456
(Plastic Ball Grid Array)

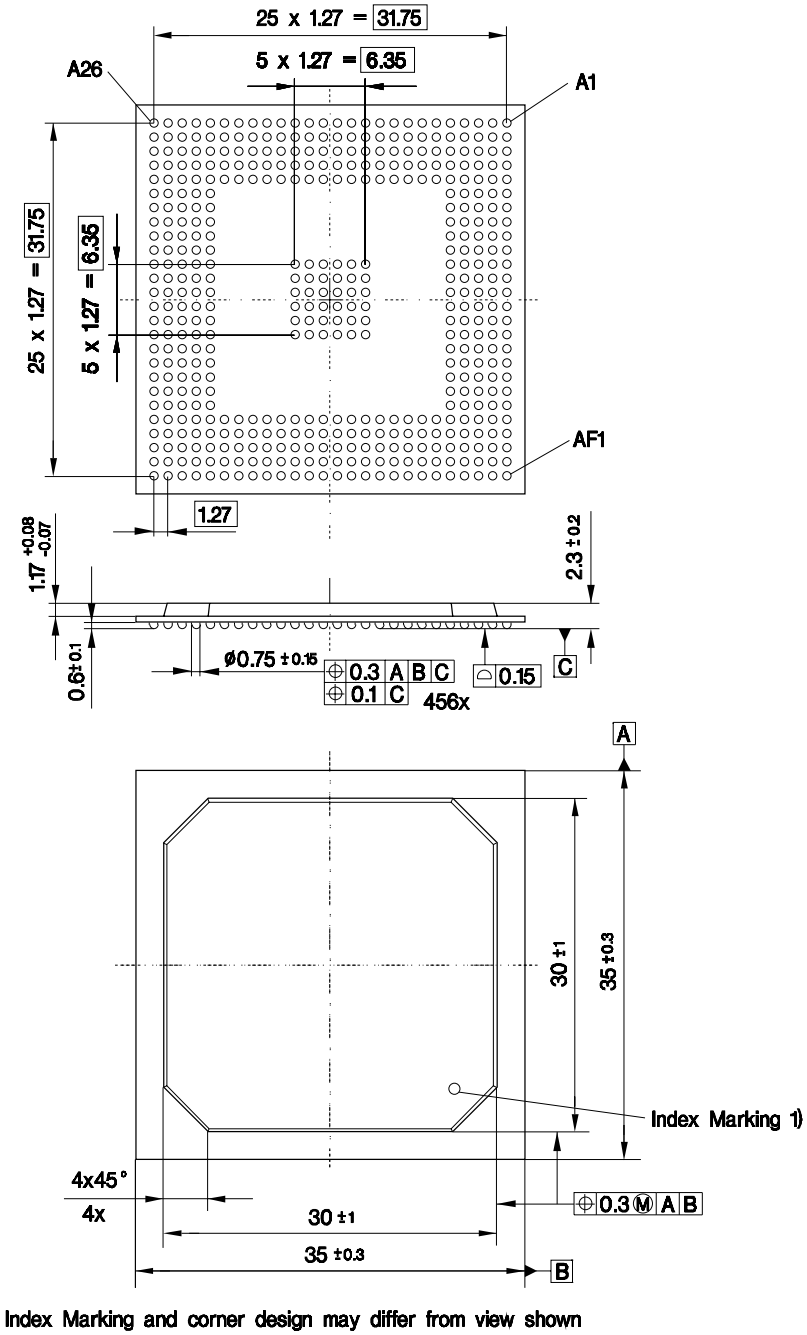


Figure 60 Sorts of Packing

Package outlines for tubes, trays etc. are contained in our Data Book “Package Information”.

SMD = Surface Mounted Device

Dimensions in mm

Table 32 Thermal Resistance

Parameter	Symbol	Limit Values	Unit
Junction to case	R_{thJC}	3.8	K/W
Junction to ambient air without air flow	R_{thJA}	18.7	K/W
Junction to ambient air with air flow 1.0 m/s	R_{thJA}	16.2	K/W
Junction to ambient air with air flow 2.0 m/s	R_{thJA}	15.2	K/W
Junction to ambient air with air flow 3.0 m/s	R_{thJA}	14.4	K/W

8 References

1. UTOPIA Level 1 Specification Version 2.01, March 21, 1994, ATM Forum
2. UTOPIA Level 2 Specification Version 1.0, June 1995, ATM Forum
3. IEEE 1596.3 Standard for Low-Voltage Differential Signals for SCI, Draft 1.3, Nov. 95
4. Joint Test Action Group JTAG standard IEEE std. 1149.1
5. T. Worster, W. Fischer, S. Davis, A. Hayter, “Buffering and flow control for statistical multiplexing in an ATM switch”, International Switching Symposium ISS’95, April 1995
6. ‘ATM Networks: Concepts, Protocols, Applications’, Händel, Schröder, Huber, Addison-Wesley, 1994, ISBN 0-201-42274-3
7. ITU-T Recommendation I.610 “B-ISDN Operation and Maintenance Principles and Functions”, 11/95
8. Bellcore TA-NWT 1248
9. PXB 4360 E CAME, Data Sheet 04.2000 DS2

8.1 Acronyms

- ABM = PXB 4330 E **A**TM **B**uffer **M**anager
- ABR = **A**vailable **B**it **R**ate
- ABT = **A**TM **B**lock **T**ransfer
- AIS = **A**larm **I**ndication **S**ignal (OAM function)
- ATM-LP = PXB 4350 E **A**TM **L**ayer **P**rocessor
- AOP = PXB 4340 E **A**TM **O**AM **P**rocessor
- ARC = **A**ddress **R**eduction **C**ircuit (CAME PXB 4360 E)
- BIP-16 = **B**it **I**nterleaved **P**arity, 16 bit
- BR = **B**ackward **R**eporting (PM function)
- byte = octet = 8 bit
- CAME = **C**ontent **A**ddressable **M**emory **E**lement
- CC = **C**ontinuity **C**heck (OAM function)
- CCA = **C**ontinuity **C**heck **A**ctivation
- CDV = **C**ell **D**elay **V**ariation
- CLP = **C**ell **L**oss **P**riority of standardized ATM cell
- DBR = **D**eterministic **B**it **R**ate
- double word = 32 bit
- F4 = Virtual Path Layer
- F5 = Virtual Channel Layer
- FIFO = **F**irst-**i**n-**f**irst-**o**ut buffer
- FM = **F**orward **M**onitoring (PM cell type)
- HK = **H**ouse**K**eeping bits of UDF1 field in UTOPIA cell format
- HT = **H**eader **T**ranslation
- I/O = **I**nput / **O**utput
- ICC = **I**nternal **C**ontinuity **C**heck (proprietary OAM function)
- IP = **I**ntermediate **P**oint
- ITU-T = **I**nternational **T**elecommunications **U**nion - **T**elecommunications standardization sector
- IWE8 = PXB 4220 **I**nter**w**orking **E**lement for 8 channels
- LB = **L**oop**b**ack (OAM function)
- LB = **L**eaky **B**ucket
- LCI = **L**ocal **C**onnection **I**dentifier

- LIC = **L**ine **I**nterface **C**ard or Line Interface Circuit
- LOC = **L**oss **O**f **C**ontinuity (OAM state)
- LPS = **L**ine **P**rotection **S**witching
- LSB = **L**east **S**ignificant **B**it
- MBS = **M**aximum **B**urst **S**ize
- MCR = **M**inimum **C**ell **R**ate
- NPC = **N**etwork **P**arameter **C**ontrol
- octet = byte = 8 bit
- OAM = **O**peration **a**nd **M**aintenance
- OEP = **O**riginating **E**nd **P**oint
- OSP = **O**riginating **S**egment **P**oint
- PCR = **P**eak **C**ell **R**ate
- PM = **P**erformance **M**onitoring (OAM function)
- PN = **P**ort **N**umber
- PTI = **P**ayload **T**ype **I**ndication field of standardized ATM cell
- RAM = **R**andom **A**ccess **M**emory
- RDI = **R**emote **D**efect **I**ndication (OAM function)
- RM = **R**esource **M**anagement Cell
- RWR RAM = µP Read/Write RAM
- RXR RAM = Rx 12 cell extraction Buffer
- SCR = **S**ustainable **C**ell **R**ate
- SSRAM = **S**ynchronous **S**tatic **RAM**
- tbd = **t**o **b**e **d**efined
- TEP = **T**erminating **E**nd **P**oint
- TM = **T**raffic **M**anagement
- TRM RAM = **Tr**affic **M**easurement Port Table
- UCW RAM = Upstream workbench
- UPC = **U**ser **P**arameter **C**ontrol
- UTOPIA = **U**niversal **T**est and **Op**eration **I**nterface for **A**TM
- UTRXD Buffer = **UT**OPIA **Rx**-**d**ownstream cell FIFO
- UTRXU Buffer = **UT**OPIA **Rx**-**u**pstream cell FIFO
- UTTXD Buffer = **UT**OPIA **Tx**-**d**ownstream shared memory Buffer
- UTTXU Buffer = **UT**OPIA **Tx**-**u**pstream cell FIFO
- VC- = **V**irtual **C**hannel specific
- VCC = **V**irtual **C**hannel **C**onnection
- VCI = **V**irtual **C**hannel **I**dentifier of standardized ATM cell
- VP- = **V**irtual **P**ath specific
- VPC = **V**irtual **P**ath **C**onnection
- VPI = **V**irtual **P**ath **I**dentifier of standardized ATM cell
- word = 16 bit

w w w . i n f i n e o n . c o m

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