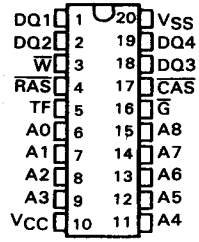
JUNE 1986 — REVISED MAY 1988

- **262,144 × 4 Organization**
- **Single 5-V Supply (10% Tolerance)**
- **Performance Ranges:**

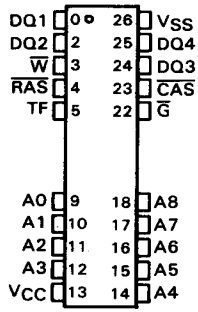
	ACCESS TIME $t_{a(R)}$ (t_{RAC}) (MAX)	ACCESS TIME $t_{a(C)}$ (t_{CAC}) (MAX)	ACCESS TIME $t_{a(CA)}$ (t_{CAA}) (MAX)	READ OR WRITE CYCLE (MIN)
TMS44C25_-10	100 ns	25 ns	45 ns	190 ns
TMS44C25_-12	120 ns	30 ns	55 ns	220 ns
TMS44C25_-15	150 ns	40 ns	70 ns	260 ns

- **TMS44C256 — Enhanced Page Mode Operation with $\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **TMS44C257 — Static Column Decode Mode Operation with $\overline{CAS}$-Before-$\overline{RAS}$ Refresh**
- **Long Refresh Period . . . 512-Cycle Refresh in 8 ms (Max)**
- **3-State Unlatched Output**
- **Lower Power Dissipation**
- **Texas Instruments EPIC™ CMOS Process**
- **All Inputs and Clocks Are TTL Compatible**
- **High-Reliability Plastic 20-Pin 300-Mil-Wide DIP or 20/26-Lead Surface Mount (SOJ) Package**
- **Operation of TI's Megabit CMOS DRAMs Can Be Controlled by TI's SN74ALS6301 and SN74ALS6302 Dynamic RAM Controllers**
- **Operating Free-Air Temperature . . . 0°C to 70°C**

N PACKAGE
(TOP VIEW)



DJ PACKAGE†
(TOP VIEW)



†The packages shown here are for pinout reference only. The DJ package is actually 75% of the length of the N package.

PIN NOMENCLATURE	
A0-A8	Address Inputs
$\overline{CAS}$	Column-Address Strobe
DQ1-DQ4	Data In/Data Out
$\overline{G}$	Data-Output Enable
$\overline{RAS}$	Row-Address Strobe
TF	Test Function
$\overline{W}$	Write Enable
V_{CC}	5-V Supply
V_{SS}	Ground

description

The TMS44C256 and TMS44C257 series are high-speed, 1,048,576-bit Dynamic Random-Access Memories organized as 262,144 words of four bits each. They employ state-of-the-art EPIC™ (Enhanced Process Implanted CMOS) technology for high performance, reliability, and low power at a low cost.

operation

enhanced page mode (TMS44C256)

Page-mode operation allows faster memory access by keeping the same row address while selecting random column addresses. The time for row-address setup and hold and address multiplex is thus eliminated. The maximum number of columns that may be accessed is determined by the maximum $\overline{RAS}$ low time and

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the $\overline{CAS}$ page-mode cycle time used. With minimum $\overline{CAS}$ page cycle time, all 512 columns specified by column addresses A0 through A8 can be accessed without intervening $\overline{RAS}$ cycles.

Unlike conventional page-mode DRAMs, the column-address buffers in this device are activated on the falling edge of $\overline{RAS}$. The buffers act as transparent or flow-through latches while $\overline{CAS}$ is high. The falling edge of $\overline{CAS}$ latches the column addresses. This feature allows the TMS44C256 to operate at a higher data bandwidth than conventional page-mode parts, since data retrieval begins as soon as column address is valid rather than when $\overline{CAS}$ transitions low. This performance improvement is referred to as "enhanced page mode." Valid column address may be presented immediately after $t_{h(RA)}$ (row address hold time) has been satisfied, usually well in advance of the falling edge of $\overline{CAS}$. In this case, data is obtained after $t_{a(C)}$ max (access time from $\overline{CAS}$ low), if $t_{a(CA)}$ max (access time from column address) has been satisfied. In the event that column addresses for the next page cycle are valid at the time $\overline{CAS}$ goes high, access time for the next cycle is determined by the later occurrence of $t_{a(C)}$ or $t_{a(CP)}$ (access time from rising edge of $\overline{CAS}$).

static column decode mode (TMS44C257)

The static column decode mode of operation allows high-speed read, write, or read-modify-write by reducing the number of required signal setup, hold, and transition timings. This is achieved by first addressing the row and column in the normal manner, but after the first access maintain $\overline{CAS}$ low. Subsequently changing the column address produces valid data at the $t_{a(CA)}$. The first bit is accessed in the normal manner with read data coming out at $t_{a(C)}$ time. Similarly, write or read-modify-write cycle times can be achieved with appropriate toggling of $\overline{W}$. The addresses are latched during the write operation, but at the completion of the internal write operation the addresses are unlatched.

address (A0 through A8)

Eighteen address bits are required to decode 1 of 262,144 storage cell locations. Nine row-address bits are set up on pins A0 through A8 and latched onto the chip by the row-address strobe ($\overline{RAS}$). Then nine column-address bits are set up on pins A0 through A8 and latched onto the chip by the column-address strobe ($\overline{CAS}$). All addresses must be stable on or before the falling edges of $\overline{RAS}$ and $\overline{CAS}$. $\overline{RAS}$ is similar to a chip enable in that it activates the sense amplifiers as well as the row decoder. The TMS44C256 $\overline{CAS}$ is used as a chip select activating the output buffer, as well as latching the address bits into the column-address buffers. The TMS44C257 column addresses are latched only on write cycles with the later of the $\overline{CAS}$ or $\overline{W}$ falling edge.

write enable ($\overline{W}$)

The read or write mode is selected through the write-enable ($\overline{W}$) input. A logic high on the $\overline{W}$ input selects the read mode and a logic low selects the write mode. The write-enable terminal can be driven from standard TTL circuits without a pull-up resistor. The data input is disabled when the read mode is selected. When $\overline{W}$ goes low prior to $\overline{CAS}$ (early write), data out will remain in the high-impedance state for the entire cycle permitting a write operation with $\overline{G}$ grounded. The TMS44C257 latches the column addresses on write cycles with the later of $\overline{CAS}$ or $\overline{W}$ falling edge.

data in (DQ1-DQ4)

Data is written during a write or read-modify-write cycle. Depending on the mode of operation, the falling edge of $\overline{CAS}$ or $\overline{W}$ strobes data into the on-chip data latch. In an early write cycle, $\overline{W}$ is brought low prior to $\overline{CAS}$ and the data is strobed in by $\overline{CAS}$ with setup and hold times referenced to this signal. In a delayed write or read-modify-write cycle, $\overline{CAS}$ will already be low, thus the data will be strobed in by $\overline{W}$ with setup and hold times referenced to this signal. In a delayed or read-modify-write cycle, $\overline{G}$ must be high to bring the output buffers to high impedance prior to impressing data on the I/O lines.

data out (DQ1-DQ4)

The three-state output buffer provides direct TTL compatibility (no pull-up resistor required) with a fanout of two Series 74 TTL loads. Data out is the same polarity as data in. The output is in the high-impedance (floating) state until $\overline{CAS}$ and $\overline{G}$ are brought low. In a read cycle the output becomes valid after the access time interval $t_{a(C)}$ that begins with the negative transition of $\overline{CAS}$ as long as $t_{a(R)}$ and $t_{a(CA)}$ are satisfied. The output becomes valid after the access time has elapsed and remains valid while $\overline{CAS}$ and $\overline{G}$ are low. $\overline{CAS}$ or $\overline{G}$ going high returns it to a high-impedance state. This is accomplished by bringing $\overline{G}$ high prior to applying data, thus satisfying $t_{d(GHD)}$.

output enable ($\overline{G}$)

$\overline{G}$ controls the impedance of the output buffers. When $\overline{G}$ is high, the buffers will remain in the high-impedance state. Bringing $\overline{G}$ low during a normal cycle will activate the output buffers putting them in the low-impedance state. It is necessary for both $\overline{RAS}$ and $\overline{CAS}$ to be brought low for the output buffers to go into the low-impedance state. Once in the low-impedance state, they will remain in the low-impedance state until either $\overline{G}$ or $\overline{CAS}$ is brought high.

refresh

A refresh operation must be performed at least once every eight milliseconds to retain data. This can be achieved by strobing each of the 512 rows (A0-A8). A normal read or write cycle will refresh all bits in each row that is selected. A $\overline{RAS}$-only operation can be used by holding $\overline{CAS}$ at the high (inactive) level, thus conserving power as the output buffer remains in the high-impedance state. Externally generated addresses must be used for a $\overline{RAS}$-only refresh. Hidden refresh may be performed while maintaining valid data at the output pin. This is accomplished by holding $\overline{CAS}$ at V_{IL} after a read operation and cycling $\overline{RAS}$ after a specified precharge period, similar to a $\overline{RAS}$-only refresh cycle.

$\overline{CAS}$-before-$\overline{RAS}$ refresh

$\overline{CAS}$-before-$\overline{RAS}$ refresh is utilized by bringing $\overline{CAS}$ low earlier than $\overline{RAS}$ [see parameter $t_{d(CLRL)R}$] and holding it low after $\overline{RAS}$ falls [see parameter $t_{d(RLCH)R}$]. For successive $\overline{CAS}$-before-$\overline{RAS}$ refresh cycles, $\overline{CAS}$ can remain low while cycling $\overline{RAS}$. The external address is ignored and the refresh address is generated internally. The external address is also ignored during the hidden refresh option.

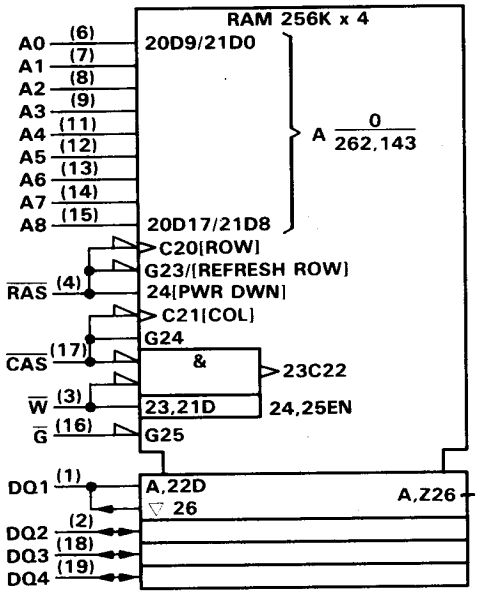
power up

To achieve proper device operation, an initial pause of 200 μs followed by a minimum of eight initialization cycles is required after power up to the full V_{CC} level.

test function pin

During normal device operation, the TF pin must be either disconnected or biased at a voltage less than or equal to V_{CC}.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

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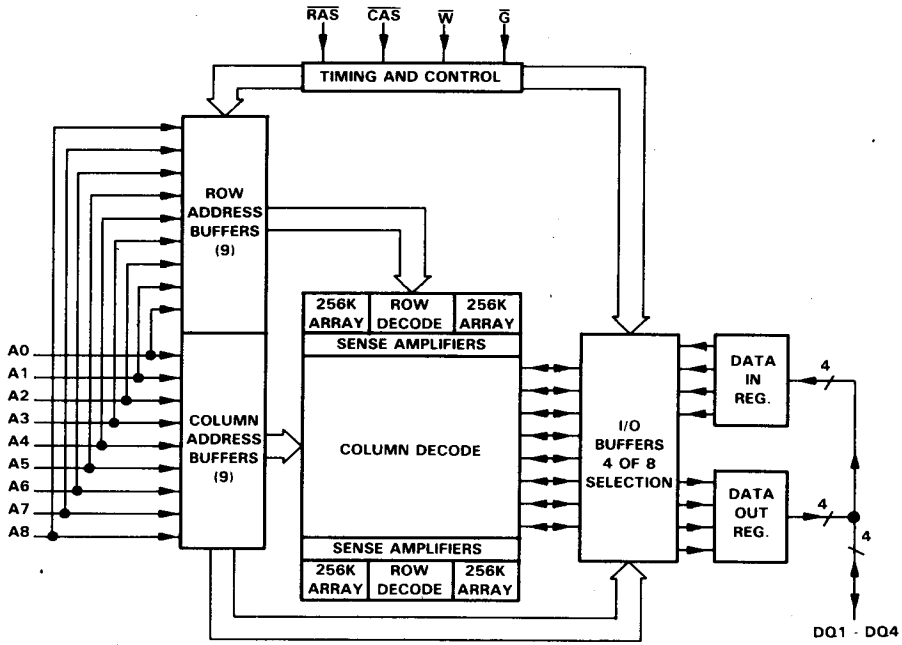
functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Voltage range on any pin (see Note 1)	−1 V to 7 V
Voltage range on V_{CC}	0 V to 7 V
Short circuit output current	50 mA
Power dissipation	1 W
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C

†Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values in this data sheet are with respect to V_{SS}.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{SS}	Supply voltage		0		V
V_{IH}	High-level input voltage	2.4		6.5	V
V_{IL}	Low-level input voltage (see Note 2)	−1		0.8	V
T_A	Operating free-air temperature	0		70	°C

NOTE 2: The algebraic convention, where the more negative (less positive) limit is designated as minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over full ranges of recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TMS44C25_-10		TMS44C25_-12		TMS44C25_-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
V_{OH}	High-level output voltage	I_{OH} = −5 mA	2.4		2.4		2.4		V
V_{OL}	Low-level output voltage	I_{OL} = 4.2 mA		0.4		0.4		0.4	V
I_I	Input current (leakage)	V_I = 0 V to 5.8 V, V_{CC} = 5 V, All other pins = 0 V to V_{CC}		±10		±10		±10	μA
I_O	Output current (leakage)	V_O = 0 V to V_{CC}, V_{CC} = 5.5 V, $\overline{CAS}$ high		±10		±10		±10	μA
I_{CC1}	Read/write cycle current	$t_{c(rdW)}$ = minimum, V_{CC} = 5.5 V		70		60		55	mA
I_{CC2}	Standby current	After 1 memory cycle, $\overline{RAS}$ and $\overline{CAS}$ high, V_{IH} = 2.4 V		3		3		3	mA
I_{CC3}	Average refresh current	$t_{c(rdW)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ cycling, $\overline{CAS}$ high		65		55		50	mA
I_{CC4}	Average page current	$t_{c(P)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		45		35		30	mA
I_{CC6}	Average static column decode current	$t_{c(rdW)}$ = minimum, V_{CC} = 5.5 V, $\overline{RAS}$ low, $\overline{CAS}$ cycling		45		35		30	mA

capacitance over recommended supply voltage range and operating free-air temperature range, f = 1 MHz (see Note 3)

PARAMETER		MIN	MAX	UNIT
$C_{i(A)}$	Input capacitance, address inputs		6	pF
$C_{i(RC)}$	Input capacitance, strobe inputs		7	pF
$C_{i(W)}$	Input capacitance, write-enable input		7	pF
C_o	Output capacitance		7	pF

NOTE 3: V_{CC} equal to 5.0 V ± 0.5 V and the bias on pins under test is 0.0 V.

switching characteristics over recommended supply voltage range and operating free-air temperature range (see Figure 1)

PARAMETER		ALT. SYMBOL	TMS44C25_-10		TMS44C25_-12		TMS44C25_-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{a(C)}$	Access time from $\overline{CAS}$ low	t_{CAC}		25		30		40	ns
$t_{a(CA)}$	Access time from column address	t_{CAA}		45		55		70	ns
$t_{a(R)}$	Access time from $\overline{RAS}$ low	t_{RAC}		100		120		150	ns
$t_{a(G)}$	Access time from $\overline{G}$ low	t_{GAC}		25		30		40	ns
$t_{a(CP)}$	Access time from column precharge (TMS44C256 only)	t_{CAP}		50		60		75	ns
$t_{a(WHQ)}$	Access time from $\overline{W}$ high, Static column decode mode (see Note 4) (TMS44C257 only)	t_{WRA}		30		35		40	ns
$t_{a(WLQ)}$	Access time from $\overline{W}$ low, Static column decode mode (see Note 4) (TMS44C257 only)	t_{ALW}		95		115		120	ns
$t_{dis(CH)}$	Output disable time after $\overline{CAS}$ high (see Note 5)	t_{OFF}	0	25	0	30	0	35	ns
$t_{dis(G)}$	Output disable time after $\overline{G}$ high (see Note 5)	t_{GOFF}	0	25	0	30	0	35	ns

NOTES: 4. Read-modify-write operation only.
5. $t_{dis(CH)}$ and $t_{dis(G)}$ are specified when the output is no longer driven.

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TMS44C256-10		TMS44C256-12		TMS44C256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 7)	t_{RC}	190		220		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	190		220		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	220		255		305		ns
$t_{c(P)}$	Page-mode read or write cycle time (see Note 8)	t_{PC}	55		65		80		ns
$t_{c(PM)}$	Page-mode read-modify-write cycle time	t_{PCM}	85		100		125		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		15		25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 9)	t_{CAS}	25	10,000	30	10,000	40	10,000	ns
$t_{w(RH)}$	Pulse duration $\overline{RAS}$ high (precharge)	t_{RP}	80		90		100		ns
$t_{w(RL)}$	Non-page-mode pulse duration, $\overline{RAS}$ low (see Note 10)	t_{RAS}	100	10,000	120	10,000	150	10,000	ns
$t_{w(RL)P}$	Page-mode pulse duration, $\overline{RAS}$ low (see Note 10)	t_{RASP}	100	100,000	120	100,000	150	100,000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		20		25		ns
$t_{su(CA)}$	Column-address setup time before $\overline{CAS}$ low	t_{ASC}	0		0		0		ns
$t_{su(RA)}$	Row-address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		0		ns
$t_{su(D)}$	Data setup time before $\overline{W}$ low (see Note 11)	t_{DS}	0		0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 12)	t_{WCS}	0		0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	25		30		40		ns
$t_{su(WRH)}$	$\overline{W}$-low setup time before $\overline{RAS}$ high	t_{RWL}	25		30		40		ns
$t_{h(CA)}$	Column-address hold time after $\overline{CAS}$ low (see Note 11)	t_{CAH}	20		20		25		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	15		15		20		ns

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NOTES: 6. Timing measurements are referenced to V_{IL} max and V_{IH} min.
7. All cycle times assume t_t = 5 ns.
8. $t_{c(P)} > t_{w(CH)}$ min + $t_{w(CL)}$ min + $2t_t$.
9. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time $[t_{w(CL)}]$.
10. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time $[t_{w(RL)}]$.
11. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. Early write operation only.

timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

		ALT. SYMBOL	TMS44C256-10		TMS44C256-12		TMS44C256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 13)	t_{AR}	70		80		100		ns
$t_{h(D)}$	Data hold time after $\overline{CAS}$ low (see Note 11)	t_{DH}	20		25		30		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 13)	t_{DHR}	70		85		110		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high (see Note 15)	t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high (see Note 15)	t_{RRH}	10		10		10		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low (see Note 12)	t_{WCH}	20		25		30		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 13)	t_{WCR}	70		85		100		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		150		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	25		30		40		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 4)	t_{CWD}	50		60		70		ns
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	t_{RCD}	25	75	25	90	30	110	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address (see Note 14)	t_{RAD}	20	55	20	65	25	80	ns
$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high	t_{RAL}	45		55		70		ns
$t_{d(CACH)}$	Delay time, column address to $\overline{CAS}$ high	t_{CAL}	45		55		70		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 4)	t_{RWD}	100		120		150		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 4)	t_{AWD}	45		55		70		ns
$t_{d(GHD)}$	Delay time, $\overline{G}$ high before data at DQ	t_{GDD}	25		30		40		ns
$t_{d(GLRH)}$	Delay time, $\overline{G}$ low to $\overline{RAS}$ high	t_{GSR}	20		25		35		ns

Continued next page.

NOTES: 4. Read-modify-write operation only.
11. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. Early write operation only.
13. The minimum value is measured when $t_{d(RLCL)}$ is set to $t_{d(RLCL)}$ min as a reference.
14. Maximum value specified only to guarantee access time.
15. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.

timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

		ALT. SYMBOL	TMS44C256-10		TMS44C256-12		TMS44C256-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	t_{CHR}	25		25		30		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		15		ns
$t_{d(RHCL)R}$	Delay time, $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 16)	t_{RPC}	0		0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	ns

NOTE 16: $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

timing requirements over recommended supply voltage range and operating free-air temperature range

		ALT. SYMBOL	TMS44C257-10		TMS44C257-12		TMS44C257-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{c(rd)}$	Read cycle time (see Note 7)	t_{RC}	190		220		260		ns
$t_{c(W)}$	Write cycle time	t_{WC}	190		220		260		ns
$t_{c(rdW)}$	Read-write/read-modify-write cycle time	t_{RWC}	220		255		305		ns
$t_{c(rd)SC}$	Static column decode mode read-only cycle time	t_{SCR}	50		60		90		ns
$t_{c(W)SC}$	Static column decode mode write-only cycle time	t_{CSW}	50		60		90		ns
$t_{c(rdW)SC}$	Static column decode mode read-modify-write cycle time	t_{SCRDW}	100		120		150		ns
$t_{w(CH)}$	Pulse duration, $\overline{CAS}$ high	t_{CP}	10		15		25		ns
$t_{w(CL)}$	Pulse duration, $\overline{CAS}$ low (see Note 9)	t_{CAS}	20	10,000	25	10,000	35	10,000	ns
$t_{w(RH)}$	Pulse duration, $\overline{RAS}$-high (precharge)	t_{RP}	80		90		100		ns
$t_{w(RL)}$	Non-static column decode mode pulse duration, $\overline{RAS}$ low (see Note 10)	t_{RAS}	100	10,000	120	10,000	150	10,000	ns
$t_{w(RL)P}$	Static column decode mode pulse duration, $\overline{RAS}$ low (see Note 10)	t_{RASP}	100	100,000	120	100,000	150	100,000	ns
$t_{w(WL)}$	Write pulse duration	t_{WP}	15		20		25		ns
$t_{w(CA)}$	Static column decode mode column address pulse duration	t_{ADP}	45		55		70		ns
$t_{w(WH)}$	Static column decode mode $\overline{W}$ high pulse duration	t_{WI}	10		15		25		ns
$t_{su(CA)}$	Column-address setup times before $\overline{CAS}$ low or $\overline{W}$ low (see Note 11)	t_{ASC}	0		0		0		ns
$t_{su(RA)}$	Row address setup time before $\overline{RAS}$ low	t_{ASR}	0		0		0		ns
$t_{su(D)}$	Data setup time before $\overline{W}$ low (see Note 11)	t_{DS}	0		0		0		ns
$t_{su(rd)}$	Read setup time before $\overline{CAS}$ low	t_{RCS}	0		0		0		ns
$t_{su(WCL)}$	$\overline{W}$-low setup time before $\overline{CAS}$ low (see Note 12)	t_{WCS}	0		0		0		ns
$t_{su(WCH)}$	$\overline{W}$-low setup time before $\overline{CAS}$ high	t_{CWL}	25		30		40		ns
$t_{su(WHCH)}$	$\overline{W}$-high setup time before $\overline{CAS}$ high (see Note 12)	t_{WHCH}	0		0		0		ns

Continued next page.

NOTES: 6. Timing measurements are referenced to V_{IL} max and V_{IH} min.
7. All cycle times assume t_t = 5 ns.
9. In a read-modify-write cycle, $t_{d(CLWL)}$ and $t_{su(WCH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{CAS}$ low time [$t_{w(CL)}$].
10. In a read-modify-write cycle, $t_{d(RLWL)}$ and $t_{su(WRH)}$ must be observed. Depending on the user's transition times, this may require additional $\overline{RAS}$ low time [$t_{w(RL)}$].
11. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.
12. Early write operation only.

timing requirements over recommended supply voltage range and operating free-air temperature range (continued)

		ALT. SYMBOL	TMS44C257-10		TMS44C257-12		TMS44C257-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{su(WRH)}$	$\overline{W}$-low setup time before $\overline{RAS}$ high	t_{RWL}	25		30		40		ns
$t_{su(RLrd)}$	Read-command setup time before $\overline{RAS}$ low	t_{WRP}	0		0		0		ns
$t_{su(CAR)}$	Column-address setup time before $\overline{RAS}$ high	t_{CAR}	50		60		75		ns
$t_{h(CA)}$	Column-address hold time after $\overline{CAS}$ low, $\overline{W}$ low (see Note 11)	t_{CAH}	20		20		25		ns
$t_{h(RA)}$	Row-address hold time after $\overline{RAS}$ low	t_{RAH}	15		15		20		ns
$t_{h(RLCA)}$	Column-address hold time after $\overline{RAS}$ low (see Note 17)	t_{AR}	100		120		150		ns
$t_{h(D)}$	Data hold time after $\overline{CAS}$ low (see Note 11)	t_{DH}	20		25		30		ns
$t_{h(RLD)}$	Data hold time after $\overline{RAS}$ low (see Note 17)	t_{DHR}	70		85		110		ns
$t_{h(CHrd)}$	Read hold time after $\overline{CAS}$ high (see Note 15)	t_{RCH}	0		0		0		ns
$t_{h(RHrd)}$	Read hold time after $\overline{RAS}$ high (see Note 15)	t_{RRH}	10		10		10		ns
$t_{h(CLW)}$	Write hold time after $\overline{CAS}$ low	t_{WCH}	20		25		30		ns
$t_{h(RLW)}$	Write hold time after $\overline{RAS}$ low (see Note 17)	t_{WCR}	70		85		100		ns
$t_{h(RHCA)}$	Column-address hold time after $\overline{RAS}$ high	t_{AH}	10		15		15		ns
$t_{h(CAQ)}$	Output hold time after address change	t_{OH}	5		5		5		ns
$t_{d(RLCH)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high	t_{CSH}	100		120		150		ns
$t_{d(CHRL)}$	Delay time, $\overline{CAS}$ high to $\overline{RAS}$ low	t_{CRP}	0		0		0		ns
$t_{d(CLRH)}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ high	t_{RSH}	25		30		40		ns
$t_{d(CLWL)}$	Delay time, $\overline{CAS}$ low to $\overline{W}$ low (see Note 4)	t_{CWD}	25		30		40		ns

Continued next page.

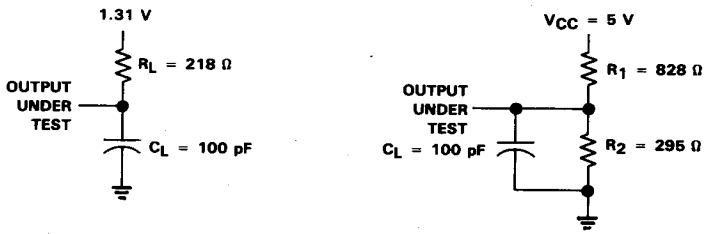
NOTES: 4. Read-modify-write operation only.
11. Later of $\overline{CAS}$ or $\overline{W}$ in write operations.
15. Either $t_{h(RHrd)}$ or $t_{h(CHrd)}$ must be satisfied for a read cycle.
17. The minimum value is measured when $t_{d(RLCA)}$ is set to $t_{d(RLCA)}$ min as a reference.

timing requirements over recommended supply voltage range and operating free-air temperature range (concluded)

		ALT. SYMBOL	TMS44C257-10		TMS44C257-12		TMS44C257-15		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
$t_{d(RLCL)}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ low (see Note 14)	t_{RCD}	25	75	25	90	30	110	ns
$t_{d(RLCA)}$	Delay time, $\overline{RAS}$ low to column address (see Note 14)	t_{RAD}	20	55	20	65	25	80	ns
$t_{d(CARH)}$	Delay time, column address to $\overline{RAS}$ high	t_{RAL}	45		55		70		ns
$t_{d(CACH)}$	Delay time, column address to $\overline{CAS}$ high	t_{CAL}	45		55		70		ns
$t_{d(RLWL)}$	Delay time, $\overline{RAS}$ low to $\overline{W}$ low (see Note 4)	t_{RWD}	100		120		150		ns
$t_{d(CAWL)}$	Delay time, column address to $\overline{W}$ low (see Note 4)	t_{AWD}	45		55		70		ns
$t_{d(GHD)}$	Delay time, $\overline{G}$ high before data at DQ	t_{GDD}	25		30		40		ns
$t_{d(GLRH)}$	Delay time, $\overline{G}$ low to $\overline{RAS}$ high	t_{GSR}	20		25		35		ns
$t_{d(WQ)}$	Delay time, $\overline{W}$ high to output transition from high impedance to active	t_{OW}	0		0		0		ns
$t_{d(RLCH)R}$	Delay time, $\overline{RAS}$ low to $\overline{CAS}$ high (see Note 16)	t_{CHR}	25		25		30		ns
$t_{d(CLRL)R}$	Delay time, $\overline{CAS}$ low to $\overline{RAS}$ low (see Note 16)	t_{CSR}	10		10		15		ns
$t_{d(RHCL)R}$	Delay time $\overline{RAS}$ high to $\overline{CAS}$ low (see Note 16)	t_{RPC}	0		0		0		ns
t_{rf}	Refresh time interval	t_{REF}		8		8		8	ms
t_t	Transition time	t_T	3	50	3	50	3	50	ns

NOTES: 4. Read-modify-write operation only.
14. Maximum value specified only to guarantee access time.
16. $\overline{CAS}$-before-$\overline{RAS}$ refresh only.

PARAMETER MEASUREMENT INFORMATION

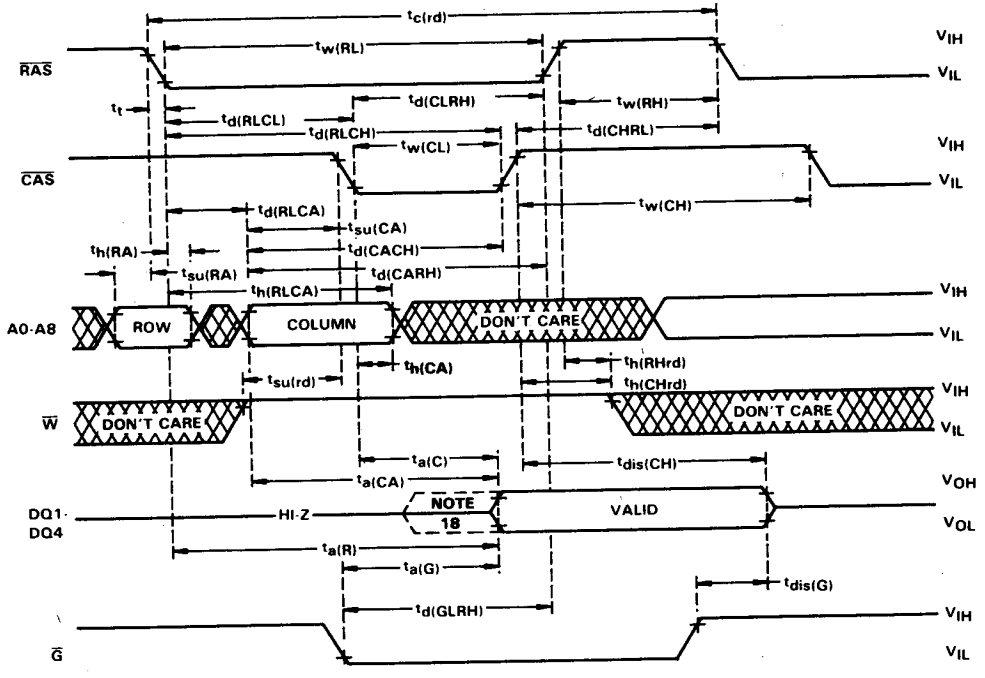


(a) LOAD CIRCUIT

(b) ALTERNATE LOAD CIRCUIT

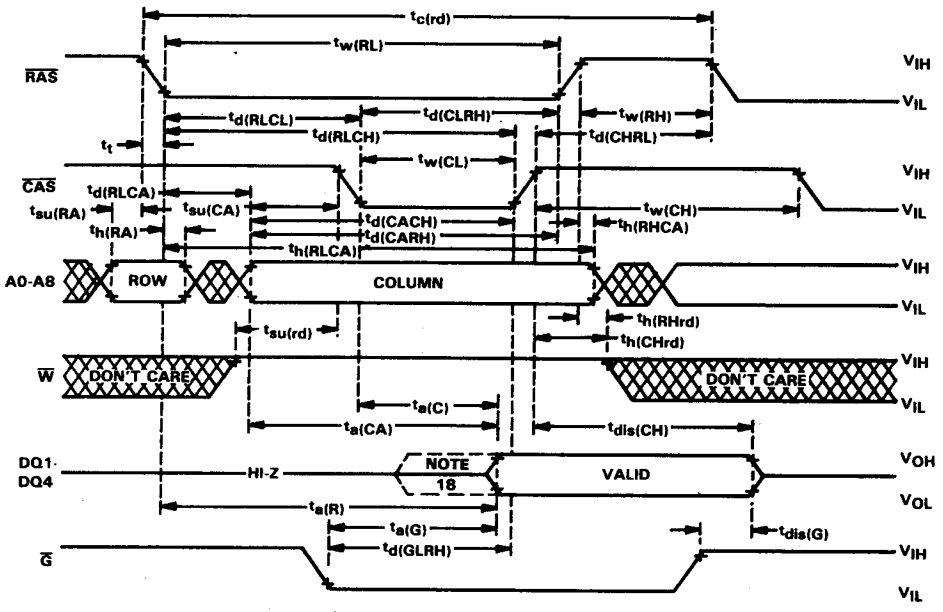
FIGURE 1. LOAD CIRCUITS FOR TIMING PARAMETERS

read cycle timing



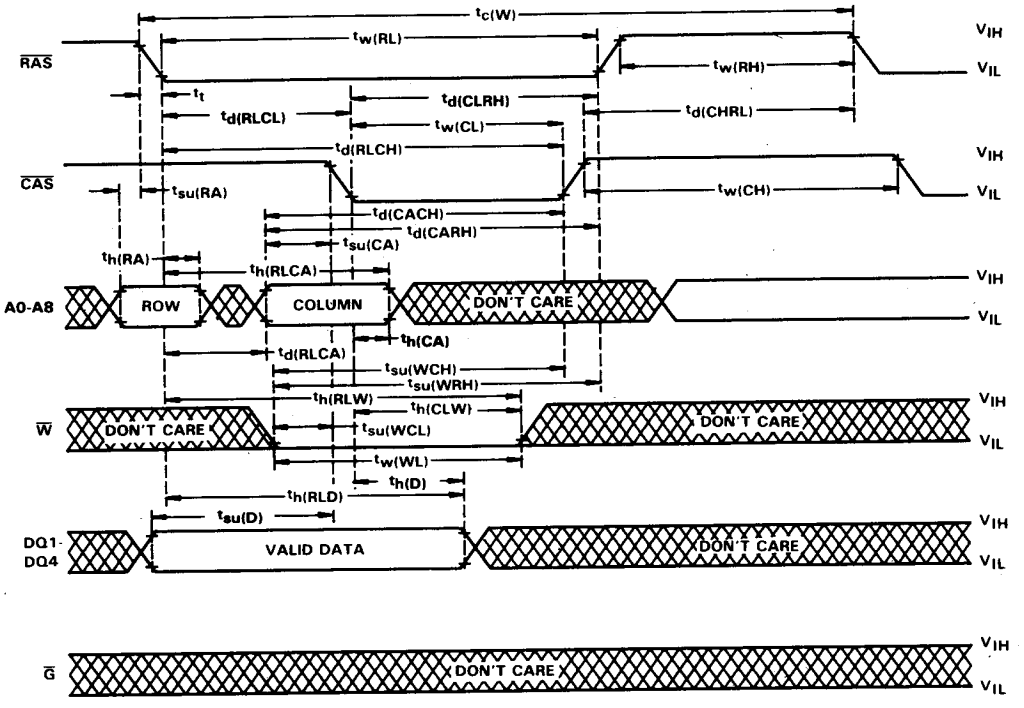
NOTE 18: Output may go from high impedance to an invalid data state prior to the specified access time.

read cycle timing

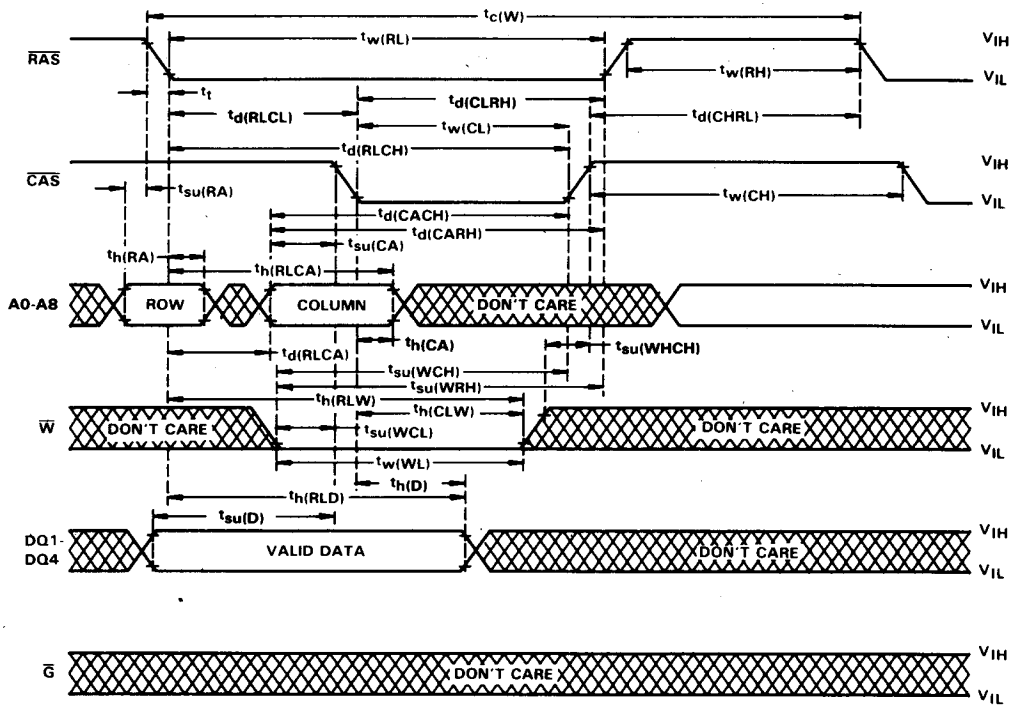


NOTE 18: Output may go from high impedance to an invalid data state prior to the specified access time.

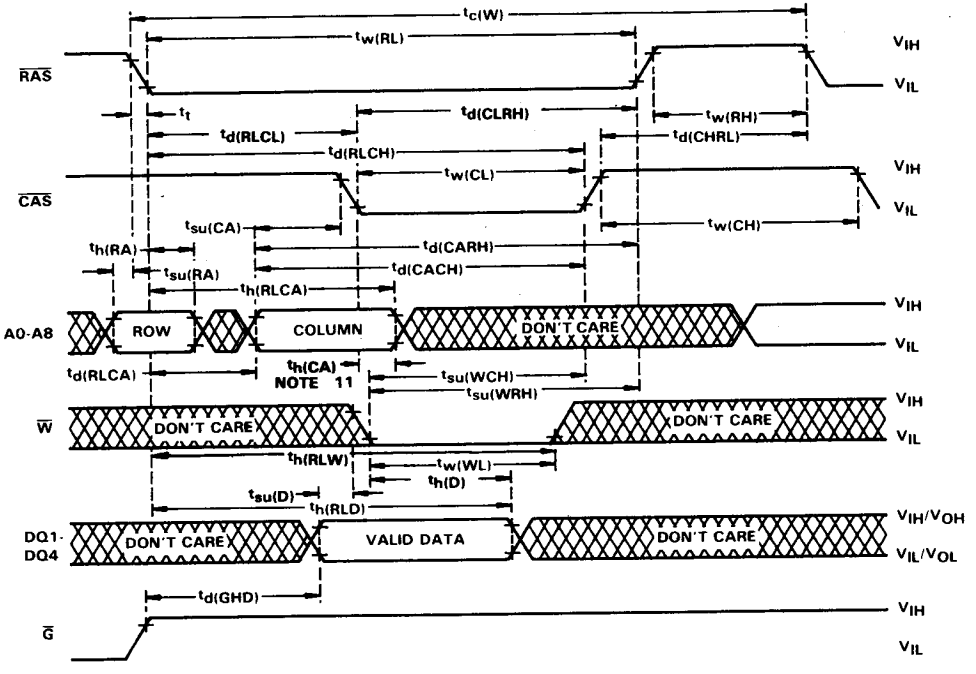
early write cycle timing



early write cycle timing



write cycle timing



NOTE 11: Later of $\overline{CAS}$ or $\overline{W}$ in write operation.

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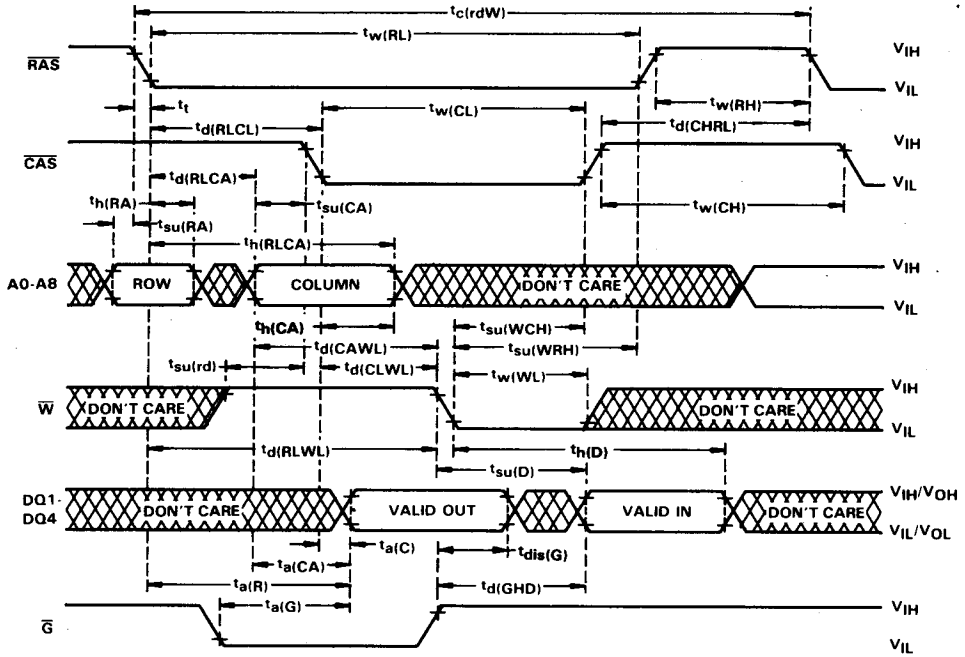
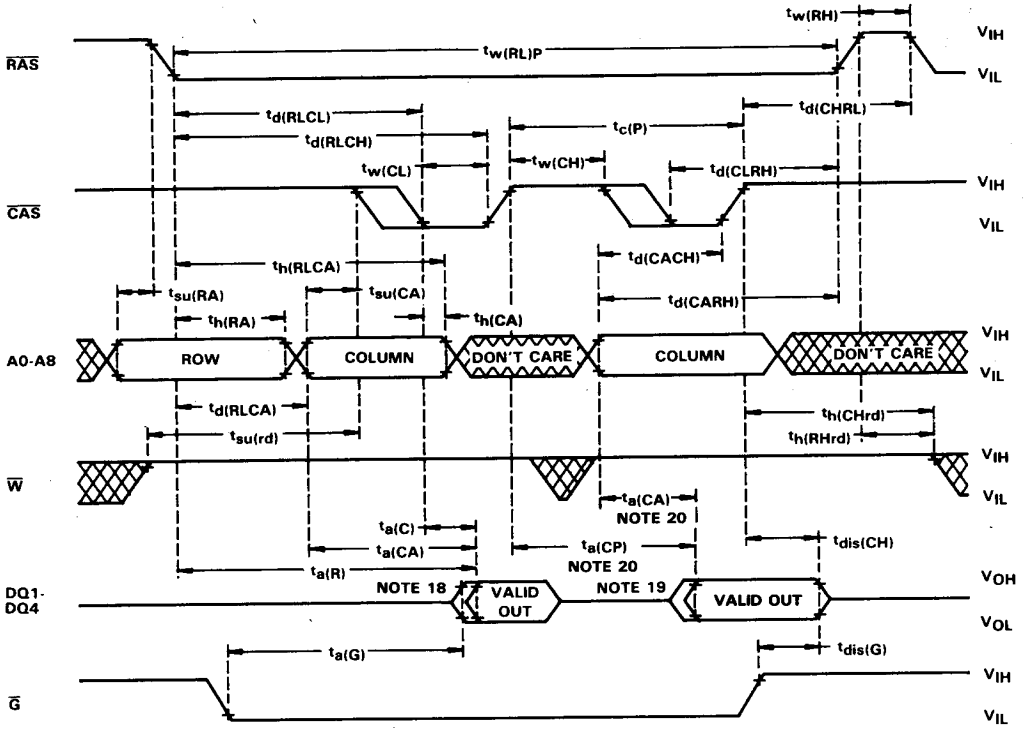
read-write/read-modify-write cycle timing

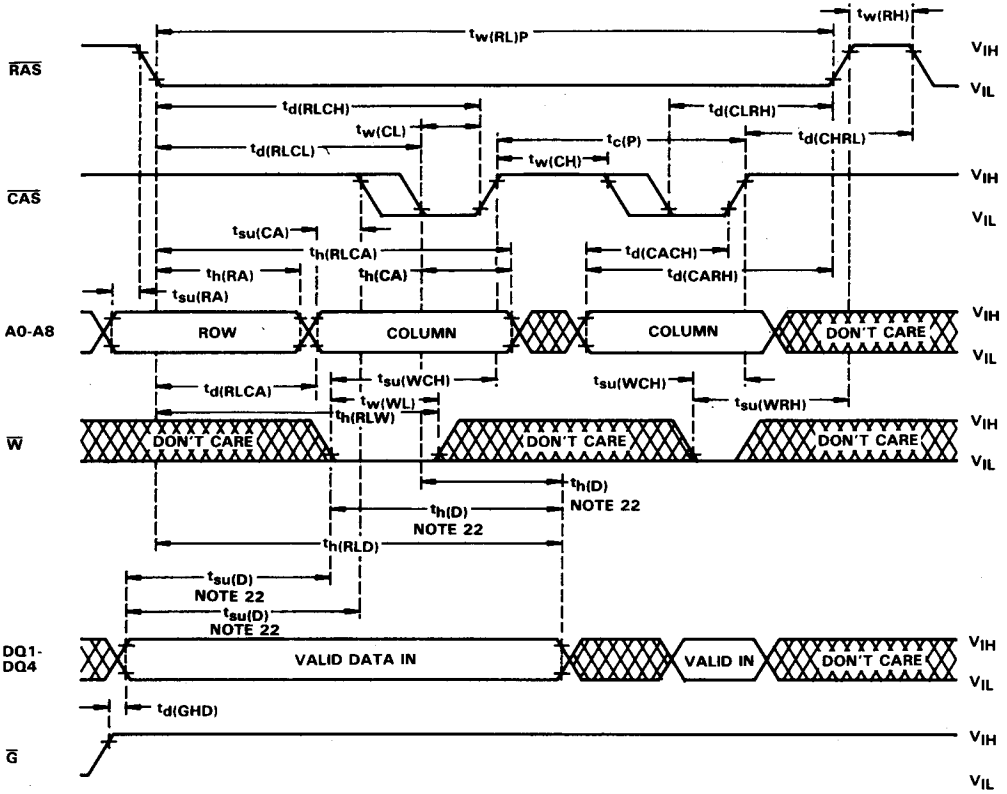


enhanced page-mode read cycle timing



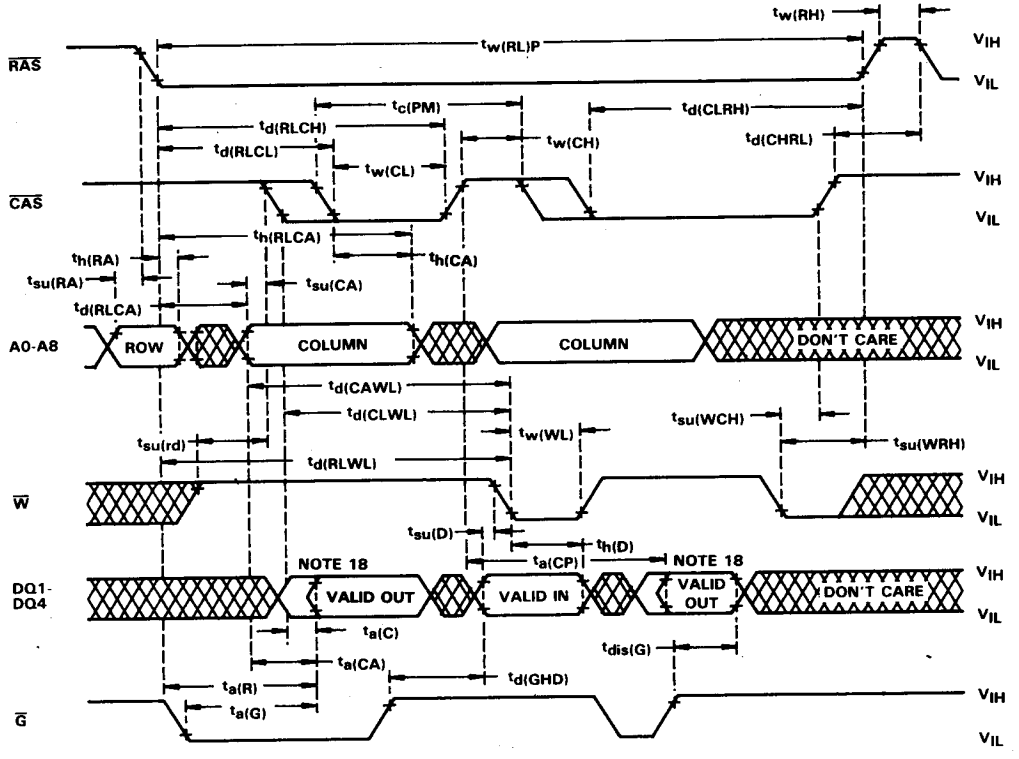
NOTES: 18. Output may go from high impedance to an invalid data state prior to the specified access time.
19. A write cycle or read-modify-write cycle can be mixed with the read cycles as long as the write and read-modify-write timing specifications are not violated.
20. Access time is $t_{a(CP)}$ or $t_{a(CA)}$ dependent.

enhanced page-mode write cycle timing



NOTES: 21. A read cycle or a read-modify-write cycle can be intermixed with the write cycles as long as the read and read-modify-write timing specifications are not violated.
22. Referenced to $\overline{CAS}$ or $\overline{W}$, whichever occurs last.

enhanced page-mode read-modify-write cycle timing



NOTES: 18. Output may go from high impedance to an invalid data state prior to the specified access time.
23. A read or a write cycle can be intermixed with read-modify-write cycles as long as the read and write cycle timing specifications are not violated.

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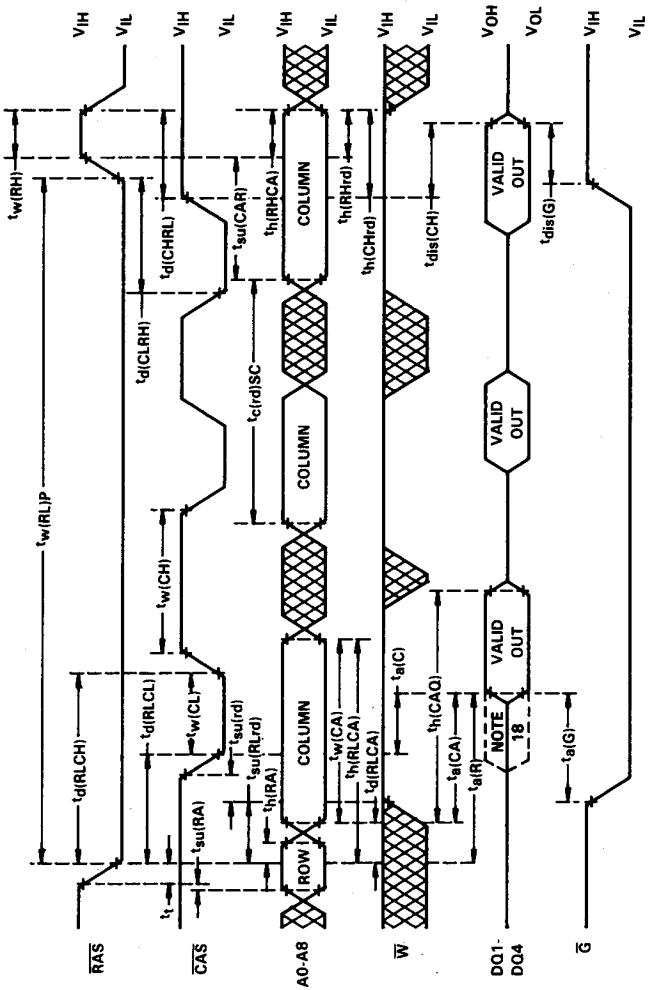
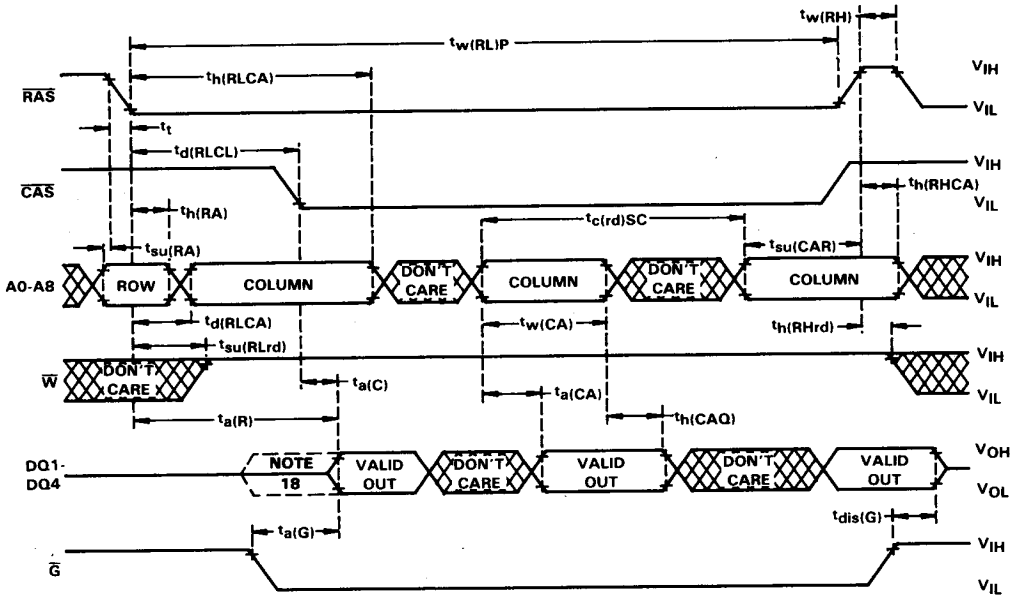
static column decode mode read timing with $\overline{CAS}$ cycling



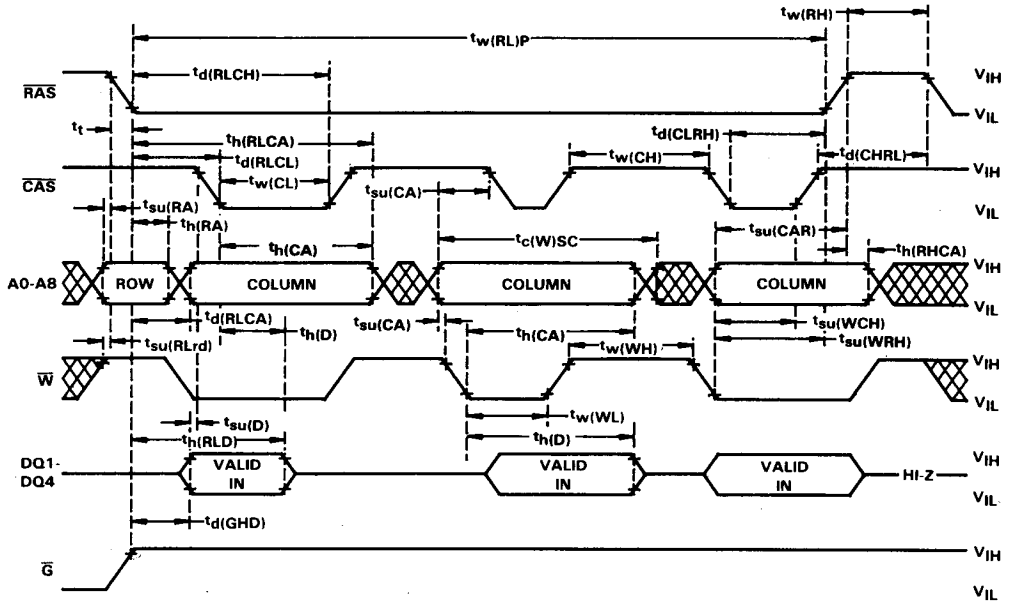
NOTE 18: Output may go from high impedance to an invalid data state prior to the specified access time.

static column decode mode read cycle timing

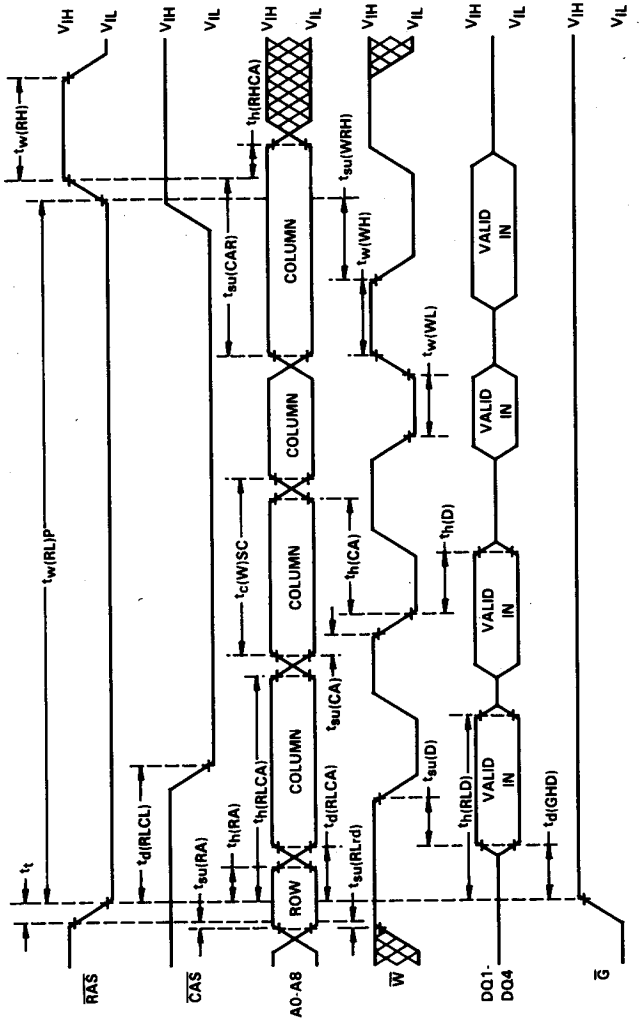


NOTE 18: Output may go from high impedance to an invalid data state prior to the specified access time.

static column decode mode early write cycle timing



static column decode mode write cycle timing



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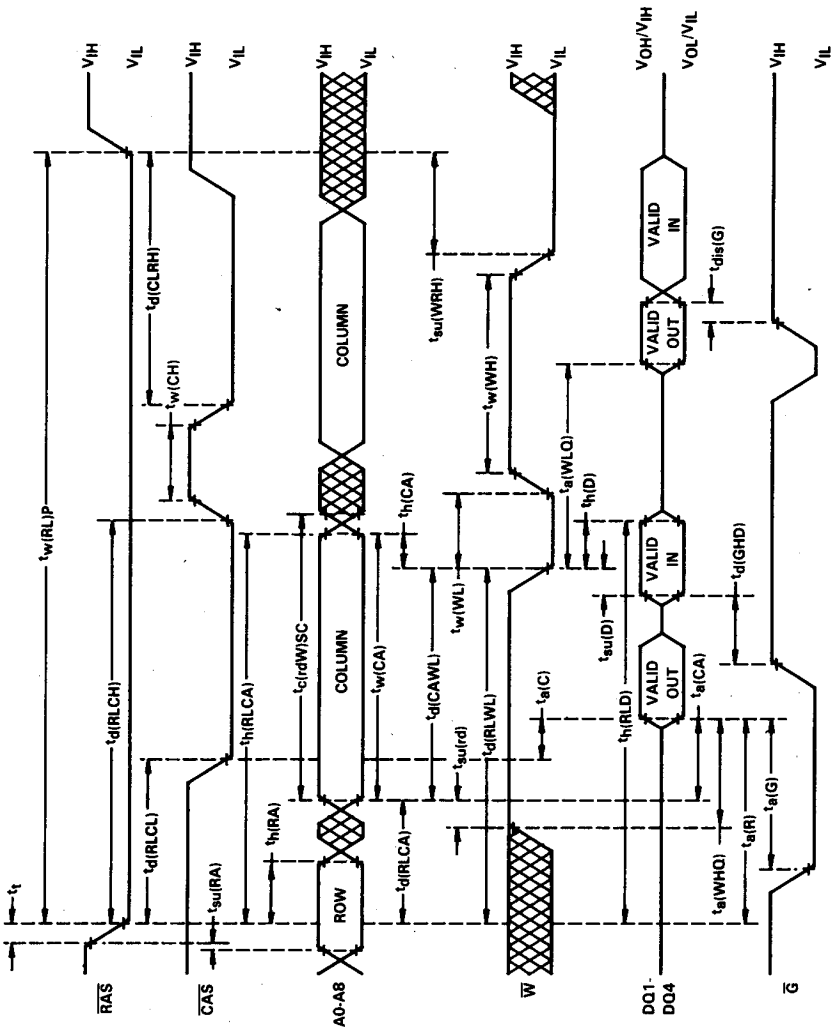
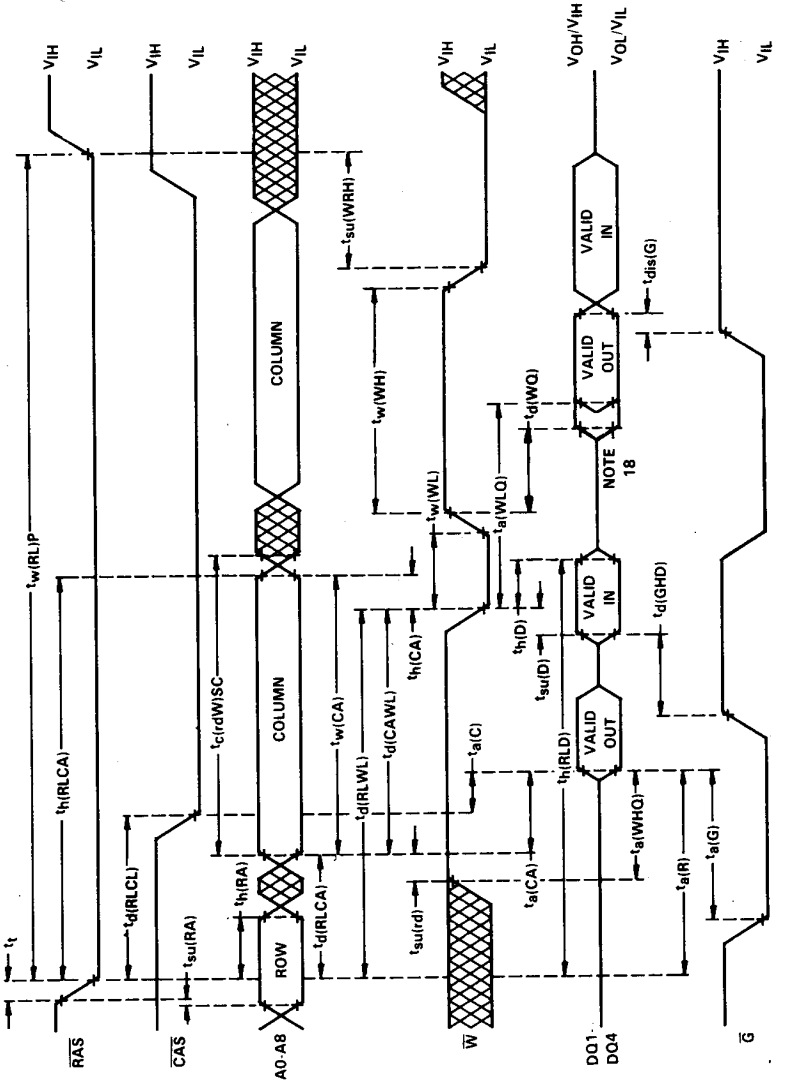
static column decode mode read-modify-write cycle timing with $\overline{CAS}$ cycling

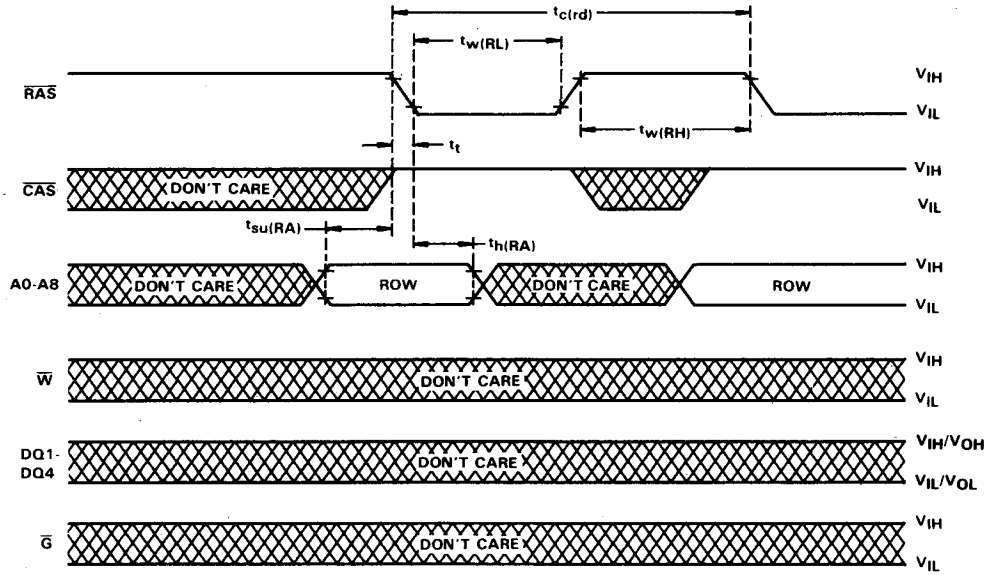


static column decode mode read-modify-write cycle timing

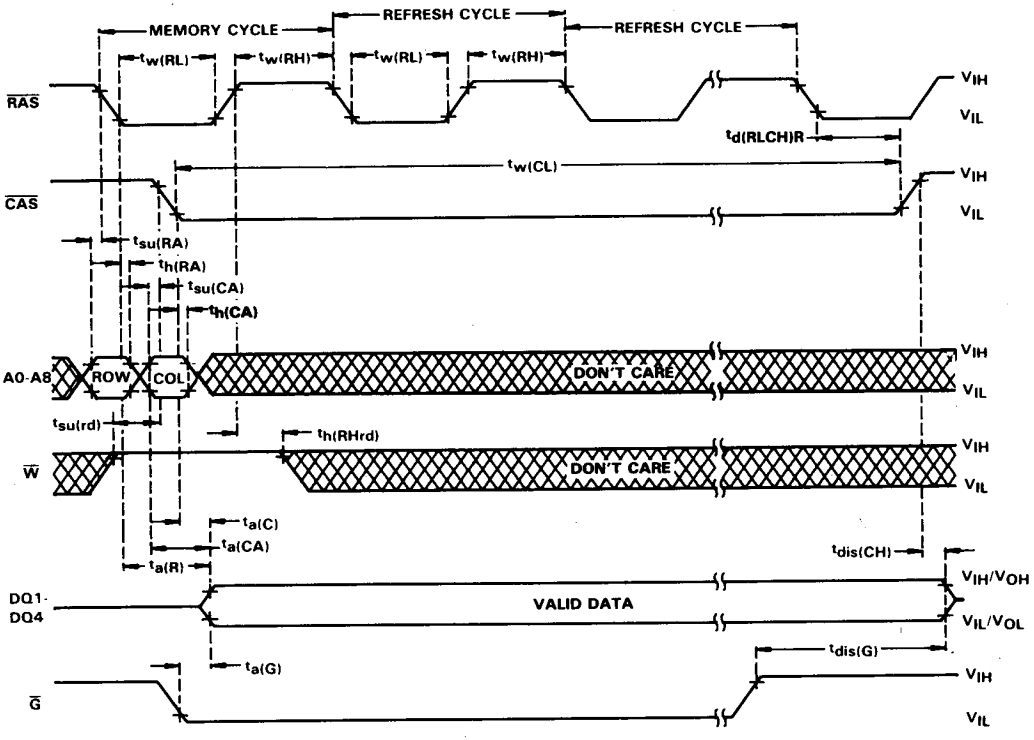


NOTE 18: Output may go from high impedance to an invalid data state prior to the specified access time.

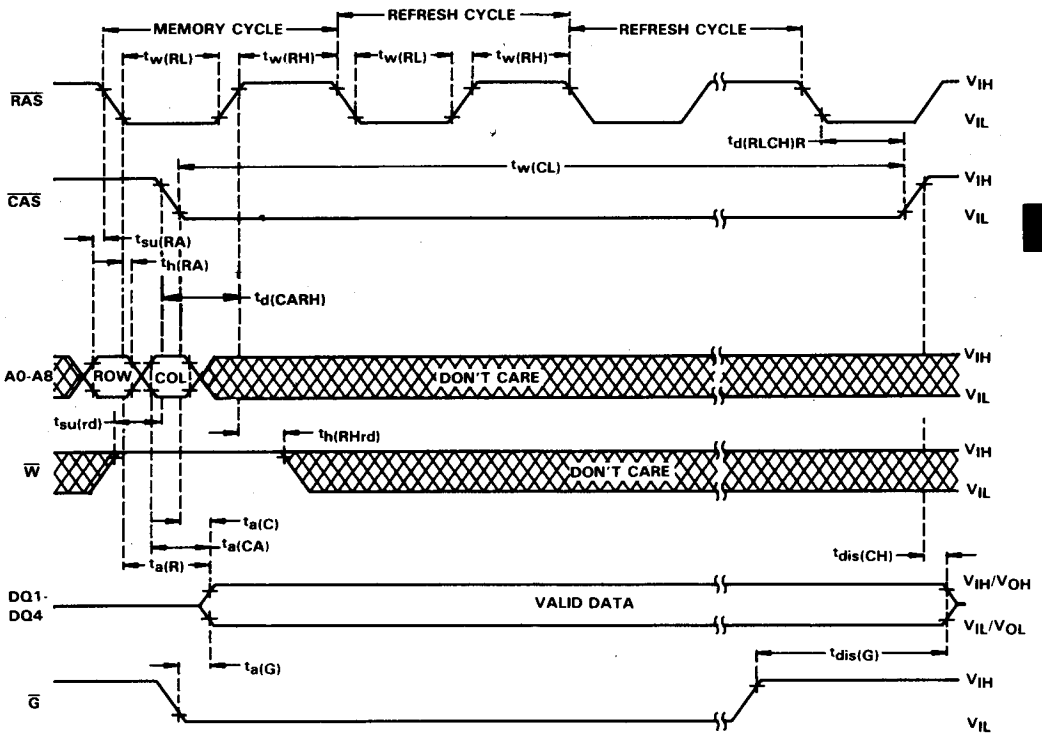
$\overline{\text{RAS}}$-only refresh timing



hidden refresh cycle (enhanced page mode)



hidden refresh cycle (static column decode mode)



automatic ($\overline{CAS}$-before-$\overline{RAS}$) refresh cycle timing