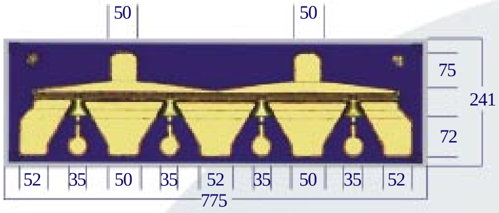
MwT-15

26 GHz Power
GaAs FET

DOWNLOAD ADDITIONAL DATA WWW.MWTINC.COM



CHIP THICKNESS = 125 MICRONS

All Dimensions in Microns

FEATURES

- **+24 dBm POWER OUTPUT AT 12 GHz**
- **9.5 dB SMALL SIGNAL GAIN AT 12 GHz**
- **0.3 MICRON REFRACTORY METAL/GOLD GATE**
- **630 MICRON GATE WIDTH**

DESCRIPTION

The MwT-15 is a GaAs MESFET device whose nominal quarter micron gate length and 630 micron gate width make it ideally suited to applications requiring high-gain in the 500 MHz to 26 GHz frequency range with power outputs ranging from 100-200 milli-watts. The straight geometry of the MwT-15 makes it equally effective for either wideband (e.g. 6 to 18 GHz) or narrow-band applications. The chip is produced using MwT's reliable metal system and all devices are screened to insure reliability. All chips are passivated using MwT's patented "Diamond-Like Carbon" process for increased durability. Designers can use MwT's unique BIN selection feature to choose devices from narrow Idss ranges, insuring consistent circuit operation.

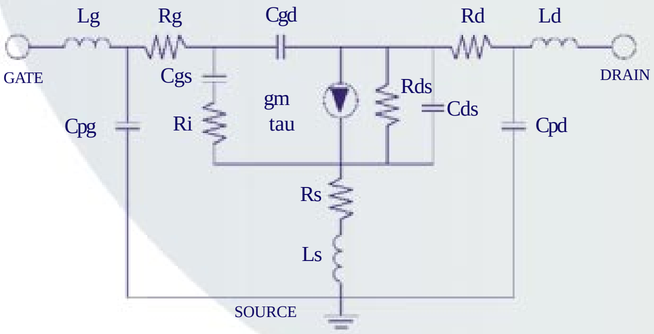
DC SPECIFICATIONS AT Ta = 25°C

SYMBOL	PARAM. & CONDITIONS	UNITS	MIN	TYP	MAX
IDSS	Saturated Drain Current Vds= 4.0 V VGS= 0.0 V	mA	60		240
Gm	Transconductance Vds= 2.0 V VGS= 0.0 V	mS	75	100	
Vp	Pinch-off Voltage Vds= 3.0 V IDS= 4.0 mA	V		-2.0	-5.0
BVGSO	Gate-to-Source Breakdown Volt. Igs= -0.4mA, Igd= 0	V	-6.0	-12.0	
BVGDO	Gate-to-Drain Breakdown Volt. Igd= -0.4 mA, Igs= 0	V	-8.0	-12.0	
Rth	Thermal Resistance MwT-15 Chip	°C/W		80	

RF SPECIFICATIONS AT Ta = 25°C

SYMBOL	PARAMETERS AND CONDITIONS	FREQ	UNITS	MIN	TYP
P1dB	Output Power at 1 dB Compression VDS= 6.0 V Idss= 0.6 IDS=110mA	12 GHz 18 GHz	dBm dBm	23.0	24.5 24.0
SSG	Small Signal Gain VDS= 6.0 V Idss= 0.6 IDS=110mA	12 GHz 18 GHz	dB dB	8.5 7.0	9.5 8.0
PAE	Power Added Efficiency VDS= 6.0 V Idss= 0.6 IDS=110mA	12 GHz	%	30	35
Idss	Recommended IDSS Range for Optimum P1dB		mA		160-220

DEVICE EQUIVALENT CIRCUIT MODEL

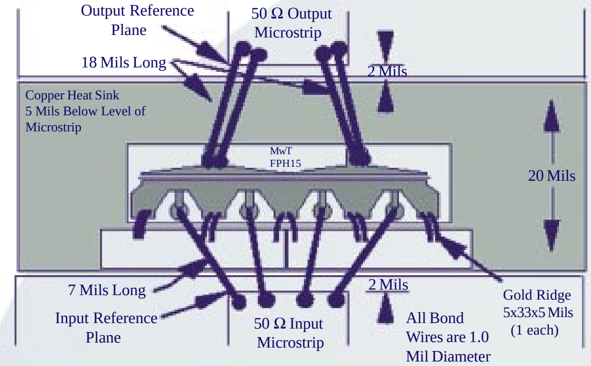


PARAMETER		VALUE	
Source Resistance	Rs	0.10	Ω
Source Inductance	Ls	0.03	nH
Drain-Source Resistance	Rds	170.0	Ω
Drain-Source Capacitance	Cds	0.08	pF
Drain Resistance	Rd	.84	Ω
Drain Pad Capacitance	Cpd	0.05	pF
Drain Inductance	Ld	0.10	nH
Gate Bond Wire Inductance	Lg	0.07	nH
Gate Pad Capacitance	Cpg	0.20	pF
Gate Resistance	Rg	0.10	Ω
Gate-Source Capacitance	Cgs	0.61	pF
Channel Resistance	Ri	2.31	Ω
Gate-Drain Capacitance	Cgd	0.03	pF
Transconductance	gm	100.0	mS
Transit Time	tau	2.6	psec

ORDERING INFORMATION

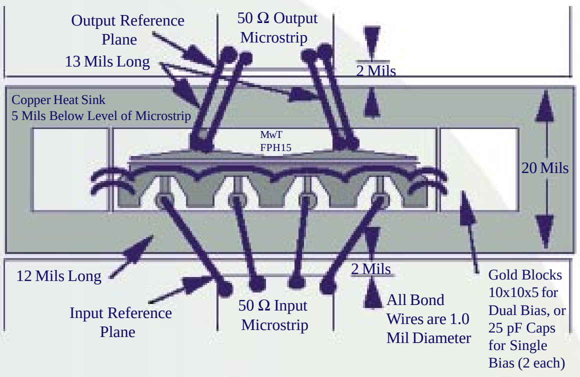
Chip	MwT-15	***When placing order or inquiring, please specify BIN range, wafer no., if known, and screening level required.***

MwT-15
DUAL BIAS

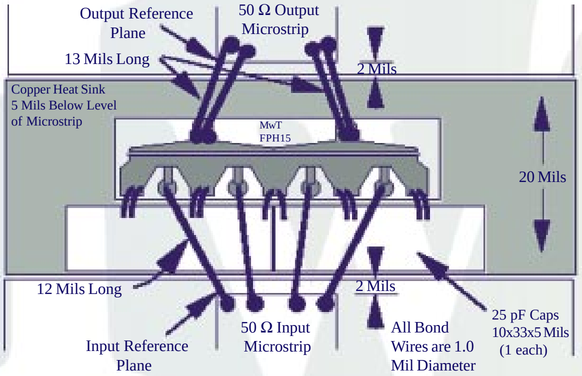


Bonding Configuration used to Obtain "S" Data

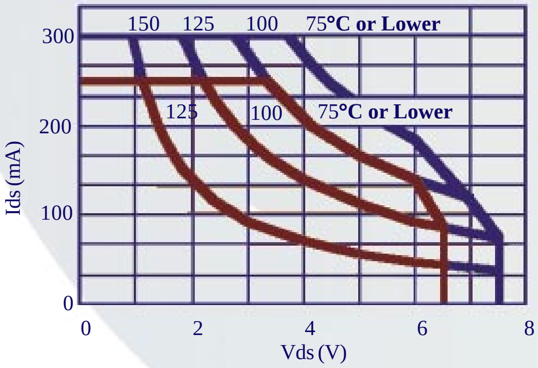
MwT-15
OPTIONAL BONDING



MwT-15
OPTIONAL SINGLE BIAS WITH CAPS



SAFE OPERATING LIMITS vs. BACKSIDE CHIP



🟦 Absolute Maximum
🟥 Continuous Maximum

MAXIMUM RATINGS AT Ta = 25°C

SYMBOL	PARAMETER	UNITS	CONT MAX[1]	ABSOLUTE MAX[2]
VDS	Drain to Source Voltage	V	See Safe Operating Limits	
Tch	Channel Temperature	°C	+150	+175
Tst	Storage Temperature	°C	-65 to +150	+175
Pin	RF Input Power	mW	200	300

NOTES: 1. Exceeding any one of these limits in continuous operation may reduce the mean-time-to-failure below the design goals.
2. Exceeding any one of these limits may cause permanent damage.

BIN SELECTION

BIN#	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
IDSS (mA)	60-70	70-80	80-90	90-100	100-110	110-120	120-130	130-140	140-150	150-160	160-170	170-180	180-190	190-200	200-210	210-220	220-230	230-240

BIN ACCURACY STATEMENT

When placing order or inquiring, please specify BIN range, wafer no., if known, and screening level required.