

OBJECTIVE SPECIFICATIONS

Features

- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs:
 $I_{OL} = 8 \text{ mA} @ V_{OL} = 0.5\text{V}$
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:

74HCTLS: -40°C to +85°C

54HCTLS: -55°C to +125°C

Dual J-K Flip-Flops with Preset and Clear

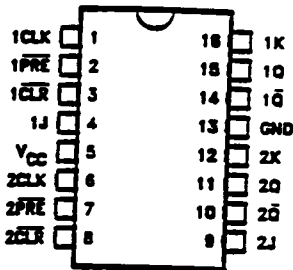
Description

These parts consist of two negative-edge-triggered J-K flip-flops with independent J, K, preset, clear and clock inputs and complementary outputs. The J-K inputs at each flip-flop are enabled when the clock goes high. The input data are transferred to the outputs on the negative-going edge of the clock pulse, provided the setup requirements have been met.

Fabrication using ISI proprietary ICE-MOS process, these devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Pin Configuration



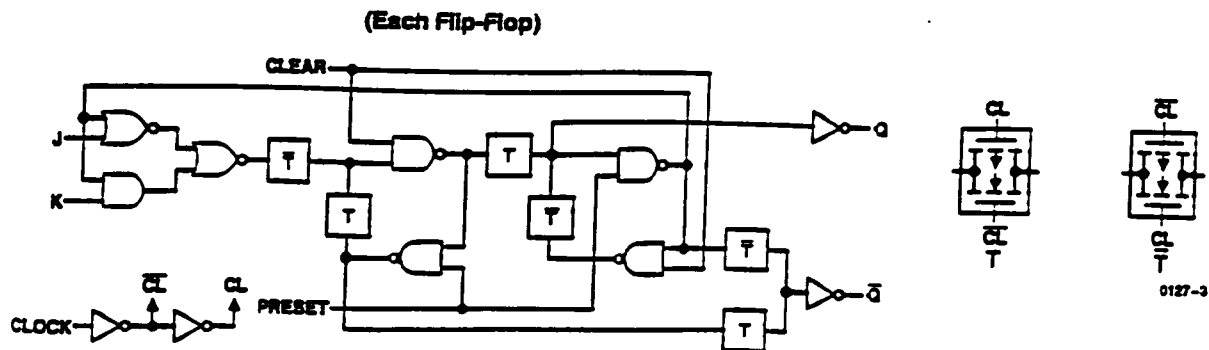
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Function Table

Inputs					Outputs	
PRE	CLR	CLK	J	K	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q ₀	\bar{Q}_0
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q ₀	\bar{Q}_0

*Both outputs will remain high as long as preset and clear are low, but the output states are unpredictable if preset and clear go high simultaneously.

Logic Diagrams



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Absolute Maximum Ratings*

Supply Voltage Range, V_{CC} -0.5V to 7V
 DC Input Diode Current, I_{IK}
 ($V_i < -0.5V$ or $V_i > V_{CC} + 0.5V$)..... ± 20 mA
 DC Output Diode Current, I_{OK}
 ($V_o < -0.5V$ or $V_o > V_{CC} + 0.5V$)..... ± 20 mA
 Continuous Output Current Per Pin, I_o
 ($-0.5V < V_o < V_{CC} + 0.5V$)..... ± 35 mA
 Continuous Current Through
 V_{CC} or GND pins..... ± 125 mA
 Storage Temperature Range, T_{STG} -65°C to +150°C
 Power Dissipation Per Package, P_D *500 mW

*Power Dissipation temperature derating:
 Plastic Package (N): -12mW/°C from 65°C to 85°C
 Ceramic Package (J): -12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} 4.5V to 5.5V
 DC Input & Output Voltages*, V_{IN} , V_{OUT} 0V to V_{CC}

Operating Temperature

Range 74HCTLS: -40°C to +85°C
 54HCTLS: -55°C to +125°C

Input Rise & Fall Times, t_r , t_f Max 500 ns

*Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC Electrical Characteristics ($V_{CC} = 5V \pm 10\%$ Unless Otherwise Specified)

Sym	Parameter	Test Conditions	74HCTLS			54HCTLS	Unit
			$T_A = 25^\circ C$	$T_A = -40^\circ C$ to $+85^\circ C$			
			Typ	Guaranteed Limits			
V_{IH}	Minimum High-Level Input Voltage			2.0	2.0	2.0	V
V_{IL}	Maximum Low-Level Input Voltage			0.8	0.8	0.8	V
V_{OH}	Minimum High-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_o = -20 \mu A$ $I_o = -4 mA$	V_{CC} 4.2	$V_{CC} - 0.1$ 3.98	$V_{CC} - 0.1$ 3.84	$V_{CC} - 0.1$ 3.7	V
V_{OL}	Maximum Low-Level Output Voltage	$V_{IN} = V_{IH}$ or V_{IL} $I_o = 20 \mu A$ $I_o = 4 mA$ $I_o = 8 mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
I_{IN}	Maximum Input Current	$V_{IN} = V_{CC}$ or GND		± 0.1	± 1.0	± 1.0	μA
I_{CC}	Maximum Quiescent Supply Current	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0 \mu A$		4.0	40.0	80.0	μA

AC Electrical Characteristics (Input $t_r, t_f \leq 6$ ns), HCTLS76A

Sym	Parameter	Conditions •	$T_A = 25^\circ\text{C}$ $V_{CC} = 5.0\text{V}$		74HCTLS	54HCTLS	Unit
			Typ	Guaranteed Limits			
					$T_A = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	$T_A = -55^\circ\text{C to } +125^\circ\text{C}$ $V_{CC} = 5.0\text{V} \pm 10\%$	
f_{max}	Maximum Clock Frequency	$C_L = 50$ pF	40	30	25	21	MHz
t_{PLH}	Maximum Propagation Delay, CLK to Q or \bar{Q}		15	20	25	30	ns
t_{PHL}			15	20	25	30	
t_{PLH}	Maximum Propagation Delay, \overline{PRE} or \overline{CLR} to Q or \bar{Q}		15	20	25	30	ns
t_{PHL}		15	20	25	30		
t_{su}	Minimum Setup Time before CLK \downarrow	J or K	10	13	17	20	ns
	\overline{PRE} or \overline{CLR} Inactive		10	13	17	20	
t_h	Minimum Hold Time, J or K after CLK \downarrow		0		0	0	ns
t_w	Minimum Pulse Width	CLK High or Low	10	13	17	20	ns
		\overline{PRE} or \overline{CLR} Low	10	13	17	20	
C_{IN}	Maximum Input Capacitance		5				pF
C_{PD}	Power Dissipation Capacitance*	(per flip-flop)	40				pF

* C_{PD} determines the no-load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$

• For AC switching test circuits and timing waveforms see section 2.