

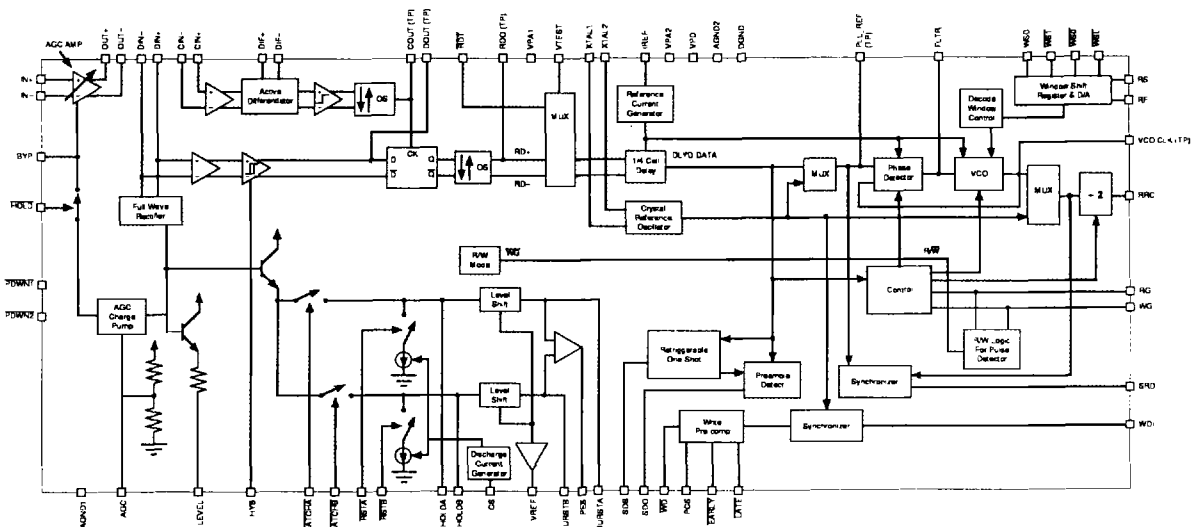
DESCRIPTION

The SSI 32P548 is a low power, high performance Pulse Detection, Data Synchronization combination device. This device is designed for use in low power applications requiring +5V only power supplies. The pulse detection portion of this device detects and validates amplitude peaks in the output from a disk drive read amplifier, as well as detecting embedded servo information to provide position signals used for read head positioning. The data synchronization portion is a 2, 7 data synchronizer with window shift and write pre-compensation capability. The SSI 32P548 achieves low system operating power three ways, with a low operating power (+5V only design) and with two independent power down modes. Mode 1 is a complete shutdown or sleep mode. Mode 2 is a low power mode for use while acquiring servo, where all circuitry not associated with obtaining servo information is powered down. The SSI 32P548 is available in a 52-pin fine pitch QFP, and 68-pin PLCC.

FEATURES

- Highly Integrated Pulse Detector and Data Synchronizer
- +5V only Power Supplies
- Low Power <750 mW (max)
- Dual Power Down Modes
- Dual Servo Burst Channels with Position Error Signal
- Low Pulse Pairing ($\leq \pm 1$ ns)
- 5-12 Mbit/s operation

BLOCK DIAGRAM



CAUTION: Use handling procedures necessary for a static sensitive component.

SSI 32P548

Pulse Detector & Data Synchronizer

CIRCUIT OPERATION

PULSE DETECTOR SECTION

READ MODE

In read mode the SSI 32P548 is used to process either data or servo signals. In the Data Read Mode the input signal is amplified and qualified using an AGC amplifier and pulse level qualification of the detected signal peaks. In the servo read mode the input signal is amplified and rectified. Two servo burst channels are available that provide A and B burst levels.

DATA READ MODE

An amplified head output signal is AC coupled to the IN+ and IN- pins of the AGC amplifier. Gain control is accomplished by full wave rectifying and amplifying the [(DIN+)-(DIN-)] voltage level and comparing it to a reference voltage level at the AGC pin.

The SSI 32P548 contains a dual rate attack charge pump. The value of the attack current is dependent on the instantaneous level at DIN±. For signal levels above 125% of the desired level a fast attack mode is invoked that supplies a 1.3 mA charge current to the network on the BYP pin. Between 125% and 100% of the desired level the circuit enters a slow attack mode and supplies 0.18 mA of charge current to the BYP pin.

Two decay modes are available and are automatically controlled within the device.

Upon a switch to write mode, the device will hold the gain at its previous value. When the device is then switched back to read mode the AGC holds the gain and stays in a low impedance state for 0.9 μs. It then switches into a fast/slow attack mode if the new gain required is less than the previously held gain or a fast decay mode if the gain required is more than its previous value. The fast decay current is 0.12 mA and stays on 0.9 μs. After the 0.9 μs time period the device stays in a steady state slow attack, slow decay mode. The slow decay discharge current is 4.5 μA.

The AGC pin is internally biased so that the target differential voltage input at DIN± is 1.0 Vp-p under nominal conditions. The voltage on this pin can be modified by tying a resistor between AGC and GND or VPA. A resistor to GND decreases the voltage level, while a resistor to VPA increases it. The resulting AGC

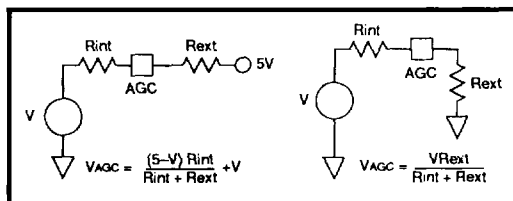


FIGURE 1: AGC Voltage

voltage level is shown in Figure 1; where:

V = Voltage at AGC w/pin open (2.3V, nom)

Rint = AGC pin input impedance (2.5 kΩ, typ)

Rext = External resistor

The new DIN± input target level is nominally 0.45 Vp-p/V_{AGC}.

The maximum AGC amplifier output swing is 3.0 Vp-p at OUT±, which allows for up to 6dB loss in any external filter between OUT± and DIN±.

AGC gain is a linear function of the BYP-pin voltage (VBYP) as shown in Figure 2.

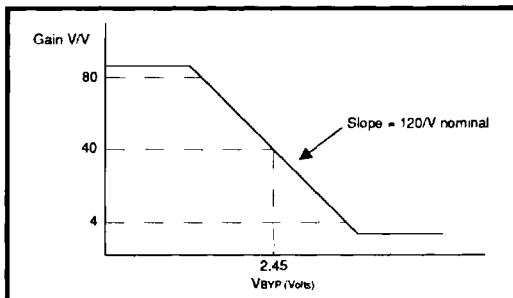


FIGURE 2: AGC Gain

The AGC amplifier has an open collector output and can sink 4.0 mA. For correct operation to the gain range the outputs should be pulled up to VPA through a 340Ω resistor as shown in Figure 3.

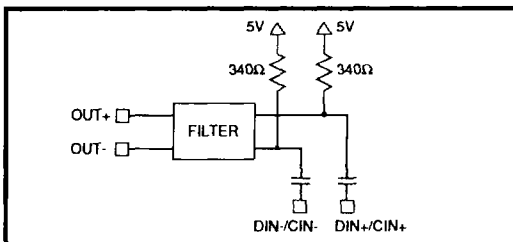


FIGURE 3: AGC Filter

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In the 52-pin package configuration CIN+ and DIN+ will be bonded together, likewise CIN- and DIN- will be bonded together. In this situation one filter must be used for both time and amplitude channels. A multipole Bessel filter is typically used for its linear phase or constant group delay characteristics.

In the amplitude channel the signal is sent to a hysteresis comparator. The hysteresis threshold level is set so that it will be tripped only by valid signal pulses and not by baseband noise. It can be fixed level or a fraction of the DIN± voltage level.

The latter approach is accomplished by using an external filter/network between the LEVEL and HYS pins. This allows setting the AGC slow attack and decay times slow enough to minimize time channel distortion and setting a shorter time constant for the hysteresis level. The LEVEL pin output is a rectified and amplified version of DIN±, 1.0 p-p at DIN± results in 1.0 Vo-p nominally, at the LEVEL pin. A voltage divider is used from LEVEL to ground to set the Hysteresis threshold at a percentage of the peak DIN± voltage. For example, if DIN± is 1.0 Vp-p, then using an equal valued resistor divider will result in 0.5 Vpk at the HYS pin. This will result in a nominal ±0.18V threshold or a 36% threshold of a ±0.500V DIN± input. The capacitor is chosen to set an appropriate time constant. This "feed forward" technique speeds up transient recovery by allowing qualification of the input pulses while the AGC is still settling. This helps in the two critical areas of write to read and head change recovery. Some care in the selection of the hysteresis level time constant must be exercised so as to not miss pattern (resolution) induced lower amplitude signals. The output of the hysteresis comparator is the "D" input of a D-type flip-flop. The DOUT pin is a comparator output signal for testing purposes only.

In the time channel the signal is differentiated to transform signal peaks to zero crossings which are detected and used to trigger a bi-directional one-shot. The one-shot output pulses are used as the clock input of the D flip-flop. The COUT pin provides the one-shot output for test purposes.

The differentiator function is accomplished by an external network between the DIF+ and DIF- pins. The transfer function from CIN± to the comparator input (not DIF±) is:

$$A_v = \frac{-2000Cs}{LCs^2 + C(R+92)s + 1}$$

where: C, L, R are external passive components
20 pF < C < 150 pF
s = jω = j2πf

During normal operation, the time channel clocks the D flip-flop on every positive and negative peak of the CIN± input. The D input to the flip-flop only changes state when the DIN± input exceeds the hysteresis comparator threshold opposite in polarity to the previous threshold exceeding peak.

The time channel, then, determines signal peak timing and the amplitude channel determines validity by blocking signal peaks that do not exceed the hysteresis comparator threshold. The delays in each of these channels to the D flip-flop inputs are well matched.

SERVO READ MODE

A position error signal (PES) is generated based on the relative amplitude of two servo signals, BURST A and BURST B.

Rectified servo signal peaks are captured on hold capacitors at the HOLDA/B pins. This is accomplished by pulling LATCHA or LATCHB low for a sample period. Additionally, a hold capacitor discharge current of up to 1.5 mA can be turned on by pulling RSTA/RSTB low.

Outputs BURSTA/B and PES are referenced to an internal reference supplied by the VREF pin.

WRITE MODE

In Write Mode the SSI 32P548 Pulse Detector section is disabled and preset for the following Read Mode. The digital circuitry is disabled, the input AGC amplifier gain is held at its previous value and the AGC amplifier input impedance is reduced.

Holding the AGC amplifier gain and reducing input impedance shortens system Write to Read recovery times.

The lowered input impedance improves settling time by reducing the time constant of the network between the SSI 32P548 and a head preamplifier such as the SSI 32R1200R. Write to read timing is controlled to maintain the reduced impedance for 0.9 μs before the AGC circuitry is activated. Coupling capacitors should be chosen with as low a value as possible consistent with adequate bandwidth to allow more rapid settling.

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DATA SYNCHRONIZER SECTION

The SSI 32P548 is designed to perform data synchronization and write precompensation in rotating memory systems which utilize a 2, 7 RLL and MFM encoding format. In the Read Mode the SSI 32P548 performs Data Synchronization, and Preamble Detect. In the Write Mode, the SSI 32P548 performs write precompensation. The interface electronics and architecture of the SSI 32P548 have been optimized for use as a companion device to the WD 42C22 controllers.

The SSI 32P548 can operate with data rates ranging from 5 to 12 Mbit/s. This data rate is established by a single 1% external resistor, RR, connected from pin IREF to VPA2. This resistor establishes a reference current which sets the VCO center frequency, the phase detector gain, and the 1/4 cell delay. The value of this resistor is given by:

$$RR = 50/DR - 1.7 \text{ (k}\Omega\text{)}$$

Where: DR = Data Rate in Mbit/s

An internal crystal reference oscillator, operating at twice the data rate, generates the standby reference for the PLL. A series resonant crystal between XTAL1 and XTAL2 should be selected at twice the Data Rate. If a crystal oscillator is not desired, then an external TTL compatible reference may be applied to XTAL1, leaving XTAL2 open.

The SSI 32P548 employs a Dual Mode Phase Detector; Harmonic in the Read Mode and Non-Harmonic in Write and Idle Modes. In the Read Mode the Harmonic Phase Detector updates the PLL with each occurrence of a DLYD DATA pulse. In the Write and Idle Modes the Non-Harmonic Phase Detector is continuously enabled, thus maintaining both phase and frequency lock. By acquiring both phase and frequency lock to the crystal reference oscillator and utilizing a zero phase restart technique, false lock to DLYD DATA is eliminated.

The phase detector incorporates a charge pump in order to drive the loop filter directly. The polarity and width of the output current pulses correspond to the direction and magnitude of the phase error. Figure 4 depicts the average output current as function of the input phase error (relative to the VCO period.)

The READ GATE (RG), and WRITE GATE (WG), inputs control the device mode as described in Table 1. RG is an asynchronous input and may be initiated or terminated at any position on the disk. WG is also an asynchronous input, but should not be terminated prior to the last output Write Data pulse.

READ OPERATION

The Data Synchronizer utilizes a fully integrated fast acquisition PLL to accurately develop the decode window. Read Gate, RG, initiates the PLL locking sequence and selects the PLL reference input; a high level (Read Mode) selects the Read Data input and low level selects the crystal reference oscillator.

In the Read Mode the rising edge of DLYD DATA enables the Phase Detector while the falling edge is phase compared to the rising edge of the VCO. As depicted in Figure 2, DLYD DATA is a 1/4 cell wide (TVCO/2) pulse whose leading edge is defined by the leading edge of Read Data. RRC is generated from the rising edges of the VCO clock. By utilizing a fully integrated symmetrical VCO running at twice the data rate, RRC is insured to be accurate and centered symmetrically about the falling edges of DLYD DATA. The accuracy of the 1/4 cell delay only affects the retrace angle of the phase detector and does not influence the accuracy of RRC.

Shifting the symmetry of the VCO clock effectively shifts the relative position of the DLYD DATA pulse within the decode window. This powerful capability easily facilitates defect mappings, automatic calibration, window margin testing, error recovery, and systematic error cancellation. For enhanced disk drive testability and error recovery, decode window control is provided via a μ P port (WSL, WSD, WS0, WS1) as described in Table 2. In application not utilizing this feature, WSL should be left open or connected to VPA2, while WSD, WS0, and WS1 can be left open.

Window shifts in the range of $\pm 1.5\%$ to $\pm 7.5\%$ of TORC are easily programmed by latching the appropriate control word into the Window Shift Register with the WSL pin. Shifts in the positive or negative directions result in early or late decode windows respectively, as depicted in Figure 6. Additionally, for small systematic error cancellation, a resistor, R, connected from either RS (Early) or RF (Late) to ground will provide analog control over the decode window. The magnitude of this shift, TSA is determined by:

$$TSA = 0.125 \text{ TORC} \left(1 - \frac{790 + R}{1450 + R} \right)$$

Where: R is in Ω

Pins RF and RS are intended to be used as a trim and should be restricted to $\pm 1.5\%$ window shifts. They can be used in conjunction with the digital control port.

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In Non-Read Modes, the PLL is locked to the crystal reference oscillator. This forces the VCO to run at a frequency which is very close to that required for tracking actual data and thus minimizes the associated frequency step during acquisition. When RG transitions, the VCO is stopped momentarily, then restarted in an accurate phase alignment with the next PLL reference input pulse. By minimizing the phase alignment in this manner (phase error ≤ 0.5 rads), the acquisition time is substantially reduced.

PREAMBLE DETECTION

Preamble detection timing is set by the sum of the 1/4 cell delay and the retriggerable one-shot delay. The 1/4 cell timing capacitor is included on-chip and its timing is externally set by resistor RR. The retriggerable one-shot timing is externally set by resistor Rd and capacitor Cd. The sum of their delays is set to exceed the preamble bit spacing. Therefore, a continuous stream of input pulses at the preamble pulse rate keeps the SDO high, and a longer bit cell time input period allows the one-shot to time out producing a low at SDO.

WRITE OPERATION

Write precompensation circuitry is provided to compensate for media bit shift caused by intersymbol interference. The magnitude of the time shift, TC, is determined by an external R-C network on the PCS pin given by:

$$TC = 0.155 R_p C_p$$

Direction of the time shift is determined by the state of the EARLY and LATE inputs.

POWER DOWN MODE

Two power down modes are provided to reduce power usage during the idle periods. Taking PDWN1 low causes the device to go into complete shutdown, and taking the PDWN2 pin low shuts down all functions not required for servo acquisition.

MODE CONTROL

The SSI 32P548 circuit mode is controlled by the PDWN1, PDWN2, HOLD, RG, and WG pins as shown in Table 1.

TABLE 1: Mode Control

WG	RG	HOLD	PDWN1	PDWN2	
0	0	1	1	1	Read Mode VCO Locked to XTAL
0	1	1	1	1	Read Mode VCO Locked to Read Data
0	X	0	1	1	Read Mode AGC gain held constant*
1	0	X	1	1	Write Mode AGC gain held constant* Input impedance reduced
X	X	X	0	X	Power Down 1 - Power shutdown mode
X	X	X	1	0	Power Down 2 - Servo mode

* AGC gain will drift at a rate determined by BYP and Hold mode discharge current.

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Ts, NOMINAL WINDOW SHIFT	WSD	WS1	WS0
+TS3	0	0	0
+TS2	0	0	1
+TS1	0	1	0
0	0	1	1
-TS3	1	0	0
-TS2	1	0	1
-TS1	1	1	0
0	1	1	1

TABLE 2: Decode Window Symmetry Control

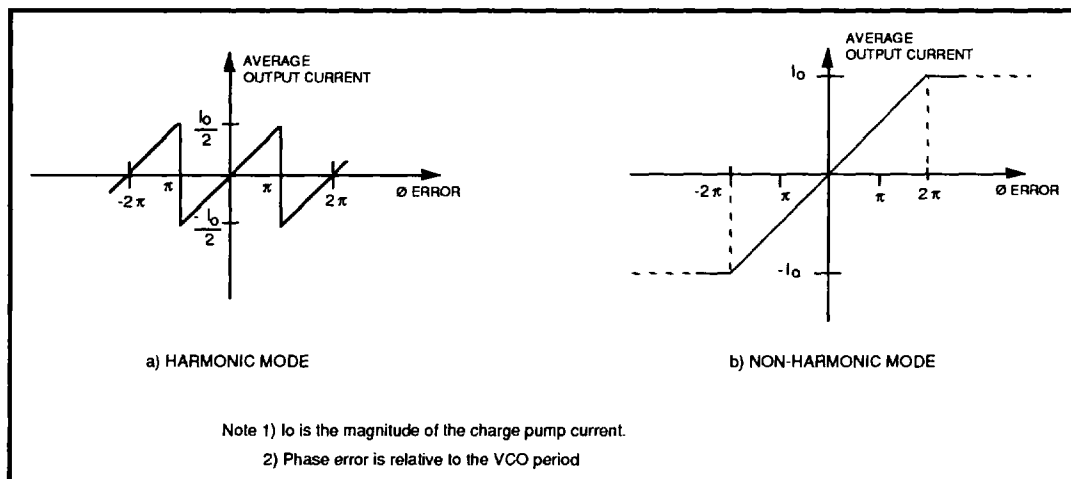


FIGURE 4: Phase Detector Transfer Function

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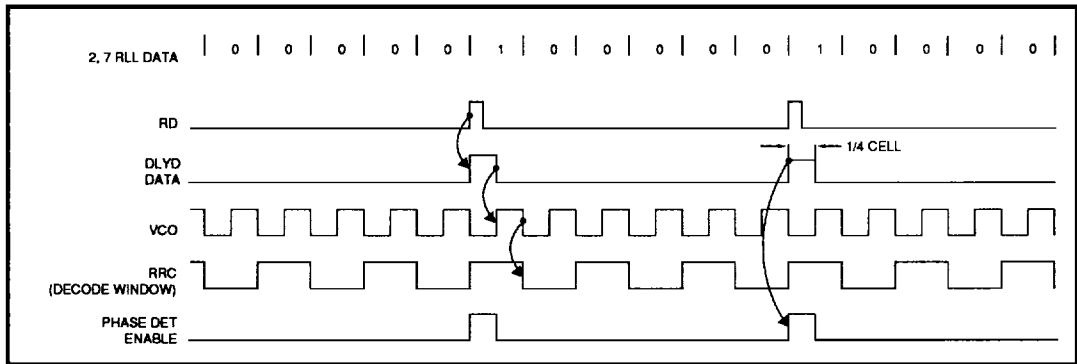


FIGURE 5: Data Synchronization Waveform Diagram

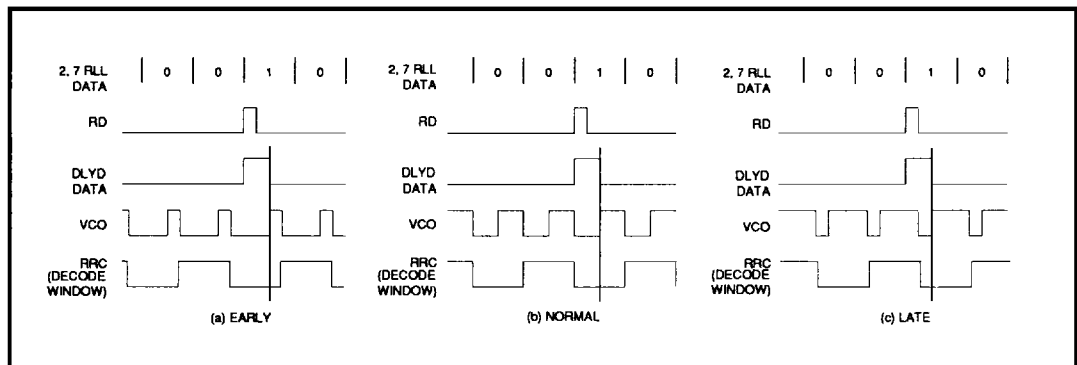


FIGURE 6: Decode Window

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PIN DESCRIPTION

NAME	TYPE	DESCRIPTION
VPA1	I	Analog (+5V) power supply for pulse detector.
AGND1	I	Analog ground pin for pulse detector block.
VPA2	I	Analog (+5V) supply pin for data synchronizer block.
AGND2	I	Analog ground pin for data synchronizer block.
VPD	I	Digital (+5V) power supply pin.
DGND	I	Digital ground pin.
IN+, IN-	I	Analog signal input pins.
OUT+, OUT-	O	Read path AGC Amplifier output pins.
DIN+, DIN- *	I	Analog input to the hysteresis comparator.
CIN+, CIN- *	I	Analog input to the differentiator.
DIF+, DIF-	I/O	Pins for external differentiating network.
COUT	O	Test point for monitoring the flip-flop clock input.
DOUT	O	Test point for monitoring the flip-flop D-input.
RDO	O	Test point for ECL like read data prior to input to the data synchronizer.
BYP	I/O	An AGC timing capacitor or network is tied between this pin and AGND1.
AGC	I	Reference input voltage for the read data AGC loop.
LEVEL	O	Output from fullwave rectifier that may be used for input to the hysteresis comparator.
HYS	I	Hysteresis level setting input to the hysteresis comparator.
HOLD	I	TTL compatible pin that holds the AGC gain when pulled low.
LATCHA, LATCHB	I	TTL compatible inputs that switch channel A or B into peak acquisition mode when low.
RST, RSTA, RSTB **	I	TTL compatible input that enables the discharge of channels A & B hold capacitors when held low.
CS***	I	Hold capacitor discharge current magnitude is controlled by a resistor from this pin to VPA or GND. If left open the default current is 1.5 mA.
HOLDA, HOLDB	I/O	Peak holding capacitors are tied from each of these pins to AGND1.
VREF	O	Reference voltage for Servo outputs.
BURSTA, BURSTB	O	Buffered hold capacitor voltage outputs.
PES	O	Position error signal, A minus B output.
PDWN1	I	Low state on this pin puts the device in a low power "off" state.
PDWN2	I	Low state on this pin disables all circuitry not required for use during Servo mode.
XTAL1, XTAL2	I	Crystal oscillator connections: if a crystal oscillator is not desired, XTAL1 may be driven by a TTL source with XTAL2 open.

*In 52-pin package CIN+ will be internally bonded to DIN+, CIN- will be internally bonded to DIN-.

**RSTA and RSTB will be internally bonded to RST in 52-pin package, and separately bonded out in 68-pin package.

***Not available in 52-pin package.

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PIN DESCRIPTION (Continued)

NAME	TYPE	DESCRIPTION
IREF	I	Timing program pin: the VCO center frequency, Phase Detector Gain and the 1/4 cell delay are a function of the current source into pin IREF. The current is set by an external resistor, RR connected from IREF to VPA2.
FLTR	I/O	Filter pin: the phase detector output and VCO input node. The loop filter is connected to this pin.
SRD	O	Synchronized Read Data: read data that has been re-synchronized to read clock.
WSD	I	Window Symmetry Direction: controls the directions of the optional window symmetry shift. Pin WSD has an internal resistor pull-up.
$\overline{WS0}$	I	Window symmetry control bit: a low level introduces a window shift of 1.5% TORC (read reference clock period) in the direction established by WSD pin. $\overline{WS0}$ has an internal resistor pull-up.
$\overline{WS1}$	I	Window Symmetry Control bit: a low level introduces a window shift of 6% TORC (read reference clock period) in the direction established by WSD. A low level at both $\overline{WS0}$ and $\overline{WS1}$ will produce the sum of the two window shifts. Pin $\overline{WS1}$ has an internal resistor pull-up.
WSL	I	Window Symmetry Latch: used to latch the input window symmetry control bits WSD, $\overline{WS0}$, $\overline{WS1}$ into the internal DAC. An active low level latches the input bits.
RF, RS*	I	WINDOW SYMMETRY ADJUST PINS: Provides analog control over the decode window symmetry; typically used to null out any window symmetry offset. A resistor connected from either RF or RS to AGND will provide magnitude and direction control. They can be used in conjunction with the digital control port WSD, $\overline{WS0}$, $\overline{WS1}$.
RRC	O	Read/Reference Clock: a multiplexed clock source used by the controller. In the read mode, this clock is the VCO frequency divided by two (1/TORC) and in the write mode it is the crystal reference frequency divided by two (1/TORO). No short clock pulses are generated during a mode change.
SDS	I	Sync Detect Set: used to program the preamble detect timing with an external RC Network. Connect the capacitor, Cd to VPA2 and the resistor, Rd, to AGND2.
RG	I	Read gate: selects the PLL reference input and initiates the PLL synchronization sequence. A high level selects the internal RD± inputs. A low level selects the crystal reference oscillator, Pin RG has an internal resistor pull-up.
WG	I	Write Gate: enables the write mode. Pin WG has an internal resistor pull-up.
SDO	O	Sync Detect Output: an active high output that indicates successful detection of the preamble sync field.
WDI	I	Write Data Input, active high.
\overline{WD}	O	Write Data: encoded write data output, active low.
PCS	I	Precomp Set: used to set the magnitude of the write pre-compensation time shift via an external capacitor, Cp to VPA2 and an external resistor, Rp to AGND2.
\overline{EARLY}	I	Early pin: shifts Write Data pulses earlier in their relative position; \overline{EARLY} and \overline{LATE} cannot be active simultaneously.

*Not available in 52-pin package.

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PIN DESCRIPTION (Continued)

NAME	TYPE	DESCRIPTION
LATE	I	Late Pin: shifts Write Data pulses later in their relative position LATE and EARLY cannot be active simultaneously.
PLL_REF	O	An open emitter ECL output test point. The positive edges of this output signal are phase locked with the positive edges of the VCO CLK signal. These two edges may be used to estimate window centering. The time jitter of the negative edge of the PLL_REF is an indication of media bit shift. Two external resistors are required to use this pin. They should be removed during normal operation for reduced power dissipation.
VCO CLK*	O	VCO CLK: An open emitter ECL output test point. Two external resistors are required to perform this test. They should be removed during normal operation for reduced power dissipation.
RDT, VTEST*	I	Input test pins for testing the Data Synchronizer section only. To test the Data Synchronizer, connect VTEST pin to VPA2 and feed the TTL level test signal to RDT pin.

* Not available on 52-pin package

ELECTRICAL CHARACTERISTICS

Recommended conditions apply unless otherwise specified.

ABSOLUTE MAXIMUM RATINGS

Operation outside these rating limits may cause permanent damage to this device.

PARAMETER	RATING	UNIT
5V Supply Voltage, VPA1, VPA2, VPD	6.0	V
Pin Voltage (Analog pins)	-0.3 to VPA1, 2 + 0.3	V
Pin Voltage (All others)	-0.3 to VPD + 0.3 or +12 mA	V
Storage Temperature	65 to 150	°C
Lead Temperature (Soldering 10 sec.)	260	°C

RECOMMENDED OPERATING CONDITIONS

Currents flowing into the chip are positive.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Supply Voltage (VPA1, 2 & VPD)		4.75	5.0	5.25	V
T _j Junction Temperature		25		135	°C

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POWER SUPPLY

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
IVPA1, 2 Supply Current IVPD	Outputs unloaded; $\overline{\text{PDWN1}}$, $\overline{\text{PDWN2}}$ = high or open			160	mA
Pd Power dissipation	$T_a = 25^\circ\text{C}$, outputs unloaded		650	750	mW
	$\overline{\text{PDWN1}}$ = low, Outputs unloaded		300	380	mW
	$\overline{\text{PDWN2}}$ = low, $\overline{\text{PDWN1}}$ = high		450	550	mW

LOGIC SIGNALS

VIL Input Low Voltage		-0.3		0.8	V
VIH Input High Voltage		2.0		VCC+0.3	V
IIL Input Low Current	VIL = 0.4V	0.0		-0.4	mA
IIL WG Input Low Current	VIL = 0.4V	0.0		-0.8	mA
IIH Input High Current	VIH = 2.7V			100	μA
VOL Output Low Voltage	IOL = 4.0 mA			0.5	V
VOH Output High Voltage	IOH = -400 μA	2.7			V
VIHX XTAL1 Input High Voltage		2.6			V

* Output load is a 4K resistor to 5V and a 10 pF capacitor to DGND.

MODE CONTROL

Enable to/from $\overline{\text{PDWN1}}$, $\overline{\text{PDWN2}}$ Transition Time	Settling time of external capacitors not included, pin high to/from low			20	μs
Read to Write Transition Time	WG pin low to high			1.0	μs
Write to Read Transition Time	WG pin high to low AGC setting not included	0.5	0.9	1.3	μs
HOLD On to/from HOLD Off Transition Time	$\overline{\text{HOLD}}$ pin high to/from low			1.0	μs
RG Time Delay				100	ns

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READ MODE WG is low

AGC AMPLIFIER

Unless otherwise specified, recommended operating conditions apply. Input signals are AC coupled to IN±. OUT± are loaded differentially with >340Ω x 2, and each side is loaded with < 10 pF to AGND, and AC coupled to DIN±. A 2000 pF capacitor is connected between BYP and AGND. AGC pin is open.

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Gain Range	$1.0 V_{p-p} \leq (OUT+) - (OUT-) \leq 3.0 V_{p-p}$	4		80	V/V
Output Offset Voltage	Over entire gain range	-400		+400	mV
Maximum Output Voltage Swing	Set by BYP pin	3.0			V _{p-p}
Differential Input Resistance	(IN+) - (IN-) = 100 mV _{p-p} @ 2.5 MHz		5.0		kΩ
Differential Input Capacitance	(IN+) - (IN-) = 100 mV _{p-p} @ 2.5 MHz			10	pF
Common Mode Input Impedance	WG = low, IN+ or IN-		2.7		kΩ
	WG = high, IN+ or IN-			250	Ω
Input Noise Voltage	Gain set to maximum			15	nV/√Hz
Bandwidth	-3 dB bandwidth at maximum gain	16			MHz
OUT+ & OUT- Pin Current	No DC path to AGND		-4.0		mA
CMRR (Input Referred)	(IN+) = (IN-) = 100 mV _{p-p} @ 5 MHz, gain set to max	40			dB
PSRR (Input Referred)	VPA1, 2 = 100 mV _{p-p} @ 5 MHz, gain set to max	30			dB
(DIN+) - (DIN-) Input Swing vs. AGC Input	$25 mV_{p-p} \leq (IN+) - (IN-) \leq 250 mV_{p-p}$, $\overline{HOLD} = \text{high}$, $0.5 V_{p-p} \leq (DIN+) - (DIN-) \leq 1.5 V_{p-p}$	0.37	0.45	0.56	V _{p-p} /V
(DIN+) - (DIN-) Input Voltage Swing Variation	$25 mV_{p-p} \leq (IN+) - (IN-) \leq 250 mV_{p-p}$			8.0	%
AGC Voltage	AGC open		2.3		V
AGC Pin Input Impedance			2.5		kΩ
Slow AGC Discharge Current	(DIN+) - (DIN-) = 0V		4.5		μA
Fast AGC Discharge Current	Starts at 0.9 μs after WG goes low, stops at 1.8 μs after WG goes low	0.12			mA
AGC Leakage Current	$\overline{HOLD} = \text{low}$	-0.2		+0.2	μA
Slow AGC Charge Current	(DIN+) - (DIN-) = 0.8 VDC, vary AGC until slow charge begins	-0.12	-0.18	-0.24	mA

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AGC AMPLIFIER (Continued)

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Fast AGC Charge Current	(DIN+) - (DIN-) = 0.8 VDC, V _{AGC} = 3.0V	-0.9	-1.3	-1.7	mA
Fast to Slow Attack Switchover Point	$\frac{[(DIN+) - (DIN-)]}{[(DIN+) - (DIN-)]_{FINAL}}$		125		%
Gain Decay Time (T _d)	(IN+) - (IN-) = 250 mVp-p to 125 mVp-p @ 2.5 MHz, (OUT+) - (OUT-) to 90% final value		12		μs
	(IN+) - (IN-) = 50 mVp-p to 25 mVp-p at 2.5 MHz (OUT+) - (OUT-) to 90% final value		60		μs
Gain Attack Time	WG = high to low (IN+) - (IN-) = 250 mVp-p @ 2.5 MHz, (OUT+) - (OUT-) to 110% final value		2		μs

WRITE MODE WG is high

PARAMETER	CONDITION	MIN	NOM	MAX	UNIT
Common Mode Input Impedance			250		Ω

HYSTERESIS COMPARATOR

Unless otherwise specified, recommended operating conditions apply. Input (DIN+) - (DIN-) is an AC coupled, 1.0 Vp-p, 2.5 MHz sine wave. 0.5 VDC is applied to the HYS pin. WG pin is low.

Input Signal Range				1.5	Vp-p
Differential Input Resistance	(DIN+) - (DIN-) = 100 mVp-p @ 2.5 MHz	8	10	14	kΩ
Differential Input Capacitance	(DIN+) - (DIN-) = 100 mVp-p @ 2.5 MHz			5.0	pF
Common Mode Input Impedance (Both Sides)		2	2.5	3.5	kΩ
Level Pin Output Voltage vs. (DIN+) - (DIN-)	0.6 Vp-p < (DIN+) - (DIN-) < 1.5 Vp-p, 10K between LEVEL and AGND		1		V/Vp-p
Level Pin Output Impedance	I _{LEVEL} = 0.2 mA		250		Ω
Level pin Maximum Output Current		1.5			mA
Hysteresis Voltage at DIN± vs. HYS Pin Voltage	0.3 V < HYS < 1.0V		0.36		V/V

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HYSTERESIS COMPARATOR (Continued)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
HYS Pin Current	0.5 V < HYS < 1.5V	0.0		-10	μA
Comparator Offset Voltage	HYS pin at AGND ≤ 1.5 kΩ across DIN±			5.0	mV
DOUT Pin Output Low Voltage	5 kΩ from DOUT to GND		VPA2 -2		V
DOUT Pin Output High Voltage	5 kΩ from DOUT to GND		VPA2 -1.6		V

ACTIVE DIFFERENTIATOR

Unless otherwise specified, recommended operating conditions apply. Input (CIN+) - (CIN-) is an AC-coupled, 1.0 Vp-p, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-.

Input Signal Range				1.5	Vp-p
Differential Input Resistance	(CIN+) - (CIN-) = 100 mVp-p @ 2.5 MHz	8	10	14	kΩ
Differential Input Capacitance	(CIN+) - (CIN-) = 100 mVp-p @ 2.5 MHz			5.0	pF
Common Mode Input Impedance	Both sides	2.0	2.5	3.5	kΩ
Voltage Gain From CIN± to DIF±	(DIF+ to DIF-) = 2 kΩ		1		V/V
DIF+ to DIF- Pin Current	Differentiator impedance must be set so as to not clip the signal for this current level	±0.7			mA
Comparator Offset Voltage	DIF+, DIF- are AC-coupled			5.0	mV
COUT Pin Output Low Voltage	5 kΩ from COUT to GND		VPA2 -2		V
COUT Pin Output High Voltage	5 kΩ from COUT to GND		VPA2 -1.6		V
COUT Pin Output Pulse Width			30		ns

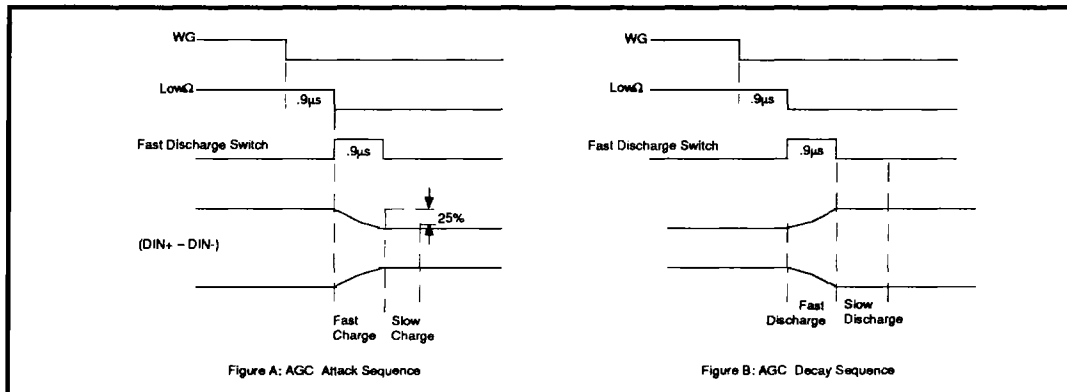


FIGURE 7: AGC Timing Diagram

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QUALIFIER TIMING (See Figure 8)

Unless otherwise specified, recommended operating conditions apply. Inputs (CIN+) - (CIN-) and (DIN+) - (DIN-) are in-place as a coupled, 1.0 Vp-p, 2.5 MHz sine wave. 100Ω in series with 65 pF are tied from DIF+ to DIF-. 0.5V is applied to the HYS pin. COUT, DOUT and RD has a 5 kΩ pull-down resistor (for test purposes only.) WG pin is low.

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
Td1 D Flip-Flop Set Up Time	Minimum allowable time delay from (DIN+) - (DIN-) exceeding hysteresis point to (DIF+) - (DIF-) hitting a peak value.	0			ns
Td3 Propagation Delay			15		ns
Td3-Td4 Pulse Pairing				1.0	ns

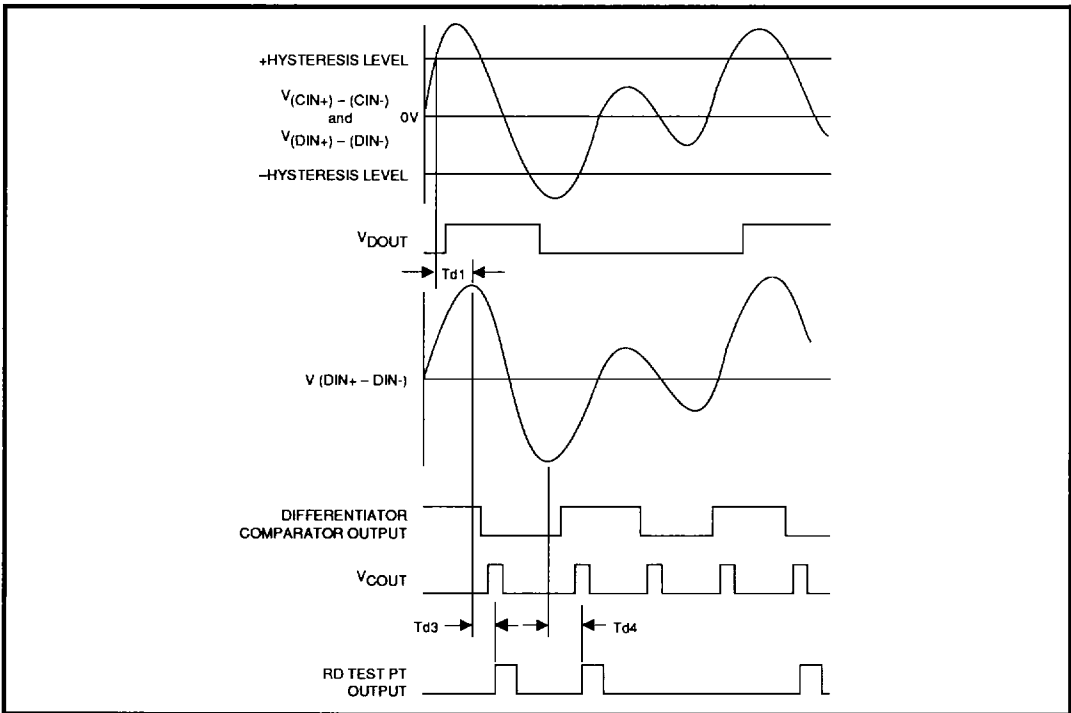


FIGURE 8: Read Mode Digital Section Timing Diagram

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SERVO SECTION (Unless otherwise specified, recommended operating conditions apply.)

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
VREF Voltage Range Output			2.0		V
BURSTA/B Pin Output Voltage vs (DIN+) - (DIN-)	$\overline{\text{LATCHA/B}} = \text{Low}$ $\frac{V_{\text{BURSTAB}} - V_{\text{REF}}}{(\text{DIN+}) - (\text{DIN-})}$		1.0		V/Vp-p
BURSTA/B Output Offset Voltage, $V_{\text{BURST}} - V_{\text{REF}}$	$\overline{\text{LATCHA/B}} = \text{Low}$, (DIN+) = (DIN-)	-50		+50	mV
BURSTA - BURSTB Output Offset Match	$\overline{\text{LATCHA/B}} = \text{low}$ (DIN+) = (DIN-)	-10		+10	mV
Output Resistance, BURSTA/B, PES				20	Ω
PES Pin Output Offset Voltage	$V_{\text{BURSTA}} - V_{\text{BURSTB}} + V_{\text{REF}}$ (DIN+) = (DIN-), $\overline{\text{LATCHA/B}} = \text{Low}$	-10		+10	mV
HOLDA/B Discharge Current	$\overline{\text{RST}} = \text{low}$,		1.5		mA
HOLDA/B Leakage Current	$\overline{\text{RST}} = \text{high}$, $\overline{\text{LATCHA/B}} = \text{high}$	-0.5		+0.5	μA
Load Resistance, BURSTA/B, PES	Resistors to VREF	10.0	20.0		k Ω
Load Capacitance, BURSTA/B, PES				20	pF
$\overline{\text{LATCHA/B}}$ pin set up time	TDS1, Figure 14	150			ns
$\overline{\text{LATCHA/B}}$ pin Hold Time	TDS2, Figure 14	150			ns
Channel A/B Discharge Current Turn On time	$\overline{\text{RST}}$ high \rightarrow low			150	ns
Channel A/B Discharge Current Turn Off time	$\overline{\text{RST}}$ low \rightarrow high			150	ns

SYNCHRONIZER SECTION

WRITE MODE (See Figure 9)

PARAMETER	CONDITIONS	MIN	MAX	UNIT
TWD, Write Data Pulse Width	$\text{CL} \leq 15 \text{ pF}$	(TORC/2)-12 -1.65 TPCO -TPC -12	(TORC/2)+12 -1.65 TPCO -TPC +12	ns
TFWD, Write Data Fall Time	2.0V to 0.8V, $\text{CL} \leq 15 \text{ pF}$		8	ns
TSWD, Write Data Input Setup Time	Either edge of WDI to either edge of RRC	15		ns

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WRITE MODE (continued)

PARAMETER	CONDITIONS	MIN	MAX	UNIT
THWD, Write Data Input Hold Time	Either edge of RRC to either edge of WDI	3		ns
TSP, Early*/Late* Input Setup Time	Falling edge of Early*/Late* to either edge of RRC	15		ns
THP, Early*/Late* Input Hold Time	Rising edge of Early*/Late* to either edge of RRC	10		ns
TPC, Precompensation Time Shift Magnitude Accuracy	TPCO = 0.155 Rp Cp Rp = 1K to 2K	0.8TPC0	1.2TPC0	ns

READ MODE

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TRRC, Read Clock Rise Time	0.8V to 2.0V, CL ≤ 15 pF			8	ns
TFRC, Read Clock Fall Time	2.0V to 0.8V, CL ≤ 15 pF			5	ns
TSRD, Read Data Pulse Width		(TORC/2)-12		(TORC/2)+12	ns
TRSRD, Read Data Rise Time	0.8V to 2.0V, CL ≤ 15 pF			10	ns
TFSRD, Read Data Fall Time	2.0V to 0.8V, CL ≤ 15 pF			8	ns
TPSRD, SRD Output Setup/HoldTime		-15		15	ns
1/4 Cell + Retriggerable One-Shot Delay*	TD = 5.0 (RR + 1.2) + 0.154 Rd (Cd + Cs)** ns RR in kΩ, Rd in kΩ, Cd in pF Cd = 68 pF to 100 pF	0.89TD		1.11TD	ns
1/4 Cell + Retriggerable One-Shot Detect Stability	4.5V < VPA2 < 5.5V	-4		+4	%

*Excludes External Capacitor and Resistor Tolerances. ** Cs = Stray Capacitance

WINDOW SYMMETRY CONTROL CHARACTERISTICS

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TWSS $\overline{WS0}$, $\overline{WS1}$, WSD Set Up Time		50			ns
TWSH $\overline{WS0}$, $\overline{WS1}$, WSD Hold Time		0			ns

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DATA SYNCHRONIZATION

PARAMETER	CONDITIONS	MIN	NOM	MAX	UNIT
TVCO VCO Center Frequency Period	VCO IN = 2.7V TO = TBD VPA2 = 5.0V	0.8TO		1.2TO	sec
VCO Frequency Dynamic Range	$1.0V \leq VCO\ IN \leq VPA2-0.6V$ VPA2 = 5.0V	± 27		± 40	%
KVCO VCO Control Gain	$\omega_0 = 2\pi / TO$ $1.0V \leq VCO\ IN \leq VPA2-0.6V$	0.14 ω_0		0.20 ω_0	rad/s V
KD Phase Detector Gain	$KD = 0.62 / (RR+500)$ VPA2 = 5.0V, Input = 3T Sync Field	0.83 KD		1.17 KD	A/rad
* KVCO x KD Product Accuracy		-28		+28	%
* VCO Phase Restart Error			6		ns
Decode Window Centering Accuracy				$\pm (0.01\ TORC + 2)$	ns
Decode Window		(TORC/2) - 2			ns
TS1 Decode Window Time Shift Magnitude	TS1 = 0.015 TORC WSO = 0; WSI = 1	0.8 TS1 -0.5		1.2 TS1 +0.5	ns
TS2 Decode Window Time Shift Magnitude	TS2 = 0.06 TORC WSO = 1; WSI = 0	0.8 TS2		1.2 TS2	ns
TS3 Decode Window Time Shift Magnitude	TS3 = 0.075 TORC WSO = 0; WSI = 0	0.8 TS3		1.2 TS3	ns
TSA Decode Window Time Shift Magnitude	$TSA = 0.015\ TORC - (-\frac{TORC}{2})$	0.65 TSA		1.35 TSA	ns

* Not directly testable; design characteristics

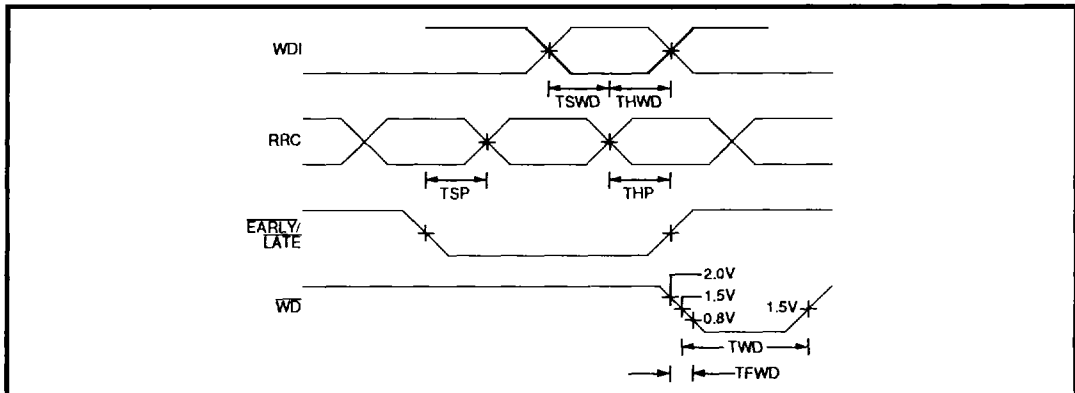


FIGURE 9: Write Mode Timing

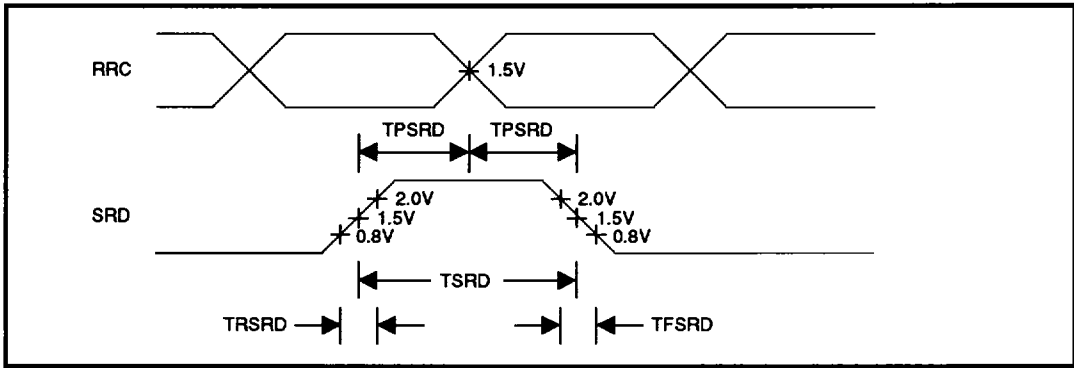


FIGURE 10: Read Mode Timing

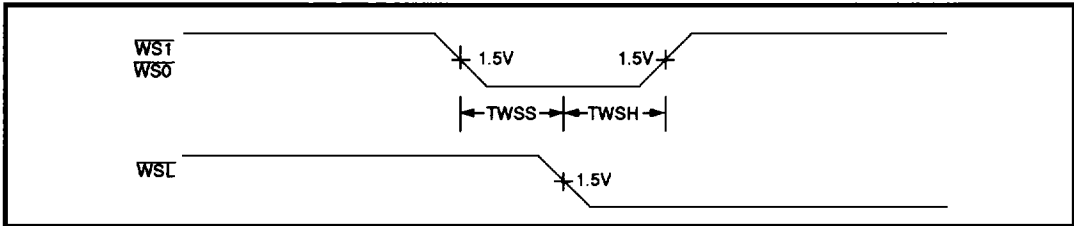


FIGURE 11: Window Symmetry Control Timing

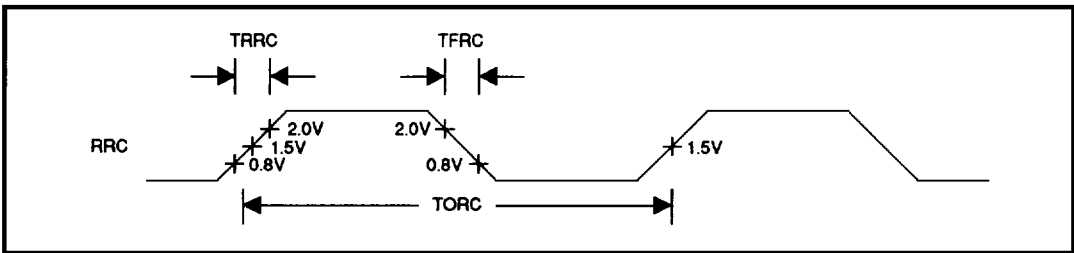


FIGURE 12: RRC Timing

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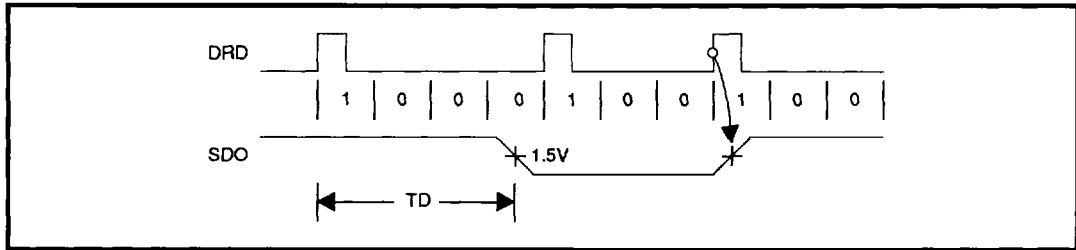


FIGURE 13: SDO Timing

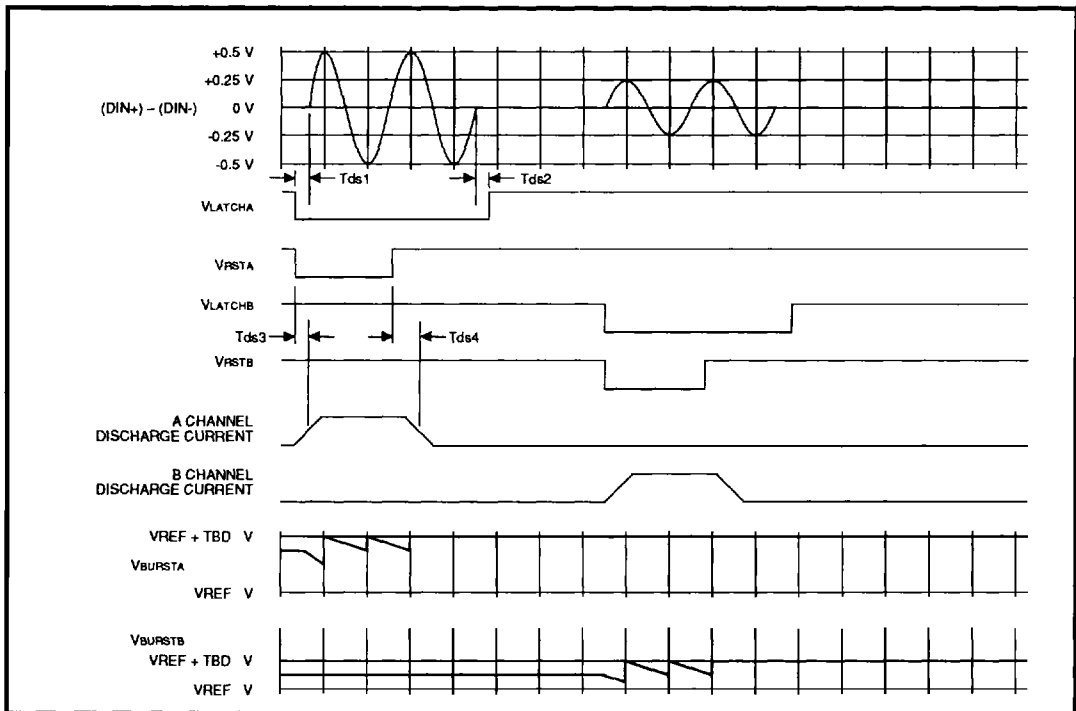


FIGURE 14: Servo Read Mode Timing

APPLICATIONS INFORMATION

The SSI 32P548 PLL uses a new architecture which incorporates an accurate quarter cell delay circuit. The standard architecture of a data synchronizer PLL is shown in Figure 17A. In read mode, the rising edge of the quarter cell delay enables the phase detector, and the falling edge is locked to the VCO. Ideally, the quarter cell delay enables the phase detector one half of an encoded bit cell time before the phase comparison takes place. A data bit could then shift early or late by one half of an encoded bit cell time before a phase detector output error would occur. If the quarter cell delay is not exactly one half of an encoded bit cell time, a phase detector error will occur when the read data shifts by an amount that is smaller than one half of an encoded bit cell time when shifting in one direction and an amount larger than one half of an encoded bit cell time in the other direction. In addition, when an error occurs, the resulting charge pump output goes from maximum output one way to maximum output the other way. This can cause loss of lock to occur. The timing is shown in Figure 18.

The 32P548 achieves an accurate quarter cell delay time by using the VCO control voltage to compensate the quarter cell delay one-shot circuit for process, temperature and power supply induced timing variations. The modified architecture of the 32P548 data synchronizer is shown in Figure 19B. Because the quarter cell delay timing is adjusted by the VCO control voltage, there is an effect on the PLL transfer function due to the new quarter cell delay circuit.

The quarter cell delay circuit produces a time delay output in response to a voltage input. In order to include this function in a phase-locked loop, the time delay function must be converted into a phase function. This is straightforward, since a time delay is equivalent to a phase angle. The equivalent phase representation of the quarter cell delay is derived below.

For the VCO:
$$K_o = \frac{d\omega_o}{dV} \quad (1a)$$

$$\frac{dT_o}{dV} = \frac{d}{dV} \left(\frac{1}{f_o} \right) = -\frac{1}{f_o^2} \frac{df_o}{dV} = -T_o^2 \frac{df_o}{dV} = -\frac{T_o^2}{2\pi} \frac{d\omega_o}{dV} \quad (1b)$$

where:

- K_o = VCO gain
- ω_o = VCO center frequency (rad/s)
- f_o = VCO center frequency (Hz)
- T_o = VCO center frequency (sec)

For the quarter cell delay,

$$K_T = \frac{dq_o}{dV} = \frac{2\pi}{T_o} a \frac{dT_o}{dV} = -\alpha T_o \frac{d\omega_o}{dV} = -\alpha T_o K_o$$

where:

- θ_o = Phase due to quarter cell delay circuit
- T_o = VCO center frequency period
- T_q = Quarter cell delay time
- $\alpha = T_q/T_o = 0.5$ for the 32P548

The gain of the quarter cell delay block is constant in the 32P548, regardless of the values of other components.

For the 32P548, the nominal value of K_T is 0.17π .

PLL TRANSFER FUNCTION

There are two modes of operation of the PLL, and two transfer functions. In write and idle modes, the PLL is locked to the reference oscillator, and the quarter cell delay does not enter into the transfer function. In read mode, the PLL is locked to read data, and the quarter cell delay is included in the transfer function. In addition, the effective loop gain of the PLL increases in idle mode due to the phase detector. This will be explained later in more detail.

The transfer functions for read and idle modes are given in (3) and (4), respectively.

$$\frac{\theta_o(s)}{\theta_r(s)} = \frac{\frac{nK_o K_d F(s)}{S}}{1 + nK_T K_d F(s) + \frac{nK_o K_d F(s)}{S}} \quad (3)$$

$$\frac{\theta_o(s)}{\theta_r(s)} = \frac{\frac{nK_o K_d F(s)}{S}}{1 + \frac{nK_o K_d F(s)}{S}} \quad (4)$$

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where:

K_T = Quarter cell delay one-shot gain

K_O = VCO gain

K_d = Phase detector gain

$F(s)$ = Loop filter transfer function

n = Ratio of input freq. to reference freq.

In (3) the K term in the denominator is a result of the quarter cell delay. Substituting $K_T = \alpha K_O T_O$ into (3),

$$\frac{\theta_o(s)}{\theta_r(s)} = \frac{\frac{nK_O K_d F(s)}{s}}{1 + (1 - \alpha T_O) \frac{nK_O K_d F(s)}{s}}$$

The additional $-\alpha T_O$ term in the denominator due to the quarter cell delay introduces positive feedback. However, the gain of the positive feedback is always less than one, so there is no instability. The additional term is not always negligible, and must be taken into account in the loop analysis and design.

Two loop filter configurations, shown in Figure 15, will be considered. Both filters result in a second order type 2 loop transfer function, with only minor differences in the loop equation.

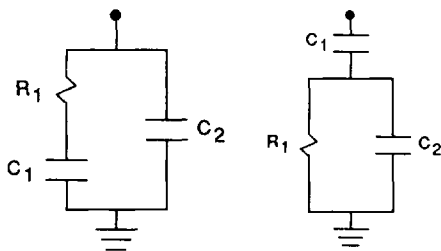


FIGURE 15: Loop Filter

The transfer function of the loop filter for a charge-pump PLL is the transimpedance, $V_o/I_i(s)$, where $V_o(s)$ is the output voltage, and $I_i(s)$ is the input current. The transfer functions of (a) and (b) are given by:

$$F_a(s) = \frac{sR_1C_1 + 1}{s(C_1 + C_2) \left(sR_1 \frac{C_1C_2}{C_1 + C_2} + 1 \right)} \quad (6)$$

$$F_b(s) = \frac{sR_1(C_1 + C_2) + 1}{sC(sR_1C_2 + 1)} \quad (7)$$

For loop filter (a), C is normally chosen to be much smaller than C_1 so that it does not affect the loop transfer function significantly. Assuming the $C \gg C_1$ and $sRC \ll 1$ at the frequencies of interest, (6) reduces to:

$$F_a(s) = \frac{sR_1C_1 + 1}{sC_1} \quad (8)$$

For loop filter (b), C is normally chosen to be much smaller than C_1 , so that it does not affect the loop transfer function significantly. Assuming the $C \gg C_1$ and that $sRC \ll 1$ at the frequencies of interest, (7) reduces to:

$$F_b(s) = \frac{sR_1C_1 + 1}{sC_1} \quad (9)$$

Equations (8) and (9) are the same, and either loop filter may be used. Substituting (8) into (3) gives:

$$\frac{\theta_o(s)}{\theta_r(s)} = \frac{\frac{nK_O K_d}{C_1(1 - \alpha T_O nK_O K_d R_1)} (sR_1C_1 + 1)}{s^2 + s \frac{nK_O K_d}{1 - \alpha T_O nK_O K_d R_1} \left(R_1 - \frac{\alpha T_O}{C_1} \right) + \frac{nK_O K_d}{C_1(1 - \alpha T_O nK_O K_d R_1)}} \quad (10)$$

This is in the form of a standard second order transfer function. The denominator has the form:

$$D(s) = s^2 + 2\zeta\omega_n s + \omega_n^2 \quad (11)$$

where: ζ = damping factor
 ω_n = natural frequency

The damping factor and natural frequency of (10) can be extracted:

$$\omega_n = \sqrt{\frac{nK_O K_d}{C_1(1 - \alpha T_O nK_O K_d R_1)}} \quad (12)$$

$$\zeta = \frac{R_1 - \frac{\alpha T_O}{C_1}}{2} \sqrt{\frac{nK_O K_d C_1}{1 - \alpha T_O nK_O K_d R_1}} \quad (13)$$

Substituting (8) into (4) gives the transfer function for idle mode:

$$\frac{\theta_o(s)}{\theta_r(s)} = \frac{\frac{nK_O K_d}{C_1} (sR_1C_1 + 1)}{s^2 + s(nK_O K_d R_1) + \frac{nK_O K_d}{C_1}} \quad (14)$$

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Again, this is in the form of a second order transfer function. The damping factor and natural frequency are found to be:

$$\omega_n = \sqrt{\frac{nK_oK_d}{C_1}} \quad (15)$$

$$\zeta = \frac{R_1}{2} \sqrt{nK_oK_dC_1} \quad (16)$$

To design the loop for proper read mode operation using (12) and (13), R, and C, must be found in terms of the damping factor and natural frequency.

To do this, first find ζ/ω_n , then solve for R_1C_1 .

$$R_1C_1 = \frac{2\zeta}{\omega_n} + \alpha T_o \quad (17)$$

Substitute this value for R_1C_1 into the equation for ω_n and solve for C_1 .

$$C_1 = \frac{nK_oK_d}{\omega_n^2} + \alpha T_o nK_oK_d \left(\frac{2\zeta}{\omega_n} + \alpha T_o \right) \quad (18)$$

Now that C_1 is known, R_1 can be found by dividing (17) through by C_1 .

$$R_1 = \left(\frac{2\zeta}{\omega_n} + \alpha T_o \right) \frac{1}{C_1} \quad (19)$$

EXAMPLE 1

Assume that the data rate is 10 Mbit/s, a 3T preamble pattern is used, and that $\omega_n = 10^6$ and $\zeta = 0.707$ are desired.

For the SSI 32P548:

$$\begin{aligned} R_n &= 50/DR - 1.7 \text{ k}\Omega \\ K_o &= 0.17\omega_o = 21.4 \cdot 10^6 \\ K_d &= 0.62/(R_n+500) = 160 \cdot 10^6 \\ K_r &= 0.17\pi = 0.534 \end{aligned}$$

Due to the 3T preamble pattern, the input frequency is one third the VCO frequency, so $n = 1/3$.

$$\begin{aligned} \omega_o &= 2\pi(2 \cdot 10^7), \alpha = 0.5, \text{ and } T_o = 1/(20 \cdot 10^6) = 50 \text{ ns} \\ C_1 &= 1160 \text{ pF} + 41.9 \text{ pF} = 1.21 \text{ nF} \\ R_1 &= 1.20 \text{ k}\Omega \end{aligned}$$

The resulting loop filter is shown in Figure 16.

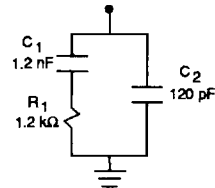


FIGURE 16

The value of $C_2 = C_1/10$ is chosen to damp out transients on the FILT pin and meet the requirement $C_2 \ll C_1$.

When the loop locks to the reference oscillator in idle mode, the loop transfer function is given by (14), and ω_n and ζ are given by (15) and (16). R_1 and C_1 from Example 1 can be substituted into these equations to find the resulting natural frequency and damping factor in idle mode.

EXAMPLE 2

When locking onto the reference oscillator, the input frequency is the same as the VCO frequency, so $n = 1$. Using the values of R_1 and C_1 found in Example 1, the values of ω_n and ζ when locking to the reference oscillator are found to be:

$$\begin{aligned} \omega_n &= 1.7 \cdot 10^6 \text{ rad/s} \\ \zeta &= 1.23 \end{aligned}$$

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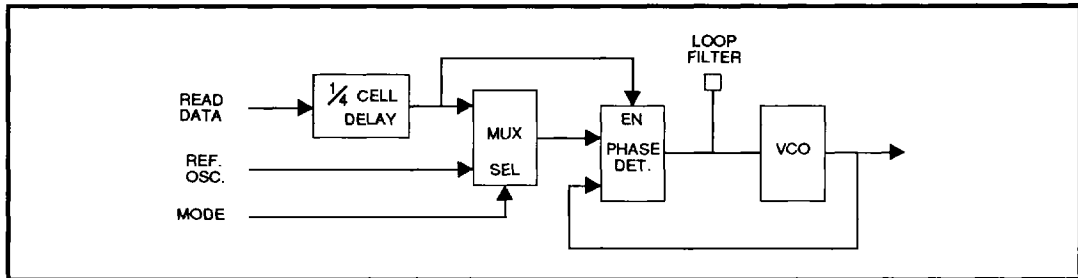


FIGURE 17A: Standard Configuration of a Data Synchronizer Phase-Locked Loop

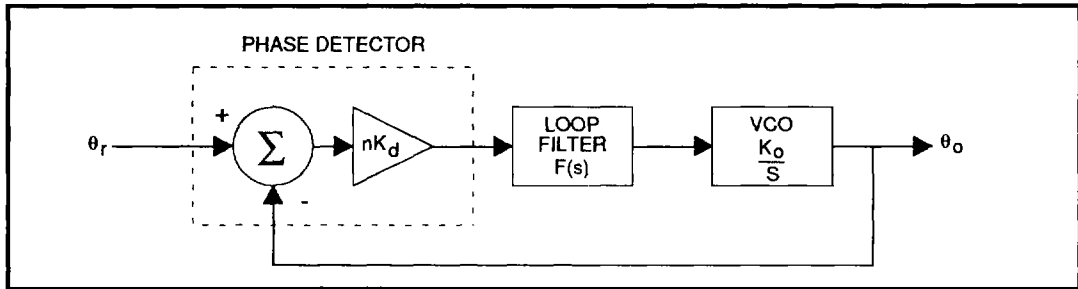


FIGURE 17B: Phase-Lock Loop System Representation

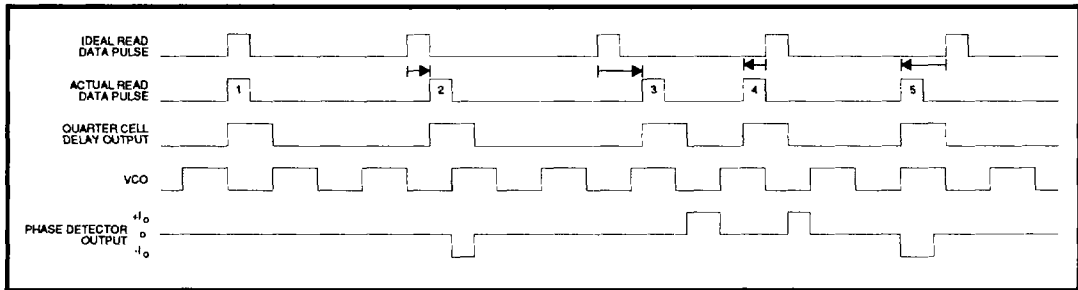


FIGURE 18A: Phase Detector Timing with Ideal Quarter Cell Delay. For an ideal pulse (1), there is no phase detector output. When a pulse is shifted late (2) or early (4) by less than the quarter cell delay time, the phase detector output is negative or positive, respectively. When the read data is shifted late (3) or early (5) by more than the quarter cell delay time, a phase detector output polarity error occurs. In this case, the output polarity becomes positive for a late shifted pulse and negative for an early shifted pulse.

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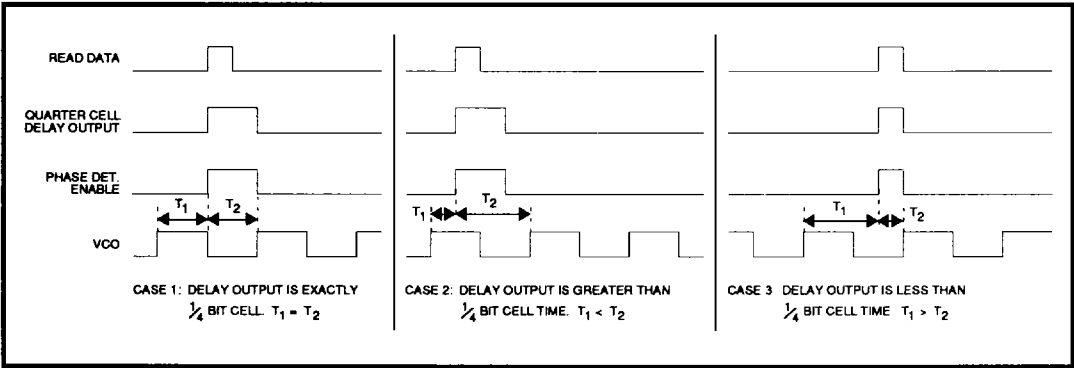


FIGURE 18B: Timing of Phase Detector Enable Logic. The read data input pulse can shift to the left by T1 and to the right by T2 before an error occurs in the phase detector output polarity. If the quarter cell delay output is not exactly 1/4 bit cell wide, then $T_1 \neq T_2$, as shown in cases 2 and 3.

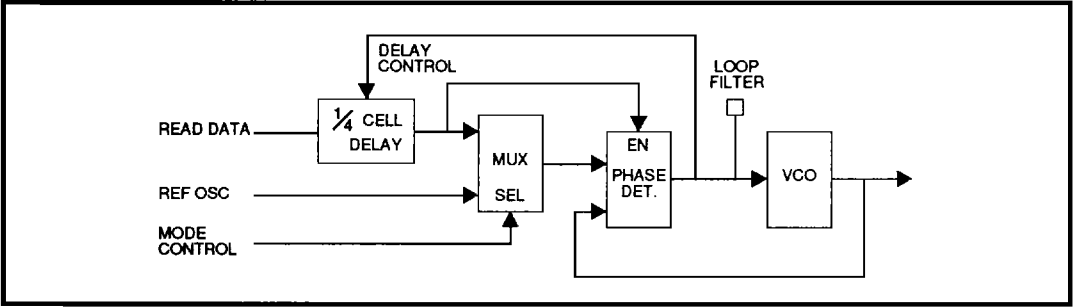


FIGURE 19A: Modified Data Synchronizer Phase-Locked-Loop with Quarter Cell Delay Control

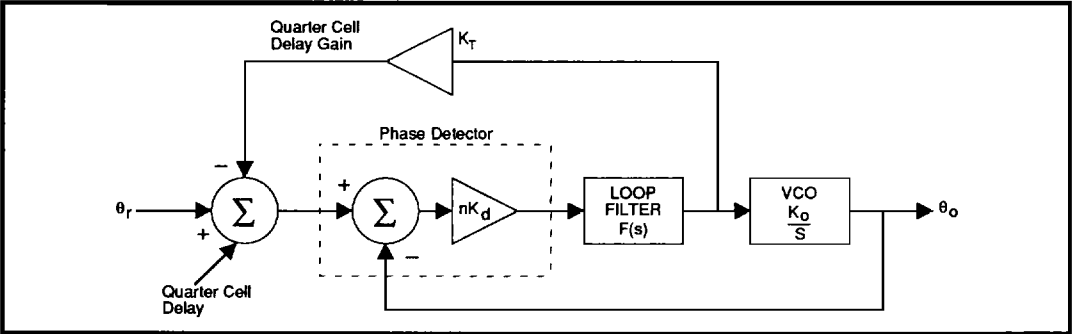


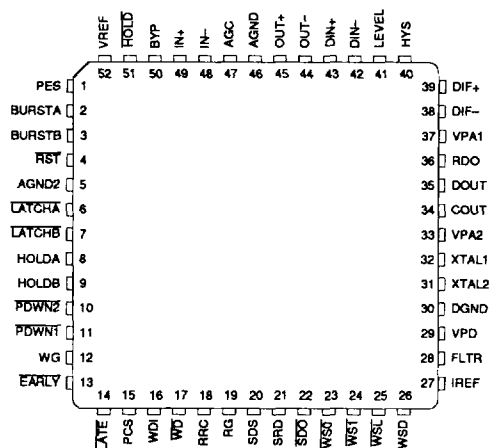
FIGURE 19B: Modified Data Synchronizer System Representation

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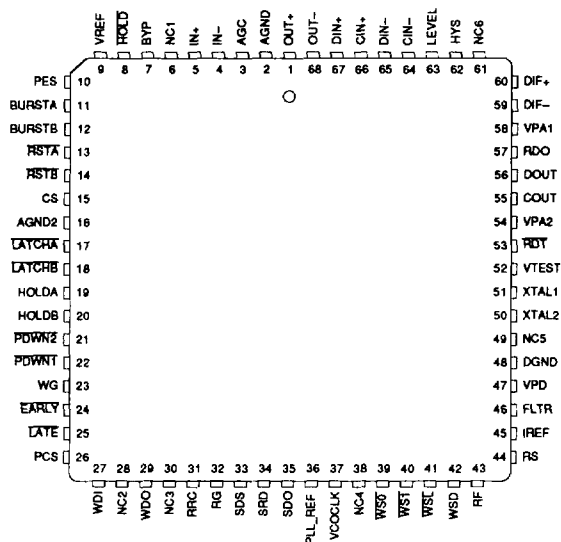
Pulse Detector & Data Synchronizer

PACKAGE PIN DESIGNATIONS

(Top View)



52-Pin QFP



68-Pin PLCC

Advance Information: Indicates a product still in the design cycle, and any specifications are based on design goals only.

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