Acapella Optical Modem IC ACS103

3 Channel, Synchronous or Asynchronous Single Fiber Modem

Main Features:

* Enables three full-duplex serial transmission channels through a single fiber optic cable, providing a virtual six fiber path.
* Link lengths up to 5 km.
* Uses a single Ping Pong LED (PPLED) to both transmit and receive data.
* Supports 7 synchronous data rates up to 64 kbps or asynchronous data rates from DC to 19.2/ 9.6 kbps.
* Supports three additional low frequency asynchronous channels or RS-232 handshake signals: RTS, CTS, DTR and DSR.
* BER 10^{-9}.
* Digital mode, allowing the user to add an external amplifier. Also enables the ACS103 be used in non-fiber applications e.g. IR/RF.
* ACS101 emulation mode giving 100 % compatibility with the ACS101.

General Description:

The ACS103 is a complete synchronous optical-modem controller/driver IC, supporting various user-programmable, full-duplex data-rates to 256 kbps over a single fiber. Alternatively, up to 3 channels of 64 kbps each can be carried. In 'Standard' mode, the fiber may be up to 2.5 km long, or up to 5 km in 'Double' mode.

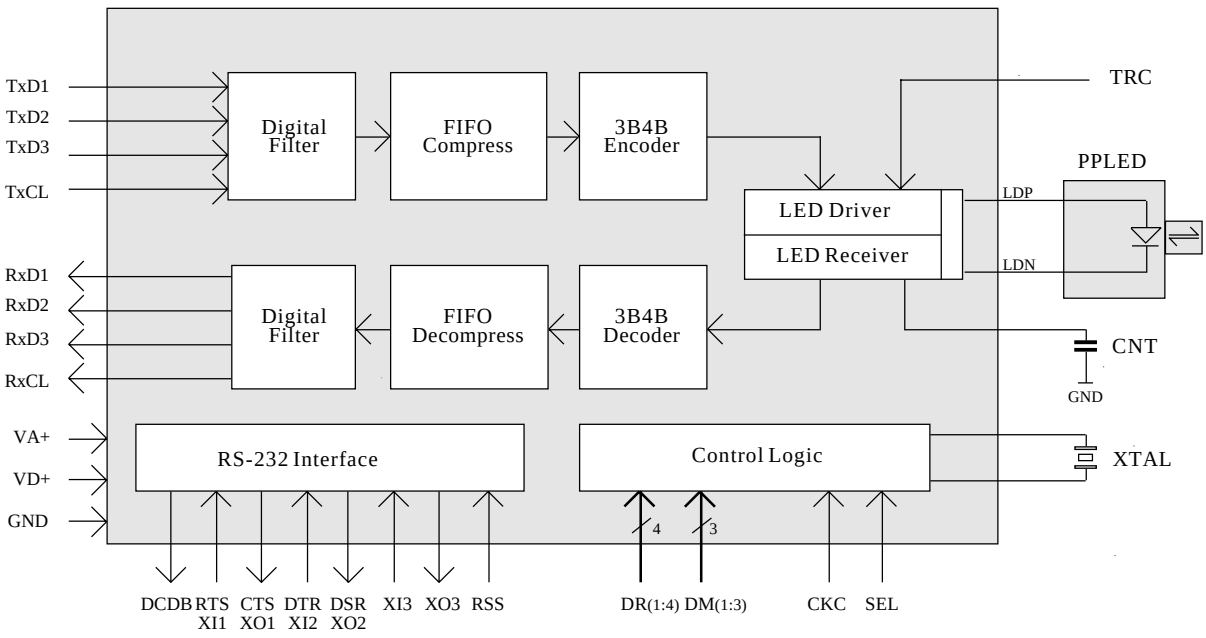
Communicating optical-modems automatically maintain synchronisation with each other such that the receive phase of one modem is lined-up with the transmit phase of the other, compensating for the propagation delay presented by the link. Link lengths from zero to maximum distance are catered for automatically.

The ACS103 incorporates ACS101 functionality, with additional logic to support 3 channels.

Inter-IC Encoding Technique

The 3B4B encoding method is used for communication between ACS103s, thus ensuring that there is no DC component in the signal. The encoding and decoding is transparent to the user.

Block diagram of ACS103



ACS101 Emulation mode using "SEL" input

The "SEL" input pin is normally held Low in order to configure the device in ACS103 mode. If the "SEL" input pin is allowed to pull High via an internal resistor the device will be configured in ACS101 emulation mode. In ACS101 emulation mode the device is fully compatible with the ACS101. The TxD2, TxD3 and XI3 inputs are internally disabled with the RxD2, RxD3 and XO3 outputs forced into the high impedance state. A full-duplex path then exists between TxD1 and RxD1.

Transmitter and Receiver Functions

The TxD input data of the transmitting modem is compressed, filtered, and 3B4B encoded. In the receiving modem, 3B4B encoding ensures easy extraction of the bit-clock. The received data is filtered, decoded, then stored in an output memory. The memory provides time expansion, de-jittering and frequency compensation. The data is filtered again to improve BER then directed to the RxD output pin. Signals TxD and RxD in this specification refer to the set of signals TxD1/2/3 and RxD1/2/3 respectively.

Transmit Current

The transmit current to the LED can be defined by the Transmit Current pin (TRC). The current is set to the maximum value (~100 mA) when TRC is unconnected. The current is set to the minimum value (~10 mA) when TRC is connected directly to ground. To obtain current values between minimum and maximum, TRC is connected to ground through a resistor. The resistor value R is given by:

$$\text{LED current drive (mA)} = \frac{100 * (110+R)}{(1100 + R)}$$

Data-rate Selection

ACS103 mode SEL = 0

DR4	DR3	DR2	DR1	Data-rate (kbps)	Distance
0	0	0	0	n/a	
0	0	0	1	9.6	Double
0	0	1	0	19.2	Double
0	0	1	1	38.4	Double
0	1	0	0	n/a	
0	1	0	1	n/a	
0	1	1	0	DC - 4.8	Double
0	1	1	1	n/a	
1	0	0	0	2.4	Standard
1	0	0	1	9.6	Standard
1	0	1	0	19.2	Standard
1	0	1	1	38.4	Standard
1	1	0	0	48.0	Standard
1	1	0	1	56.0	Standard
1	1	1	0	DC - 9.6	Standard
1	1	1	1	64.0	Standard

n/a = not available

The data rates given in the previous table apply to TxD1, TxD2 and TxD3.

ACS101 mode SEL = 1

DR4	DR3	DR2	DR1	Data-rate (kbps)	Distance
0	0	0	0	256.0	Standard
0	0	0	1	9.6	Double
0	0	1	0	19.2	Double
0	0	1	1	38.4	Double
0	1	0	0	48.0	Double
0	1	0	1	192.0	Standard
0	1	1	0	DC - 19.2	Double
0	1	1	1	64.0	Double
1	0	0	0	2.4	Standard
1	0	0	1	9.6	Standard
1	0	1	0	19.2	Standard
1	0	1	1	38.4	Standard
1	1	0	0	48.0	Standard
1	1	0	1	56.0	Standard
1	1	1	0	DC - 38.4	Standard
1	1	1	1	64.0	Standard

The ACS101 mode is a single channel mode configuration - the data rates given in the previous table apply to TxD1 only.

'Standard' mode of operation is up to 2.5 km and 'Double' mode is up to 5 km. The two asynchronous modes are selected when DR3 = 1, DR2 = 1, DR1= 0. The above data-rates are obtained when used in conjunction with a crystal of 9.216 MHz. Non-standard data-rates may be generated by using the appropriate crystal frequency. For example, to generate 160 kbps data-rate in ACS101 mode, use a crystal frequency of: (160/192) * 9.216 MHz, i.e. 7.68 MHz. Other "non-standard" data-rates may be generated in the same way as long as the 5 - 10 MHz crystal range is observed.

For the data-rates 9.6, 19.2, and 38.4 kbps in ACS103 mode (9.6, 19.2, 38.4, 48 and 64 kbps in ACS101 mode), the data-rate selection pins DR3-DR1 are common to 'Standard' and 'Double' modes of operation with DR4 selecting the mode.

Modem Control Signals

RSS.

The RTS/XI1, CTS/XO1, DTR/XI2, DSR/XO2, XI3 and XO3 signals may be used in either of two modes, depending on the RSS setting:

RSS = Low; data transmission mode

RSS = High; modem handshake mode

RSS Low - Data Transmission Mode.

When configured in data transmission mode the inputs XI1, XI2 and XI3 are sampled continuously with the outputs appearing at XO1, XO2 and XO3 (respectively) of the far-end modem. The sample frequency for 'Standard' mode is: (crystal freq.)/1536,

or 6.0 kHz using the recommended crystal frequency - 9.216 MHz. The sample frequency for 'Double' mode is: (crystal freq)/3072, or 3 kHz using the recommended crystal of 9.216 MHz.

The output filters for XO1/2/3 require a minimum over-sampling of 6 on data presented to the XI1/2/3 inputs.

In ACS101 mode the XI3 input is internally disabled and the XO3 output is forced into the high impedance state.

RSS High - Modem Handshake Mode.

In modem handshake mode the control signals are used as conventional handshake signals between the DTE (terminal) and the DCE (modem):

DSR (Data Set Ready) DCE → DTE.

The DCE is powered up and asserts a Low (active level) on DSR. The DTE is informed that it is connected to a “live” DCE.

DTR (Data Terminal Ready) DTE → DCE.

The DTE is powered up and asserts a Low (active level) on DTR. The DCE is informed that it is connected to a “live” DTE. If DTR is set High, the DCE responds by taking DCDB High.

RTS (Request to Send) DTE → DCE.

The DTE recognises that synchronisation has been achieved (DCDB active) and asserts a Low (active level) on RTS. This constitutes a request by the DTE to send data to the far-end modem.

CTS (Clear to Send) DCE → DTE.

The DCE recognises the active RTS signal and responds by asserting a Low (active level) on CTS. If RTS is set High the DCE responds by bringing CTS High.

DCDB (Data Carrier Detect) DCE → DTE.

When synchronisation is achieved between DCEs the DCDB signal is set Low (active level). If synchronisation is lost the DCE sets DCDB and CTS High.

Crystal Clock

A crystal may be connected between the pins XLI and XLO. Alternatively, XLI may be driven directly by an external clock. The operational frequency range is 5 MHz to 10 MHz, though communicating devices must be driven at the same nominal frequency with a tolerance of 100 ppm. In synchronous mode the frequency should be 9.216 MHz, resulting in the standard range of synchronous communication frequencies selected by DR1-DR4.

For asynchronous operation, the choice of crystal clock frequency dictates the sample rate of the asynchronous data appearing at the input TxD, and consequently the jitter on the output RxD. The sample frequency is always 1/108 of the chosen clock frequency in 'Standard' mode and 1/216 in 'Double' mode. In ACS101 emulation mode the sample frequency is 1/36 of crystal clock frequency in 'Standard' mode and 1/72 of the crystal clock frequency in 'Double' mode.

Integrating Capacitor

The ACS103 requires the use of an integrating ceramic capacitor of value 22 nF - 33 nF between pins CNT and GND for a crystal oscillator frequency range of 5 - 10 MHz.

DCDB

The Data Carrier Detect (DCDB) signal goes Low when the modems are locked and ready for data transmission.

PORB

The PORB pin is a single-pin alternative to the reset combination DM3 = 0, DM2 = 0, DM1 = 1. If left unconnected the input pulls High to the operational state. Selecting reset using DM1-DM3 or holding PORB Low turns off the LED and most of the digital logic. The device has been designed to power-up correctly and operate without the aid of PORB.

Transmission Clock TxCL

The ACS103 gives a choice between internally and externally generated transmission clocks (see Figure 2. Timing diagrams for set-up and hold specifications).

When the CKC pin is held Low, TxCL is configured as an output producing a clock at the frequency defined by DR1-DR4. Data is clocked into the device on the rising edge of the internally supplied clock.

When the CKC pin is held High, TxCL is configured as an input, and will accept an externally produced transmission clock with a tolerance of up to 500 ppm with respect to the transmission rate determined by DR1-DR4. The ACS103 performance is at its best when external changes on input pins are synchronised with internal clocks. Therefore, superior performance is likely when using the internally generated data transmission clock. If however, an externally generated transmission clock is used, then TxCL and TxD are generally asynchronous to the ACS103 internal clocks, performance in this case will be enhanced by limiting the edge speed of the TxCL and TxD signals so that they are greater than 150 ns. The modem has been designed to cope with very slow edges on inputs, without fear of metastability problems.

Receive Clock RxCL

In synchronous mode data is valid on the rising edge of RxCL clock (see Figure 2. Timing diagrams). To ensure that the average receive frequency is the

same as the transmitted frequency RxCL is generated from a Digital Phase-Lock Loop (DPLL) system. The DPLL makes periodic corrections to the output RxCL clock to compensate for differences in the crystal values, and in the case of an externally supplied transmission clock (TxCL), compensation is also made for differences in frequency between this supplied data clock and the selected clock rate (DR1-DR4). The DPLL is adaptive and will minimise the frequency of correction and jitter when the crystal values and transmission clocks are tightly toleranced.

If the ACS103 receive FIFO empties (e.g. transmissions at far-end are halted) the RxCL clock stops, therefore rising edges of the RxCL clock always correspond to valid received data bits. This enables the system designer to use the ACS103 for the transmission of packets of data with blank periods between packets. The minimum quanta of data that can be sent over the link is three bits.

In asynchronous mode the RxCL clock is turned off.

Diagnostic/Operational Modes

The diagnostic/operational modes input pins DM1-DM3 may be changed asynchronously within a window of (crystal clock period) * 1536. The diagnostic mode signals are sampled 1536 * (crystal clock period) after a change is detected on any of the DM inputs. The sampled value is taken as the valid diagnostic mode.

Diagnostic Mode	Lock	DM3	DM2	DM1
Full-duplex	drift	0	0	0
Reset		0	0	1
Remote loop-back	active	0	1	0
Full-duplex	random	0	1	1
Local loop-back	drift	1	0	0
Full-duplex slave	active	1	0	1
Full-duplex	active	1	1	1

Local loopback and remote loop-back are only available in ACS101 emulation mode.

Full-duplex

In full-duplex configuration the RxCL clock of both devices tracks the average frequency of the TxCL clock of the opposing end of the link. The receiving Digital Phase-Lock Loop (DPLL) system makes periodic adjustments to the RxCL clock to ensure that the average frequency is exactly the same as the far-end TxCL clock. In this mode each TxCL is an independent master clock and each RxCL a slave clock.

Full-duplex slave

In slave mode the TxCL and the RxCL clock is derived from the TxCL clock of the opposing side of the link, such that the average frequency is exactly the same. It is therefore essential that only one modem is configured in slave mode at a time. The CKC pin is overridden so that TxCL is always configured as an output.

Local Loopback

Local loopback is only available in ACS101 emulation mode.

In local loopback mode data is looped back inside the near-end modem and is output at its own RxD output. The data is also sent to the far-end modem; synchronisation between the modems is maintained. In local loopback mode, data received from the far-end device is ignored, except to maintain lock. When local loopback is activated the DCDB signal assumes the logic High state. If concurrent requests occur for local and remote loopback, local loopback is selected.

When RSS = 0, RTS and DTR are looped back to CTS and DSR respectively.

Remote Loopback

Remote loopback is only available in ACS101 emulation mode.

In remote loopback mode the near-end modem sends a request to the far-end modem to loopback its received data, thus returning the data. The far-end modem also outputs the received data at its RxD. Both modems are exercised completely, as well as the LEDs and the fiber optic link. Once remote loopback is established, DCDB on the near-end (initiating) modem is Low, and DCDB on the far-end modem is set High. Any data appearing on the TxD input of the far-end modem is ignored.

When RSS = 0, RTS and DTR are looped back to CTS and DSR respectively.

Drift lock

Communicating modems attain a stable state where the "transmit window" of one modem coincides with the "receive window" of the other allowing for delay through the optical link. Adjustments to machine cycles are made automatically during operation to compensate for differences in crystal frequencies which cause loss of synchronisation.

Using drift lock, synchronisation described above depends on a difference in the crystal frequencies at each end of the link, the greater the difference the faster the locking. Therefore, if the difference between crystal frequencies is very small (a few ppm), automatic locking may take tens of seconds.

Active Lock Mode

Active lock mode may be used to accelerate synchronisation of a pair of communicating modems. This mode synchronises the modems with less than 250 ms delay, by adjusting the machine cycle of the modem. Active lock reduces the machine cycle of the device by 0.5 % ensuring rapid lock. After

synchronisation the machine cycle reverts automatically to normal.

Note that only one device can be configured in active lock at any one time, and thus the DM pins must not be permanently wired High on both devices in a production system. Active lock mode is usually invoked on power-up. One common way of temporarily invoking active lock is to adopt the standard RC time-constant method. This is achieved on the ACS103 by connecting DM1, DM2 and DM3 together, and attaching that node to an RC arrangement, i.e. with the capacitor to 5 V and the resistor to ground. This creates a 5 V → 0 V ramp on power-up. The RC time-constant should be Ca. 1 second.

Random Lock

This is a new mode of operation (over the ACS100), both ends of a link can be permanently configured in this mode (i.e. with hard-wired DM1-DM3 pins), which will achieve lock in typically 1 second, and worst case 5 seconds.

Like active lock, random lock will operate even when both ends of the link are driven by identical clock frequencies (0 ppm). Random lock mode is compatible with drift lock available on the ACS100.

Mixing Lock modes

It is possible to mix all combinations of locking modes once the modems are locked, however, prior to synchronisation two modems configured in active lock will not operate. Normally, random lock will be the preferred mode. The effect of mixing locking modes on locking speed is tabulated below:

Device A Mode	Device B Mode	Locking Speed
Drift	Drift	Drift
Drift	Active	Active
Drift	Random	Random
Active	Active	Not allowed
Active	Random	Random
Random	Random	Random

LIN (Lock Indicator)

LIN goes High when synchronisation or 'lock' is achieved. Lock is normally an invert of DCDB. But unlike DCDB is not affected by the status of RTS and DTR, or the selected diagnostic mode.

ERD (Error Detector)

This signal can be used to give an indication of the quality of the optical link. Even when a DC signal is applied to the TxD and TxCL inputs, the ACS103 transmits approximately 256 kbps over the link in each direction. This control data is used to maintain the timing and the relative positioning of transmit and receive windows. The transmit data and the control data is constantly monitored to make sure it is compatible with the 3B4B format. If an error is detected then ERD will go High and will remain High until ERD is initialised. ERD may be initialised by applying reset DM1-DM3 or PORB, or by removing the fiber-optic cable from one side of the link thereby forcing the device temporarily out of lock. ERD is only an indication and is not a substitute for BER tests.

LED Considerations

Since LEDs from different suppliers may emit different wavelengths, it is recommended that the LEDs in a communicating pair of modems are obtained from the same supplier. The emission spectrum of an LED is a function of temperature, so a temperature difference between the ends of a link reduces the responsivity of the receiving diode. This results in a reduction in the link budget. Information is given in the LED suppliers' data sheets. The following manufacturers have LEDs that have been successfully tested with the ACS103 and Acapella will be glad to assist with contact names and addresses on request.

Suppliers:

ABB-Hafo	(e.g. 1A-212-*connector*)
Acapella	(e.g. A-*connector*)
GCA	(e.g. 1A-212-*connector*)
Honeywell	(e.g. HFE4214-013, HFE4404-013)
Optek	(e.g. OPF372, OPF322)

Most suppliers support the standard range of fiber *connectors*, e.g. ST, SMA and FC.

Power Supply Decoupling

The ACS103 contains a highly sensitive amplifier, capable of responding to extremely low current levels. To exploit this sensitivity it is important to reduce external noise to a low level compared to the input signal from the LED. The modem should have an independent power trace to the point where power enters the board.

Figure 3. shows the recommended power supply decoupling. The LED should be sited very close to the LDN and LDP pins. A generous ground plane should be provided, especially around the sensitive LDN and LDP pins. The modem should be protected from EMI/RFI sources in the standard ways.

Link Budgets

The link budget is the difference between the power coupled to the fiber via the transmit LED and the power required to realise a current of 650 nA (minimum amplifier sensitivity) via the receive LED.The link budget is normally specified in dB or dBm, and represents the maximum attenuation allowed between communicating LEDs. The budget is utilised in terms of the cable length, cable connectors and splices. It usually includes an operating margin to allow for degradation in LED performance.

The power coupled to the cable is a function of the efficiency of the LED, the current applied to the LED and the diameter of the fiber optic cable. The larger the cable diameter the greater the power coupled. The conversion current produced by the receive diode is a function of the LED efficiency and the cable diameter. The conversion efficiency is measured in terms of its ability to convert the available power to current, known as the responsivity, given by (A/W). Some examples of link budgets are given in the Table 1., though note that significantly better "A" spec. LEDs available, e.g. from Acapella. “A” spec. LEDs can offer > 12 dB link budget on 50 µm fiber.

Maximum Link Length

The internal timing chain within the ACS103 limits the link length to 2.5 km ('Standard' mode) and 5 km ('Double' mode) with a crystal frequency of 9.216 MHz. However, the maximum link length as determined by the ACS103 timing chain is inversely proportional to the crystal frequency. Please contact Acapella if you wish to discuss longer links.

TxD inputs

There is a choice of pins for TxD1, pins 12 and 41. Only one input should be used. The other input will pull-up to VDD via an internal resistor. Pin 12 is the recommended choice since it is further away from the sensitive analogue pins. However, pin 41 is available for designers if required.

Digital Mode

The ACS103 may be used as a controller and data buffer which allows the device to be used with an external amplifier and receiver, e.g. for non-fiber applications. Check with Acapella for details.

Data delay and skew

The data delay in synchronous mode is typically 48 data-bit periods and worst case 100 data-bit periods. When configured in asynchronous mode the worst case data delay is 300 µs at 9.216 MHz and 550 µs at 5 MHz. The additional data transmission channels (XI1/2/3) are delayed by up to 1.2 ms in 'Standard' mode and up to 2.4 ms in 'Double' mode when used with a crystal frequency of 9.216 MHz. For other crystal values the delay changes inversely proportional to the frequency of operation.

The worst case data skews between the main data channels TxD1/RxD1, TxD2/RxD2 and TxD3/RxD3 across the link are as follows.

Synchronous : zero data bits.
Asynchronous : 216 * (crystal clock period).

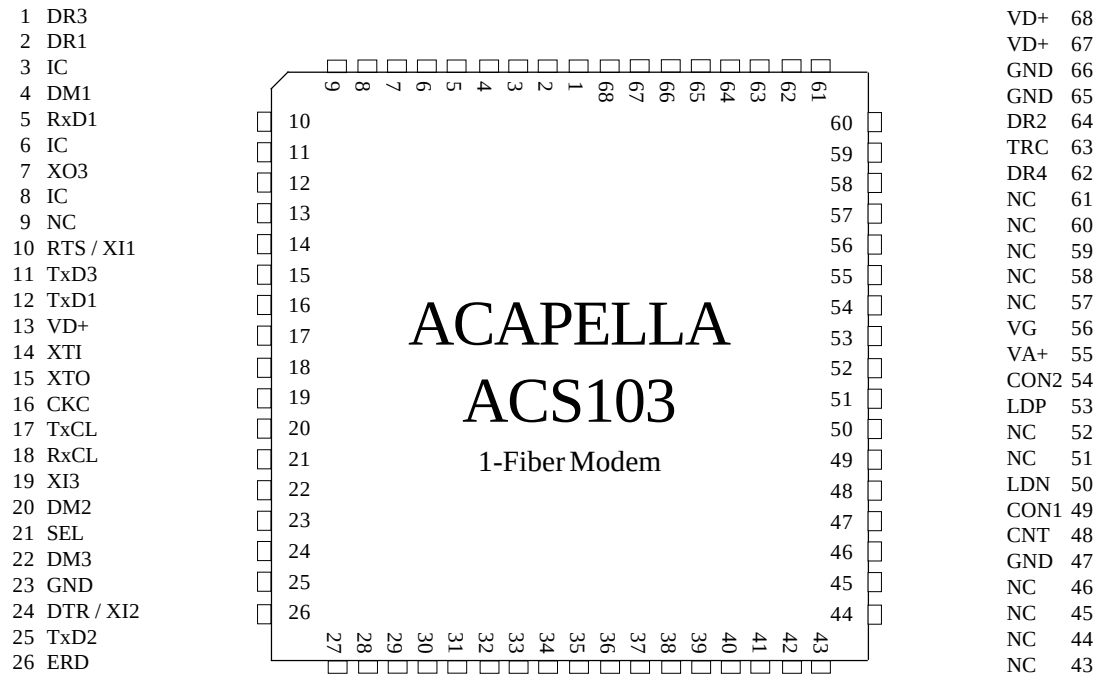
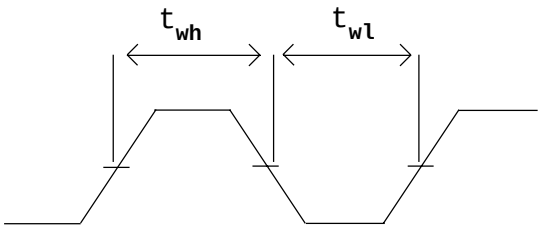
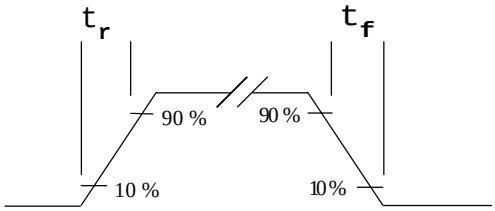


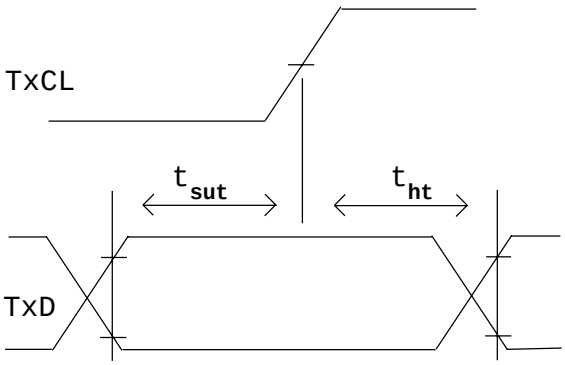
Figure 1. Top view of 68 PLCC package
NC = Not Connected IC = Internally Connected



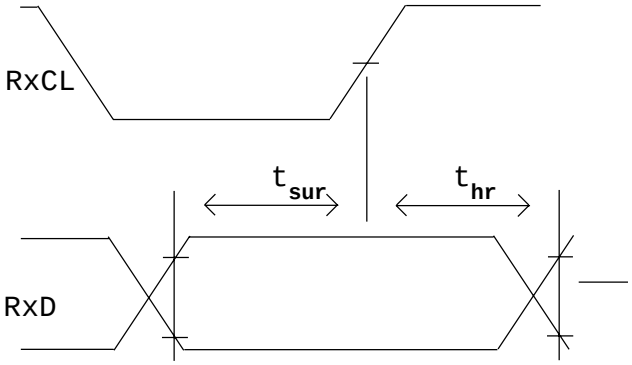
TxCL and RxCL clock pulse widths



Digital Outputs rise and fall times



Transmit set-up and hold times



Receive set-up and hold times

Figure 2. Timing diagrams

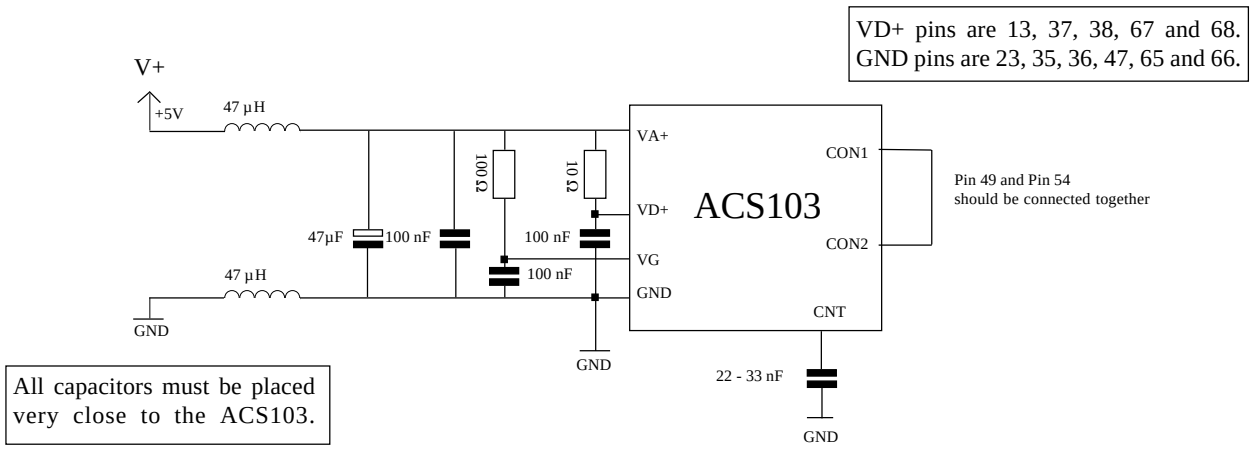


Figure 3. Recommended power supply layout

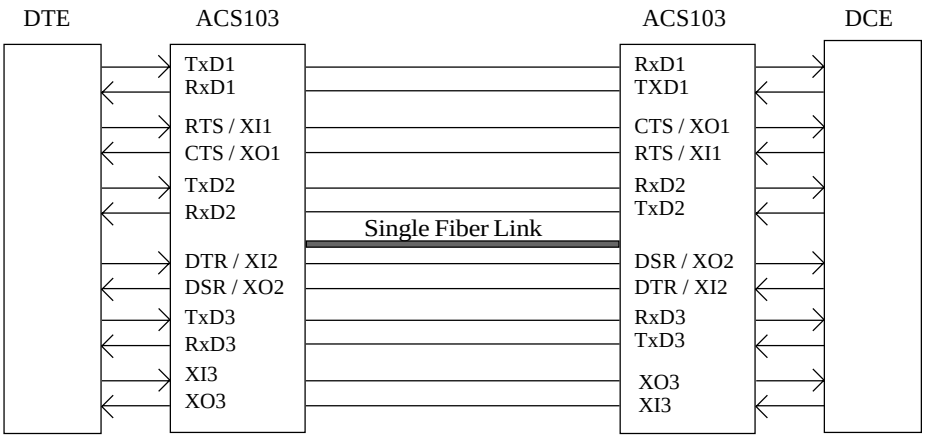


Figure 4. 6 Full-duplex channels in data transmission mode

Link Budget Examples

Cable	200 micron	100 micron	62.5 micron	50 micron
Typical transmit couple power to fiber (µW)	1200	260	100	40
Minimum LED responsivity (A/W)	0.05	0.06	0.1	0.12
Available current (µA)	60	15.6	10	4.8
Minimum ACS103 sensitivity (nA)	650	650	650	650
Link Budget (dB)	20	14	12	8

Above examples using nominal "B" spec. LED diodes. "A" spec. LEDs offer superior performance, e.g. > 12 dB link budget on 50 µm fiber. "A" spec. LEDs are available from Acapella.

Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
Power supply VD+ and VA+ (VDD = VD+ or VA+)	VDD	-0.3	6.0	V
Input voltage (non-supply pins)	Vin	GND - 0.3	VDD + 0.3	V
Input current (except LDN,LDP,CNT,VG)	Iin	-	10.0	mA
Input current (LDN,LDP,CNT)	Iin	-	1.0	mA
Storage temperature	Tstor	-50	160	ºC

Operating Conditions

Parameter	Symbol	Min	Typ	Max	Units
Power supply (VA+ and VD+)	V+	4.75	5.0	5.25	V
Ambient temperature range	TA	-40	-	85	ºC

Static Digital Input Characteristics (for specified operating conditions)

`Input pins: DR 1/2/3/4 , DM 1/2/3, SEL, CKC, RSS, TXD1/2/3, RTS, DTR, XI3, XTI, PORB, TxCL(input).`

Parameter	Symbol	Min	Typ	Max	Units
Vin High (except PORB)	Vih	2.0	-	-	V
Vin Low (except PORB)	Vil	-	-	0.8	V
Vin High (PORB)	Vih	0.8 * VD+	-	-	V
Vin Low (PORB)	Vil	-	-	0.2 * VD+	V
Pull-up resistor (except XTI and TxCL)	PU	50k	125k	340k	Ω
Input current (Note 1)	Iin	-	-	100	µA

Note 1: Input current is mainly attributed to pull-up resistor, so it applies when input is Low. The High input current is < +/-10 µA.

Static Digital Output Characteristics (for specified operating conditions)

`Output pins: RxD1/2/3, CTS, DSR, XO3, DCDB, LIN, ERD, XLO, RxCL, TxCL(output)`

Parameter	Symbol	Min	Typ	Max	Units
Vout Low (Iout = 4mA)	Vol	0	-	0.5	V
Vout High (Iout = 4mA)	Voh	VDD-0.5	-	-	V
Max load capcitance	Cl	-	-	50	pF
XLO (Note 2)	-	-	-	-	pF

Note 2: XLO does not have a drive capability other than that of the load presented by a parallel resonant crystal and appropriate padding capacitor.

Dynamic Characteristics

Parameter	Symbol	Min	Typ	Max	Units
Crystal frequency (XTI, XTO)	frc	5	9.216	10	MHz
External clock (XTI) High or Low time	fcl	40	-	60	%
RxD and TxD data rate ACS101 mode Synchronous standard double Asynchronous standard double	fckc	 2.4 9.6 DC DC	-	 256 64 38.4 19.2	kbps
RxD and TxD data rate ACS103 mode Synchronous standard double Asynchronous standard double	fckc	 2.4 9.6 DC DC	-	 64 38.4 9.6 4.8	kbps
RxCL and TxCL duty cycle (with TxCL = output)	twh twl	-	50	-	%
Frequency deviation at TxCL from selected value (with TxCL = input)	Fd	-	-	500	ppm
TxD to TxCL set-up time	tsut	300	-	-	ns
TxD to TxCL hold time	tht	25	-	-	ns
RxD to RxCL set-up time	tsur	-	0.5 *1/RxCL	-	ns
RxD to RxCL hold time	thr	-	0.5 *1/RxCL	-	ns
Digital output - fall time	tf	-	-	100	ns
Digital output - rise time	tr	-	-	100	ns
Power consumption: TCL floating (or 100kOhms) TCL tied to GND (Note 3)	Pc	-	 200 150	 300 250	mW

Note 3: Power consumption assumes that digital outputs drive CMOS loads.

Matching Characteristics (for specified operating conditions)

Parameter	Symbol	Min	Typ	Max	Units
Crystal tolerance use parallel resonate crystal and recommended padding capacitors	Ct	-100	0	100	ppm
Amplifier sensitivity input current standard double	Irec	 650 500	 500 300	 -	nA
Maximum amplifier input current	Imax	30	50	-	mA
Rtrc placed between TRC and GND	Rtrc	0	-	-	Ω
LED current with TRC floating: peak current average curent (Note 4)	Icur	 70 14	 - -	 130 26	mA
LED capacitance with Vr = 0 Volts (Note 5)	Cled	-	-	100	pF
LED leakage current Vr = 1.8 Volts	Cl	-	1	100	nA
LED reverse bias	Vr	1.3	1.5	1.8	V

Note 4: The LED is switched on for approximately 1/5th of the time with a cycle of 160 µs at 9.216 MHz.
5: The ACS103 is at its best with low capacitance LEDs - Acapella is able to supply LEDs with lower than 20 pF capacitance.

For additional information, contact the following:

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