Signetics

54F676
Shift Register

16-Bit Shift Register

Product Specification

Military FAST Products

FEATURES

- **16-bit parallel-to-serial conversion**
- **16-bit serial-in, serial-out**
- **Chip Select control**
- **Power supply current 48mA typical**
- **Shift frequency 110MHz typical**

DESCRIPTION

The 54F676 contains 16 flip-flops with provision for synchronous parallel or serial entry and serial output. When the Mode (M) input is High, information present on the parallel data (D_0-D_{15}) inputs is entered on the falling edge of the Clock Pulse ($\overline{CP}$) input signal. When M is Low, data is shifted out of the most significant bit position while information present on the Serial (S1) input shifts into the least significant bit position. A High signal on the Chip Select ($\overline{CS}$) input prevents both parallel and serial operations.

The 16-bit shift register operates in one of three modes, as indicated in the Shift Register Operations Table.

Hold – a High signal on the Chip Select ($\overline{CS}$) input prevents clocking, and data is stored in the 16 registers.

Shift/Serial Load – data present on the S1 pin shifts into the register on the falling edge of $\overline{CP}$. Data enters the Q_0 position and shifts toward Q_{15} on successive clocks, finally appearing on the SO pin.

Parallel Load – data present on P_0 - P_{15} are entered into the register on the falling edge of $\overline{CP}$. The SO output represents the Q_{15} register output.

To prevent false clocking, $\overline{CP}$ must be Low during a Low-to-High transition of $\overline{CS}$.

ORDERING INFORMATION

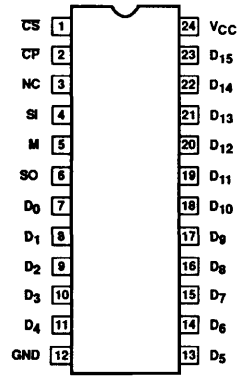
DESCRIPTION	ORDER CODE
24-Pin Ceramic DIP	54F676/BLA
24-Pin Ceramic Flatpack	54F676/BKA
28-Pin Ceramic LLCC	54F676/B3A

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	54F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
$\overline{CS}$	Chip Select input (active Low)	1.0/1.0	20μA/0.6mA
SI	Serial data input	1.0/1.0	20μA/0.6mA
M	Mode select input	1.0/1.0	20μA/0.6mA
D_0 - D_{15}	Parallel data inputs	1.0/1.0	20μA/0.6mA
$\overline{CP}$	Clock Pulse input (active falling edge)	1.0/1.0	20μA/0.6mA
SO	Serial data output	50/33	1mA/20mA

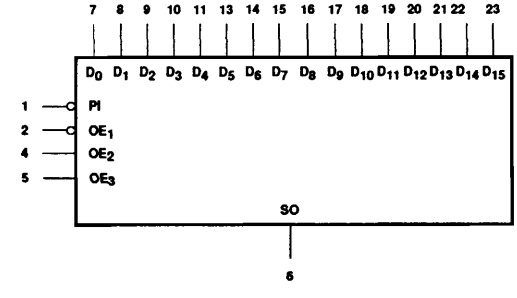
NOTE: One (1.0) FAST Unit Load (U.L.) is defined as: 20μA in the High State and 0.6mA in the Low state.

PIN CONFIGURATION



For LLCC pin assignments, see JEDEC Standard No. 2

LOGIC SYMBOL



For LLCC pin assignments, see JEDEC Standard No. 2

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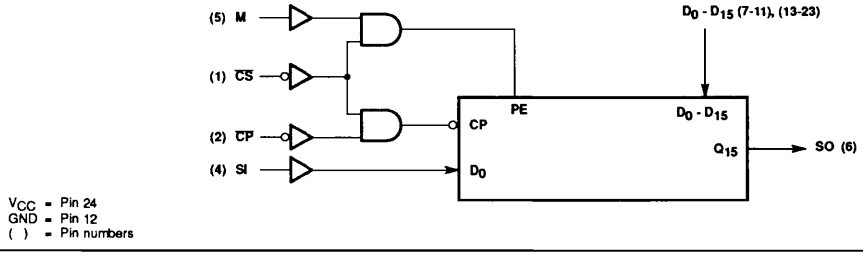
FUNCTION TABLE

CONTROL INPUT			OPERATING MODE
$\overline{CS}$	M	$\overline{CP}$	
H	X	X	Hold
L	L	↓	Shift/serial load
L	H	↓	Parallel load

H = High voltage level
L = Low voltage level
X = Don't care
↓ = High-to-Low clock transition

LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage range	-0.5 to +7.0	V
V_I	Input voltage range	-0.5 to +7.0	V
I_I	Input current range	-30 to +5	mA
V_O	Voltage applied to output in High output state range	-0.5 to +V_{CC}	V
I_O	Current applied to output in Low output state	40	mA
T_{STG}	Storage temperature range	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply Voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	-55		+125	°C

DC ELECTRICAL CHARACTERISTICS (Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS[1]	LIMITS			UNIT
			Min	Typ[2]	Max	
V_{OH}	High-level output voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OH} = Max	2.5			V
V_{OL}	Low-level output voltage	V_{CC} = Min, V_{IL} = Max, V_{IH} = Min, I_{OL} = Max		0.35	0.50	V
V_{IK}	Input clamp voltage	V_{CC} = Min, I_I = I_{IK}		-0.73	-1.2	V
I_{IH2}	Input current at maximum input voltage	V_{CC} = Max, V_I = 7.0V			100	µA
I_{IH1}	High-level input current	V_{CC} = Max, V_I = 2.7V			20	µA
I_{IL}	Low-level input current	V_{CC} = Max, V_I = 0.5V			-0.6	mA
I_{OS}	Short-circuit output current[3]	V_{CC} = Max	-60		-150	mA
I_{CC}	Supply current (total)	V_{CC} = Max		48	72	mA

AC ELECTRICAL CHARACTERISTICS

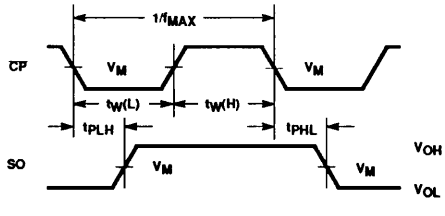
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = 25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55 TO +125°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Waveform 1	100	110		90[4]		MHz
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$ to SO	Waveform 1	4.5 5.0	8.0 7.0	11 12.5	4.5 5.0	12 13.5	ns

AC SETUP REQUIREMENTS

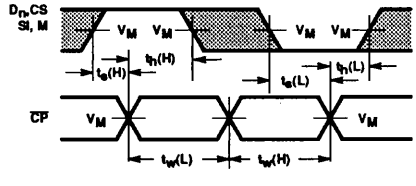
SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T_A = 25°C, V_{CC} = +5.0V, C_L = 50pF, R_L = 500Ω			T_A = -55 TO +125°C, V_{CC} = +5.0V ±10%, C_L = 50pF, R_L = 500Ω		
			Min	Typ	Max	Min	Max	
$t_S(H)$ $t_S(L)$	Setup time, High or Low SI to $\overline{CP}$	Waveform 2	4.0 4.0			4.0 4.0		ns ns
$t_H(H)$ $t_H(L)$	Hold time, High or Low SI to $\overline{CP}$	Waveform 2	4.0 4.0			4.0 4.0		ns ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low D_N $\overline{CP}$	Waveform 2	3.0 3.0			3.0 3.0		ns ns
$t_H(H)$ $t_H(L)$	Hold time, High or Low D_N $\overline{CP}$	Waveform 2	4.0 4.0			4.0 4.0		ns ns
$t_S(H)$ $t_S(L)$	Setup time, High or Low M to $\overline{CP}$	Waveform 2	8.0 8.0			8.0 8.0		ns ns
$t_H(H)$ $t_H(L)$	Hold time, High or Low M to $\overline{CP}$	Waveform 2	2.0 2.0			2.0 2.0		ns ns
$t_S(L)$	Setup time, Low $\overline{CS}$ to $\overline{CP}$	Waveform 2	10.0			10.0		ns
$t_H(H)$	Setup time, High $\overline{CS}$ to $\overline{CP}$	Waveform 2	10.0			10.0		ns
$t_W(H)$ $t_W(L)$	$\overline{CP}$ pulse width High or Low	Waveform 1	4.0 6.0			4.0 6.0		ns ns

NOTES:
1. For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions for the applicable type and function table for operating mode.
2. All typical values are at V_{CC} = 5V and T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. This test is guaranteed, but not tested.

AC WAVEFORMS



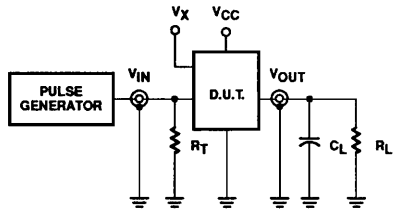
Waveform 1. Propagation Delay, Clock Input to Output, Clock Widths and Maximum Clock Frequency



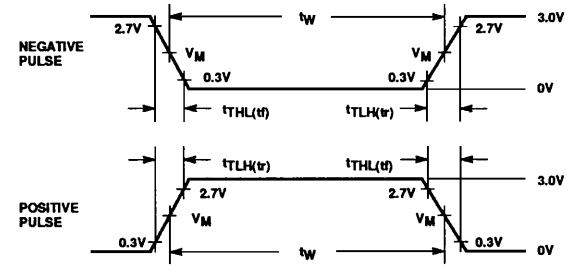
Waveform 2. Propagation Delay for Data to Output, Data and Select Setup, and Hold Times

NOTE: V_M = 1.5V.
The shaded areas indicate when the input is permitted to change for predictable output performance.

AC WAVEFORMS



Test Circuit for Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS:

R_L = Load Resistor; see AC Characteristics for value.
C_L = Load capacitance includes jig and probe capacitance; see AC Characteristics for value.
R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.
V_X = Unclocked pins must be held at: ≤0.8V; ≥2.7V or open per FunctionTable.

INPUT PULSE CHARACTERISTICS				
Family	**Rep. Rate**	**Pulse Width**	**t_{TLH}**	**t_{THL}**
54F	1MHz	500ns	≤2.5ns	≤2.5ns