Rockwell

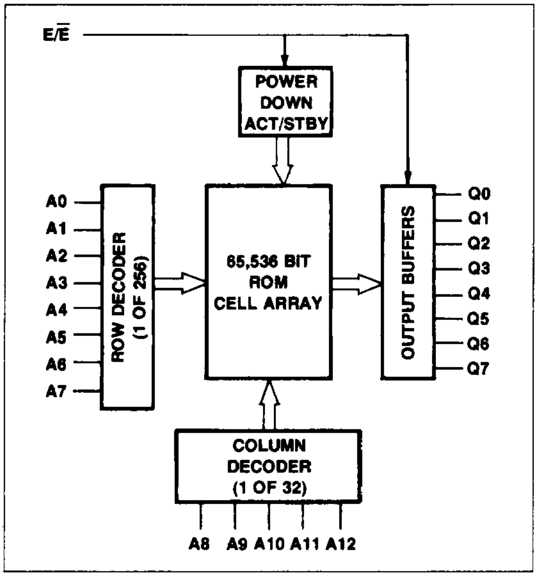
R2364A
64K (8K × 8) STATIC ROM

DESCRIPTION

The R2364A2, R2364A25 and R2364A3 are 65,536-bit static Read-Only Memories (ROMs), organized as 8,192 eight-bit bytes, that offer maximum access times of 200, 250 and 300 nanoseconds, respectively. These ROMs are in industry-standard 24-pin, dual in-line packages, and are available in ceramic or low-cost plastic. These fully-static 64K-bit ROMs are compatible with industry standard microprocessors.

All three R2364A ROMs operate totally asynchronously, and require no clock input. These devices provide tri-state output buffers for memory expansion. The R2364A ROMs offer TTL input and output levels with a minimum noise immunity of 0.4 volts.

The mask-programmable chip enable input (E/$\overline{E}$) may be programmed to function as a chip select without power down standby mode or as a chip enable with power down standby mode. The active level of the enable input is also programmable.



R2364A Block Diagram

FEATURES

- 8,192 × 8 organization
- Access time: 200 ns, 250 ns, and 300 ns (max.)
- Low power dissipation: 125 mW active, 37.5 mW standby
- Drives two TTL loads and 100 pf
- Single +5V ± 10% power supply
- Totally static operation, no input clock required
- Completely TTL compatible
- Mask-programmable chip enable
- Tri-state outputs for memory expansion

ORDERING INFORMATION

Part Number: R2364A— — — — —

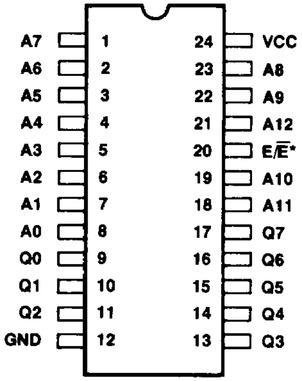
Package:
C = Ceramic
P = Plastic

Temperature Range:
No letter = 0°C to +70°C
E = −40°C to +85°C

Power Down Standby Mode:
S = Yes
No letter = No

Access Time (Max):
2 = 200 ns
25 = 250 ns
3 = 300 ns

Note: Submit ROM codes using Rockwell ROM Code Order Form, Order No. 2137.



***Mask-programmable option**

R2364A Pin Configuration

ABSOLUTE MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.5 to +7.0	Vdc
Input Voltage	V_{IN}	−0.5 to +7.0	Vdc
Output Voltage	V_{OUT}	−0.5 to +7.0	Vdc
Temperature Under Bias Commercial Industrial	T_A	 −10 to +80 −50 to +95	°C
Storage Temperature	T_{STG}	−65 to +150	°C
Power Dissipation	P	1.0	W

***NOTE:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	Min	Typ[3]	Max	Units	Test Conditions
V_{OH}	Output High Voltage	2.4		V_{CC}	V	V_{CC} = 4.5V, I_{OH} = −400 μA
V_{OL}	Output Low Voltage			0.4	V	V_{CC} = 4.5V, I_{OL} = 3.3 mA
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	−0.5		0.8	V	
I_{LI}	Input Load Current			10	μA	V_{CC} = 5.5V, 0V ≤ V_{IN} ≤ 5.5V
I_{LO}	Output Leakage Current			±10	μA	V_{CC} = 5.5V, chip deselected, V_{OUT} = +0.4V to V_{CC}
I_{CC}	Power Supply Current, Active		25	55	mA	V_{CC} = 5.5V
I_{SB}	Power Supply Current, Standby[1]		7.5	16	mA	
C_I	Input Capacitance[2]			7	pF	V_{CC} = 5.0V, chip deselected, pin under test at 0V, T_A = 25°C
C_O	Output Capacitance[2]			10	pF	f = 1 MHz

Notes:
1. Applies only to chip enable with power down standby mode.
2. This parameter is periodically sampled and is not 100% tested.
3. Typical values are for T_A = 25°C and V_{CC} = 5.0V.

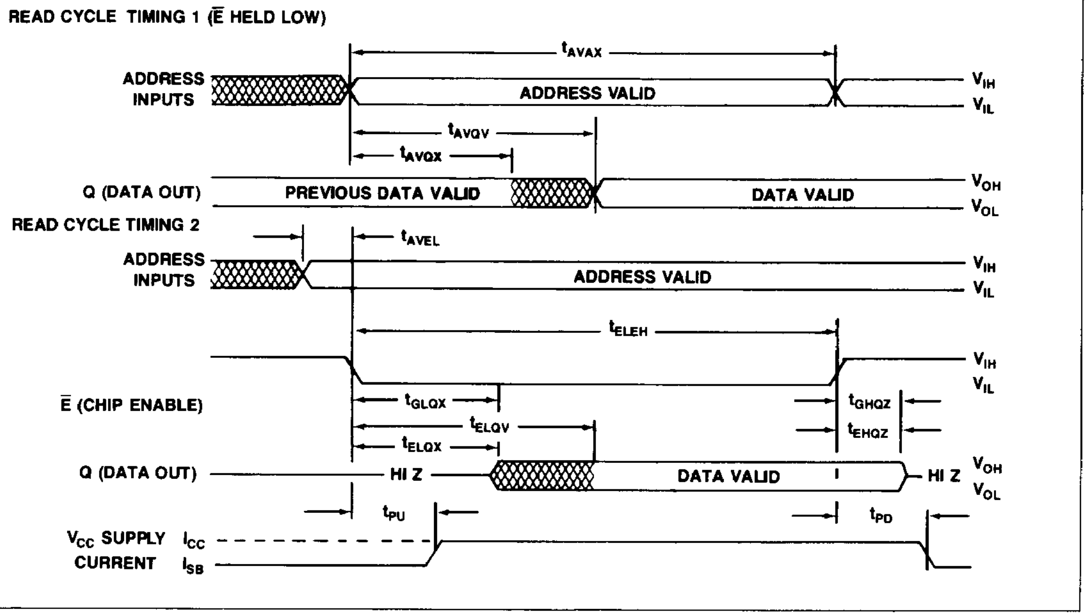
AC CHARACTERISTICS

V_{CC} = 5.0V ± 10%, T_A = 0°C to 70°C (unless otherwise specified)

Symbol	Parameter	R2364A2		R2364A25		R2364A3		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t_{AVAX}	Address Valid to Address Don't Care	200		250		300		ns
t_{ELEH}	Chip Enable Low to Chip Enable High[2]	200		250		300		ns
t_{AVQV}	Address Valid to Output Valid (t_{ACC}) (Access)		200		250		300	ns
t_{ELQV}	Chip Enable Low to Output Valid (Access)[2]		200		250		300	ns
t_{AVQX}	Address Valid to Output (t_{OH}) Invalid	10		10		10		ns
t_{ELQX}	Chip Enable Low to Output (t_{CO}) Invalid	10		10		10		ns
t_{EHQZ}	Chip Enable High to Output High Z (t_{DF})	10	70[4]	10	70[4]	10	70[4]	ns
t_{PU}	Chip Selection to Power Up Time[2]	0		0		0		ns
t_{PD}	Chip Deselection to Power Down Time[2]		100[4]		100[4]		100[4]	ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		0		ns
t_{GLQX}	Chip Select Low to Output Invalid[3]	10	90[4]	10	90[4]	10	90[4]	ns
t_{GHQZ}	Chip Select High to Output High Z	10	70[4]	10	70[4]	10	70[4]	ns

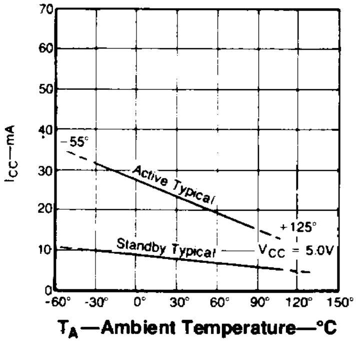
Notes:
1. Test Conditions:
   Output Load: 2 TTL Loads and 100 pF; Input Transition Time: 20 ns; Timing Reference Levels: Input: 1.5V, Output: 0.8V, 2.0V.
2. Mask-programmed for chip enable with power down standby mode.
3. Mask-programmed for chip enable without power down standby mode.
4. Add 20 ns for extended temperature devices (−40°C to +85°C).

TIMING DIAGRAMS

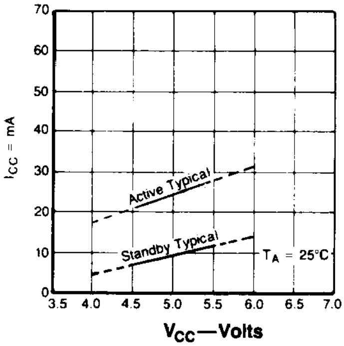


TYPICAL CHARACTERISTICS

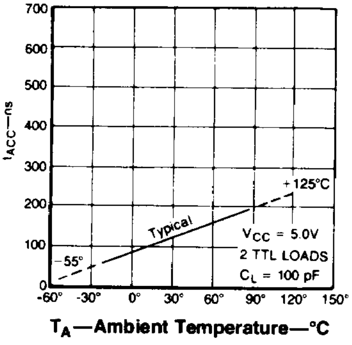
SUPPLY CURRENT VS AMBIENT TEMPERATURE



SUPPLY CURRENT VS SUPPLY VOLTAGE

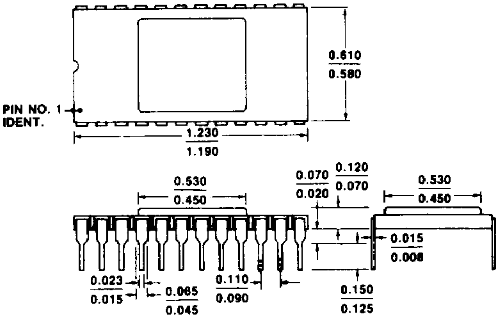


ACCESS TIME VS AMBIENT TEMPERATURE



PACKAGE DIMENSIONS

24-PIN CERAMIC DIP



24-PIN PLASTIC DIP