TC74HC160/162AP/AF
TC74HC161/163AP/AF/AFN

Synchronous Presettable 4-Bit Counter
TC74HC160 Decade, Asynchronous Clear
TC74HC161 Binary, Asynchronous Clear
TC74HC162 Decade, Synchronous Clear
TC74HC163 Binary, Synchronous Clear

The TC74HC160A,161A, 162A and 163A are high speed CMOS SYNCHRONOUS PRESETTABLE COUNTERs fabricated with silicon gate C^2MOS technology.

They achieve the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

The 74HC160A/162A are BCD decade counters and the TC74HC161A/163A are 4 bit binary counters.

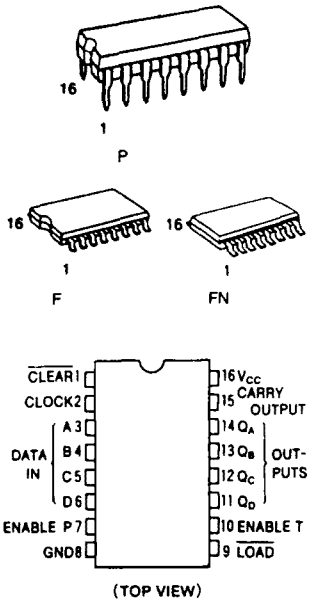
The CLOCK input is active on the rising edge. Both $\overline{LOAD}$ and $\overline{CLEAR}$ inputs are active on low logic level.

Presetting of all four IC's is synchronous to the rising edge of CLOCK.

The clear function of the TC74HC162A/163A is synchronous to CLOCK, while the TC74HC160A/161A are cleared asynchronously.

Two enable inputs (ENP and ENT) and CARRY OUTPUT are provided to enable easy cascading of counters, which facilitates easy implementation of n-bit counters without using external gates.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

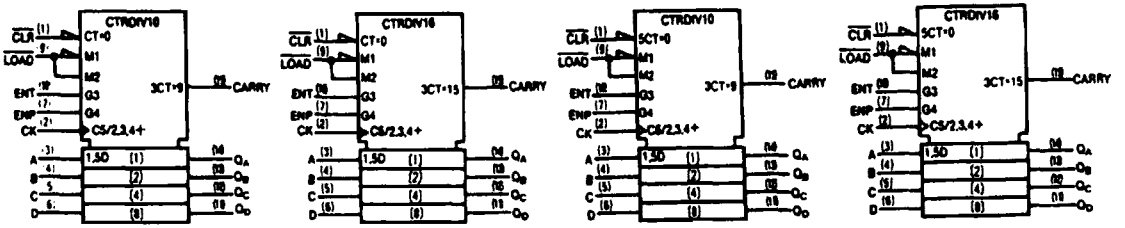


Pin Assignment

Features

- High Speed: t_{MAX} = 63MHz(Typ.) at V_{CC} = 5V
- Low Power Dissipation: I_{CC} = 4μA(Max.) at Ta = 25°C
- High Noise Immunity: $V_{NIH} = V_{NIL}$ = 28%V_{CC}(Min.)
- Output Drive Capability: 10 LSTTL Loads
- Symmetrical Output Impedance: $|I_{OH}| = I_{OL}$ = 4mA(Min.)
- Balanced Propagation Delays: $t_{pLH} = t_{pHL}$
- Wide Operating Voltage Range: V_{CC}(opr) = 2V ~ 6V
- Pin and Function Compatible with 74LS160 ~ 163

TC74HC160A TC74HC161A TC74HC162A TC74HC163A

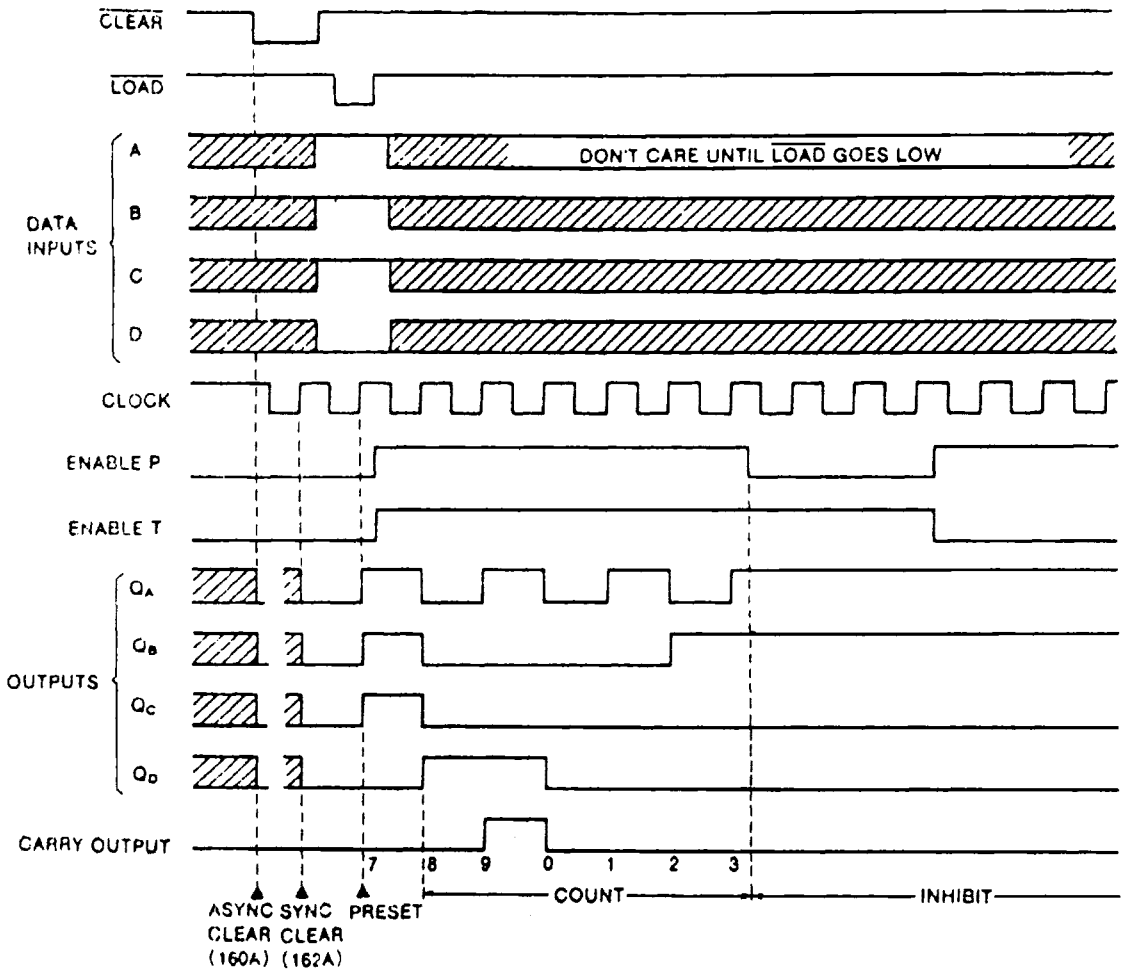


IEC Logic Symbol

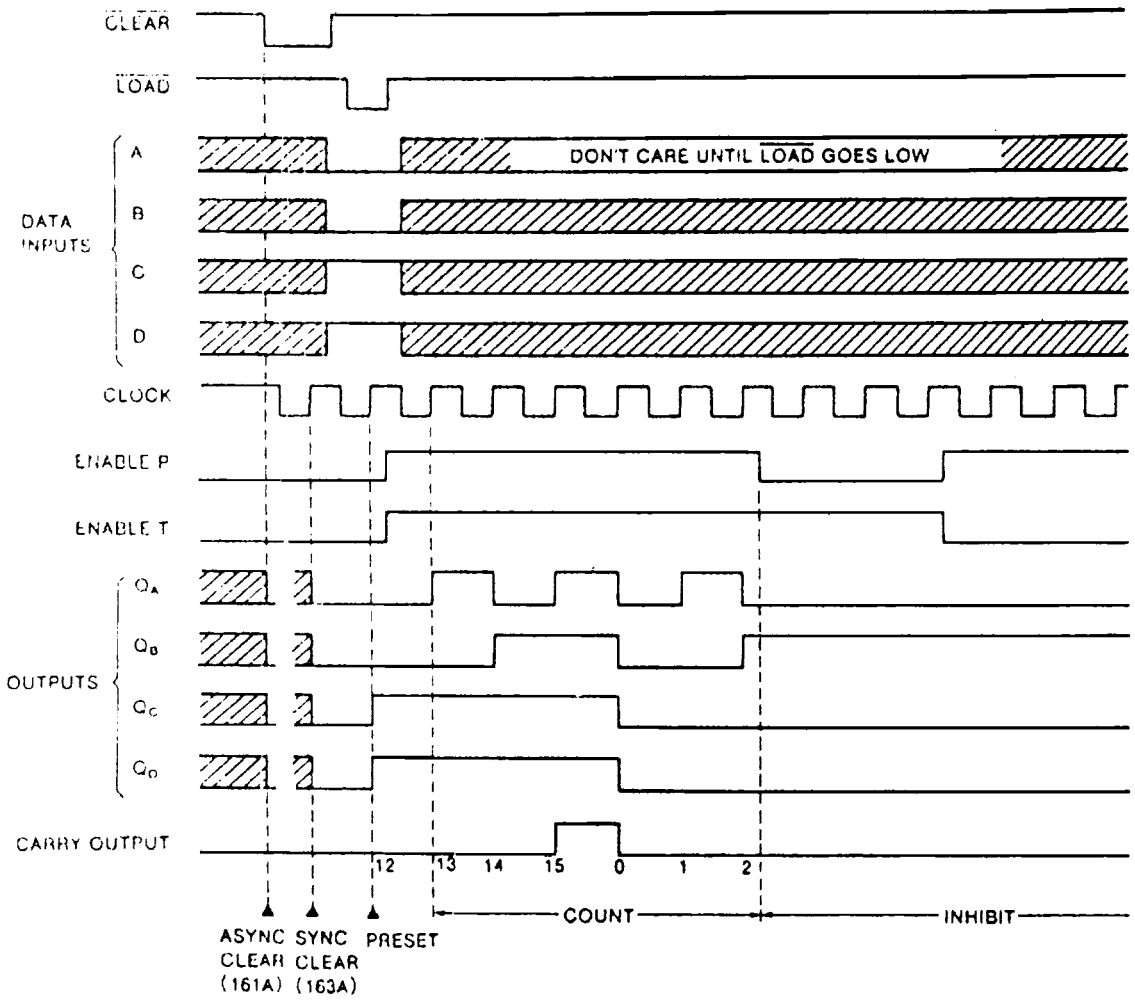
Truth Table

TC74HC160A/161A					TC74HC162A/163A					Outputs				Function
Inputs					Inputs									
$\overline{CLR}$	$\overline{LD}$	ENP	ENT	CK	$\overline{CLR}$	$\overline{LD}$	ENP	ENT	CK	Q_A	Q_B	Q_C	Q_D	
L	X	X	X	X	L	X	X	X	⌐	L	L	L	L	Reset To "0"
H	L	X	X	⌐	H	L	X	X	⌐	A	B	C	D	PRESET Data
H	H	X	L	⌐	H	H	X	L	⌐	No Change				No Count
H	H	L	L	⌐	H	H	L	X	⌐	No Change				No Count
H	H	H	H	⌐	H	H	H	H	⌐	Count Up				Count
H	X	X	X	⌙	X	X	X	X	⌙	No Change				No Count

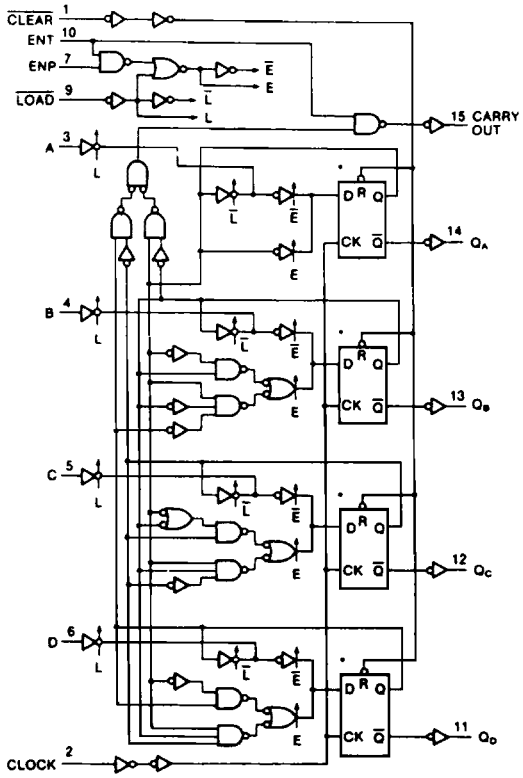
X: Don't Care
A, B, C, D: Logic Level of Data Inputs
Carry: CARRY = ENT•Q_A•$\overline{Q}_B$•$\overline{Q}_C$•Q_D .....(TC74HC160A/162A)
CARRY = ENT•Q_A•Q_B•Q_C•Q_D .....(TC74HC161A/163A)



Timing Chart (TC74HC160A/162A: Decade Counter)



Timing Chart (TCHC161A/163A: Binary Counter)

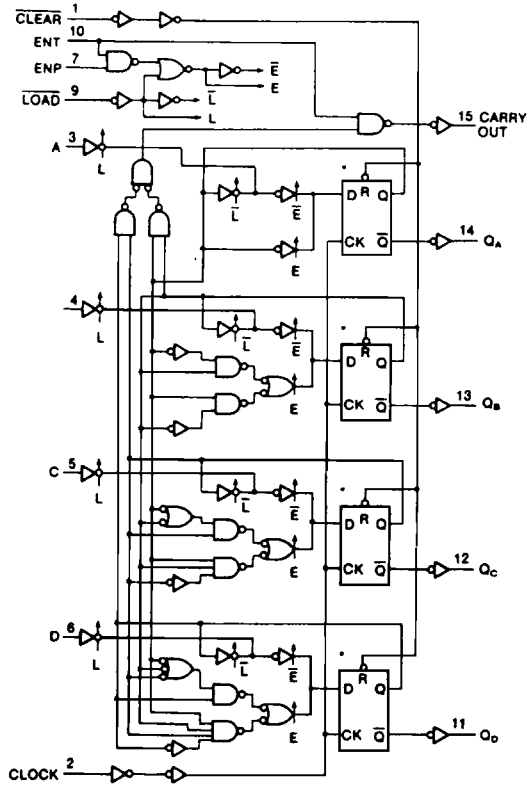


Logic Diagram

Truth Table of Internal F/F

TC74HC160A					TC74HC162A				
D	CK	R	Q	$\overline{Q}$	D	CK	R	Q	$\overline{Q}$
X	X	L	L	H	X	↓	L	L	H
L	↓	H	L	H	L	↓	H	L	H
H	↓	H	H	L	H	↓	H	H	L
X	↑	H	NO CHANGE		L	↑	H	No Change	

X: Don't Care



Logic Diagram

Truth Table of Internal F/F

TC74HC161A					TC74HC163A				
D	CK	R	Q	$\overline{Q}$	D	CK	R	Q	$\overline{Q}$
X	X	L	L	H	X	↓	L	L	H
L	↓	H	L	H	L	↓	H	L	H
H	↓	H	H	L	H	↓	H	H	L
X	↑	H	NO CHANGE		L	↑	H	No Change	

X: Don't Care

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Supply Voltage Range	V_{CC}	-0.5 ~ 7	V
DC Input Voltage	V_{IN}	-0.5 ~ V_{CC} + 0.5	V
DC Output Voltage	V_{OUT}	-0.5 ~ V_{CC} + 0.5	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC}/Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500(DIP)*/180(MFP)	mW
Storage Temperature	T_{stg}	-65 ~ 150	°C
Lead Temperature 10sec	T_L	300	°C

*500mW in the range of Ta = -40°C ~ 65°C. From Ta = 65°C to 85°C a derating factor of -10mW/°C shall be applied until 300mW.

Recommended Operating Conditions

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	2 ~ 6	V
Input Voltage	V_{IN}	0 ~ V_{CC}	V
Output Voltage	V_{OUT}	0 ~ V_{CC}	V
Operating Temperature	T_{opr}	-40 ~ 85	°C
Input Rise and Fall Time	t_r, t_f	0 ~ 1000(V_{CC} = 2.0V) 0 ~ 500(V_{CC} = 4.5V) 0 ~ 400(V_{CC} = 6.0V)	ns

DC Electrical Characteristics

Parameter	Symbol	Test Condition		V_{CC}	Ta = 25°C Min.	Ta = 25°C Typ.	Ta = 25°C Max.	Ta = -40 ~ 85°C Min.	Ta = -40 ~ 85°C Max.	Unit
High-Level Input Voltage	V_{IH}	–		2.0 4.5 6.0	1.7 3.6 4.8	– – –	– – –	1.7 3.6 4.8	– – –	V
Low-Level Input Voltage	V_{IL}	–		2.0 4.5 6.0	– – –	– – –	0.3 0.9 1.2	– – –	0.3 0.9 1.2	V
High-Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	I_{OH} = -20μA	2.0 4.5 6.0	1.8 4.0 5.5	2.0 4.5 5.9	– – –	1.8 4.0 5.5	– – –	V
			I_{OH} = -4 mA I_{OH} = -5.2mA	4.5 6.0	4.18 5.68	4.31 5.80	– –	4.13 5.63	– –	
Low-Level Output Voltage	V_{OL}	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 20μA	2.0 4.5 6.0	– – –	0.0 0.0 0.1	0.2 0.5 0.5	– – –	0.2 0.5 0.5	V
			I_{OL} = 4 mA I_{OL} = 5.2mA	4.5 6.0	– –	0.17 0.18	0.26 0.26	– –	0.33 0.33	
Input Leakage Current	I_{IN}	V_{IN} = V_{CC} or GND		6.0	–	–	±0.1	–	±1.0	μA
Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND		6.0	–	–	4.0	–	40.0	

Timing Requirements (Input $t_r = t_f = 6ns$)

Parameter	Symbol	Test Condition		Ta = 25°C		Ta = -40 ~ 85°C	Unit
			V_{CC}	Typ.	Limit	Limit	
Minimum Pulse Width (CLOCK)	$t_{W(L)}$ $t_{W(H)}$	Fig. 1	2.0 4.5 6.0	– – –	75 15 13	95 19 16	ns
Minimum Pulse Width ($\overline{CLEAR}$)*	$t_{W(L)}$	Fig. 4	2.0 4.5 6.0	– – –	75 15 13	95 19 16	
Minimum Setup Time ($\overline{LOAD}$, ENP, ENT)	t_s	Fig. 4	2.0 4.5 6.0	– – –	100 20 17	125 25 21	
Minimum Setup Time (A, B, C, D)	t_s	Fig. 2	2.0 4.5 6.0	– – –	75 15 13	95 19 16	
Minimum Set-up Time ($\overline{CLEAR}$)**	t_s	Fig. 5	2.0 4.5 6.0	– – –	75 15 13	95 19 16	
Minimum Hold Time	t_h	Fig 2, 3, 5	2.0 4.5 6.0	– – –	0 0 0	0 0 0	
Minimum Removal Time ($\overline{CLEAR}$)*	t_{rem}	Fig 4	2.0 4.5 6.0	– – –	50 10 9	65 13 11	
Clock Frequency	f	–	2.0 4.5 6.0	– – –	6 31 36	5 25 29	MHz

AC Electrical Characteristics ($C_L = 15pF$, $V_{CC} = 5V$, Ta = 25°C, Input $t_r = t_f = 6ns$)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Output Transition Time	t_{TLH} t_{THL}	Fig. 1	–	4	8	ns
Propagation Delay Time (CLOCK-Q)	t_{pLH} t_{pHL}	Fig. 1	–	13	21	
Propagation Delay Time (CLOCK-CARRY) (Count Mode)	t_{pLH} t_{pHL}	Fig. 1	–	16	26	
Propagation Delay Time (CLOCK-CARRY) (Preset Mode)	t_{pLH}	Fig. 2	–	18	30	
	t_{pHL}		–	20	35	
Propagation Delay Time (ENT-CARRY)	t_{pLH} t_{pHL}	Fig. 6	–	10	17	
Propagation Delay Time ($\overline{CLEAR}$- Q)*	t_{pHL}	Fig. 4	–	17	26	
Propagation Delay Time ($\overline{CLEAR}$- CARRY)*	t_{pHL}	Fig. 4	–	20	35	
Maximum Clock Frequency	f_{MAX}	–	36	63	–	MHz

*: for TC74HC160A/161A only
**: for TC74HC162A/163A only

AC Electrical Characteristics (C_L = 50pF, Input $t_r = t_f$ = 6ns)

Parameter	Symbol	Test Condition		Ta = 25°C			Ta = -40 ~ 85°C		Unit
			V_{CC}	Min.	Typ.	Max.	Min.	Max.	
Output Transition Time	t_{TLH} t_{THL}	–	2.0 4.5 6.0	– – –	25 7 6	75 15 13	– – –	95 19 16	ns
Propagation Delay Time (CLOCK-Q)	t_{pLH} t_{pHL}	Fig. 1	2.0 4.5 6.0	– – –	48 16 14	125 25 21	– – –	155 31 26	
Propagation Delay Time (CLOCK-CARRY) (Count Mode)	t_{pLH} t_{pHL}	Fig. 1	2.0 4.5 6.0	– – –	57 19 16	150 30 26	– – –	190 38 33	
Propagation Delay Time (CLOCK-CARRY) (Preset Mode)	t_{pLH}	Fig. 2	2.0 4.5 6.0	– – –	66 22 19	175 35 30	– – –	220 44 37	
	t_{pHL}		2.0 4.5 6.0	– – –	72 24 20	200 40 34	– – –	250 50 43	
Propagation Delay Time (ENT-CARRY)	t_{pLH} t_{pHL}	Fig. 6	2.0 4.5 6.0	– – –	39 13 11	100 20 17	– – –	125 25 21	
Propagation Delay Time ($\overline{CLEAR}$- Q)	t_{pHL}	Fig. 4	2.0 4.5 6.0	– – –	60 20 17	150 30 26	– – –	190 38 33	
Propagation Delay Time ($\overline{CLEAR}$- CARRY)	t_{pHL}	Fig. 4	2.0 4.5 6.0	– – –	72 24 20	200 40 34	– – –	250 50 43	
Maximum Clock Frequency	f_{MAX}	–	2.0 4.5 6.0	6 31 36	18 53 62	– – –	5 25 29	– – –	MHz
Input Capacitance	C_{IN}	–		–	5	10	–	10	pF
Power Dissipation Capacitance	C_{PD}(1)	(1)		–	34	–	–	–	

Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$I_{CC(opr)} = C_{PD} \bullet V_{CC} \bullet f_{IN} + I_{CC}$

When the outputs drive a capacitive load, total current consumption is the sum of CPD, and ICC which is obtained from the following formula:

In case of TC74HC160A/162A:

$$\Delta I_{CC} = f_{CK} \bullet V_{CC} \left(\frac{C_{QA}}{2} + \frac{C_{QB}}{5} + \frac{C_{QC}}{10} + \frac{C_{QD}}{10} + \frac{C_{CO}}{10}\right)$$

In case of TC74HC161A/163A:

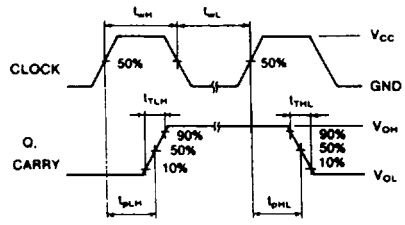
$$\Delta I_{CC} = f_{CK} \bullet V_{CC} \left(\frac{C_{QA}}{2} + \frac{C_{QB}}{4} + \frac{C_{QC}}{8} + \frac{C_{QD}}{16} + \frac{C_{CO}}{16}\right)$$

C_{QA} ~ C_{QD} and C_{CO} are the capacitances at QA ~ QD and CARRY OUT, respectively.

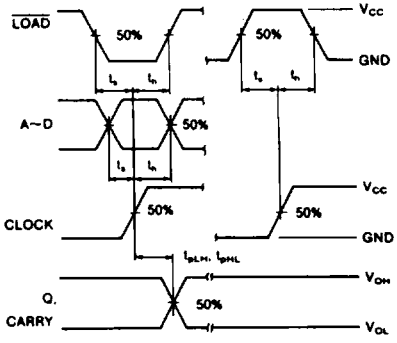
f_{CK} is the input frequency of the CLOCK

(2) * for TC74HC160A/161A only
** for TC74HC162/163A only

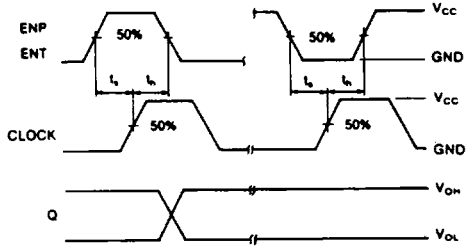
Count Mode (Fig. 1)



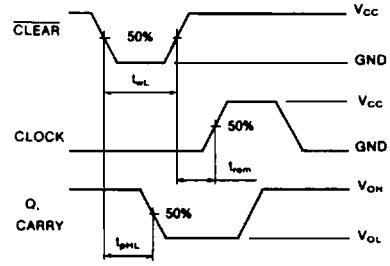
Preset Mode (Fig.2)



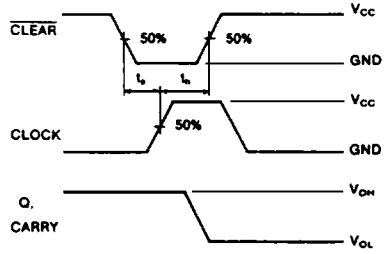
Count Enable Mode (Fig. 3)



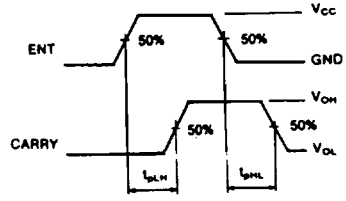
Clear Mode (TC74HC160A/161A) (Fig. 4)



Clear Mode (TC74HC162A/163A) (Fig. 5)

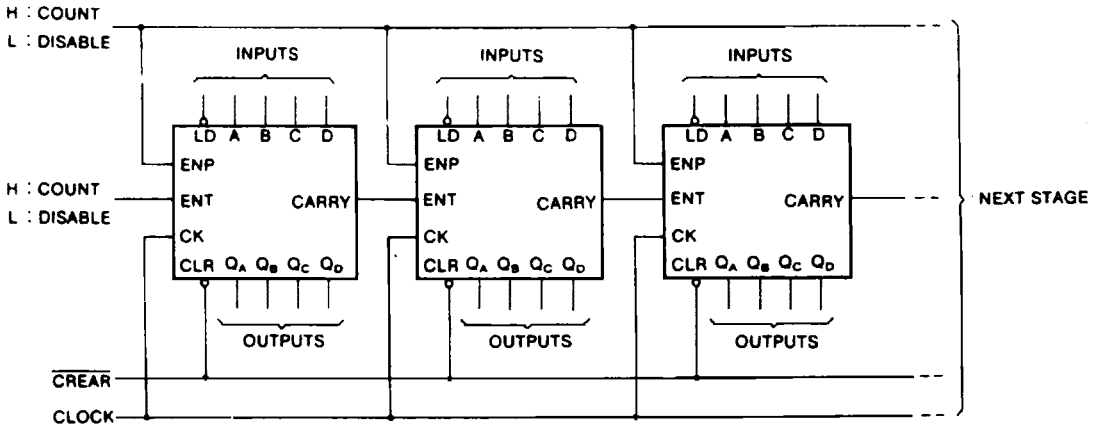


Cascade Mode (Fig. 6)
(Fix Maximum Count)



Switching Characteristics Test Waveform

PARALLEL CARRY N-BIT COUNTER



Typical Application