# 12-36GHz Frequency Multiplier

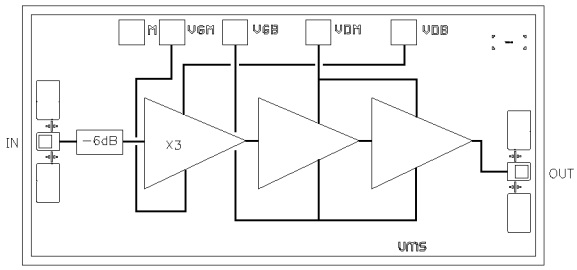
## GaAs Monolithic Microwave IC

Preliminary

## Description

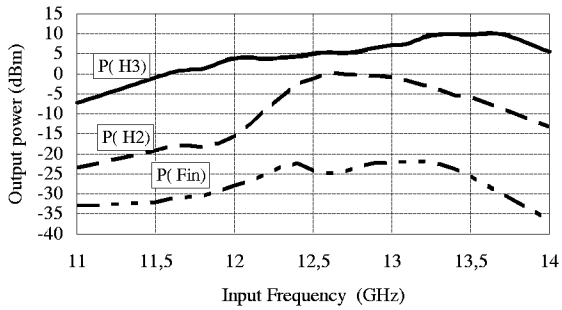
The CHX1094 is a cascadable by 3 frequency multiplier monolithic circuit.
It is designed for a wide range of applications, from military to commercial communication systems. The backside of the chip is both RF and DC grounds. This helps simplify the assembly process.

The circuit is manufactured with a PM-HEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.




## Main Features

Broadband performances : 12-14GHz
5dBm output power for +14dBm input power
DC bias : Vd=3.Volt @Id=40mA
Chip size : 2.07 x 1.03 x 0.10 mm




*typical measurement*

## Main Characteristics

Tamb. = 25°C

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Fin | Input frequency range | 12 | | 14 | GHz |
| Fout | Output frequency range | 36 | | 42 | GHz |
| Pin | Input power | | 14 | | dBm |
| Pout | Output power @ Pin= 14dBm | | 5 | | dBm |

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !



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## Electrical Characteristics

Tamb = +25°C, Vd = 3V , Vgm = -1.6V , Vgb = -0.4V.

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Fin | Input frequency range | 12 | | 14 | GHz |
| Fout | Output frequency range | 36 | | 42 | GHz |
| Pin | Input power | | 14 | | dBm |
| Pout | Output power @ Pin=14dBm | | 5 | | dBm |
| Is/2Fin | 2Fin level at the output ( Pin ≤ 14dBm) | | | 0 | dBm |
| Is/Fin | Fin level at the output ( Pin ≤ 14dBm) | | | -20 | dBm |
| VSWRin | Input VSWR | | | 2:1 | |
| VSWRout | Output VSWR | | | 2.5:1 | |
| Id | Bias current | | 40 | | mA |

## Absolute Maximum Ratings

Tamb. = 25°C (1)

| Symbol | Parameter | Values | Unit |
|---|---|---|---|
| Vd | Drain bias voltage | 4 | V |
| Id | Drain bias current | 120 | mA |
| Vg | Gate bias voltage | -2 to +0.4 | V |
| Ta | Operating temperature range | -40 to +85 | °C |
| Tstg | Storage temperature range | -55 to +155 | °C |

(1) Operation of this device above anyone of these parameters may cause permanent damage.



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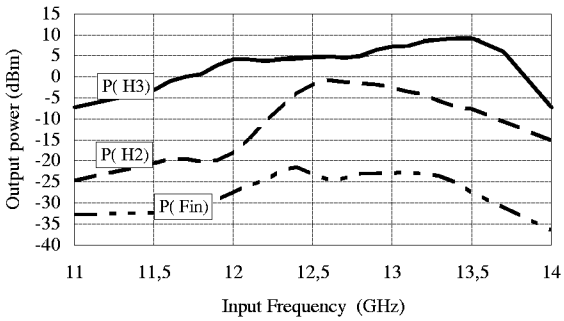
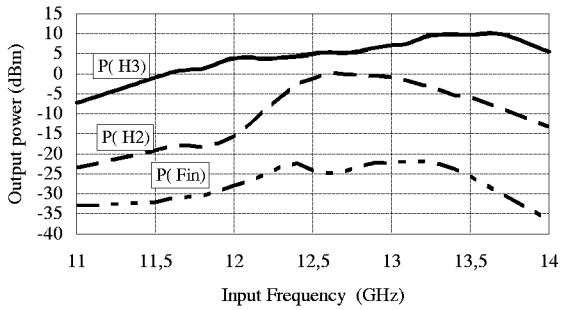
## Typical on Jig Measurements.

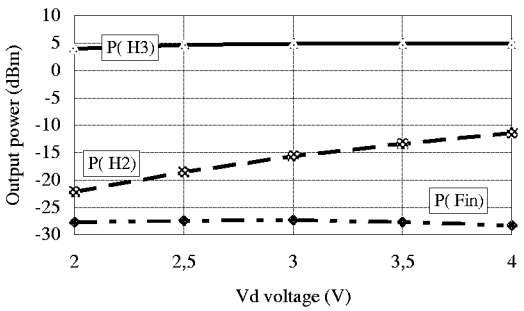
Bias conditions : Vd = 2.5V , Vgm = -1.6V , Vgb = -0.4V.



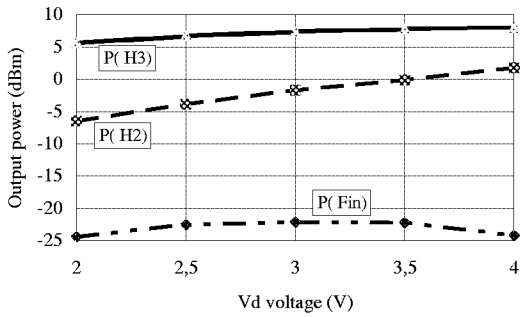

**Pout versus Fin @ Pin=14 dBm & Vd=2.5V**



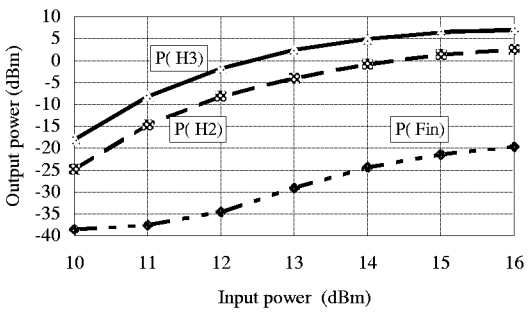

**Pout versus Fin @ Pin=14 dBm & Vd=3V**



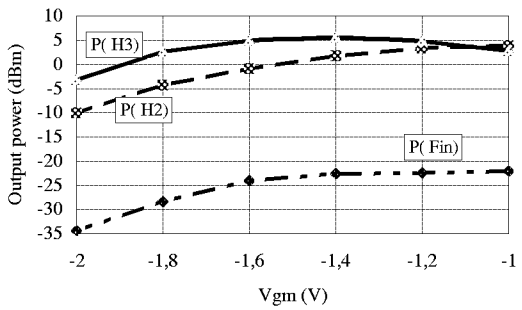

**Pout versus Vd @ Pin=14dBm & Fin=13GHz**




**Pout versus Vd @ Pin=14dBm & Fin=12GHz**




**Pout versus Pin @ Fin=12.5GHz**




**Pout versus Vgm @ Pin=14dBm & Fin=12.5GHz**



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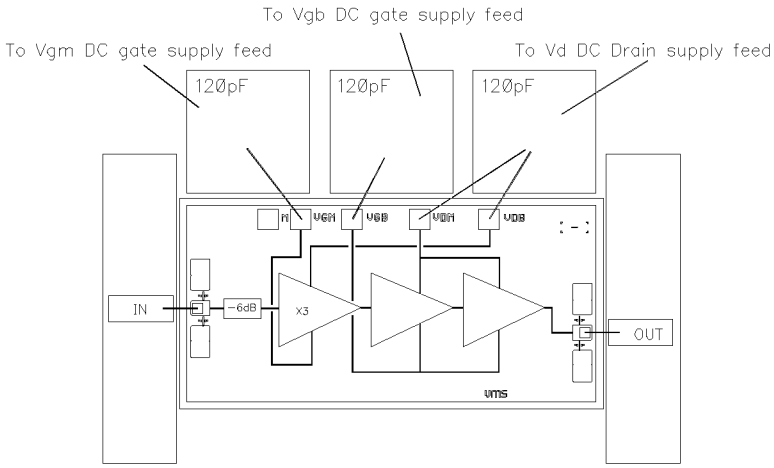
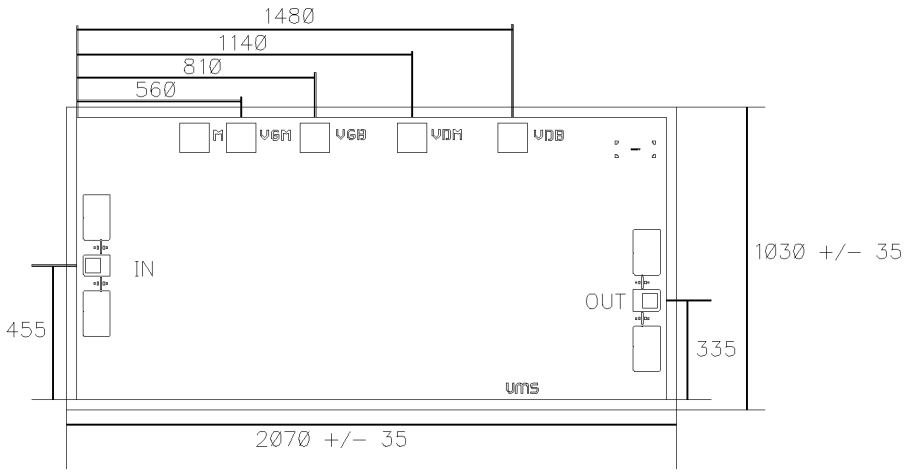
## Chip Assembly and Mechanical Data




Note : Supply feed should be capacitively bypassed. 25µm diameter gold wire is to be prefered
Bond Pad:100 x 100 $\mu^2$m.




**Bonding pad positions.**
( Chip thickness : 100µm. All dimensions are in micrometers )

## Ordering Information

Chip form : CHX1094-99F/00

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