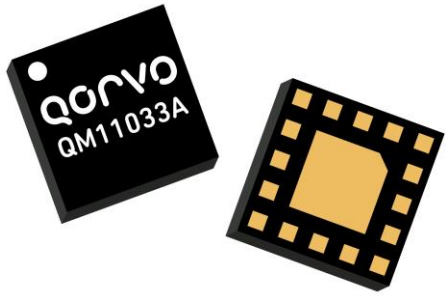
QM11033A

BROADBAND HIGH LINEARITY 3P3T ROUTING SWITCH

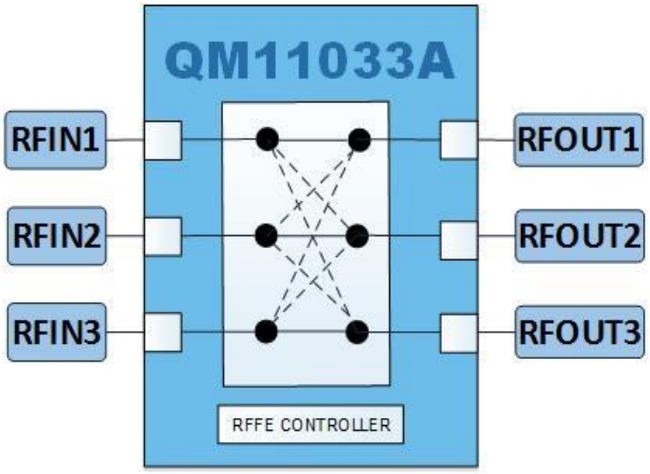
Product Overview

The QM11033A is a low loss, high linearity three-pole three throw addressable switch with performance optimized for transfer routing applications. The QM11033A integrates a serial control system compatible with the RFFE standard. The select lines (SID) provide USID addressability and up to two placements of the QM11033A on the same RFFE bus. The QM11033A runs off a single VIO voltage supply and is packaged in a 16 pin compact 2.0mm x 2.0mm x 0.6mm size device.This offers mobile handset designers a compact, easy-to-use, switch component for quick integration into multimode, multi-band systems.



16 Pin 2.0 x 2.0 X x 0.6 mm package

Functional Block Diagram



Key Features

- **All Paths <2.5us Switching Speed for optimized SRS applications**
- Excellent Insertion Loss and Isolation performance
- High Linearity
- RFFE 2.1 Control Interface with HW Masked Writes
- Broadband Performance Suitable for Multiple Air Interfaces including 5G applications, 100MHz to 6GHz
- Slave ID for Multiple Placements on the Same Board
- Very Low Current Consumption
- DC blocking capacitors are not required
- Single VIO supply

Applications

- Cellular Handset Applications
- Cellular Modems and USB Devices
- Multi-Mode GSM, CDMA, WCDMA, LTE, 5G Applications

Ordering Information

Part Number	Description
QM11033ADK	Design Kit
QM11033ASB	Sample Bag with 5 pcs
QM11033ASR	Sample Reel with 100 pcs
QM11033ATR13	Standard 13” Reel with 10,000 pcs

Absolute Maximum Ratings

Parameter	Conditions	Rating
Storage Temperature		-40 to +125 °C
Operating Temperature		-30 to +90°C
V_{IO}, SDATA, SCLK, & USID		2.5 V
Max GSM or LTE/NR Peak (Instantaneous) Power	1:1 VSWR, +25°C	38dBm
Max Power (CW, 100% DC)	1:1 VSWR, +90°C	35dBm

Operation of this device outside the parameter ranges given above may cause permanent damage.

Recommended Operating Conditions

Parameter	Min.	Typ.	*MAX*	Units
V_{IO} Interface Supply Voltage High	1.65	1.8	1.95	V
V_{IO} Interface Supply Voltage Low	0	0	0.45	V
V_{IO} Interface Supply Current	0	36	55	uA
USID Control Voltage High	1.3	1.8	1.95	V
USID Control Voltage High	0	0	0.45	V
SDATA, SCLK – Voltage High	0.8 x V_{IO}	1.8	V_{IO}	V
SDATA, SCLK – Voltage Low	0.00	0.00	0.2 x V_{IO}	V
Switching Time – 50% last CLK rising edge to 90% RF		1.8	2.5*	µs

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

* Max switching speed includes multi-path simultaneous switching.

Electrical Specifications

Test conditions unless otherwise stated: all unused RF ports terminated in 50Ω, Input and Output = 50Ω, T = 25°C,

V_{IO}/SDATA/SCLK/SID = 1.8 V / 0 V

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
Insertion Loss					
RFOUT1/2/3-RFIN1/2/3	617 MHz to 960 MHz		0.35		dB
RFOUT1/2/3-RFIN1/2/3	1427 MHz to 2200 MHz		0.5		dB
RFOUT1/2/3-RFIN1/2/3	2300 MHz to 2690 MHz		0.6		dB
RFOUT1/2/3-RFIN1/2/3	3300 MHz to 3800 MHz		0.8		dB
RFOUT1/2/3-RFIN1/2/3	4200 MHz to 5000 MHz		1.1		dB
RFOUT1/2/3-RFIN1/2/3	5000 MHz to 6000 MHz		1.2		dB

PARAMETER	ACTIVE PATH	MEASURED PATH	FREQUENCY (MHZ)	MIN	TYP.	MAX	UNITS
Isolation	RFIN1 – RFOUT1	RFIN1 – RFOUT2					
			617 to 960		43		dB
			1427 to 2200		36		dB
			2300 to 2690		34		dB
			3300 to 4200		31		dB
			4200 to 6000		29		dB
		RFIN1 – RFOUT3	617 to 960		58		dB
			1427 to 2200		52		dB
			2300 to 2690		50		dB
			3300 to 4200		49		dB
			4200 to 6000		47		dB
		RFIN1 – RFIN2	617 to 960		47		dB
			1427 to 2200		41		dB
			2300 to 2690		39		dB
			3300 to 4200		38		dB
			4200 to 6000		35		dB
		RFIN1 – RFIN3	617 to 960		60		dB
			1427 to 2200		54		dB
			2300 to 2690		53		dB
			3300 to 4200		51		dB
			4200 to 6000		44		dB
	RFIN1 – RFOUT2		617 to 960		54		dB
			1427 to 2200		50		dB

Isolation		RFIN1 – RFOUT1	2300 to 2690		50		dB
			3300 to 4200		53		dB
			4200 to 6000		42		dB
		RFIN1 – RFOUT3	617 to 960		53		dB
			1427 to 2200		47		dB
			2300 to 2690		46		dB
			3300 to 4200		44		dB
			4200 to 6000		39		dB
		RFIN1 – RFIN2	617 to 960		42		dB
			1427 to 2200		36		dB
			2300 to 2690		34		dB
			3300 to 4200		32		dB
			4200 to 6000		32		dB
		RFIN1 – RFIN3	617 to 960		53		dB
			1427 to 2200		47		dB
			2300 to 2690		46		dB
			3300 to 4200		45		dB
			4200 to 6000		45		dB
Isolation	RFIN1 – RFOUT3	RFIN1 – RFOUT1	617 to 960		59		dB
			1427 to 2200		53		dB
			2300 to 2690		51		dB
			3300 to 4200		49		dB
			4200 to 6000		42		dB
		RFIN1 – RFOUT2	617 to 960		43		dB
			1427 to 2200		37		dB
			2300 to 2690		35		dB
			3300 to 4200		34		dB
			4200 to 6000		34		dB
		RFIN1 – RFIN2	617 to 960		42		dB
			1427 to 2200		35		dB
			2300 to 2690		33		dB
			3300 to 4200		29		dB
			4200 to 6000		27		dB
		RFIN1 – RFIN3	617 to 960		37		dB
			1427 to 2200		31		dB
			2300 to 2690		29		dB
			3300 to 4200		27		dB
			4200 to 6000		26		dB
		RFIN2 – RFOUT2	617 to 960		39		dB
			1427 to 2200		32		dB
			2300 to 2690		30		dB
			3300 to 4200		28		dB
			4200 to 6000		26		dB
			617 to 960		45		dB

Isolation	RFIN2 – RFOUT1	RFIN2 – RFOUT3	1427 to 2200		39		dB
			2300 to 2690		36		dB
			3300 to 4200		33		dB
			4200 to 6000		29		dB
		RFIN2 – RFIN1	617 to 960		47		dB
			1427 to 2200		41		dB
			2300 to 2690		39		dB
			3300 to 4200		37		dB
			4200 to 6000		37		dB
		RFIN2 – RFIN3	617 to 960		45		dB
			1427 to 2200		39		dB
			2300 to 2690		37		dB
			3300 to 4200		35		dB
			4200 to 6000		35		dB
Isolation	RFIN2 – RFOUT2	RFIN2 – RFOUT1	617 to 960		55		dB
			1427 to 2200		50		dB
			2300 to 2690		50		dB
			3300 to 4200		57		dB
			4200 to 6000		47		dB
		RFIN2 – RFOUT3	617 to 960		44		dB
			1427 to 2200		38		dB
			2300 to 2690		36		dB
			3300 to 4200		33		dB
			4200 to 6000		31		dB
		RFIN2 – RFIN1	617 to 960		39		dB
			1427 to 2200		33		dB
			2300 to 2690		31		dB
			3300 to 4200		29		dB
			4200 to 6000		28		dB
		RFIN2 – RFIN3	617 to 960		43		dB
			1427 to 2200		37		dB
			2300 to 2690		35		dB
			3300 to 4200		33		dB
			4200 to 6000		34		dB
Isolation	RFIN2 – RFOUT3	RFIN2 – RFOUT1	617 to 960		59		dB
			1427 to 2200		54		dB
			2300 to 2690		53		dB
			3300 to 4200		51		dB
			4200 to 6000		44		dB
		RFIN2 – RFOUT2	617 to 960		45		dB
			1427 to 2200		39		dB
			2300 to 2690		38		dB
			3300 to 4200		36		dB
			4200 to 6000		38		dB

Isolation		RFIN2 – RFIN1	617 to 960		46		dB
			1427 to 2200		40		dB
			2300 to 2690		38		dB
			3300 to 4200		37		dB
			4200 to 6000		38		dB
		RFIN2 – RFIN3	617 to 960		35		dB
			1427 to 2200		29		dB
			2300 to 2690		27		dB
			3300 to 4200		25		dB
			4200 to 6000		25		dB
	RFIN3 – RFOUT1	RFIN3 – RFOUT2	617 to 960		48		dB
			1427 to 2200		43		dB
			2300 to 2690		42		dB
			3300 to 4200		42		dB
			4200 to 6000		44		dB
		RFIN3 – RFOUT3	617 to 960		38		dB
			1427 to 2200		32		dB
			2300 to 2690		30		dB
			3300 to 4200		28		dB
			4200 to 6000		28		dB
Isolation		RFIN3 – RFIN1	617 to 960		60		dB
			1427 to 2200		55		dB
			2300 to 2690		55		dB
			3300 to 4200		55		dB
			4200 to 6000		49		dB
		RFIN3 – RFIN2	617 to 960		45		dB
			1427 to 2200		39		dB
			2300 to 2690		37		dB
			3300 to 4200		36		dB
			4200 to 6000		36		dB
	RFIN3 – RFOUT2	RFIN3 – RFOUT1	617 to 960		54		dB
			1427 to 2200		49		dB
			2300 to 2690		49		dB
			3300 to 4200		50		dB
			4200 to 6000		46		dB
		RFIN3 – RFOUT3	617 to 960		38		dB
			1427 to 2200		32		dB
			2300 to 2690		30		dB
			3300 to 4200		29		dB
Isolation			4200 to 6000		30		dB
		RFIN3 – RFIN1	617 to 960		43		dB
			1427 to 2200		37		dB
			2300 to 2690		35		dB
			3300 to 4200		32		dB

Isolation			4200 to 6000		32		dB
		RFIN3 – RFIN2	617 to 960		42		dB
			1427 to 2200		35		dB
			2300 to 2690		33		dB
			3300 to 4200		31		dB
			4200 to 6000		31		dB
	RFIN3 – RFOUT3	RFIN3 – RFOUT1	617 to 960		59		dB
			1427 to 2200		53		dB
			2300 to 2690		52		dB
			3300 to 4200		51		dB
			4200 to 6000		47		dB
		RFIN3 – RFOUT2	617 to 960		50		dB
			1427 to 2200		44		dB
			2300 to 2690		43		dB
			3300 to 4200		43		dB
			4200 to 6000		44		dB
		RFIN3 – RFIN1	617 to 960		60		dB
			1427 to 2200		54		dB
			2300 to 2690		52		dB
			3300 to 4200		49		dB
			4200 to 6000		46		dB
		RFIN3 – RFIN2	617 to 960		41		dB
			1427 to 2200		34		dB
			2300 to 2690		32		dB
			3300 to 4200		30		dB
			4200 to 6000		28		dB

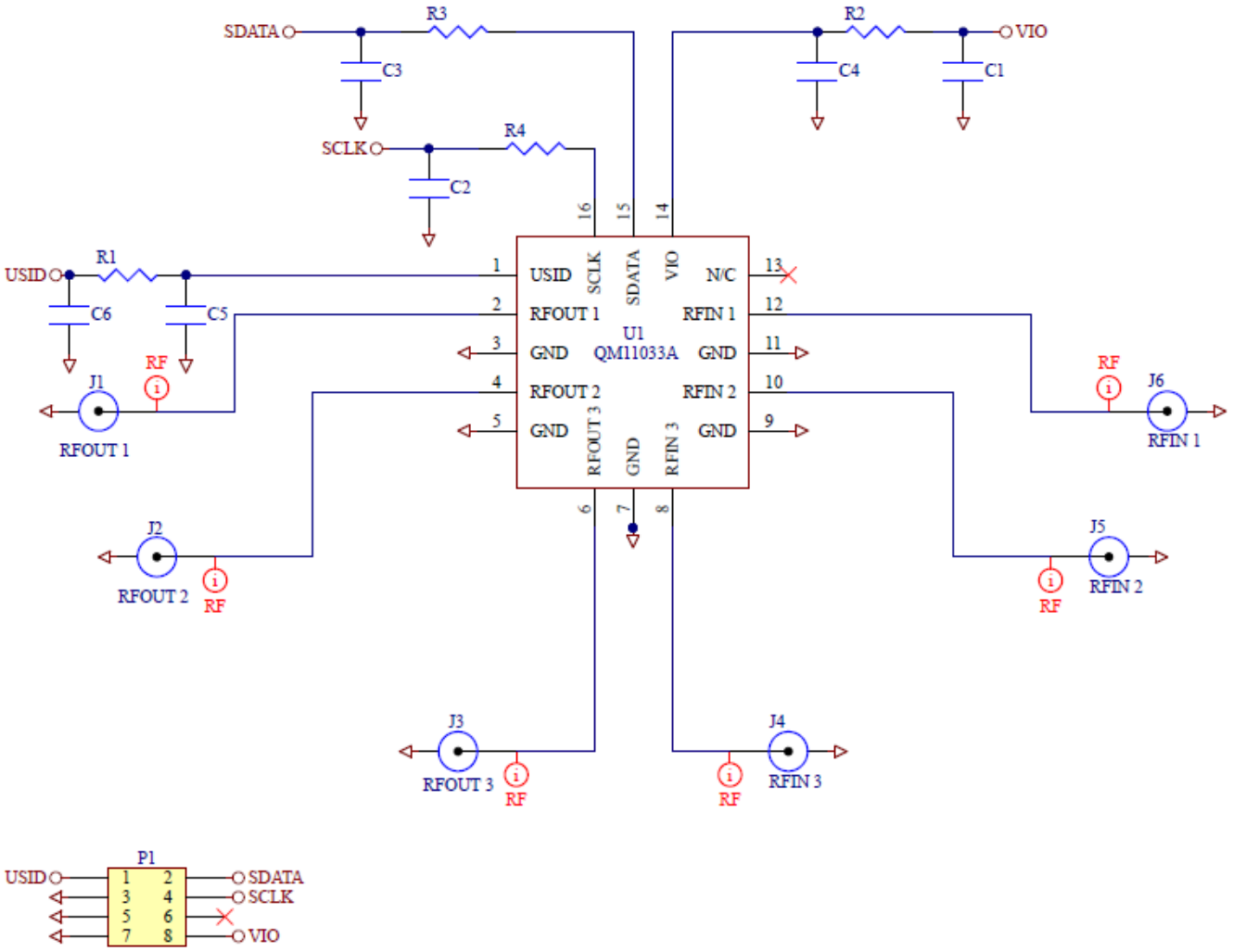
PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
VSWR					
Input/Output VSWR	699 MHz to 960 MHz		1.15		:1
	1427 MHz to 2200 MHz		1.3		:1
	2300 MHz to 2690 MHz		1.4		:1
	3300 MHz to 4200 MHz		1.6		:1
	4200 MHz to 6000 MHz		2.2		:1

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
Harmonics	**VSWR 1:1**				
2nd Harmonic	Freq = 617-960MHz; P_{IN} = 26dBm		-85		dBm
3rd Harmonic			-85		dBm
≥ 4th Harmonic			-120		dBm
2nd Harmonic	Freq = 1710-2170MHz; P_{IN} = 26dBm		-78		dBm
3rd Harmonic			-78		dBm
≥ 4th Harmonic			-120		dBm
2nd Harmonic	Freq = 2300-2690MHz; P_{IN} = 26dBm		-78		dBm
3rd Harmonic			-78		dBm
≥ 4th Harmonic			-120		dBm
2nd Harmonic	Freq = 3300-3800MHz; P_{IN} = 26dBm		-69		dBm
3rd Harmonic			-72		dBm
≥ 4th Harmonic			-100		dBm
2nd Harmonic	Freq = 3800-4200MHz; P_{IN} = 26dBm		-70		dBm
3rd Harmonic			-75		dBm
≥ 4th Harmonic			-100		dBm
2nd Harmonic	Freq = 4400-5000MHz; P_{IN} = 26dBm		-66		dBm
3rd Harmonic			-74		dBm
≥ 4th Harmonic			-100		dBm

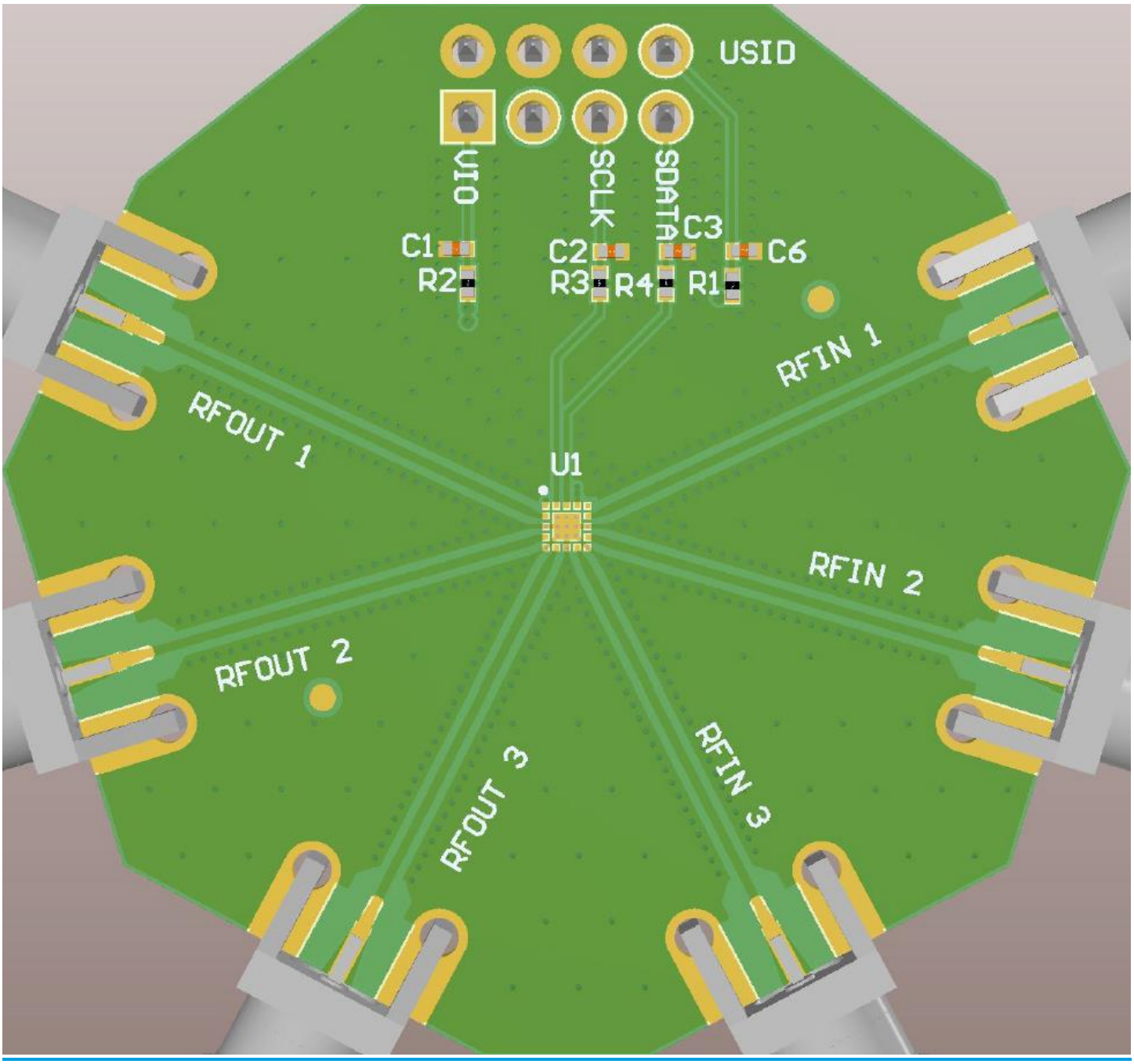
PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
Standard IMD					
2nd Order intermodulation	CW P1 1950 MHz @20dBm, CW P2 190 MHz, 4090MHz @ -15 dBm		-120		dBm
	CW P1 @ 835 MHz @20 dBm CW P2 @ 45 MHz , 1715 MHz @-15 dBm		-128		dBm
	CW P1 @ 2535 MHz @20 dBm CW P2 @ 120 MHz @-15 dBm		-123		dBm
3rd Order intermodulation	CW P1 1950 MHz @20 dBm, CW P2 1760 MHz @ -15 dBm		-123		dBm
	CW P1 835 MHz @20 dBm, CW P2 790 MHz @ -15 dBm		-128		dBm
	CW P1 @ 2535 MHz @20 dBm CW P2 @ 2415 MHz @-15 dBm		-121		dBm

PARAMETER	CONDITIONS	MIN	TYP.	MAX	UNITS
2 Tx IMD					
2nd Order intermodulation	CW P1 @ 2560 MHz @ 26dBm CW P2 @ 3500 MHz @ 26dBm		-95		dBm
	CW P1 @ 1960 MHz @ 26dBm CW P2 @ 3500 MHz @ 26dBm		-100		dBm
	CW P1 @ 890 MHz @ 26dBm CW P2 @ 3500 MHz @ 26dBm		-94		dBm
	CW P1 @ 1960 MHz @ 26dBm CW P2 @ 2600 MHz @ 26dBm		-100		dBm
	CW P1 @ 890 MHz @ 26dBm CW P2 @ 2600 MHz @ 26dBm		-95		dBm
	CW P1 @ 890 MHz @ 26dBm CW P2 @ 1970 MHz @ 26dBm		-90		dBm
3rd Order intermodulation	CW P1 @ 3400 MHz @ 26dBm CW P2 @ 3500 MHz @ 26dBm		-90		dBm
	CW P1 @ 2560 MHz @ 26dBm CW P2 @ 3500 MHz @ 26dBm		-120		dBm
	CW P1 @ 1960 MHz @ 26dBm CW P2 @ 2600 MHz @ 26dBm		-110		dBm
	CW P1 @ 890 MHz @ 26dBm CW P2 @ 1970 MHz @ 26dBm		-120		dBm

Application Circuit Schematic



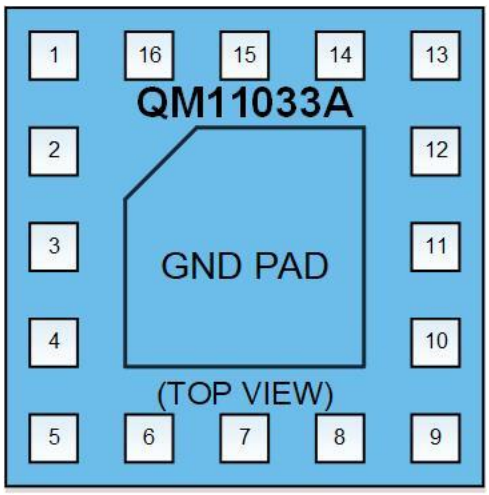
Evaluation Board Layout



Pin Description

PIN	LABEL	DESCRIPTION
1	USID	MIPI Control
2	RFOUT 1	RF Path
3	GND	Ground
4	RFOUT 2	RF Path
5	GND	Ground
6	RFOUT 3	RF Path
7	GND	Ground
8	RFIN 3	RF Path
9	GND	Ground
10	RFIN 2	RF Path
11	GND	Ground
12	RFIN 1	RF Path
13	N/C	No Connection
14	VIO	MIPI Control
15	SDATA	MIPI Control
16	SCLK	MIPI Control

Pin Configuration



Register Configuration

Register 0x0000 – SW_CTRL_0

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/WM
7:6	SPARE	Reserved for future use	0x0	No	0 and 1 and/or 2	R/WM
5:3	Input_Sel_2	Input port 2 routing 000: connect to none 001: connect to OUT port 1 010: connect to OUT port 2 011: connect to OUT port 3 100: connect to OUT port 1,2 101: connect to OUT port 2,3 110: connect to OUT port 1,3 111: connect to OUT port 1,2.3	0x0	No	0 and 1 and/or 2	R/WM
2:0	Input_Sel_1	Input port 1 routing 000: connect to none 001: connect to OUT port 1 010: connect to OUT port 2 011: connect to OUT port 3 100: connect to OUT port 1,2 101: connect to OUT port 2,3 110: connect to OUT port 1,3 111: connect to OUT port 1,2.3	0x0	No	0 and 1 and/or 2	R/WM
		Note: See Truth Table for example of operation				

Register 0x0001 – SW_CTRL_1

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/WM
7:3	SPARE	Reserved for future use	0x00	No	0 and 1 and/or 2	R/WM
2:0	Input_Sel_3	Input port 3 routing 000: connect to none 001: connect to OUT port 1 010: connect to OUT port 2 011: connect to OUT port 3 100: connect to OUT port 1,2 101: connect to OUT port 2,3 110: connect to OUT port 1,3 111: connect to OUT port 1,2.3	0x0	No	0 and 1 and/or 2	R/WM

		Note: See Truth Table for example of operation				

Register 0x001A – RFFE_STATUS

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	UDR_RST	Setting this bit initiates a software reset *Note: On software reset, this register and all User Defined registers (UDRs) are reset. This bit will always read as 0.*	0	No	No	W
6	CMD_FR_P_ERR	Command Frame received with a parity error	0	No	No	R/W
5	CMD_LEN_ERR	Command Sequence received with an incorrect length	0	No	No	R/W
4	ADDR_FR_P_ERR	Address Frame received with a parity error	0	No	No	R/W
3	DATA_FR_P_ERR	Data Frame received with a parity error	0	No	No	R/W
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	0	No	No	R/W
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	0	No	No	R/W
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	0	No	No	R/W
		Note: Reading this register resets this register.				

Register 0x001B – GSID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	GSID0[3:0]	Group Slave ID0	0x0	No	No	R/W
3:0	GSID1[3:0]	Group Slave ID1	0x0	No	No	R/W

Register 0x001C – PM_TRIG

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	PWR_MODE[1]	0: Normal Operation 1: Low Power - Antenna in isolation	1	B/G	No	R/W
6	PWR_MODE[0]	0: ACTIVE 1: STARTUP - Reset all registers to default settings *Note: Setting PWR_MODE to STARTUP is identical to a hardware reset initiated by the VIO signal.*	0	B/G	No	R/W
5:3	TriggerMask[2:0]	Setting bit TriggerMask[N] disables Trigger[N] TriggerMask[N] updates before Trigger[N] is processed	0b000	No	No	R/W

		Note: When Trigger[N] is disabled, writing to a register associated with Trigger[N] sends data directly to that register. *If a register is associated with multiple triggers, then all associated triggers must be disabled to allow direct writes to the associated register.*				
2:0	Trigger[2:0]	Setting bit Trigger[N] loads Trigger[N]'s associated registers *Note 1: When Trigger[N] is enabled, writing to a register associated with Trigger[N] sends data to that register's shadow. Setting the Trigger[N] bit loads data from shadow. All triggers are processed immediately and simultaneously and then cleared. Trigger[0], [1], and [2] will always read as 0.* *Note 2: : Use Trigger[0] along with Triggers[1] and/or Trigger[2]*	0b000	B/G	No	W

Register 0x001D – PRODUCT_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	PROD_ID[7:0]	Lower eight bits of Product Number *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x29	No	No	R

Register 0x001E – MANUFACTURER_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	MFG_ID[7:0]	Lower eight bits of MIPI Manufacturer ID *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0xC6	No	No	R

Register 0x001F – MAN_USID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	MFG_ID[11:8]	Upper four bits of MIPI Manufacturer ID *Note: This is a read-only register. However, as part of the special programming sequence for writing USID, a write command sequence is performed on this register, but does not update it. See MIPI 6.6.2 for details.*	0x3	No	No	R
3:0	USID[3:0]	Programmable Unique Slave ID	0x6	No	No	R/W

The default value at reset is selected via pin SID0.

SID0	USID
0	0x6
1	0x7

Note: USID is only writeable using a special programming sequence. See MIPI 6.6.2 for details.

Register 0x0020 – EXT_PRODUCT_ID

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	PROD_ID[15:8]	Upper eight bits of Product Number *Note: These are read-only registers. However, as part of the special programming sequence for writing USID, a write command sequence is performed on one or both registers, but does not update them. See MIPI 6.6.2 for details.*	0x00	No	No	R

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:6	MAJOR_REV[1:0]	Major Revisions - all layer	0b00	No	No	R
5:4	MINOR_REV[1:0]	Minor Revisions - metal only	0b00	No	No	R
3:0	MISC_REV[3:0]	Misc Revisions - mask variants	0b0001	No	No	R
		Note: The REVISION_ID register contains this product's revision number which is set by Qorvo according to manufacture date. The value may change throughout the product life cycle.				

Register 0x0022 – GSID0-1

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:4	GSID0[3:0]	Group Slave ID0	0x0	No	No	R/W
3:0	GSID1[3:0]	Group Slave ID1	0x0	No	No	R/W

Register 0x0023 – UDR_RST

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	UDR_RST	Setting this bit initiates a software reset *Note: On software reset, this register and all User Defined registers (UDRs) are reset. This bit will always read as 0.*	0	B/G	No	W
6:0	RESERVED		0x00	No	No	R

Register 0x0024 – ERR_SUM

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7	SPARE	Reserved for future use	0	No	No	R/W
6	CMD_FR_P_ERR	Command Frame received with a parity error	0	No	No	R/W
5	CMD_LEN_ERR	Command Sequence received with an incorrect length	0	No	No	R/W
4	ADDR_FR_P_ERR	Address Frame received with a parity error	0	No	No	R/W
3	DATA_FR_P_ERR	Data Frame received with a parity error	0	No	No	R/W
2	RD_INVLD_ADDR	Read Command Sequence received with an invalid address	0	No	No	R/W
1	WR_INVLD_ADDR	Write Command Sequence received with an invalid address	0	No	No	R/W
0	BID_GID_ERR	Read Command Sequence received with a BSID or GSID	0	No	No	R/W
		Note: Reading this register resets this register.				

Register 0x002C – TEST_PATT

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	TEST_PATT[7:0]	Test Pattern	0xD2	No	No	R

Register 0x002D – EXT_TRIG_MASK

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	TriggerMask[10:3]	Setting bit TriggerMask[N] disables Trigger[N] If using an Extended Write to update both TriggerMask and Trigger, than TriggerMask[N] updates before Trigger[N] is processed *Note: Extended Triggers do not cause state change.*	0x00	No	No	R/W

Register 0x002E – EXT_TRIG

Bit(s)	Field Name	Description	Reset	B/G	Trig	R/W
7:0	Trigger[10:3]	Setting bit Trigger[N] loads Trigger[N]'s associated registers	0x00	B/G	No	W

Note: Extended Triggers do not cause state change.
Trigger[10 - 3] will always read as 0.

Truth Table

sw_decoder_1		
IN port	OUT port	reg_00[2:0]
		in_decoder[2:0]
1	NONE	000
1	1	001
1	2	010
1	3	011
1	1,2	100
1	2,3	101
1	1,3	110
1	1,2,3	111

sw_decoder_2		
IN port	OUT port	reg_00[5:3]
		in_decoder[2:0]
2	NONE	000
2	1	001
2	2	010
2	3	011
2	1,2	100
2	2,3	101
2	1,3	110
2	1,2,3	111

sw_decoder_3		
IN port	OUT port	reg_01[2:0]
		in_decoder[2:0]
3	NONE	000
3	1	001
3	2	010
3	3	011
3	1,2	100
3	2,3	101
3	1,3	110
3	1,2,3	111

Power On and Off Sequence

It is very important that the user adheres to the correct timing sequences in order to avoid damaging the device. Figures are NOT drawn to scale.

1. Once VIO is powered down to 0V, wait a minimum of 10 µs to reapply power to VIO. (see Figure: Digital Supply Detail)

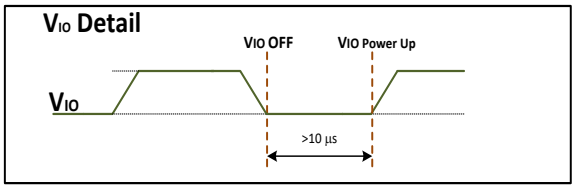


Figure: Digital Supply Detail

2. VIO must be applied for a minimum of 120 ns before sending SDATA/SCLK to ensure correct data transmission. (see Figure: RF Power-Up Detail)
3. VIO must be applied for a minimum of 15 µs before applying RF power. (see Figure: Digital Signal / RF Power-On Detail)
4. Wait a minimum of 5 µs after RFFE bus is idle to apply an RF signal. (see Figure: RF Power-Up Detail)

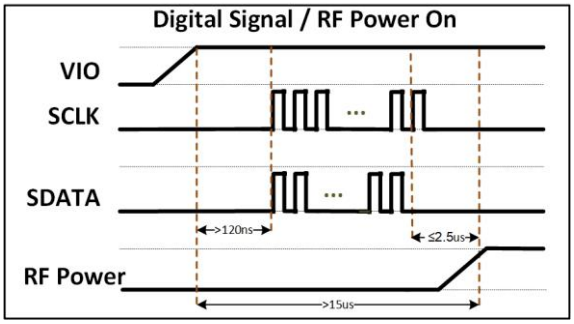


Figure: Digital Signal / RF Power-On Detail

5. RF power must not be applied during switching events. To ensure this, remove RF power before completing a register write that will change the switch mode. (see Figure: Switch Event Timing)

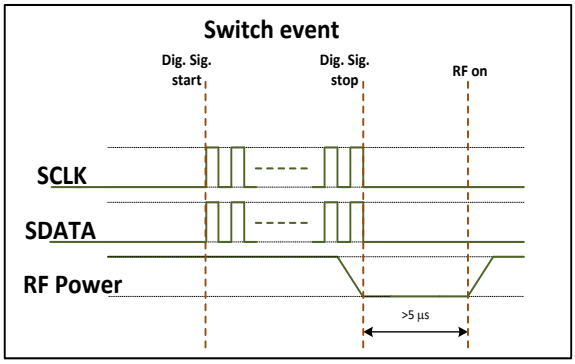


Figure: Switch Event Timing

6. If “Low Power Mode” is utilized, there must be a delay of 10 µs before exiting “Low Power Mode”. (see Figure: Low-Power Mode Exit Timimg)

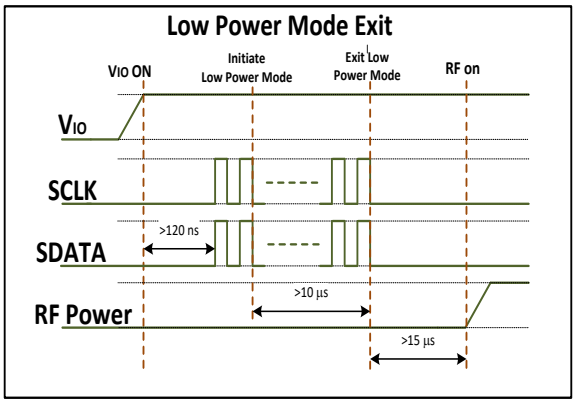
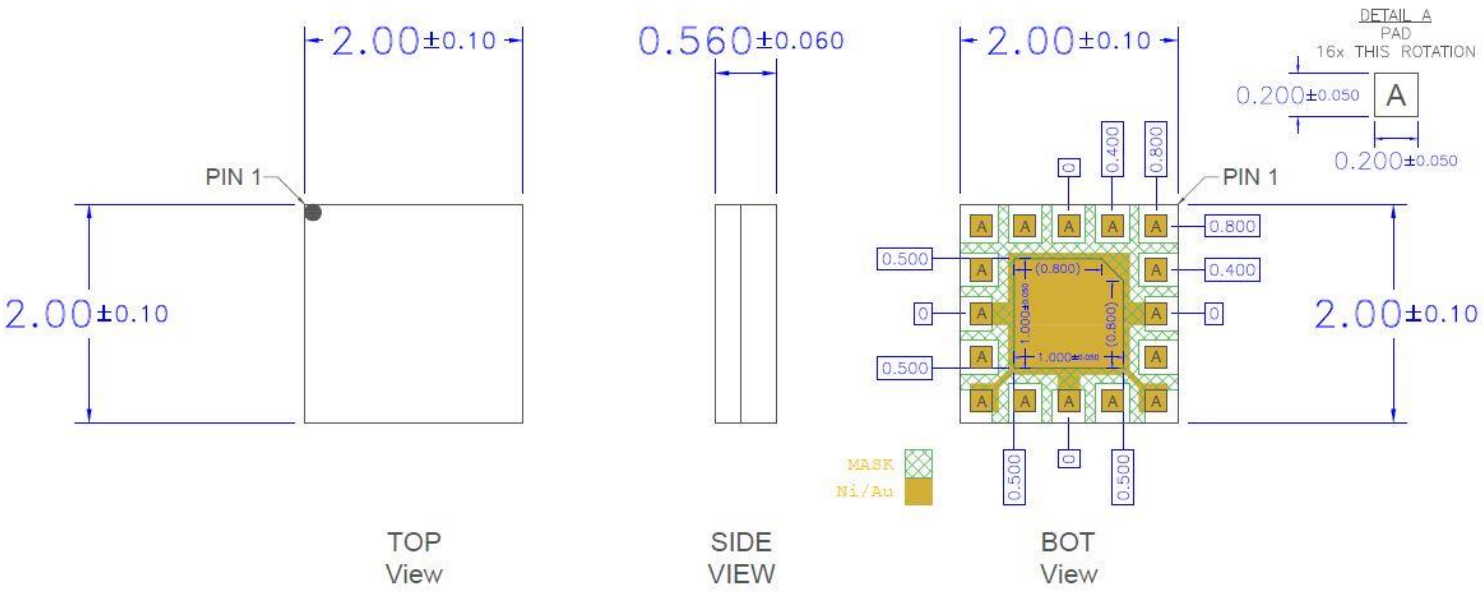
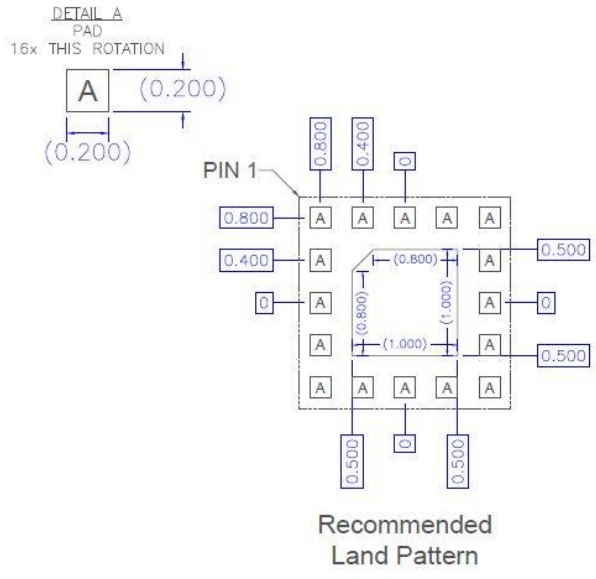


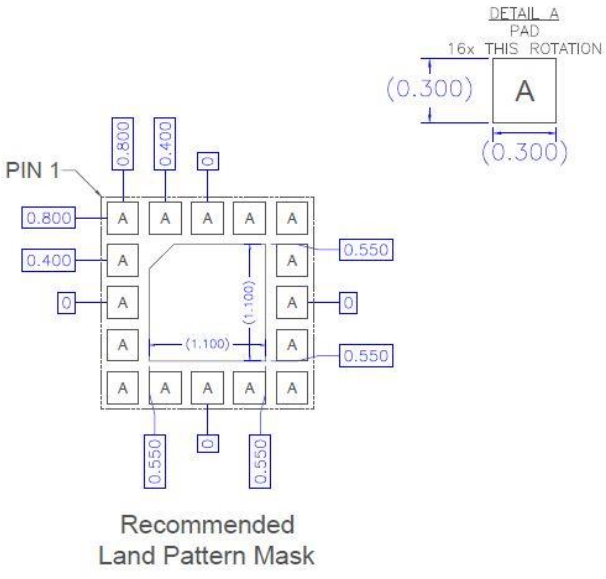
Figure: Low-Power Mode Exit Timing

Mechanical Drawing

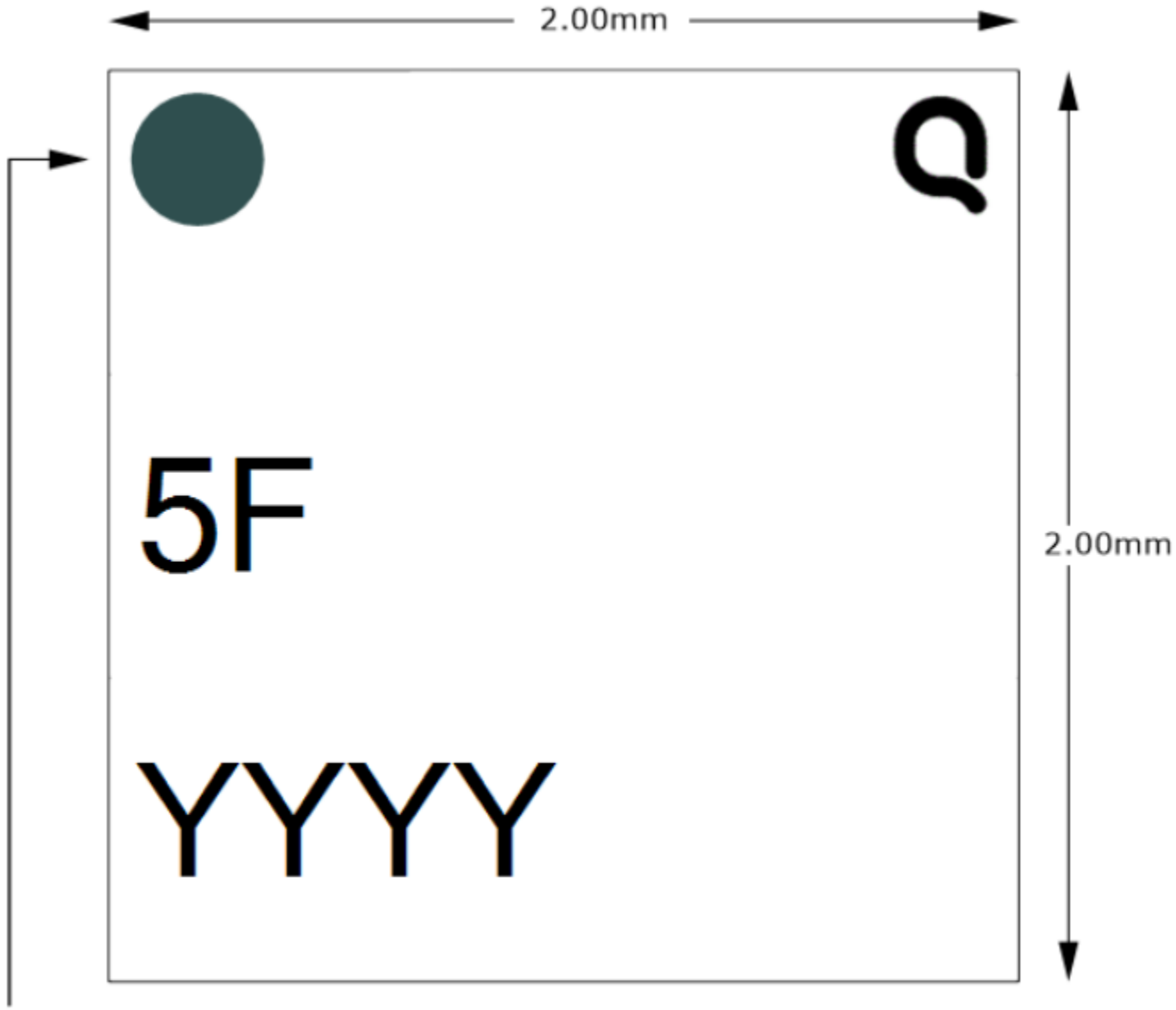


PCB Drawing Requirements





Branding Diagram



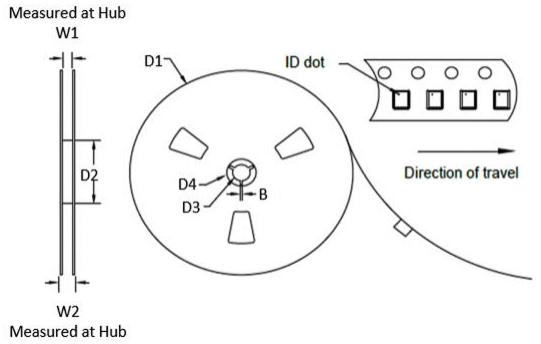
Pin 1 Indicator

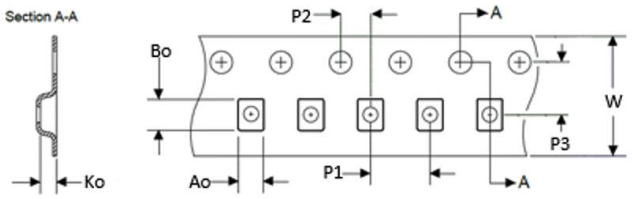
Qorvo Logo - Use Q5D

Trace Code to be assigned by SubCon

5F is the Product Code
YYYY is the Trace Code

Tape and Reel Information





Feature	Measure	Symbol	Size (mm)
Flange	Diameter	D1	330.0
	Thickness	W2	18.2
	Space Between Flange	W1	12.8
Hub	Outer Diameter	D2	102.0
	Arbor Hole Diameter	D3	13.0
	Key Slit Width	B	2.0
	Key Slit Diameter	D4	20.2

Feature	Measure	Symbol	Size (mm)
Cavity	Length	Ao	2.20
	Width	Bo	2.20
	Depth	Ko	0.95
	Pitch	P1	4.0
Centerline Distance	Cavity to Perforation (Length)	P2	2.0
	Cavity to Perforation (Width)	P3	5.5
Carrier Tape	Width	W	12.0

(Unless otherwise specified, all dimension tolerances per EIA-481)

Handling Precautions

Parameter	Rating	Standard
ESD – Human Body Model (HBM)	Class 2	ANSI/ESD/JEDEC JS-001
ESD – Charged Device Model (CDM)	Class C3	ANSI/ESD/JEDEC JS-002
MSL – Moisture Sensitivity Level	Level 3	IPC/JEDEC J-STD-020

Caution!

ESD sensitive device

Solderability

Compatible with both lead-free (260 °C INFIN TYP reflow temperature) and tin/lead (245 °C INFIN TYP reflow temperature) soldering processes.

Package lead plating: Electrolytic plated Au over Ni

RoHS Compliance

This part is compliant with the 2011/65/EU RoHS directive (Restrictions on the Use of Certain Hazardous Substances in Electrical and Electronic Equipment), as amended by Directive 2015/863/EU.

This product also has the following attributes:

- Lead free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_4O_2$) Free
- SVHC Free

Revision History

Revision	Description
H	Initial Production Release
I	Updated Switching Time Description
J	Updated data with limits and extreme data
K	Updated Harmonics data
L	Added Input to Input Isolation, Added Harmonics by path on focus areas, Added Matching Data
M	Updated Matched data for RFOUT1 paths
N	Updated Register Map Trigger usage
O	Updated Timing Diagram and limits
P	Updated Switching Speed with Multipath Info

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations:

Web: www.qorvo.com

Tel: 1-844-890-8163

Email: customer.support@qorvo.com

Important Notice