

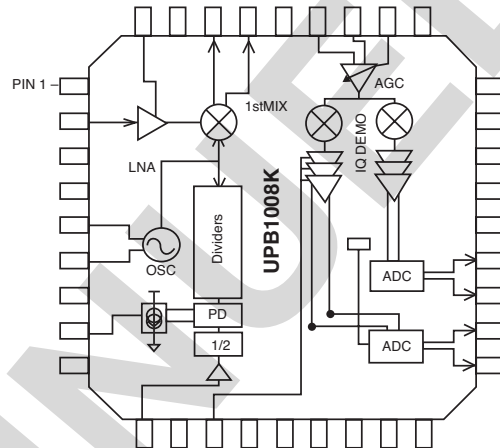
### FEATURES

- **LOW POWER CONSUMPTION:** 52 mW
- **DUAL-CONVERSION IQ DOWN CONVERTER<sup>1</sup>:**  
Reference frequency: REF<sub>in</sub> = 27 MHz
- **PSEUDO-BASEBAND WITH 2-BIT DIGITIZED OUTPUT**
- **ON-CHIP LNA, ON-CHIP FREQUENCY SYNTHESIZER,  
IF AGC AMPLIFIER:**  
with 45 dB typical range of adjustable gain
- **SMALL 36 PIN QFN PACKAGE:**  
Flat lead style for better RF performance

Note:

1. Based on eRide's proprietary GPS DSP architecture

### BLOCK DIAGRAM



### APPLICATIONS

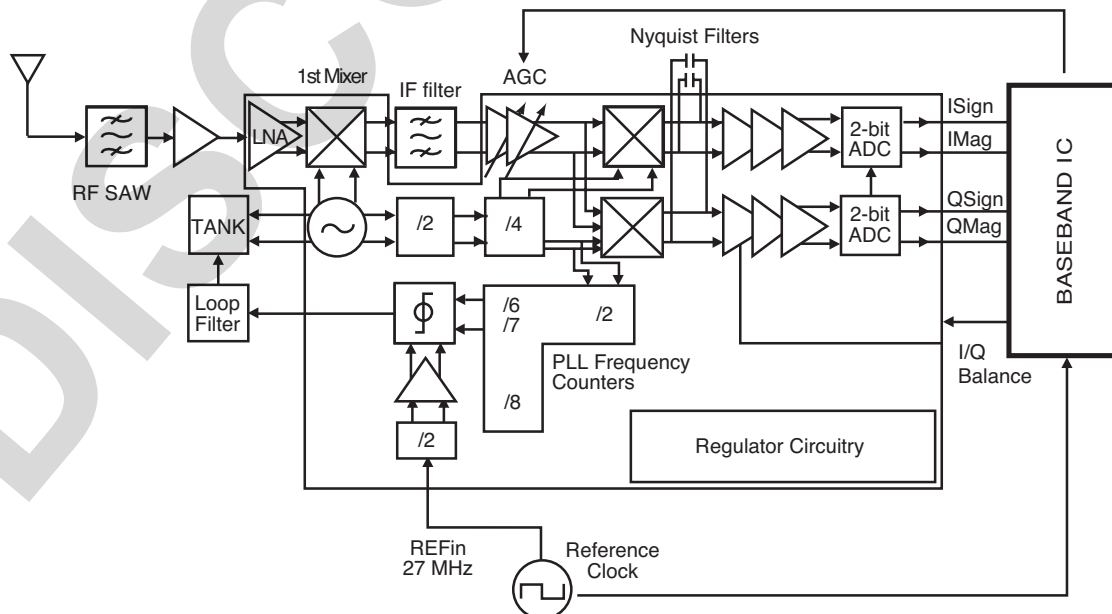
- **E911 ENABLED MOBILE PHONE**
- **IN-VEHICLE NAVIGATION SYSTEMS**
- **LOW POWER HANDHELD GPS RECEIVER**
- **PC/PDA+GPS INTEGRATION**
- **ASSET TRACKING**

### DESCRIPTION

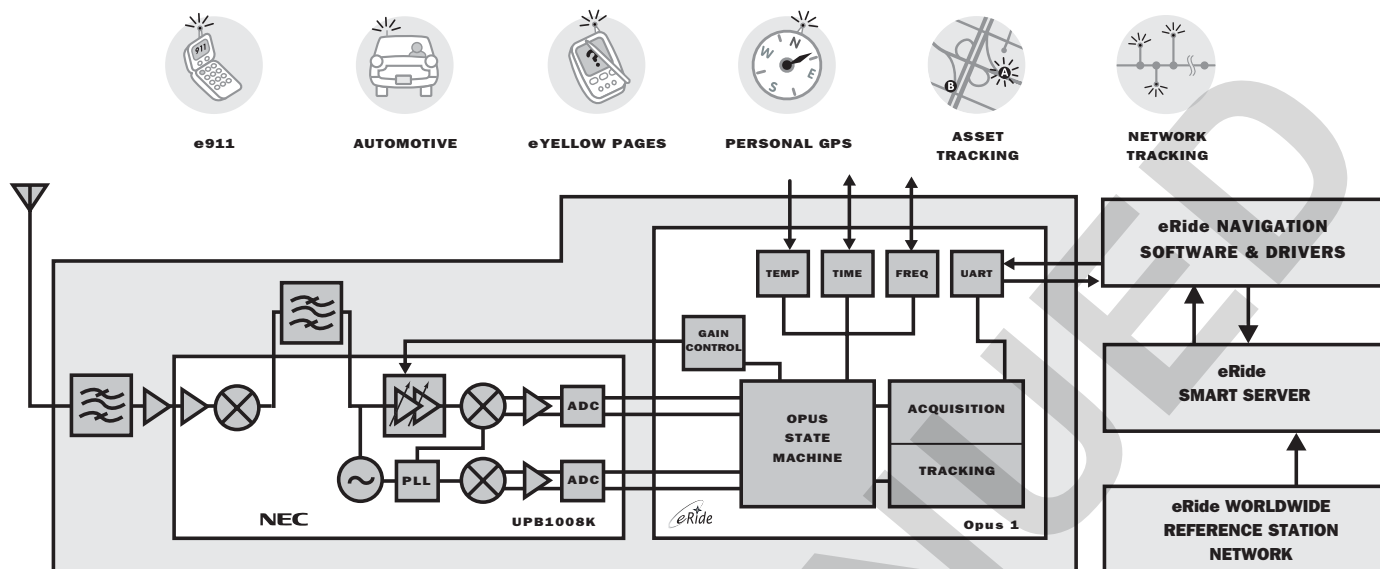
NEC's UPB1008K is a Silicon RFIC especially designed for handheld low power/low cost GPS receivers. The IC combines an LNA, followed by a double-conversion RF/IF downconverter block and a PLL frequency synthesizer on one chip. The second IF Frequency is a pseudo-baseband signal into a on-chip 2-bit A/D converters. The device can operate on a supply voltage as low as 2.7 V, and is housed in a small 36 pin QFN (Quad, Flat, No-lead) package, resulting in a very low power consumption and reduced board space.

NEC's stringent quality assurance and test procedures ensure the highest reliability and performance.

### RF APPLICATION DIAGRAM



## ADVANCED GPS COMPLETE SOLUTION



### ADVANCED GPS COMPLETE SOLUTION

"NEC Corporation and eRide, Inc. have teamed to provide an advanced positioning solution delivering high GPS performance, accuracy, integration and architecture flexibility. The chip set combines CEL's **UPB1008K** receiver IC with eRide's **Opus One** SOC (System-on-a-Chip) Baseband ASIC and is suitable for standard GPS products as well as Cellular Handset applications. Also provided are scalable client navigation software and drivers, plus location-aiding data from eRide's Smart Server. Together, they offer a complete hardware/infrastructure solution.

The chip set's design allows it to operate independently of wireless interface standards - and independently of the host product's CPU and Operating System. This unique approach to system integration makes it easy to deploy the chip set into an wireless application, in any wireless network. A "Universal Hardware" solution, the design promises lower manufacturing costs and, ultimately lower cost to the consumer.

The chip set's advanced positioning architecture offers unmatched sensitivity providing fast, accurate positioning architecture offers unmatched sensitivity providing fast and accurate position fixes, even when indoors or in deep in urban canyons."

### HIGH PERFORMANCE GPS OMNI MODE

LI, C/A code receiver

Performance	Indoor	Outdoor
Time to First Fix w/ aiding	5-7sec	1-3sec
Time to First Fix w/o aiding	10-20sec	3-5sec
Accuracy	10-25m cep	2-5m cep
Sensitivity	-155dBm in 1sec dwells	-142dBm in two 10msec dwells

Superior performance in high reflection indoor environments and in urban canyon types of outdoor environments

### POWER DISSIPATION

First Fix	400 mW
Tracking	200-300 mW
Stand By	30 mW

**ELECTRICAL CHARACTERISTICS** (TA = 25°C, VCC = 3.0 V, unless otherwise specified)

SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
Icc	Total Circuit Current, No Signals	mA	14	18	23.5
Vcc	Supply Voltage	V	2.7	3.0	3.3
Icc_PD	Power down current, PIN 13 = VIL	μA	–	1	10
Icc_rf	RF Block Circuit Current (pin 3), No signal	μA	0.4	0.5	0.7
Icc_lo	VCO Block Circuit Current (pin 7), No signal	mA	4.1	5.6	7.2
Icc_pll	PLL Block Circuit Current (pin 9), No signal	mA	2.7	3.6	4.7
Icc_bb	Baseband Block Circuit Current (pin 23), No signal, open load	mA	2.5	3.4	4.3
Icc_if	IF Block Circuit Current (pin 28) , No signal	mA	2.7	3.7	4.7
Icc_ina	Pre-Amplifier Open Connector Current (pin 36), No signal	mA	1.0	1.4	1.8

**LNA/RF DOWNCONVERTER**

(fRFIn = 1575.42 MHz, f1stLOin = 1400 MHz, PLO = -10 dBm, f1stIF = 175 MHz, Pin 13: VIL = 3 V, ZL differential = 32Ω & Zs = Γopt)

SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
CGLNA_MIX	Power conversion gain from 2nd LNA/mixer to 1st IF, P <sub>RFIn</sub> = -50 dBm	dB	18	23	28
NFLNA_MIX	Noise Figure of 2nd LNA/mixer(SSB), Input matched	dB	–	5	–
P1dB <sub>LNA_MIX</sub>	1 dB Compression refer to source, Input matched	dBm	–	-38	–
ZLNAin	RF Input Impedance of LNA	Ohm	–	31	–
ZMIXout	IF Output Impedance of Mixer	Ohm	–	32	–
ALO-IF	Local Signal Leak to IF, f1stLOin=1400 MHz, PLO = 0 dBm	dBm	–	-35	–
ALO-RF	Local Signal Leak to RF, f1stLOin=1400 MHz, PLO = 0 dBm	dBm	–	-50	–

**PLL**

SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
ICPOH	PLL Charge Pump High Side Current @ VCPout = VCC/2	μA	–	200	–
ICPOL	PLL Charge Pump Low Side Current @ VCPout = VCC/2	μA	–	-200	–
fPD	Phase Comparison Frequency	MHz	–	13.5	–

**CRYSTAL OSCILLATOR/REFERENCE AMPLIFIER BLOCK**

SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
VREFin	Reference input minimum level	mVpp	50	200	–
fREF	Input Frequency of Reference Input	MHz	–	27	–
VT	VCO Control Voltage, PLL Locked	V	0.8	1.5	2.2
C/N	VCO C/N, Δ1kHz, Loop band width = 5 kHz	dBc/Hz	57	62	–

**AGC AMPLIFIER, I-Q DEMODULATOR, and ADC BLOCK**(f1stFin = 175 MHz, Zin = 600Ω)

SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
CGAGC/MIX	Maximum voltage conversion gain of AGC amplifier/ I-Q mixer, Pin = -60 dBm, VAGC = 0.5 V, Unmatched	dB	–	30	–
	Minimum voltage conversion gain of AGC amplifier/ I-Q mixer, Pin = -60 dBm, VAGC = 2.0 V, Unmatched	dB	–	-15	–
AAGC/MIX	AGC control range, VAGC = 0.5 V to 2 V	dB	25	45	–
P1dBAGC	1 dB compression input to AGC amplifier, set voltage gain = 30 dB	dBm	–	-45	–
VAGC	AGC control voltage	V	0.5	–	2.0
BW	3dB Mixer Bandwidth	MHz	–	10	–
VIQ-c	IQ BalanceControl Voltage, Gain(Ich) = Gain(Qch)	V	–	2.1	2.8
AIQ-c	IQ Balance Control Gain Range, VIQ-c = 0 to 3 V	dB	4.0	6.5	–
Duty Ich	Ich Mag Bit Output Pulse Duty, P1stIFin = -84 dBm VAGC = 0.5 V, VIQ-c = 0 V	%	50	–	–
Duty Qch	Qch Mag Bit Output Pulse Duty, PIF2in = -88 dBm VAGC = 0.5 V, VIQ-c = 0 V	%	50	–	–

**BASEBAND AMPLIFIER BLOCK** (Zs = 2kΩ & ZL = 2 kΩ)

SYMBOLS	PARAMETERS AND CONDITIONS	UNITS	MIN	TYP	MAX
VBOH	Baseband output logic high, CL = 10 pF	V	2.0	–	–
VBOL	Baseband output logic low, CL = 10 pF	V	0	–	0.5

### ABSOLUTE MAXIMUM RATINGS<sup>1,2</sup> (TA = 25°C)

SYMBOLS	PARAMETERS	UNITS	RATINGS
Vcc	Supply Voltage <sup>4</sup>	Vcc	3.6
PD	Total Power Dissipation <sup>3</sup>	mW	361
TOP	Operating Temperature	°C	-40 to +85
TSTG	Storage Temperature	°C	-55 to +150
ICC_total	Total Circuit Current <sup>4</sup>		

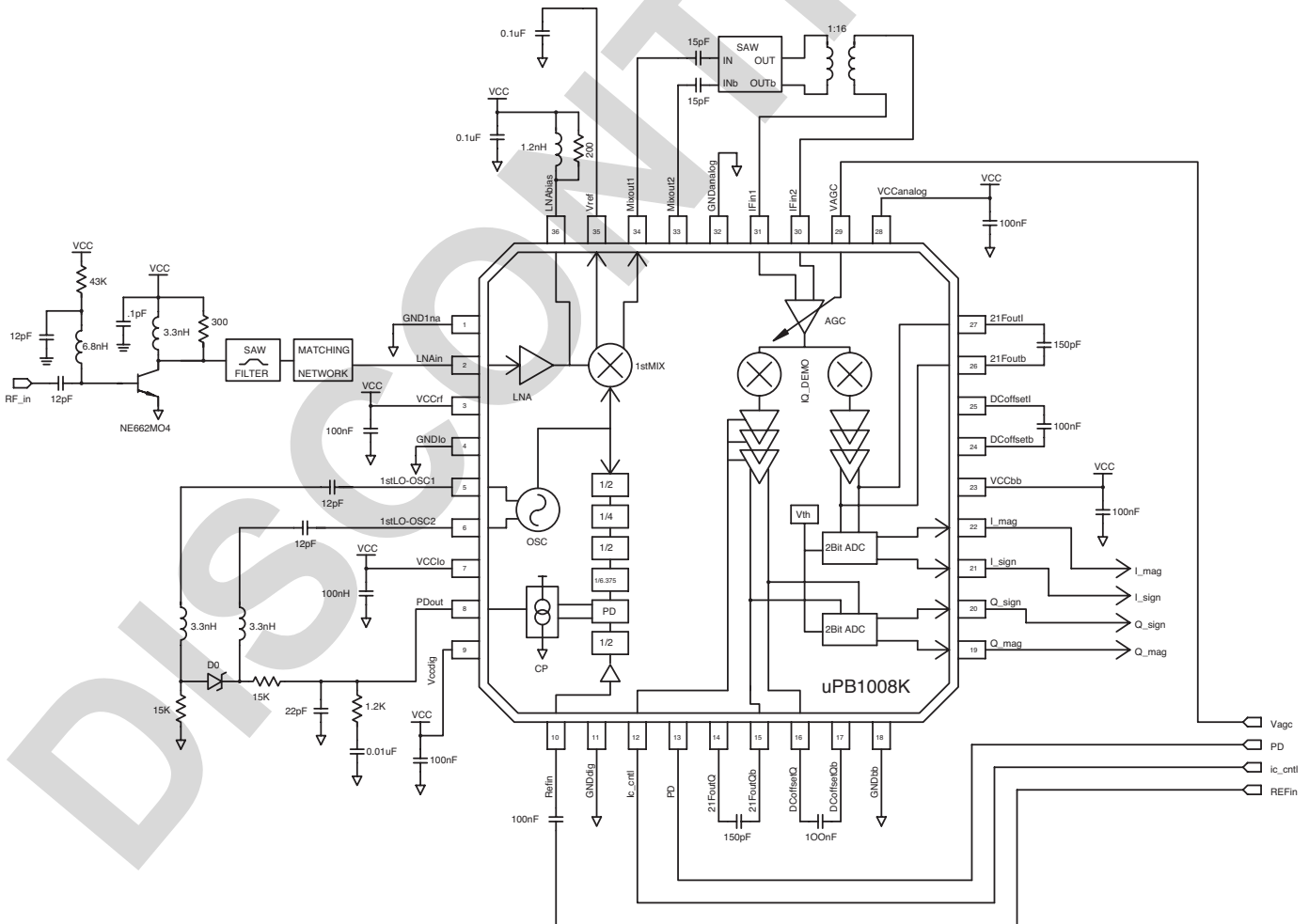
Notes:

1. Operation in excess of any one of these parameters may result in permanent damage.
2. More than two items must not be reached simultaneously.
3. TA = +85°C, mounted on a 50 x 50 x 1.6 mm double-sided copper clad epoxy glass PWB.
4. TA = 25°C

### RECOMMENDED OPERATING CONDITIONS

SYMBOLS	PARAMETERS	UNITS	MIN	TYP	MAX
Vcc	Supply Voltage	V	2.7	3.0	3.3
TOP	Operating Temperature	°C	-40	+25	+85
fRFIn	RF Input Frequency	MHz		1575	
fREFIn	Reference Frequency	MHz		27	
f1stLo	1st LO Oscillating Frequency	MHz		1400	
f1stIFIn	1st IF Input Frequency	MHz		175	
f2ndLOin	2nd LO Input Frequency	MHz		175	
VIH	Power Down Control Voltage "High"	V	2		Vcc
VIL	Power Down Control Voltage "Low"	V	0		0.5

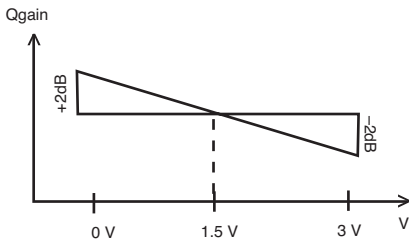
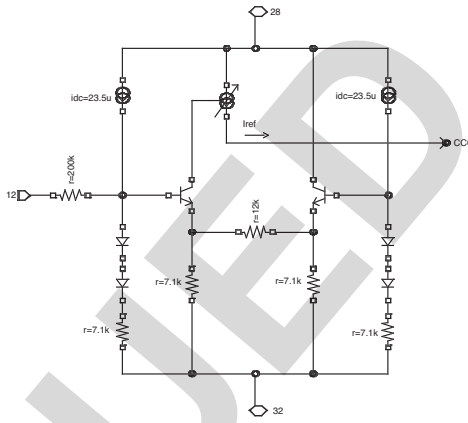
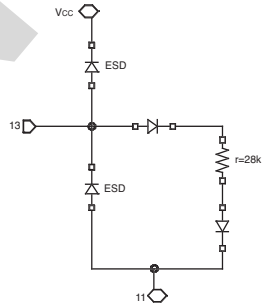
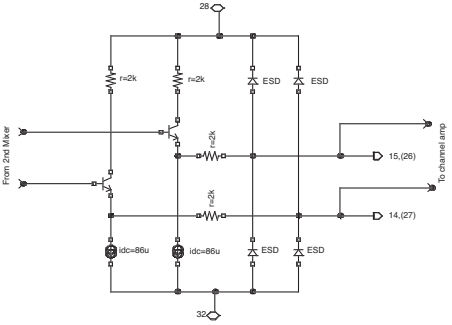
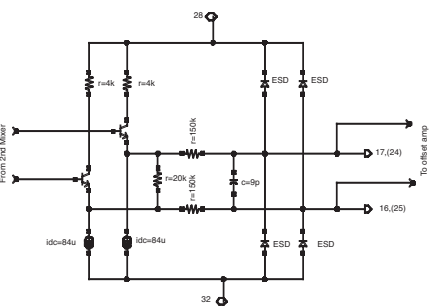
### APPLICATION CIRCUIT



**PIN FUNCTIONS**

Pin No.	Symbol	Function and Application	Internal Equivalent Circuit
1	GNDIna	Ground pin of LNA	
2	LNAin	Input pin of low noise amplifier. It is a single-ended open collector design. Capacitive coupling is required; external matching will improve gain or NF.	
3	VCCrf	Supply voltage pin of LNA, RF mixer and VCO voltage regulator.	
4	GNDlo	Ground pin of 1st LO Oscillator circuit and RF Mixer.	
5	1stLO-OSC1	Pin 5 & 6 are base pins of the differential amplifier for 1st LO oscillator. These pins require an LC (varactor) tank circuit to oscillate at around 1400 MHz.	
6	1stLO-OSC2		
7	VCClo	Supply voltage pin of oscillator circuit for 1st LO Oscillator and RF mixer	
8	PDout	This is a current mode charge pump output. For connection to a passive RC loop filter for driving external varactor diode of 1stLO-OSC.	
9	VCCdig	Supply voltage pin of digital portion of the chip.	
10	REFIn	Input pin of reference frequency buffer. This pin should be equipped with external 27 MHz oscillator (e.g. TCXO).	
11	GNDdig	Ground pin of digital portion of the chip.	

**PIN FUNCTIONS**

Pin No.	Symbol	Function and Application	Internal Equivalent Circuit
12	I/Q Balance Control	<p>The voltage on this pin controls the Q channel IF Amplifier Gain. Gain control of <math>\pm 2</math> dB can be achieved for 0~3 V. Leave open-circuited if not used.</p> 	
13	PD1	<p>Standby mode control. Low=whole chip OFF &amp; High=Whole chip ON.</p>	
14	2IFout-Q	<p>Differential output pins of quadrature demodulator Q output. Adding a lowpass shunt capacitor between these pins will define the IF Bandwidth.</p>	
15	2IFout-Qb		
16	DC offset Q	<p>DC offset compensation pin for C arm. A low pass capacitor shunt to Pin 17 is required.</p>	
17	DC offset Qb	<p>DC offset compensation pin for Q-bar arm. A low pass capacitor shunt to Pin 16 is required.</p>	

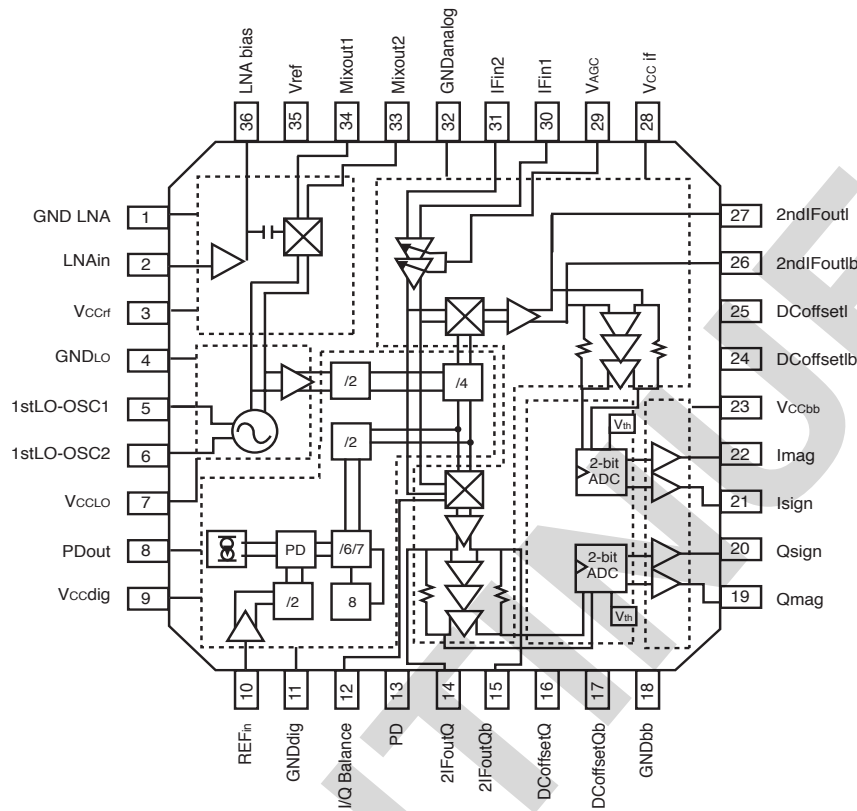
PIN FUNCTIONS

Pin No.	Symbol	Function and Application	Internal Equivalent Circuit
18	GNDbb	Ground pin of CMOS output driver.	
19	Qmag	Digitized Q signal. Magnitude bit of 2-bit ADC output.	
20	Qsign	Digitized Q signal. Sign bit of 2-bit ADC output	
21	Isign	Digitized I signal. Sign bit of 2-bit ADC output.	
22	Imag	Digitized I signal. Magnitude bit of 2-bit ADC output.	
23	VCCbb	Supply voltage pin of CMOS output driver.	
24	DCoffsetlb	DC offset compensation pin for I-bar arm. A low pass capacitor shunt to Pin 25 is required.	See pin 16 & 17 schematic
25	DCoffsetl	DC offset compensation pin for I arm. A low pass capacitor shunt to Pin 24 is required.	See pin 14 & 15 schematic
26	2IFout-lb	Differential output pins of quadrature demodulator I output. Adding a lowpass shunt capacitor between these pins will define the IF bandwidth.	
27	2IFout-l		
28	VCC if	Supply voltage pin of analog portion of the chip.	
29	VAGC	Gain control voltage pin of IF amplifier. This voltage performs reverse control, (i.e., VAGC up → gain down). If this pin is left open, then it is default at maximum gain.	
		<p>Typical AGC Gain Response</p>	
30	IF-in1	Differential input pins of 1st IF AGC amplifier	
31	IF-in2		
32	GNDanalog		
33	Mixout2	Differential output pins of RF mixer. This is an emitter follower output buffer, provide a 50Ω output load.	
34	Mixout1		

## PIN FUNCTIONS

Pin No.	Symbol	Function and Application	Internal Equivalent Circuit
35	Vref	Base-emitter junction voltage with respect to ground. May be used for biasing an external discrete transistor. Regulation will develop PTAT current.	
36	LNAbias	LNA output pin. External bias (Vcc) and matching for gain is required.	See pin 2 schematic

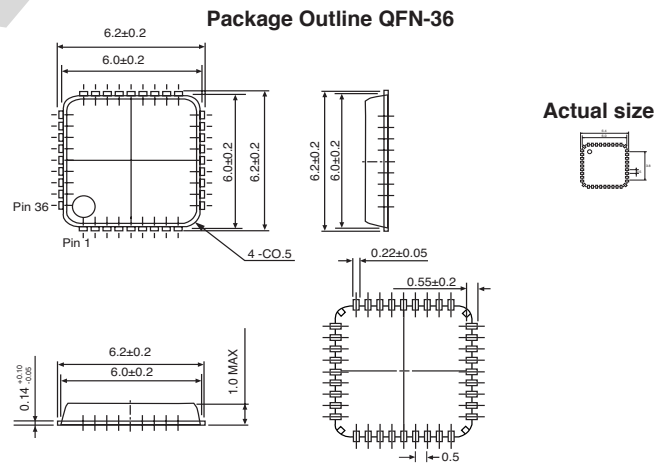
INTERNAL BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Package
UPB1008K-A	36 Pin plastic QFN

OUTLINE DIMENSIONS (Units in mm)



Caution:

The island pins located on the corners are needed to fabricate products in our plant, but do not serve any other function.

Consequently the island pins should not be soldered and should remain non-connection pins.

Life Support Applications

These NEC products are not intended for use in life support devices, appliances, or systems where the malfunction of these products can reasonably be expected to result in personal injury. The customers of CEL using or selling these products for use in such applications do so at their own risk and agree to fully indemnify CEL for all damages resulting from such improper use or sale.

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05/27/04

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Subject: Compliance with EU Directives

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This status is based on CEL’s understanding of the EU Directives and knowledge of the materials that go into its products as of the date of disclosure of this information.

Restricted Substance per RoHS	Concentration Limit per RoHS (values are not yet fixed)	Concentration contained in CEL devices	
		-A	-AZ
Lead (Pb)	< 1000 PPM	Not Detected	(*)
Mercury	< 1000 PPM	Not Detected	
Cadmium	< 100 PPM	Not Detected	
Hexavalent Chromium	< 1000 PPM	Not Detected	
PBB	< 1000 PPM	Not Detected	
PBDE	< 1000 PPM	Not Detected	

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