

MN74HC107/MN74HC107S

Dual J-K Flip-Flops with Clear

Outline

The MN74HC107/MN74HC107S consists of J-K flip-flops with clear inputs, and has two built-in circuits in one chip. The respective flip-flop has independent J input, K input, clock input, clear input, and complementary outputs Q and \bar{Q} . Each input data is transmitted to the output at the falling edge of the clock pulse. The clear input is independent of the clock input, and its active level is "L".

Owing to the silicon gate CMOS process, these flip-flop have realized low power consumption and high noise immunity equivalent to those of a standard CMOS and the operation speed as high as of an LS TTL. The MN74HC107/MN74HC107S can directly drive ten LS TTL inputs.

To protect the input and output against electrostatic breakdown, a resistor and a diode are used for the V_{CC} and the GND. The pin configuration and the function are the same as those of the standard 54LS/74LS logic family.

Truth Table

Input				Output	
CLR	CLK	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	\nearrow	L	L	Q_0	\bar{Q}_0
H	\searrow	H	L	H	L
H	\nearrow	L	H	L	H
H	\searrow	H	H	Toggle	
H	H	X	X	Q_0	\bar{Q}_0

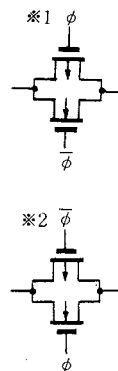
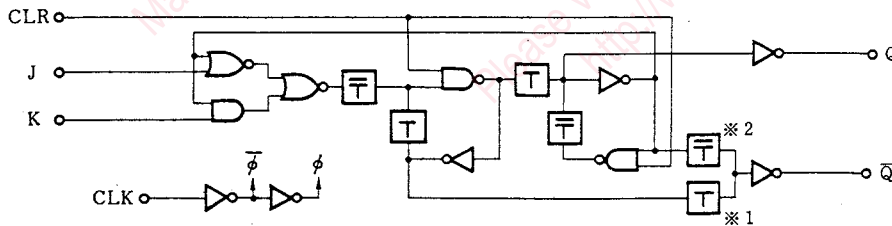
Note) 1. \nearrow : Data input is transferred to output in leading of clock from "L" to "H".

2. X : "H" or "L" either will do

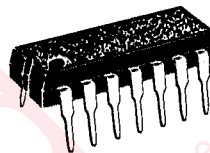
3. Q_0 (\bar{Q}_0) : Level of Q (\bar{Q}) before input conditions in table are not confirmed.

5. Toggle : Each output becomes complement of previous state by change of \nearrow .

Logic Diagram



P-1



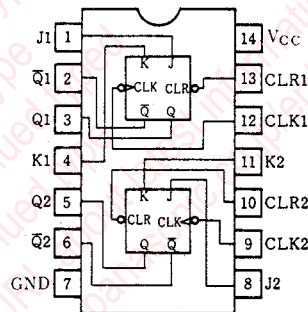
14-pin plastic DIL package

P-2



14-pin PANAFLAT package (SO-14D)

Pin Configuration



■ Absolute Maximum Ratings

Item		Symbol	Rating	Unit	
Supply voltage		V_{CC}	$-0.5 \sim +7.0$	V	
Input output voltage		V_I, V_O	$-0.5 \sim V_{CC} + 0.5$	V	
Input protective diode current		I_{IK}	± 20	mA	
Output parasitic diode current		I_{OK}	± 20	mA	
Output current		I_O	± 25	mA	
Supply current		I_{CC}, I_{GND}	± 50	mA	
Storage temperature		T_{stg}	$-65 \sim +150$	°C	
Power dissipation	MN74HC107	$T_a = -40 \sim +60^\circ\text{C}$	P_D	400	mW
		$T_a = +60 \sim +85^\circ\text{C}$		Decrease to 200mW at the rate of 8mW/°C	
	MN74HC107S	$T_a = -40 \sim +60^\circ\text{C}$	P_D	275	mW
		$T_a = +60 \sim +85^\circ\text{C}$		Decrease to 200mW at the rate of 3.8mW/°C	

■ Recommended Operating Conditions

Item		Symbol	$V_{CC}(V)$	Rating	Unit
Operating power supply voltage		V_{CC}		1.4~6.0	V
Input output voltage		V_I, V_O		$0 \sim V_{CC}$	V
Operating temperature		T_A		$-40 \sim +85$	°C
Input rise, fall time	t_r, t_f	2.0		0~1000	ns
		4.5		0~500	ns
		6.0		0~400	ns

■ DC Characteristics (GND=0V)

Item	Symbol	$V_{CC}(V)$	Test Condition		Temperature					Unit	
			V_I	V_O	$T_a = 25^\circ\text{C}$			$T_a = -40 \sim +85^\circ\text{C}$			
					Unit	min.	typ.	max.	min.		max.
Input voltage high level	V_{IH}	2.0				1.5			1.5		V
		4.5				3.15			3.15		
		6.0				4.2			4.2		
Input voltage low level	V_{IL}	2.0						0.3		0.3	V
		4.5						0.9		0.9	
		6.0						1.2		1.2	
Output voltage high level	V_{OH}	2.0		-20.0	μA	1.9	2.0		1.9		V
		4.5	V_{IH}	-20.0	μA	4.4	4.5		4.4		
		6.0	or	-20.0	μA	5.9	6.0		5.9		
		4.5	V_{IL}	-4.0	mA	3.92			3.84		
		6.0		-5.2	mA	5.48			5.34		
Output voltage low level	V_{OL}	2.0		20.0	μA		0.0	0.1		0.1	V
		4.5	V_{IH}	20.0	μA		0.0	0.1		0.1	
		6.0	or	20.0	μA		0.0	0.1		0.1	
		4.5	V_{IL}	4.0	mA			0.26		0.33	
		6.0		5.2	mA			0.26		0.33	
Input leakage current	I_I	6.0	$V_I = V_{CC}$ or GND					± 0.1		± 1.0	μA
Static supply current	I_{CC}	6.0	$V_I = V_{CC}$ or GND, $I_O = 0$					8.0		80.0	μA

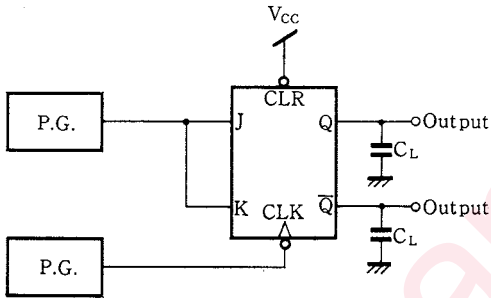
■ AC Characteristics (GND=0V, Input transition time \leq 6ns, C_L=50pF)

Item	Symbol	V _{CC} (V)	Test Condition	Temperature					Unit
				T _a =25°C			T _a =-40~+85°C		
				min.	typ.	max.	min.	max.	
Output rise time	t _{TLH}	2.0			25	75		95	ns
		4.5		8	15		19		
		6.0		7	13		16		
Output fall time	t _{THL}	2.0			20	75		95	ns
		4.5		7	15		19		
		6.0		6	13		16		
Propagation time CLK→Q, \bar{Q} (L→H)	t _{PLH}	2.0			34	125		155	ns
		4.5		14	25		31		
		6.0		11	21		26		
Propagation time CLK→Q, \bar{Q} (H→L)	t _{PHL}	2.0			37	125		155	ns
		4.5		13	25		31		
		6.0		10	21		26		
Propagation time CLR→ \bar{Q} (L→H)	t _{PLH}	2.0			48	150		190	ns
		4.5		19	30		38		
		6.0		15	26		33		
Propagation time CLR→Q (H→L)	t _{PHL}	2.0			42	125		155	ns
		4.5		15	25		31		
		6.0		13	21		26		
Minimum set-up time	t _{su}	2.0			16	75		95	ns
		4.5		6	15		19		
		6.0		5	13		16		
Minimum hold time	t _h	2.0			—	0		0	ns
		4.5		—	0		0		
		6.0		—	0		0		
Minimum pulse width CLR	t _w	2.0			17	75		95	ns
		4.5		8	15		19		
		6.0		6	13		16		
Minimum recovery time	t _{rem}	2.0			15	75		95	ns
		4.5		4	15		19		
		6.0		2	13		16		
Maximum clock frequency	f _{max}	2.0			6	24		4	MHz
		4.5		30	64		24		
		6.0		35	83		28		

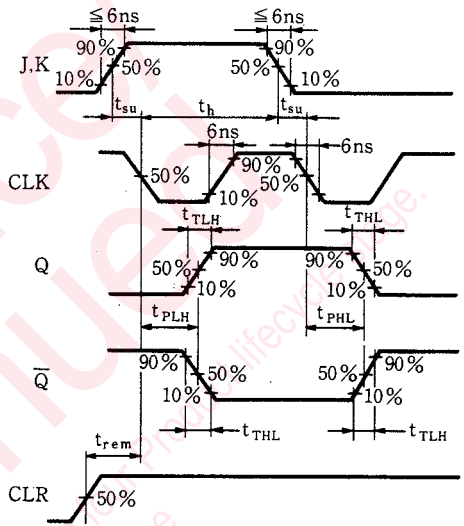
• Switching time measuring circuit and waveforms

(1) t_{TLH} , t_{THL} , t_{PLH}/t_{PHL} (CLK→Q), t_{rem} , t_h , t_{su} , t_{max}

1. Measuring circuit

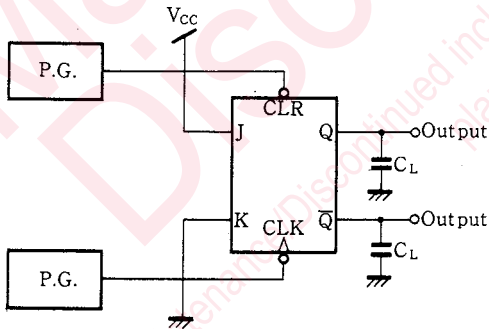


2. Switching waveforms

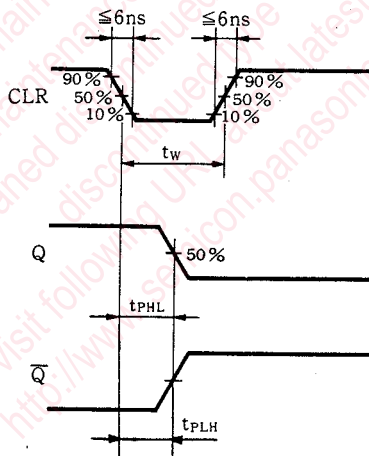


(2) t_{PLH} , t_{PHL} (CLR→Q, \bar{Q}), t_w (CLR)

1. Measuring circuit



2. Switching waveforms



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