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microelectronics group

Lucent Technologies
Bell Labs Innovations

TDAT042G5 Device Advisory and Data Addenda for Version 1 of the Device

Changes Made in This Update

The changes made to AY99-013SONT-3 are listed on page 22. References to an advance data sheet are to the *TDAT042G5 SONET/SDH 155/622/2488 Mbits/s Data Interface* Advance Data Sheet, Rev. 3. Revision 4 is the upcoming revision of the advance data sheet.

System Programming (SP)

SP1. Required Provisioning Sequence and Clocks

The core registers must be written prior to provisioning any other registers (1) to establish the internal clock rates for the device, and (2) because writing to certain core registers resets the remainder of the device. Certain clocks must be present to read/write registers prior to provisioning the device.

One of the following clocks must be present prior to provisioning to enable register access:

- TxCKP and TxCKN
- MPU clock (microprocessor interface synchronous mode only)

Provisioning must be implemented in the following sequence:

- Core register 0x0010 (mode) must be provisioned first
- Core register 0x0011 (channel [A—D] control) second
- Remainder of the core registers must then be provisioned (order does not matter)

It is recommended, but not required, that the remainder of the device be provisioned in the following order:

- OHP, PT, and DE blocks (order does not matter)
- UT block to turn on the data source to the master and slave

Workaround

Provisioning must be implemented in the following sequence:

- Apply either TxCKP and TxCKN or MPU clock.
- Provision core
  - Mode, register 0x0010
  - Channel [A—D] control, register 0x0011
  - Remainder of the core

Corrective Action

Not applicable. Use above procedure in provisioning the device.

System Programming (SP) (continued)

SP2. Behavior During Loss of Receive Line Clock

All state and counter values will be held at their current values when Rx line clock has been lost. The device will not automatically multiplex in the Tx line clock when the Rx line clock is lost.

Workaround

System software should monitor loss of line clock bits in the receive/transmit state register (addresses 0x040A—0x040D) and ignore all other alarms. This condition must be serviced as a major failure event.

Corrective Action

This is informational only. No corrective action is required for this condition.

SP3. PT Register Addressing

Addresses for the PT error counter registers are as follows:

- Channel A: 0x09B3 to 0x09E3
- Channel B: 0x09EF to 0x0A20
- Channel C: 0x0A2C to 0x0A5C
- Channel D: 0x0A68 to 0x0A98

Note: The reserved address space between the error counter registers is not symmetric. (The reserved space between channels B and C is 0x003D, and the reserved space between channels A and B and channels C and D is 0x003C.)

Workaround

This is informational only. No workaround is available for this condition.

Corrective Action

No corrective action is required for this condition.

Microprocessor Interface (MPU)

MPU1. Interface to *Motorola** MC68360 Processor Is Not Glueless

The interface between the *Motorola* MC68360 processor and TDAT042G5 requires intervening logic because of the following incompatibilities in the specifications of these two devices. For a 33 MHz microprocessor clock rate, the *Motorola* MC68360 series processors can be interfaced to TDAT042G5 without intervening glue logic if used without $\overline{\text{DT}}$ and if programmed for six wait-states. If a user wishes not to use the wait-states, then the chip select applied to TDAT042G5 must be held low until the address changes. Details are given below.

Chip Select Timing

The TDAT042G5 $\overline{\text{CS}}$ input signal requirements are not compatible with the *Motorola* MC68360 series processor $\overline{\text{CS}}$x output signals. TDAT042G5 timing does not allow simultaneous deassertion of $\overline{\text{CS}}$ and $\overline{\text{ADS}}$ signals. Chip select applied to TDAT042G5 must be held low for at least 5 ns after the MC68360 deasserts $\overline{\text{ADS}}$.

Workaround: Use external glue logic to decode the address to generate $\overline{\text{CS}}$, or provide microprocessor interface signals meeting the requirements of TDAT042G5.

$\overline{\text{DT}}$ Timing

If the *Motorola* MC68360 processor $\overline{\text{CS}}$x signal is used to drive the TDAT042G5 $\overline{\text{CS}}$, then TDAT042G5 $\overline{\text{DT}}$ output does not satisfy the MC68360 processor $\overline{\text{DSACK}}$ timing requirement. $\overline{\text{DT}}$ is not pulled to 1 before it is placed in a high-impedance state. This causes the next MPU cycle to be terminated early.

Workaround: Place a 1 kΩ resistor from $\overline{\text{DT}}$ to V_{DDD}.

Corrective Action

Corrective action for MPU1 has not been determined.

MPU2. Synchronous Microprocessor Interface Mode Is Nonfunctional

The synchronous microprocessor interface mode, MPMODE = 1 (pin D8), functions as described in the advance data sheet, but causes data errors. Placing TDAT042G5 in the synchronous mode and placing a clock on MPCLK (pin C8) will cause the data passing through the device to be corrupted. Data errors are generated at a rate of 1% or less of corrupted packets.

Workaround

Use the TDAT042G5 in the asynchronous microprocessor mode, MPMODE = 0, with no clock applied to MPCLK.

Corrective Action

This condition will be resolved in version 1A of the device.

* *Motorola* is a registered trademark of Motorola, Inc.

Core Registers (CR)

CR1. Clear on Read/Clear on Write Behavior

Bit 6 of line provisioning register 0x0010 sets the functionality of the COR/W registers.

Table CR1-1. COR/W Settings of Register 0x0010, Bit 6

Bit 6	Mode	Bit Clear Behavior of Accessed Registers
1	COR	After COR has been set (address 0x0010, bit 6 = 1), all registers that are accessed are cleared when read.
0	COW	After COW has been set (address 0x0010, bit 6 = 0), a 1 must be written to a given bit in a given register to clear that bit. Writing a 0 to a bit in a given register does not clear that bit.

Workaround

This is informational only. No workaround is available for this condition.

Corrective Action

This condition will be described in revision 4 of the advance data sheet.

Line Interface (LI)

LI1. STS-48/STM-16 Mode Lacks Facility Loopback

There is no facility loopback function (line input to line output) available in STS-48/STM-16 mode. Facility loopback is available only in STS-12/STM-4 and STS-3/STM-1 modes as described in the advance data sheet.

Workaround

This function is not a feature of TDAT042G5.

Corrective Action

No corrective action is required for this condition.

Path Terminator (PT)

PT1. Signal Degrade (SD) and Signal Fail (SF) Bit Behavior

Receive signal degrade and receive signal fail bits in the PT state registers (addresses 0x0838, 0x088A, 0x08DC, and 0x092E, bits [1:0]) do not function as described. Until the signal degrade (SD) and signal fail (SF) thresholds are programmed, the SD and SF bits will toggle on a frame-by-frame basis.

Workaround

Program thresholds during system software initialization.

Corrective Action

This functionality will be retained in its current state in future versions of the device. The advance data sheet will be corrected to reflect the actual function of the registers.

PT2. Clear-After-Write Behavior of Signal Degrade Clear Bits

Signal degrade clear (bits 15—12) of the PT one-shot control parameters register (address 0x0AA4) are described as one-shot, clear-after-write bits. Writing these bits should automatically set and then clear the bits. This one-shot behavior is not observed.

Workaround

The bits must be set to 1 and then explicitly set to 0 to clear these signal degrade bits.

Corrective Action

This functionality will be retained in its current state in future versions of the device. The advance data sheet will be corrected to reflect the actual function of the registers.

Path Terminator (PT) (continued)

PT3. Remote Defect Indicator (RDI) Behavior

The SONET standards require that when an RDI changes value, it is an objective to hold the value for a minimum of 20 frames. This applies to a **no error** state, which should be maintained for at least 20 consecutive frames. However, it is also intended by the SONET standard that the occurrence of an **error** state should be reported immediately.

TDAT042G5 responds to error conditions within 100 ms, in which case the two requirements become functionally the same.

Single-bit and enhanced RDI behave differently under the following conditions:

- Transition from **error** state to **no error** state.
- While in the **error** state, a subsequent error occurs.

The single-bit error RDI does not hold the no error condition for 20 frames as per the GR-253 specification. However, the enhanced RDI does hold the no error condition for 20 consecutive frames.

Workaround

No workaround is available for this condition.

Corrective Action

The enhanced RDI indicator in future versions of the device will behave the same as the single-bit error indicator.

PT4. SS Pointer Interpretation Algorithm

The SDH standards do not require that the SS bits are set to binary 10 for SDH equipment. The SS bit values are not used in determining a valid pointer value. Because of this, the SS pointer interpretation algorithm is not implemented in the device. Bit 5 (RSSPTRNORM[A—D]) of PT control registers 0x0AA6, 0xAAE, 0x0AB6, 0x0ABE is not used. Bits 1 and 0 (RSSEXP[1:0]) of PT provisioning register 0x0AC7 are not used.

Workaround

No workaround is available for this condition.

Corrective Action

These bits will be removed from the PT registers in future revisions of the advance data sheet.

Path Terminator (PT) (continued)

PT5. Delta/Event Registers in COR Mode

Because there is a one-cycle delay before the PT Delta Event Registers (0x802, 0x080F, 0x081C, 0x0829) are cleared after being read in COR mode, new interrupts may be lost.

Workaround

No workaround is available for this condition.

Corrective Action

This condition will be addressed in future versions of the device.

Data Engine (DE)

DE1. SDL Mode—Header Error Correction in LSB

In SDL mode, the header error correction process is susceptible to single-bit errors in the least significant bit (LSB) of the special payload.

Workaround

No workaround is available for this condition.

Corrective Action

This condition will be addressed in future versions of the device.

DE2. Incorrect ATM Loss of Cell Delineation (LCD) Implementation

Currently, the LCD is implemented in the same way that out of cell delineation (OCD) is implemented. This is not in accordance with the ITU-TI.432-2 February 1999 standard.

Workaround

No workaround is available for this condition.

Corrective Action

A software workaround will be available with version 1A of the device.

Data Engine (DE) (continued)

DE3. ATM Transmit Count of Idle Cells

For ATM mode in the transmit direction, all cells are currently counted, including the idle cells. Only the cells containing data should be counted.

Workaround

No workaround is available for this condition.

Corrective Action

This condition will be addressed in version 1A of the device.

DE4. Channel Provisioning

When using the device in STS-3/STM-1 and STS-12/STM-4 modes with either PPP, CRC, or HDLC, egress configuration registers 0x1016, 0x1017, 0x1018 and sequencer cell state register 0x1036 of all four channels must be provisioned, even if a channel is not being used.

Workaround

Provision all four transmit DE channels. Set DE egress configuration registers and the sequencer cell state register as shown in Table DE4-1.

Table DE4-1. Transmit DE Egress and Sequencer Cell State Registers

Address	Value	
	STS-3/STM-1	STS-12/STM-4
0x1016	0x4567	0x4567
0x1017	0x4567	0x4567
0x1018	0x4567	0x4567
0x1019—0x1021	—	0x4567
0x1036	0x0000	0x0000

Corrective Action

This condition will be addressed in future versions of the device.

Data Engine (DE) (continued)

DE5. Packet Behavior in POS/SDL Mode—Dry Mode

When the device is configured in POS mode with dry mode enabled, the following conditions may persist:

- PPP mode; STS-48/STS-12/STS-3.
  When running in PPP mode, the PPP header—0xFF03 0x0021 (provisionable)—may be incorrectly inserted at any point in a packet within the outgoing data stream when the FIFO runs dry, thereby corrupting the packet. Packets being sent are corrupted if the FIFO runs dry.
- PPP and CRC modes; STS-48/STS-12/STS-3.
  CRC, PPP, and HDLC modes; STS-48/STS-12/STS-3.
  In PPP, CRC, and HDLC dry modes, some of the packet data may be corrupted when the packet length is above a certain size where size is dependent upon UT clock rate and low watermark setting. Either sections of the packet may be lost or additional packets may be inserted.

Workaround

Several workarounds are possible.

- Do not provision dry mode for this device.
- If dry mode is provisioned:
  — Do not allow the FIFO to be emptied.
  — Run the UTOPIA clock fast enough, as shown in Table DE5-1, so that the FIFO is never empty.
  — Use a larger external FIFO to buffer the data.
  — Do not allow the packet size to exceed the low watermark.

Table DE5-1. Required UTOPIA Clock (TxCLK) Rates

Mode	TxCLK and Rate
STS-48/STM-16	TxCLK > 77 MHz (U3+, 32-bit mode)
STS-12/STM-4	TxCLK > 40 MHz
STS-3/STM-1	TxCLK > 10 MHz

Corrective Action

This condition will be corrected in version 1A of the device.

Data Engine (DE) (continued)

DE6. Incorrect ATM Out of Cell Delineation (OCD) Implementation

In ATM mode, the OCD reporting for channels B, C, and D is incorrect. The OCD state of channel A is reported for channels B, C, and D. The OCD reporting is correct for channel A.

Workaround

No workaround is available for this condition.

Corrective Action

This condition will be corrected in version 1A of the device.

DE7. Incorrect Frame State of ATM Data Streams

When sending a single ATM data stream to channel A, the frame states of channels B, C, and D are incorrectly set to sync mode. This prevents LCD errors from being reported on channel A as well. In addition, when sending a single ATM data stream to channels B, C, or D, the frame states always remain in hunt mode. This results in LCD errors on those channels.

Workaround

No workaround is available for this condition.

Corrective Action

A software workaround will be available with version 1A of the device.

Data Engine (DE) (continued)

DE8. Clearing DE Interrupt Register (0x1002)

DE interrupt register 0x1002 is incorrectly defined in the revision 3 of the data sheet as RO. DE interrupt register 0x1002 is correctly defined as a COR/W register. However, register 0x1002 must be used in the COR mode (register 0x0010 bit 6 set to 1). The bits of register 0x1002 are explained in detail in Table DE8-1.

Table DE8-1. Register 0x1002: DE Interrupt (COR/W)

Bits	Mode	Clear Behavior of Register 0x1002
15—12	RO	To clear these SDL Rx frame state interrupt bits, read and clear their associated interrupt source registers (addresses 0x14E0—0x14E3)
11—0	COR or COW (address 0x0010, bit 6)	To properly clear these bits, must be in COR mode (address 0x0010, bit 6 = 1).

Workaround

This is informational only. No workaround is available for this condition.

Corrective Action

This behavior will be described in future revisions of the advance data sheet.

DE9. Single Packet Transmission in HDLC-CRC, SDL-CRC, and PPP Modes

When receiving in either PPP or CRC mode, a single packet may not pass through the device. This occurs when the end of packet (which contains the CRC) never reaches the UT FIFO. The ingress channel suspends transfer to the UT when there is no end of packet in the FIFO. These bytes are transferred to the UT when the next packet is received. This problem will affect HDLC-CRC, SDL-CRC, and PPP modes.

Workaround

There are two possible workarounds:

- Set ingress payload type and mode control registers (0x1040—0x1043) to CRC strip mode. However, in CRC-16 mode, single packets may still get stuck if CRC ends on bytes A or B.
- Send a minimum 4-byte dummy packet after each packet.

Corrective Action

This condition will be addressed in future versions of the device.

Data Engine (DE) (continued)

DE10. Excessive HDLC Flag Characters

The following three issues refer to HDLC flag character (0x7E) problems in the data engine:

- An excessive number of HDLC flag characters (0x7Es) may be inserted between packets on the transmit side if the UTOPIA low watermark value is set above 2. This will have the effect of reducing the bandwidth of the device.
- The data engine operates on 32-bit boundaries. Egress packets that are not multiples of 4 will be filled with 0x7Es.
- Egress packets consisting of all 0x7Es as data will be corrupted.

Workaround

Set the UTOPIA egress low watermark value in the UTOPIA egress provisioning registers (0x0212, 0x0216, 0x021A, 0x021E) to either 1 or 2 to prevent excessive 0x7Es from being inserted between packets.

Corrective Action

This condition will be addressed in future versions of the device.

UTOPIA (UT)

UT1. Polling in Multidevice MPHY Mode

When the TDAT042G5 is polled and responds, the data bus becomes enabled. In a multidevice MPHY configuration, if the data bus is active from a different PHY device, response to a poll from the device will corrupt a data transfer already in progress. TDAT042G5 MPHY always functions without data corruption in a single-device (slave), multiple-channel configuration (point-to-point).

Workaround

No workaround is available for this condition.

Corrective Action

This condition will be addressed in future versions of the device.

UTOPIA (UT) (continued)

UT2. UTOPIA Clock Limitations

The maximum speed of the UTOPIA interface is 104 MHz. When operating at clock speeds greater than 52 MHz, RxCLK[D:A] must be placed in source mode and will use the same external clock as the corresponding TxCLK[D:A] clock. RxCLK[D:A] source mode is set by provisioning bit 6 (CLOCK_MODE_Rx) for channel A of the UTOPIA receive provisioning registers (address 0x020F).

When operating at speeds less than 52 MHz, separate external clocks for RxCLK[D:A] and TxCLK[D:A] may be used.

Workaround

This is informational only. No workaround is available for this condition.

Corrective Action

This condition will be addressed in future versions of the device. Design modifications will be directed towards allowing a maximum interface speed of 104MHz in all cases. Note that UTOPIA Level 3 clock architecture has changed in the ATM Forum’s UTOPIA Level 3 specification as of the July 1998 version.

UT3. PMRST Register Value Invalid After Reset

The value in PMRST_PECTx[A—D] (addresses 0x020B through 0x020E) is invalid after reset until the second PMRST clock period is completed. After the second PMRST, the register value is valid.

Workaround

Always have the system software execute a read of PMRST_PECTx as part of the system initialization following a reset.

Corrective Action

This condition will be addressed in future versions of the device.

UTOPIA (UT) (continued)

UT4. FIFO Overflow and Error Reporting

If the RxFIFO overflows, RxEOP is not asserted as expected. Therefore, when errors occur, two packets will be corrupted instead of one because two start of packets (SOPs) occurred without an end of packet (EOP). RxERR is not asserted when the above overflow condition occurs. No effect is noticeable in the ATM mode. Channel A works as expected; this problem occurs in channels B, C, and D.

Workaround

This error is detectable in the status registers. No workaround is available for this condition.

Corrective Action

This condition will be addressed in future versions of the device.

UT5. Timing Difference Between Direct and Polled Status Modes

In the receive direction of the MPHY mode, RxPA[A] shows the polled packet (or ATM) available status for all four slices, while the RxPA[B], RxPA[C], and RxPA[D] show the direct status states of their respective FIFOs. In some cases, the status of RxPA[A] does not agree with the status of RxPA[D:B]. The direct status indication has one additional cycle of pipeline delay from that of the polled status.

Workaround

This is informational only. No workaround is available for this condition.

Corrective Action

No corrective action is required for this condition.

UT6. UTOPIA Interface D Nonfunctional in Some Mixed MPHY and Point-to-Point Configurations

When TDAT042G5 is configured with slice D in a point-to-point mode, slice D is nonfunctional in one special case. If UTOPIA interfaces A and B are configured for 32-bit MPHY operation with slice C as part of the polled channels, interface D will be nonfunctional and cannot be independently configured in a UTOPIA Level 2 point-to-point mode. This condition does not occur in 16-bit MPHY operation.

Workaround

For mixed MPHY and point-to-point configuration, use UTOPIA slice D for MPHY mode instead of slice C. UTOPIA slice C will then be available for normal point-to point mode.

Corrective Action

This condition will be addressed in future versions of the device.

UTOPIA (UT) (continued)

UT7. Response to 0x1F MPHY Address

TDAT042G5 MPHY currently generates a polled status response to the address 0x1F (the null address), which is not compliant with the UTOPIA Level 2 standard. The address 0x1F is valid for UTOPIA Level 3 operation.

Workaround

No workaround is available for this condition.

Corrective Action

This condition will be addressed in future versions of the device.

UT8. STS-48/STM-16 Far-End Loopback Limitations

In the STS-48/STM-16 mode (U3, U3+), looping back data at the far end (UTOPIA interface) can only be accomplished without cell/packet corruption at rates below the following, as shown in Table UT8-1.

Table UT8-1. Cell/Packet Corruption Rates

Mode	ATM	Packet
STS-48/STM-16	300 Mbits/s	Rate not yet determined
STS-12/STM-4	70 Mbits/s	Rate not yet determined
STS-3/STM-1	30 Mbits/s	Rate not yet determined

When cell/packet corruption occurs, the device reports transmit FIFO underflow.

Workaround

No workaround is available for this condition.

Corrective Action

This condition will be addressed in future versions of the device.

UTOPIA (UT) (continued)

UT9. Clock Requirements in MPHY Direct Status Mode

When using the TDAT042G5 in MPHY direct status mode, receive and transmit clocks must be provided for all channels (A, B, C, and D). Also, the packet available (PA) signal for each channel must be provided on each channel's associated PA pin.

Workaround

It is possible to place RxCLK[D:A] into source mode by provisioning bit 6 (CLOCK_MODE_Rx) of the UTOPIA receive provisioning registers (addresses 0x020F, 0x0213, 0x0217, 0x021B). This will eliminate the need to supply separate receive and transmit clocks.

Corrective Action

This is informational only. No corrective action is required for this condition.

UT10. Egress Packet Mode Overflows

In the UTOPIA modes listed below, the device will report transmit packet overflow errors when no overflows have occurred. This occurs when the egress high watermark is set for the UTOPIA modes as shown in Table UT10-1.

Table UT10-1. Settings at Which Overflows Reported in Error

UTOPIA Modes	Egress High Watermark Thresholds
8-bit, U3+	≥ 0x3D
16-bit, U2+	≥ 0x3B
32-bit, U3+	≥ 0x37

Workaround

Set the egress high watermark threshold as shown in Table UT10-2. If there is a delay between TxPA deassertion and TxENB deassertion, the additional cycles should also be accounted for when setting the threshold.

Table UT10-2. Settings to Prevent Overflows Reported in Error

UTOPIA Modes	Egress High Watermark Thresholds
8-bit, U3+	< 0x3D
16-bit, U2+	< 0x3B
32-bit, U3+	< 0x37

Corrective Action

This condition will be addressed in future versions of the device.

UTOPIA (UT) (continued)

UT11. Clearing UT Interrupt Register

When a UT interrupt event occurs and COW mode is enabled, writing to UT interrupt register 0x0201 does not clear the register (this register is read-only). The interrupt is cleared by writing to the UT delta and event registers (addresses 0x0202—0x0205).

Workaround

This is informational only. No workaround is available for this condition.

Corrective Action

No corrective action is required for this condition.

UT12. Incorrect Implementation of POS Multi-PHY Mode

Because the TDAT042G5 lacks a selected PA signal (SPA), the status of a channel that is transmitting data in POS MPHY mode is not known during polling. Therefore, the PA signal cannot be used as a data valid signal. If the channel transmitting data runs dry, the master side may receive invalid data.

Workaround

Use direct status polling mode only and ensure that the address of channel A is applied to the address bus at all times except during the clock cycle when another channel is being selected.

Corrective Action

No corrective action is required for this condition.

Overhead Processor (OHP)

OHP1. Maximum BER Count

The maximum number of errors the device can report is limited to 5.00E-04 in STS-12/STM-4 mode, and 1.00E-04 in STS-48/STM-16 mode. This applies to the SDLSET, SDLCLEAR, SFLSET, and SFLCLEAR bits of the signal degrade and signal fail BER algorithm OHP registers. These bits are shown in Table OHP1-1.

Table OHP1-1. Signal Degrade and Signal Fail Algorithm OHP Registers [6:3]

OHP Bits*	Addresses
OHP_SDLSET[A—D][3:0]	0x043B, 0x043D, 0x043F, 0x0441
OHP_SDLCLEAR[A—D][3:0]	0x0447, 0x0449, 0x044B, 0x044D
OHP_SFLSET[A—D][3:0]	0x0453, 0x0455, 0x0457, 0x0459
OHP_SFLCLEAR[A—D][3:0]	0x045F, 0x0461, 0x0463, 0x0465

* The OHP prefix shown here will be added to the current bit names in revision 4 of the advance data sheet.

Workaround

This is informational only. No workaround is available for this condition.

Corrective Action

No corrective action is required for this condition.

OHP2. RDI-L Reporting

When the device is initially powered up, it defaults to STS-48/STM-16 mode. This locks a counter value into transmit control registers for channels B, C, and D. When the device is configured for STS-3/STM-1 mode, the counter does not automatically clear.

Workaround

During STS-3/STM-1 OHP configuration in the system code, manually clear transmit control registers 0x0431, 0x0433, and 0x0435 for channels B, C, and D. In order to clear these transmit control registers, the bits must be toggled. The following pseudocode shows how to clear the bits on channels B, C, and D.

```
Set address 0x0431 to 0x007F # set bits on channel B
Set address 0x0431 to 0x0000 # clear bits on channel B
Set address 0x0433 to 0x007F # set bits on channel C
Set address 0x0433 to 0x0000 # clear bits on channel C
Set address 0x0435 to 0x007F # set bits on channel D
Set address 0x0435 to 0x0000 # clear bits on channel D
```

Corrective Action

This is informational only. No corrective action is required for this condition.

Overhead Processor (OHP) (continued)

OHP3. M1 Error Counter in STS-48/STM-16 Mode

When the device receives REI-L errors in the STS-48/STM-16 mode, no M1 errors are reported.

Workaround

There are several workarounds for this problem:

- Pass the B2 error count value to the far end through system software.
- Process the M1 byte from the receive TOAC with an external FPGA.
- Pass the B2 error count from the receive to the transmit direction using transmit TOAC capability. The error count must be inserted into the eleventh Z2 byte in an STS-48/STM-16 transmit signal. The transmit TOAC signal is driven by an external device with software insert capability.
- Pass the B2 error count from the receive to the transmit direction in the section overhead byte. The device has F1 and S1 monitor capability; the protocol for sending the error message to the far end with F1 or S1 bytes is user-defined.

Corrective Action

This condition will be addressed in future versions of the device.

Packaging and Pinouts (P)

P1. Pin F5 (Previously $\overline{\text{JTEST}}$) Is No Connect (NC)

Item deleted. Corrected in the advance data sheet.

P2. Modified Pinout and Power Supply Configuration—Future Versions

Item deleted. No modifications to the power supply configuration will be made.

P3. Change to TDAT042G5 Version 1 Pinout

Item deleted. All devices conform to power pin assignments as listed in the advance data sheet.

Packaging and Pinouts (P) (continued)

P4. Power Dissipation

The worst-case power dissipation of TDAT042G5 is currently estimated to be 7.5 W. The minimum and maximum power dissipation is listed in Table P4-1, as well as the relative package thermal characteristics.

Table P4-1. Power Dissipation and Relative Package Thermal Characteristics

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Power Dissipation:	P_D					
Minimum		STS-3/STM-1 line rate	—	3	—	W
Maximum		STS-12/STM-4 and STS-48/ STM-16 line rates	—	6	—	W
Thermal Performance (JEDEC standard conditions)*	θ_{JA}	Standard JEDEC 4-layer PWB				
		■ Standard natural convection	—	9	—	°C/W
		■ 200 LFPM airflow	—	6.5	—	°C/W
		■ 800 LFPM airflow	—	5	—	°C/W
Correlation Factor Between Die and Case Temperatures[†]	ψ_{JC}	Standard JEDEC 4-layer PWB				
		■ Standard natural convection	—	0.3	—	°C/W
		■ 200 LFPM airflow	—	0.4	—	°C/W
		■ 800 LFPM airflow	—	0.5	—	°C/W

* $\theta_{JA} = (T_J - T_A)/P_D$: T_J = junction temperature, T_A = ambient temperature of medium surrounding the package, P_D = electrical power dissipated by the device.

[†] $\psi_{JC} = (T_J - T_C)/P_D$: T_J = junction temperature, T_C = package temperature (top, dead-center), P_D = electrical power dissipated by the device.

Maximum junction temperature of TDAT042G5 is 125 °C. Therefore, maximum case temperature under natural convection conditions must be less than approximately 50 °C, and in this case, an external heat sink is required.

References

Jeff Weiss, *600 LBGA Thermal Test Report*, February 25, 1999.

HL250C 3.3 Volt 0.25 µm CMOS Standard-Cell Library (MN98-060ASIC-02), pages 2-2 and 2-3.

Workaround

An external heat sink is required.

Corrective Action

Power consumption will be addressed in future versions of the device.

Data Addenda

DA1. Incorrect PT Control Register Mapping

TDAT042G5 SONET/SDH 155/622/2488 Mbits/s Data Interface Advance Data Sheet, Rev. 3 lists the following bit mapping for PT control registers 0x0AAA, 0x0AB2, 0x0ABA, and 0x0AC2:

bit #9 TRDIP_PLMPINH[A—D]
bit #8 TRDIP_UNEQUIPINH[A—D]
bit #7 TRDIP_LCDINH[A—D]

The correct bit mapping is the following:

bit #9 TRDIP_LCDINH[A—D]
bit #8 TRDIP_PLMPINH[A—D]
bit #7 TRDIP_UNEQUIPINH[A—D]

Workaround

No workaround is available for this condition.

Corrective Action

This correct bit mapping will be included in revision 4 of the advance data sheet.

AY99-013SONT-2 Replaces AY99-013SONT to Incorporate the Following Updates

1. Page 1, SP1. Required Provisioning Sequence and Clocks, added new issue.
2. Page 8, DE4. Channel Provisioning, added new issue.
3. Page 9, DE5. Packet Behavior in POS/SDL Mode—Dry Mode, added new issue.
4. Page 15, UT8. STS-48/STM-16 Far-End Loopback Limitations, added new issue.
5. Page 16, advance data sheet document number corrected.

AY99-013SONT-3 Replaces AY99-013SONT-2 to Incorporate the Following Updates

1. Page 1, Notice that the advisory issues still apply to the advance data sheet which has just been updated.

AY99-013SONT-4 Replaces AY99-013SONT-3 to Incorporate the Following Updates

1. Replaced OC- designation with STS- and STM- throughout advisory.
2. Page 2, SP2. Behavior During Loss of Receive Line Clock, added new issue.
3. Page 2, SP3. PT Register Addressing, added new issue.
4. Page 4, CR1. Clear on Read/Clear on Write Behavior, added new issue.
5. Page 5, PT2. Clear-After-Write Behavior of Signal Degrade Clear Bits, corrected description.
6. Page 6, PT4. SS Pointer Interpretation Algorithm, added new issue.
7. Page 7, PT5. Delta/Event Registers in COR Mode, added new issue.
8. Page 7, DE2. Incorrect ATM Loss of Cell Delineation (LCD) Implementation, identified the specific ITU standard with which the LCD implementation does not comply.
9. Page 8, DE4. Channel Provisioning, Table DE4-1. Transmit DE Egress and Sequencer Cell State Registers, corrected register 0x102D to 0x1021.
10. Page 9, DE5. Packet Behavior in POS/SDL Mode—Dry Mode, identified dry mode issues.
11. Page 10, DE6. Incorrect ATM Out of Cell Delineation (OCD) Implementation, added new issue.
12. Page 10, DE7. Incorrect Frame State of ATM Data Streams, added new issue.
13. Page 11, DE8. Clearing DE Interrupt Register (0x1002), added new issue.
14. Page 11, DE9. Single Packet Transmission in HDLC-CRC, SDL-CRC, and PPP Modes, added new issue.
15. Page 12, DE10. Excessive HDLC Flag Characters, added new issue.
16. Page 13, UT2. UTOPIA Clock Limitations, clarified wording.
17. Page 14, UT4. FIFO Overflow and Error Reporting, clarified wording.
18. Page 16, UT9. Clock Requirements in MPHY Direct Status Mode, added new issue.
19. Page 16, UT10. Egress Packet Mode Overflows, added new issue.
20. Page 17, UT11. Clearing UT Interrupt Register, added new issue.
21. Page 17, UT12. Incorrect Implementation of POS Multi-PHY Mode, added new issue.
22. Page 18, OHP1. Maximum BER Count, added new issue. In addition, differentiated OHP bits from PT bits with the same name; the names will be corrected in revision 4 of the advance data sheet.
23. Page 18, OHP2. RDI-L Reporting, added new issue.
24. Page 19, OHP3. M1 Error Counter in STS-48/STM-16 Mode, added new issue.
25. Removed issue P1. Pin 5 (Previously $\overline{\text{JTEST}}$) Is No Connect (NC). Pin F5 was corrected to NC in the accompanying advance data sheet, DS98-193SONT-3.

AY99-013SONT-4 Replaces AY99-013SONT-3 to Incorporate the Following Updates (continued)

26. Removed issue P2. Modified Pinout and Power Supply Configuration—Future Versions. Plans for 2.5 V power ring implementation considered, but no schedule available at this time.
27. Removed issue P3. Change to TDAT042G5 Version 1 Pinout. Listed pins have been corrected to NC in the accompanying advance data sheet, DS98-193SONT-3.
28. Page 21, DA1. Incorrect PT Control Register Mapping, added new issue.

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March 16, 2000
AY99-013SONT-4 (Replaces AY99-013SONT-3 and must accompany DS98-193SONT-3)

Lucent Technologies
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Data Addendum
October 1999

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TDAT SONET/SDH
155/622/2488 Mbits/s Data Interfaces

Introduction

The TDAT data interface is available in three different configurations as summarized in Table 1.

TDAT04622

The TDAT04622 device contains a subset of the TDAT042G5 device. The TDAT04622 device functions as described in the *TDAT042G5 SONET/SDH 155/622/2488 Mbits/s Data Interface* Data Sheet (DS98-193SONT-3) with the following limitations:

- Quad OC-3 operation only or single OC-12 operation only.
- Single UTOPIA port.

TDAT021G2

The TDAT021G2 device contains a subset of the TDAT042G5 device. The TDAT021G2 device functions as described in the *TDAT042G5 SONET/SDH 155/622/2488 Mbits/s Data Interface* Data Sheet (DS98-193SONT-3) with the following limitations:

- Quad OC-3 operation only or dual OC-12 operation only.
- Two UTOPIA ports.

TDAT042G5

The TDAT042G5 device contains all functionality as described in the *TDAT042G5 SONET/SDH 155/622/2488 Mbits/s Data Interface* Data Sheet (DS98-193SONT-3).

Table 1. TDAT Device Product Line

Device	Line Ports			UTOPIA Ports	
	OC-3	OC-12	OC-48	Ports Present	Modes
TDAT04622	4 (A, B, C, D)	1 (A)	NA	1 (A)	U2, U2+, U3, U3+ ■ 8-bit ■ 16-bit
TDAT021G2	4 (A, B, C, D)	2 (A, B)	NA	2 (A, B)	U2, U2+, U3, U3+ ■ 8-bit ■ 16-bit ■ 32-bit
TDAT042G5	4 (A, B, C, D)	4 (A, B, C, D)	1 (16-bit parallel multiplexed/ demultiplexed)	4 (A, B, C, D)	U2, U2+, U3, U3+ ■ 8-bit ■ 16-bit ■ 32-bit

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October 1999
DA00-001SONT (Must accompany DS98-193SONT-3)

Advance Data Sheet, Rev. 3
August 1999

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TDAT042G5 SONET/SDH 155/622/2488 Mbits/s Data Interface

Features

- Point-point path termination device for interface termination.
- Versatile IC supports 155/622/2488 Mbits/s SONET/SDH interface solutions for packet over SONET (POS), asynchronous transfer mode (ATM), or simplified data link (SDL) for data over fiber applications.
- Supports point-to-point and multi-PHY UTOPIA.
- Low-power 3.3 V operation.
- High-speed I/O is LVPECL. All other logic has 5 V tolerant TTL-level inputs.
- –40 °C to +85 °C temperature range.
- 600 LBGA package.

SONET/SDH Interface

- Termination of quad STS-3/STM-1, quad STS-12/STM-4, or single STS-48/STM-16.
- Supports overhead processing for transport and path overhead bytes.
- Optional insertion and extraction of overhead bytes via serial overhead interface.
- Full path termination and SPE extraction/insertion.
- SONET/SDH compliant condition and alarm reporting.
- Handles all concatenation levels of STS-3c through STS-48c (in multiples of 3; i.e., 3c, 6c, 9c, etc.), STM-1 through STM-16.
- Built-in diagnostic loopback modes.
- Compliant with the following Bellcore, ANSI, and ITU standards:
  - — GR-253 CORE: SONET Transport Systems: Common Generic Criteria.
  - — ITU-T G.707: Network Node Interface for the Synchronous Digital Hierarchy,
  - — ITU-T G.803: Architecture of Transport Networks Based on the Synchronous Digital Hierarchy
  - — T1.105: SONET-Basic Description including Multiplex Structure, Rates and Formats,
  - — T1.105.02 SONET-Payload Mappings,
  - — T1.105.03 SONET-Jitter at Network Interfaces,
  - — T1.105.06 SONET Physical Layer Specifications,
  - — T1.105.07 SONET-Sub-STS-1 Interface Rates and Formats Specification
  - — ITU-T I.432: B-ISDN User-Network Interface-Physical Layer Specification
  - — IETF RFC 1619: PPP over SONET/SDH,
  - — IETF RFC 1661: The Point-to-Point Protocal (PPP),
  - — IETF RFC 1662: PPP in HDLC-like Framing

Data Processing

- Provisionable data engine supports payload insertion/extraction and CRC-16/32 generation/verification for ATM cell or PPP, SDL, or HDLC streams.
- Maintains counts for cell/packet traffic (e.g., total number of cells, number of discarded cells).
- Integrated UTOPIA Level 2- and UTOPIA Level 3-compatible ATM physical layer interface with packet extensions for all test and operations.
- Insertion and extraction of up to four separate data channels.
- Compliant with 1998: ATM Forum, ITU standards, and IETF standards.

Microprocessor Interface

- 16-bit address and 16-bit data interface with up to 66 MHz read and write access.
- Compatible with most industry-standard processors.

Description

The TDAT042G5 SONET/SDH interface device provides a versatile solution for quad STS-3/STM-1, quad STS-12/STM-4, and for single STS-48/STM-16 point-to-point datacom/telecom applications. Constructed using Lucent Technologies Microelectronics Group's state-of-the-art CMOS technology, this device incorporates integrated SONET/SDH framing, section and line overhead insertion and extraction, path termination, and generation. (See the rest of the Description section, page 9.)

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Description (continued)

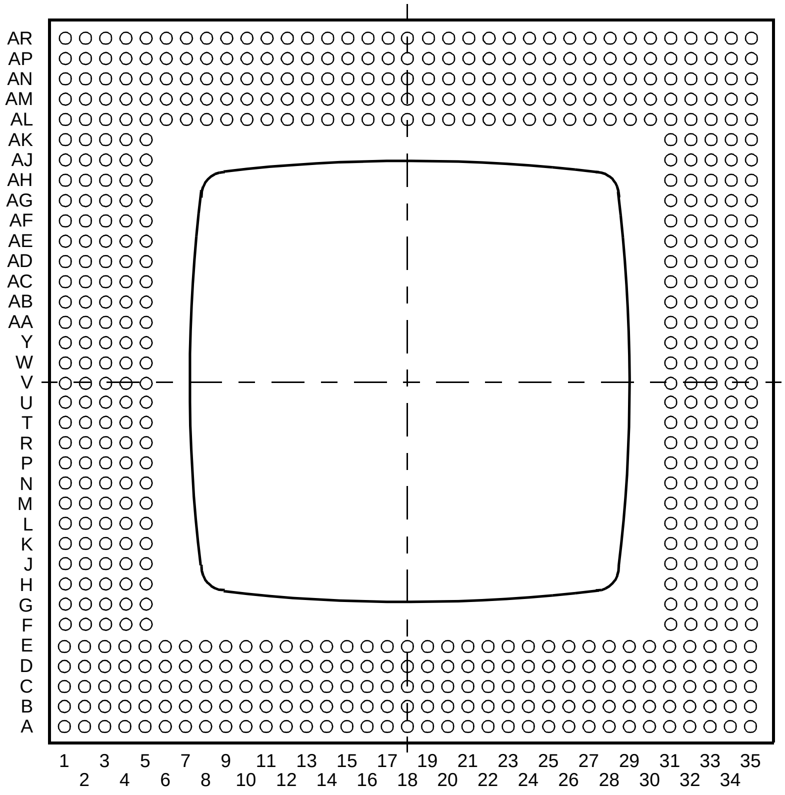
The integrated circuit provides complete encapsulation and decapsulation for packet and ATM streams into and out of SONET/SDH payloads.

Communication with the device is accomplished through a generic microprocessor interface. The device supports separate address and data buses.

With the device, construction of all types of point-to-point STS-3/STS-12/STS-48 (STM-1/STM-4/STM-16) data equipment is simplified and cost-reduced, allowing extremely efficient solutions.

Pin Information

TDAT042G5 is available in a 600-pin LBGA package. The pin diagram is shown in Figure 1. For convenience, pin assignments are listed by pin order in Table 1 and by signal name in Table 2. The pin descriptions as well as the pin assignments are listed in Table 3—Table 10 and are grouped by interface type.



5-7175(F)

Figure 1. Pin Diagram of 600-Pin LBGA (Bottom View)

Pin Information (continued)

Table 1. Pin Assignments for 600-Pin LBGA by Pin Number Order

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	VDDD	B1	VDDD	C1	GNDD	D1	GNDD
A2	VDDD	B2	VDDD	C2	GNDD	D2	GNDD
A3	GNDD	B3	GNDD	C3	VDDD	D3	GNDD
A4	GNDD	B4	GNDD	C4	GNDD	D4	VDDD
A5	VDDD	B5	NC	C5	NC	D5	NC
A6	VDDD	B6	VDDA	C6	GNDA	D6	NC
A7	GNDD	B7	$\overline{\text{INT}}$	C7	$\overline{\text{RST}}$	D7	PMRST
A8	GNDD	B8	$\overline{\text{CS}}$	C8	MPCLK	D8	MPMODE
A9	DATA[1]	B9	DATA[0]	C9	$\overline{\text{DS}}$	D9	R/$\overline{\text{W}}$
A10	DATA[6]	B10	DATA[5]	C10	DATA[4]	D10	DATA[3]
A11	DATA[10]	B11	DATA[9]	C11	DATA[8]	D11	DATA[7]
A12	DATA[15]	B12	DATA[14]	C12	DATA[13]	D12	DATA[12]
A13	GNDD	B13	ADDR[3]	C13	ADDR[2]	D13	ADDR[1]
A14	ADDR[8]	B14	ADDR[7]	C14	ADDR[6]	D14	ADDR[5]
A15	ADDR[12]	B15	ADDR[11]	C15	ADDR[10]	D15	NC
A16	GNDD	B16	ADDR[15]	C16	ADDR[14]	D16	ADDR[13]
A17	VDDD	B17	NC	C17	NC	D17	NC
A18	VDDD	B18	NC	C18	NC	D18	NC
A19	NC	B19	NC	C19	NC	D19	NC
A20	GNDD	B20	NC	C20	NC	D20	NC
A21	NC	B21	NC	C21	NC	D21	NC
A22	NC	B22	NC	C22	NC	D22	NC
A23	GNDD	B23	NC	C23	NC	D23	NC
A24	NC	B24	NC	C24	NC	D24	NC
A25	NC	B25	NC	C25	NC	D25	NC
A26	NC	B26	NC	C26	NC	D26	NC
A27	GNDD	B27	NC	C27	NC	D27	VDDD
A28	GNDD	B28	NC	C28	NC	D28	NC
A29	GNDD	B29	NC	C29	NC	D29	NC
A30	VDDD	B30	NC	C30	NC	D30	NC
A31	VDDD	B31	NC	C31	NC	D31	NC
A32	GNDD	B32	GNDD	C32	GNDD	D32	VDDD
A33	GNDD	B33	GNDD	C33	VDDD	D33	GNDD
A34	VDDD	B34	VDDD	C34	GNDD	D34	GNDD
A35	VDDD	B35	VDDD	C35	GNDD	D35	GNDD

Note: NC refers to no connect. Do not connect pins so designated.

Pin Information (continued)

Table 1. Pin Assignments for 600-Pin LBGA by Pin Number Order (continued)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
E1	VDDD	F1	VDDD	J31	TxEOP[A]	N1	GNDD
E2	NC	F2	TCK	J32	TxSOP/C[A]	N2	TxD[6]N
E3	VDDD PLL	F3	GNDD	J33	TxPRTY[A]	N3	TxD[6]P
E4	GNDD PLL	F4	TMS	J34	TxDATA[A][15]	N4	TxD[7]N
E5	VDDD	F5	NC	J35	TxDATA[A][14]	N5	TxD[7]P
E6	NC	F31	NC	K1	TxD[12]N	N31	RxDATA[A][15]
E7	$\overline{\text{ICT}}$	F32	NC	K2	TxD[12]P	N32	RxDATA[A][14]
E8	$\overline{\text{DT}}$	F33	NC	K3	TxD[13]N	N33	RxDATA[A][13]
E9	$\overline{\text{ADS}}$	F34	NC	K4	TxD[13]P	N34	RxDATA[A][12]
E10	DATA[2]	F35	VDDD	K5	VDDD	N35	GNDD
E11	VDDD	G1	GNDD	K31	TxDATA[A][13]	P1	TxD[4]N
E12	DATA[11]	G2	TDO	K32	TxDATA[A][12]	P2	TxD[4]P
E13	ADDR[0]	G3	$\overline{\text{TRST}}$	K33	TxDATA[A][11]	P3	TxD[5]N
E14	ADDR[4]	G4	NC	K34	TxDATA[A][10]	P4	VDDD
E15	ADDR[9]	G5	TDI	K35	TxDATA[A][9]	P5	TxD[5]P
E16	VDDD	G31	NC	L1	TxD[10]N	P31	RxDATA[A][11]
E17	NC	G32	TxADDR[0]	L2	TxD[10]P	P32	RxDATA[A][10]
E18	NC	G33	TxADDR[1]	L3	TxD[11]N	P33	RxDATA[A][9]
E19	NC	G34	TxCLK[A]	L4	TxD[11]P	P34	RxDATA[A][8]
E20	VDDD	G35	GNDD	L5	VDDD	P35	RxDATA[A][7]
E21	NC	H1	GNDD	L31	VDDD	R1	VDDD
E22	NC	H2	TxCKQP	L32	TxDATA[A][8]	R2	TxD[2]N/TxD[B]N
E23	NC	H3	GNDD	L33	TxDATA[A][7]	R3	TxD[2]P/TxD[B]P
E24	NC	H4	CLKDIV	L34	TxDATA[A][6]	R4	TxD[3]P/TxD[A]P
E25	VDDD	H5	GNDD	L35	TxDATA[A][5]	R5	TxD[3]N/TxD[A]N
E26	NC	H31	TxSZ[A]	M1	TxD[8]N	R31	RxDATA[A][6]
E27	NC	H32	TxERR[A]	M2	TxD[8]P	R32	RxDATA[A][5]
E28	NC	H33	TxPA[A]	M3	TxD[9]N	R33	RxDATA[A][4]
E29	NC	H34	TxENB[A]	M4	TxD[9]P	R34	RxDATA[A][3]
E30	NC	H35	GNDD	M5	VDDD	R35	RxDATA[A][2]
E31	VDDD	J1	TxD[14]N	M31	TxDATA[A][4]	T1	GNDD
E32	NC	J2	TxD[14]P	M32	TxDATA[A][3]	T2	TxD[0]P/TxD[D]P
E33	NC	J3	TxD[15]N	M33	TxDATA[A][2]	T3	TxD[1]N/TxD[C]N
E34	NC	J4	TxD[15]P	M34	TxDATA[A][1]	T4	TxD[1]P/TxD[C]P
E35	VDDD	J5	TxCKQN	M35	TxDATA[A][0]	T5	VDDD

Note: NC refers to no connect. Do not connect pins so designated.

Pin Information (continued)

Table 1. Pin Assignments for 600-Pin LBGA by Pin Number Order (continued)

Pin	Signal Name
T31	VDDD
T32	RxDATA[A][1]
T33	RxDATA[A][0]
T34	RxPRTY[A]
T35	GNDD
U1	TxFSYNCN
U2	TxD[0]N/ TxD[D]N
U3	TxFSYNCP
U4	TxCKP
U5	TxCKN
U31	RxSOP/C[A]
U32	RxEOP[A]
U33	NC
U34	RxENB[A]
U35	VDDD
V1	VDDD
V2	VDDD
V3	GNDD
V4	RxCKN/RxD[A]N
V5	RxCKP/RxD[A]P
V31	GNDD
V32	RxERR[A]
V33	RxPA[A]
V34	NC
V35	VDDD
W1	VDDD
W2	RxD[14]N/ RxCLK[A]N
W3	RxD[14]P/ RxCLK[A]P
W4	RxD[15]N/ RxD[B]N
W5	RxD[15]P/ RxD[B]P
W31	RxADDR[0]
W32	RxADDR[1]
W33	RxCLK[A]
W34	TxADDR[2]
W35	RxSZ[A]
Y1	GNDD
Y2	RxD[13]N/ RxCLK[B]N
Y3	RxD[13]P/ RxCLK[B]P
Y4	GNDD
Y5	VDDD
Y31	VDDD
Y32	TxSZ[B]
Y33	TxCLK[B]
Y34	TxADDR[3]
Y35	GNDD
AA1	RxD[11]N/RxCLK[C]N
AA2	RxD[11]P/RxCLK[C]P
AA3	RxD[12]N/RxD[C]N
AA4	RxD[12]P/RxD[C]P
AA5	GNDD
AA31	TxEOP[B]
AA32	TxSOP/C[B]
AA33	TxENB[B]
AA34	TxPA[B]
AA35	TxERR[B]
AB1	RxD[9]N/RxCLK[D]N
AB2	RxD[9]P/RxCLK[D]P
AB3	RxD[10]N/RxD[D]N
AB4	RxD[10]P/RxD[D]P
AB5	VDDD
AB31	TxDATA[B][13]
AB32	TxDATA[B][12]
AB33	TxDATA[B][14]
AB34	TxDATA[B][15]
AB35	TxPRTY[B]
AC1	GNDD
AC2	RxD[7]N
AC3	RxD[7]P
AC4	RxD[8]N
AC5	RxD[8]P
AC31	TxDATA[B][8]
AC32	TxDATA[B][9]
AC33	TxDATA[B][10]
AC34	TxDATA[B][11]
AC35	GNDD
AD1	RxD[5]N
AD2	RxD[5]P
AD3	RxD[6]N
AD4	RxD[6]P
AD5	VDDD
AD31	TxDATA[B][3]
AD32	TxDATA[B][4]
AD33	TxDATA[B][5]
AD34	TxDATA[B][6]
AD35	TxDATA[B][7]
AE1	RxD[3]N
AE2	RxD[3]P
AE3	RxD[4]N
AE4	RxD[4]P
AE5	VDDD
AE31	VDDD
AE32	RxDATA[B][15]
AE33	TxDATA[B][0]
AE34	TxDATA[B][1]
AE35	TxDATA[B][2]
AF1	RxD[1]N
AF2	RxD[1]P
AF3	RxD[2]N
AF4	RxD[2]P
AF5	VDDD
AF31	RxDATA[B][10]
AF32	RxDATA[B][11]
AF33	RxDATA[B][12]
AF34	RxDATA[B][13]
AF35	RxDATA[B][14]
AG1	RxD[0]N
AG2	RxD[0]P
AG3	ECLREFLO
AG4	ECLREFHI
AG5	GPIO[3]
AG31	RxDATA[B][5]
AG32	RxDATA[B][6]
AG33	RxDATA[B][7]
AG34	RxDATA[B][8]
AG35	RxDATA[B][9]
AH1	GNDD
AH2	GPIO[2]
AH3	GPIO[1]
AH4	GPIO[0]
AH5	TxTOHF
AH31	RxDATA[B][1]
AH32	RxDATA[B][2]
AH33	RxDATA[B][3]
AH34	RxDATA[B][4]
AH35	GNDD
AJ1	GNDD
AJ2	TxTOHCK
AJ3	TxTOHD[A]
AJ4	TxTOHD[B]
AJ5	TxTOHD[C]
AJ31	RxEOP[B]
AJ32	RxSOP/C[B]
AJ33	RxPRTY[B]
AJ34	RxDATA[B][0]
AJ35	GNDD
AK1	VDDD
AK2	TxTOHD[D]
AK3	RxREF
AK4	RxTOHF[A]
AK5	RxTOHCK[A]

Note: NC refers to no connect. Do not connect pins so designated.

Pin Information (continued)

Table 1. Pin Assignments for 600-Pin LBGA by Pin Number Order (continued)

Pin	Signal Name
AK31	RxSZ[B]
AK32	RxERR[B]
AK33	RxPA[B]
AK34	RxENB[B]
AK35	VDDD
AL1	VDDD
AL2	RxTOHD[A]
AL3	RxTOHF[B]
AL4	RxTOHCK[B]
AL5	VDDD
AL6	RxTOHCK[C]
AL7	RxTOHCK[D]
AL8	NC
AL9	RxPA[D]
AL10	RxDATA[D][0]
AL11	VDDD
AL12	RxDATA[D][9]
AL13	RxDATA[D][14]
AL14	TxDATA[D][3]
AL15	TxDATA[D][8]
AL16	VDDD
AL17	TxSOP/C[D]
AL18	VDDD
AL19	NC
AL20	VDDD
AL21	RxSOP/C[C]
AL22	RxDATA[C][3]
AL23	RxDATA[C][7]
AL24	RxDATA[C][12]
AL25	VDDD
AL26	TxDATA[C][5]
AL27	TxDATA[C][10]
AL28	TxDATA[C][14]
AL29	TxEOP[C]
AL30	TxSZ[C]
AL31	VDDD
AL32	RxADDR[3]
AL33	RxADDR[2]
AL34	RxCLK[B]
AL35	VDDD
AM1	GNDD
AM2	GNDD
AM3	GNDD
AM4	VDDD
AM5	RxTOHD[B]
AM6	RxTOHD[C]
AM7	NC
AM8	RxCLK[D]
AM9	RxENB[D]
AM10	RxDATA[D][1]
AM11	RxDATA[D][5]
AM12	RxDATA[D][10]
AM13	RxDATA[D][15]
AM14	TxDATA[D][2]
AM15	TxDATA[D][7]
AM16	TxDATA[D][12]
AM17	TxPRTY[D]
AM18	TxERR[D]
AM19	NC
AM20	RxSZ[C]
AM21	RxEOP[C]
AM22	RxDATA[C][2]
AM23	RxDATA[C][6]
AM24	RxDATA[C][11]
AM25	TxDATA[C][0]
AM26	TxDATA[C][4]
AM27	TxDATA[C][9]
AM28	TxDATA[C][13]
AM29	TxSOP/C[C]
AM30	TxERR[C]
AM31	TxADDR[4]
AM32	VDDD
AM33	GNDD
AM34	GNDD
AM35	GNDD
AN1	GNDD
AN2	GNDD
AN3	VDDD
AN4	GNDD
AN5	RxTOHF[C]
AN6	GNDD
AN7	RxTOHD[D]
AN8	RxSZ[D]
AN9	RxEOP[D]
AN10	RxDATA[D][2]
AN11	RxDATA[D][6]
AN12	RxDATA[D][11]
AN13	TxDATA[D][0]
AN14	TxDATA[D][4]
AN15	TxDATA[D][9]
AN16	TxDATA[D][13]
AN17	TxEOP[D]
AN18	TxSZ[D]
AN19	NC
AN20	RxCLK[C]
AN21	RxENB[C]
AN22	RxDATA[C][1]
AN23	RxDATA[C][5]
AN24	RxDATA[C][10]
AN25	RxDATA[C][15]
AN26	TxDATA[C][3]
AN27	TxDATA[C][8]
AN28	TxDATA[C][12]
AN29	TxPRTY[C]
AN30	TxPA[C]
AN31	NC
AN32	GNDD
AN33	VDDD
AN34	GNDD
AN35	GNDD
AP1	VDDD
AP2	VDDD
AP3	GNDD
AP4	GNDD
AP5	NC
AP6	RxTOHF[D]
AP7	NC
AP8	RxERR[D]
AP9	RxSOP/C[D]
AP10	RxDATA[D][3]
AP11	RxDATA[D][7]
AP12	RxDATA[D][12]
AP13	TxDATA[D][1]
AP14	TxDATA[D][5]
AP15	TxDATA[D][10]
AP16	TxDATA[D][14]
AP17	TxDATA[D][15]
AP18	TxPA[D]
AP19	TxCLK[D]
AP20	RxADDR[4]
AP21	RxPA[C]
AP22	RxDATA[C][0]
AP23	RxDATA[C][4]
AP24	RxDATA[C][9]
AP25	RxDATA[C][14]
AP26	TxDATA[C][2]
AP27	TxDATA[C][7]
AP28	TxDATA[C][11]
AP29	TxDATA[C][15]
AP30	TxENB[C]

Note: NC refers to no connect. Do not connect pins so designated.

Pin Information (continued)

Table 1. Pin Assignments for 600-Pin LBGA by Pin Number Order (continued)

Pin	Signal Name
AP31	TxCLK[C]
AP32	GNDD
AP33	GNDD
AP34	VDDD
AP35	VDDD
AR1	VDDD
AR2	VDDD
AR3	GNDD
AR4	GNDD
AR5	VDDD
AR6	VDDD
AR7	GNDD
AR8	GNDD
AR9	RxPRTY[D]
AR10	RxDATA[D][4]
AR11	RxDATA[D][8]
AR12	RxDATA[D][13]
AR13	GNDD
AR14	TxDATA[D][6]
AR15	TxDATA[D][11]
AR16	GNDD
AR17	TxENB[D]
AR18	VDDD
AR19	VDDD
AR20	GNDD
AR21	RxERR[C]
AR22	RxPRTY[C]
AR23	GNDD
AR24	RxDATA[C][8]
AR25	RxDATA[C][13]
AR26	TxDATA[C][1]
AR27	TxDATA[C][6]
AR28	GNDD
AR29	GNDD
AR30	VDDD
AR31	VDDD
AR32	GNDD
AR33	GNDD
AR34	VDDD
AR35	VDDD

Note: NC refers to no connect. Do not connect pins so designated.

Pin Information (continued)

Table 2. Pin Assignments for 600-Pin LBGA by Signal Name

Signal Name	Pin
ADDR[0]	E13
ADDR[1]	D13
ADDR[2]	C13
ADDR[3]	B13
ADDR[4]	E14
ADDR[5]	D14
ADDR[6]	C14
ADDR[7]	B14
ADDR[8]	A14
ADDR[9]	E15
ADDR[10]	C15
ADDR[11]	B15
ADDR[12]	A15
ADDR[13]	D16
ADDR[14]	C16
ADDR[15]	B16
$\overline{\text{ADS}}$	E9
CLKDIV	H4
$\overline{\text{CS}}$	B8
DATA[0]	B9
DATA[1]	A9
DATA[2]	E10
DATA[3]	D10
DATA[4]	C10
DATA[5]	B10
DATA[6]	A10
DATA[7]	D11
DATA[8]	C11
DATA[9]	B11
DATA[10]	A11
DATA[11]	E12
DATA[12]	D12
DATA[13]	C12
DATA[14]	B12
DATA[15]	A12
$\overline{\text{DS}}$	C9
$\overline{\text{DT}}$	E8
ECLREFHI	AG4
ECLREFLO	AG3
GNDA	C6
GNDD	A3
GNDD	A4
GNDD	A7
GNDD	A8
GNDD	A13
GNDD	A16
GNDD	A20
GNDD	A23
GNDD	A27
GNDD	A28
GNDD	A29
GNDD	A32
GNDD	A33
GNDD	B3
GNDD	B4
GNDD	B32
GNDD	B33
GNDD	C1
GNDD	C2
GNDD	C4
GNDD	C32
GNDD	C34
GNDD	C35
GNDD	D1
GNDD	D2
GNDD	D3
GNDD	D33
GNDD	D34
GNDD	D35
GNDD	F3
GNDD	G1
GNDD	G35
GNDD	H1
GNDD	H3
GNDD	H5
GNDD	H35
GNDD	N1
GNDD	N35
GNDD	T1
GNDD	T35
GNDD	V3
GNDD	V31
GNDD	Y1
GNDD	Y4
GNDD	Y35
GNDD	AA5
GNDD	AC1
GNDD	AC35
GNDD	AH1
GNDD	AH35
GNDD	AJ1
GNDD	AJ35
GNDD	AM1
GNDD	AM2
GNDD	AM3
GNDD	AM33
GNDD	AM34
GNDD	AM35
GNDD	AN1
GNDD	AN2
GNDD	AN4
GNDD	AN6
GNDD	AN32
GNDD	AN34
GNDD	AN35
GNDD	AP3
GNDD	AP32
GNDD	AP33
GNDD	AP4
GNDD	AR3
GNDD	AR4
GNDD	AR7
GNDD	AR8
GNDD	AR13
GNDD	AR16
GNDD	AR20
GNDD	AR23
GNDD	AR28
GNDD	AR29
GNDD	AR32
GNDD	AR33
GNDD PLL	E4
GPIO[0]	AH4
GPIO[1]	AH3
GPIO[2]	AH2
GPIO[3]	AG5
$\overline{\text{ICT}}$	E7
$\overline{\text{INT}}$	B7
MPCLK	C8
MPMODE	D8
NC	A19
NC	A21
NC	A22
NC	A24
NC	A25
NC	A26
NC	B5
NC	B17
NC	B18
NC	B19

Note: NC refers to no connect. Do not connect pins so designated.

Pin Information (continued)

Table 2. Pin Assignments for 600-Pin LBGA by Signal Name (continued)

Signal Name	Pin
NC	B20
NC	B21
NC	B22
NC	B23
NC	B24
NC	B25
NC	B26
NC	B27
NC	B28
NC	B29
NC	B30
NC	B31
NC	C5
NC	C17
NC	C18
NC	C19
NC	C20
NC	C21
NC	C22
NC	C23
NC	C24
NC	C25
NC	C26
NC	C27
NC	C28
NC	C29
NC	C30
NC	C31
NC	D5
NC	D6
NC	D15
NC	D17
NC	D18
NC	D19
NC	D20
NC	D21
NC	D22
NC	D23
NC	D24
NC	D25
NC	D26
NC	D28
NC	D29
NC	D30
NC	D31
NC	E2
NC	E6
NC	E17
NC	E18
NC	E19
NC	E21
NC	E22
NC	E23
NC	E24
NC	E26
NC	E27
NC	E28
NC	E29
NC	E30
NC	E32
NC	E33
NC	E34
NC	F5
NC	F31
NC	F32
NC	F33
NC	F34
NC	G4
NC	G31
NC	U33
NC	V34
NC	AL8
NC	AL19
NC	AM7
NC	AM19
NC	AN19
NC	AN31
NC	AP5
NC	AP7
PMRST	D7
R/$\overline{W}$	D9
$\overline{RST}$	C7
RxADDR[0]	W31
RxADDR[1]	W32
RxADDR[2]	AL33
RxADDR[3]	AL32
RxADDR[4]	AP20
RxCKN/RxD[A]N	V4
RxCKP/RxD[A]P	V5
RxCLK[A]	W33
RxCLK[B]	AL34
RxCLK[C]	AN20
RxCLK[D]	AM8
RxD[0]N	AG1
RxD[0]P	AG2
RxD[1]N	AF1
RxD[1]P	AF2
RxD[2]N	AF3
RxD[2]P	AF4
RxD[3]N	AE1
RxD[3]P	AE2
RxD[4]N	AE3
RxD[4]P	AE4
RxD[5]N	AD1
RxD[5]P	AD2
RxD[6]N	AD3
RxD[6]P	AD4
RxD[7]N	AC2
RxD[7]P	AC3
RxD[8]N	AC4
RxD[8]P	AC5
RxD[9]N/RxCLK[D]N	AB1
RxD[9]P/RxCLK[D]P	AB2
RxD[10]N/RxD[D]N	AB3
RxD[10]P/RxD[D]P	AB4
RxD[11]N/RxCLK[C]N	AA1
RxD[11]P/RxCLK[C]P	AA2
RxD[12]N/RxD[C]N	AA3
RxD[12]P/RxD[C]P	AA4
RxD[13]N/RxCLK[B]N	Y2
RxD[13]P/RxCLK[B]P	Y3
RxD[14]N/RxCLK[A]N	W2
RxD[14]P/RxCLK[A]P	W3
RxD[15]N/RxD[B]N	W4
RxD[15]P/RxD[B]P	W5
RxDATA[A][0]	T33
RxDATA[A][1]	T32
RxDATA[A][2]	R35
RxDATA[A][3]	R34
RxDATA[A][4]	R33
RxDATA[A][5]	R32
RxDATA[A][6]	R31
RxDATA[A][7]	P35
RxDATA[A][8]	P34
RxDATA[A][9]	P33
RxDATA[A][10]	P32
RxDATA[A][11]	P31
RxDATA[A][12]	N34
RxDATA[A][13]	N33
RxDATA[A][14]	N32

Note: NC refers to no connect. Do not connect pins so designated.

Pin Information (continued)

Table 2. Pin Assignments for 600-Pin LBGA by Signal Name (continued)

Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin
RxDATA[A][15]	N31	RxDATA[D][2]	AN10	RxSOP/C[A]	U31	TxCLK[B]	Y33
RxDATA[B][0]	AJ34	RxDATA[D][3]	AP10	RxSOP/C[B]	AJ32	TxCLK[C]	AP31
RxDATA[B][1]	AH31	RxDATA[D][4]	AR10	RxSOP/C[C]	AL21	TxCLK[D]	AP19
RxDATA[B][2]	AH32	RxDATA[D][5]	AM11	RxSOP/C[D]	AP9	TxD[0]N/TxD[D]N	U2
RxDATA[B][3]	AH33	RxDATA[D][6]	AN11	RxSZ[A]	W35	TxD[0]P/TxD[D]P	T2
RxDATA[B][4]	AH34	RxDATA[D][7]	AP11	RxSZ[B]	AK31	TxD[1]N/TxD[C]N	T3
RxDATA[B][5]	AG31	RxDATA[D][8]	AR11	RxSZ[C]	AM20	TxD[1]P/TxD[C]P	T4
RxDATA[B][6]	AG32	RxDATA[D][9]	AL12	RxSZ[D]	AN8	TxD[2]N/TxD[B]N	R2
RxDATA[B][7]	AG33	RxDATA[D][10]	AM12	RxTOHCK[A]	AK5	TxD[2]P/TxD[B]P	R3
RxDATA[B][8]	AG34	RxDATA[D][11]	AN12	RxTOHCK[B]	AL4	TxD[3]N/TxD[A]N	R5
RxDATA[B][9]	AG35	RxDATA[D][12]	AP12	RxTOHCK[C]	AL6	TxD[3]P/TxD[A]P	R4
RxDATA[B][10]	AF31	RxDATA[D][13]	AR12	RxTOHCK[D]	AL7	TxD[4]N	P1
RxDATA[B][11]	AF32	RxDATA[D][14]	AL13	RxTOHD[A]	AL2	TxD[4]P	P2
RxDATA[B][12]	AF33	RxDATA[D][15]	AM13	RxTOHD[B]	AM5	TxD[5]N	P3
RxDATA[B][13]	AF34	RxENB[A]	U34	RxTOHD[C]	AM6	TxD[5]P	P5
RxDATA[B][14]	AF35	RxENB[B]	AK34	RxTOHD[D]	AN7	TxD[6]N	N2
RxDATA[B][15]	AE32	RxENB[C]	AN21	RxTOHF[A]	AK4	TxD[6]P	N3
RxDATA[C][0]	AP22	RxENB[D]	AM9	RxTOHF[B]	AL3	TxD[7]N	N4
RxDATA[C][1]	AN22	RxEOP[A]	U32	RxTOHF[C]	AN5	TxD[7]P	N5
RxDATA[C][2]	AM22	RxEOP[B]	AJ31	RxTOHF[D]	AP6	TxD[8]N	M1
RxDATA[C][3]	AL22	RxEOP[C]	AM21	TCK	F2	TxD[8]P	M2
RxDATA[C][4]	AP23	RxEOP[D]	AN9	TDI	G5	TxD[9]N	M3
RxDATA[C][5]	AN23	RxERR[A]	V32	TDO	G2	TxD[9]P	M4
RxDATA[C][6]	AM23	RxERR[B]	AK32	TMS	F4	TxD[10]N	L1
RxDATA[C][7]	AL23	RxERR[C]	AR21	$\overline{\text{TRST}}$	G3	TxD[10]P	L2
RxDATA[C][8]	AR24	RxERR[D]	AP8	TxADDR[0]	G32	TxD[11]N	L3
RxDATA[C][9]	AP24	RxPA[A]	V33	TxADDR[1]	G33	TxD[11]P	L4
RxDATA[C][10]	AN24	RxPA[B]	AK33	TxADDR[2]	W34	TxD[12]N	K1
RxDATA[C][11]	AM24	RxPA[C]	AP21	TxADDR[3]	Y34	TxD[12]P	K2
RxDATA[C][12]	AL24	RxPA[D]	AL9	TxADDR[4]	AM31	TxD[13]N	K3
RxDATA[C][13]	AR25	RxPRTY[A]	T34	TxCKN	U5	TxD[13]P	K4
RxDATA[C][14]	AP25	RxPRTY[B]	AJ33	TxCKP	U4	TxD[14]N	J1
RxDATA[C][15]	AN25	RxPRTY[C]	AR22	TxCKQN	J5	TxD[14]P	J2
RxDATA[D][0]	AL10	RxPRTY[D]	AR9	TxCKQP	H2	TxD[15]N	J3
RxDATA[D][1]	AM10	RxREF	AK3	TxCLK[A]	G34	TxD[15]P	J4

Note: NC refers to no connect. Do not connect pins so designated.

Pin Information (continued)

Table 2. Pin Assignments for 600-Pin LBGA by Signal Name (continued)

Signal Name	Pin
TxDATA[A][0]	M35
TxDATA[A][1]	M34
TxDATA[A][2]	M33
TxDATA[A][3]	M32
TxDATA[A][4]	M31
TxDATA[A][5]	L35
TxDATA[A][6]	L34
TxDATA[A][7]	L33
TxDATA[A][8]	L32
TxDATA[A][9]	K35
TxDATA[A][10]	K34
TxDATA[A][11]	K33
TxDATA[A][12]	K32
TxDATA[A][13]	K31
TxDATA[A][14]	J35
TxDATA[A][15]	J34
TxDATA[B][0]	AE33
TxDATA[B][1]	AE34
TxDATA[B][2]	AE35
TxDATA[B][3]	AD31
TxDATA[B][4]	AD32
TxDATA[B][5]	AD33
TxDATA[B][6]	AD34
TxDATA[B][7]	AD35
TxDATA[B][8]	AC31
TxDATA[B][9]	AC32
TxDATA[B][10]	AC33
TxDATA[B][11]	AC34
TxDATA[B][12]	AB32
TxDATA[B][13]	AB31
TxDATA[B][14]	AB33
TxDATA[B][15]	AB34
TxDATA[C][0]	AM25
TxDATA[C][1]	AR26
TxDATA[C][2]	AP26
TxDATA[C][3]	AN26
TxDATA[C][4]	AM26
TxDATA[C][5]	AL26
TxDATA[C][6]	AR27
TxDATA[C][7]	AP27
TxDATA[C][8]	AN27
TxDATA[C][9]	AM27
TxDATA[C][10]	AL27
TxDATA[C][11]	AP28
TxDATA[C][12]	AN28
TxDATA[C][13]	AM28
TxDATA[C][14]	AL28
TxDATA[C][15]	AP29
TxDATA[D][0]	AN13
TxDATA[D][1]	AP13
TxDATA[D][2]	AM14
TxDATA[D][3]	AL14
TxDATA[D][4]	AN14
TxDATA[D][5]	AP14
TxDATA[D][6]	AR14
TxDATA[D][7]	AM15
TxDATA[D][8]	AL15
TxDATA[D][9]	AN15
TxDATA[D][10]	AP15
TxDATA[D][11]	AR15
TxDATA[D][12]	AM16
TxDATA[D][13]	AN16
TxDATA[D][14]	AP16
TxDATA[D][15]	AP17
TxENB[A]	H34
TxENB[B]	AA33
TxENB[C]	AP30
TxENB[D]	AR17
TxEOP[A]	J31
TxEOP[B]	AA31
TxEOP[C]	AL29
TxEOP[D]	AN17
TxERR[A]	H32
TxERR[B]	AA35
TxERR[C]	AM30
TxERR[D]	AM18
TxFSYNCN	U1
TxFSYNCP	U3
TxPA[A]	H33
TxPA[B]	AA34
TxPA[C]	AN30
TxPA[D]	AP18
TxPRTY[A]	J33
TxPRTY[B]	AB35
TxPRTY[C]	AN29
TxPRTY[D]	AM17
TxSOP/C[A]	J32
TxSOP/C[B]	AA32
TxSOP/C[C]	AM29
TxSOP/C[D]	AL17
TxSZ[A]	H31
TxSZ[B]	Y32
TxSZ[C]	AL30
TxSZ[D]	AN18
TxTOHCK	AJ2
TxTOHD[A]	AJ3
TxTOHD[B]	AJ4
TxTOHD[C]	AJ5
TxTOHD[D]	AK2
TxTOHF	AH5
VDDA	B6
VDDD	A1
VDDD	A2
VDDD	A5
VDDD	A6
VDDD	A17
VDDD	A18
VDDD	A30
VDDD	A31
VDDD	A34
VDDD	A35
VDDD	B1
VDDD	B2
VDDD	B34
VDDD	B35
VDDD	C3
VDDD	C33
VDDD	D4
VDDD	D27
VDDD	D32
VDDD	E1
VDDD	E5
VDDD	E11
VDDD	E16
VDDD	E20
VDDD	E25
VDDD	E31
VDDD	E35
VDDD	F1
VDDD	F35
VDDD	K5
VDDD	L5
VDDD	L31
VDDD	M5
VDDD	P4
VDDD	R1
VDDD	T5
VDDD	T31
VDDD	U35
VDDD	V1

Note: NC refers to no connect. Do not connect pins so designated.

Pin Information (continued)

Table 2. Pin Assignments for 600-Pin LBGA by Signal Name (continued)

Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin
V_{DDD}	V2	V_{DDD}	AK1	V_{DDD}	AL35	V_{DDD}	AR2
V_{DDD}	V35	V_{DDD}	AK35	V_{DDD}	AM4	V_{DDD}	AR5
V_{DDD}	W1	V_{DDD}	AL1	V_{DDD}	AM32	V_{DDD}	AR6
V_{DDD}	Y5	V_{DDD}	AL5	V_{DDD}	AN3	V_{DDD}	AR18
V_{DDD}	Y31	V_{DDD}	AL11	V_{DDD}	AN33	V_{DDD}	AR19
V_{DDD}	AB5	V_{DDD}	AL16	V_{DDD}	AP1	V_{DDD}	AR30
V_{DDD}	AD5	V_{DDD}	AL18	V_{DDD}	AP2	V_{DDD}	AR31
V_{DDD}	AE5	V_{DDD}	AL20	V_{DDD}	AP34	V_{DDD}	AR34
V_{DDD}	AE31	V_{DDD}	AL25	V_{DDD}	AP35	V_{DDD}	AR35
V_{DDD}	AF5	V_{DDD}	AL31	V_{DDD}	AR1	V_{DDD} PLL	E3

Note: NC refers to no connect. Do not connect pins so designated.

Pin Information (continued)

Note: 3.3 V CMOS logic inputs are 5 V tolerant. Logic inputs can be driven from standard TTL levels, and logic outputs can drive standard TTL inputs. All LVPECL buffers are differential. LVPECL is compliant with low-voltage (3.3 V) pseudo-emitter-coupled logic interface levels. All PECL outputs, including ECLREFHI and ECLREFLO require terminating resistors. The rquired termination for the PECL buffers is 50 Ω to a terminating voltage of VDDD – 2 V. The Thevenin equivalent is also acceptable (130 Ω to VDDD and 82 Ω to GNDD). Other termination syles are not recommended. LVPECL inputs with a / in the name indicate multiple functionality. The name preceding the / is the function in STS-48/STM-16 mode. The name after the / is the function in STS-3/STM-1 or STS-12/STM-4 mode.

Table 3. Pin Descriptions—Line Interface Signals

Unused LVPECL outputs should not be terminated to minimize power consumption. Unused inputs are internally disabled whenever core registers 0x0010 and 0x0011 are properly provisioned. The unused inputs can be considered to be NC (no connect).

Pin	Symbol	Type	I/O	Name/Description
V5	RxCKP/ RxD[A]P	LVPECL	I	**Receive Line Clock (STS-48/STM-16)/Receive Line Data Input Channel A.** In STS-48/STM-16 mode, these pins function as receive line clock. This 155.52 MHz clock comes from an external clock data recovery circuit. This clock is used to clock in the RxD[15:0] receive line data inputs. In STS-3/STM-1 or STS-12/STM-4 mode, these pins function as receive data input channel A at 155.52 Mbits/s or 622.08 Mbits/s, respectively. This buffer is internally disabled when not in STS-48/STM-16 mode and channel A is disabled. This buffer is internally disabled through proper provisioning when the input is not active.
V4	RxCKN/ RxD[A]N			
AG2	RxD[0]P	LVPECL	I	**Receive Line Data Inputs (STS-48/STM-16).** In STS-48/STM-16 mode, these pins function as Receive Line Data Inputs [0:8]. The remaining receive line data inputs [9:15] are listed below and are multiplexed for use in the STS-3/STM-1 or STS-12/STM-4 modes. The 2.488 Gbits/s STS-48/STM-16 serial data stream is converted to a 155.52 Mbits/s parallel 16-bit word external to TDAT042G5 by a demultiplexer. All 32 differential data input pins, RxD[15:0]P/N, are used as the parallel data input bus in the STS-48/STM-16 mode. These pins constitute a 155.52 Mbits/s parallel 16-bit word-aligned to the RxCKP/N 155.52 MHz receive line clock. RxD[15] is the most significant bit and is the first bit received. RxD[0] is the least significant bit and is the last bit received. This buffer is internally disabled through proper provisioning when the input is not active.
AG1	RxD[0]N			
AF2	RxD[1]P	LVPECL		
AF1	RxD[1]N			
AF4	RxD[2]P	LVPECL		
AF3	RxD[2]N			
AE2	RxD[3]P	LVPECL		
AE1	RxD[3]N			
AE4	RxD[4]P	LVPECL		
AE3	RxD[4]N			
AD2	RxD[5]P	LVPECL		
AD1	RxD[5]N			
AD4	RxD[6]P	LVPECL		
AD3	RxD[6]N			
AC3	RxD[7]P	LVPECL		
AC2	RxD[7]N			
AC5	RxD[8]P	LVPECL		
AC4	RxD[8]N			
AB2	RxD[9]P/ RxCLK[D]P	LVPECL	I	**Receive Line Data Input [9]/Receive Line Clock Channel D.** In STS-48/STM-16 mode, these pins function as receive line data input [9] at 155.52 Mbits/s. In STS-3/STM-1 or STS-12/STM-4 mode, these pins function as receive line clock channel D at either 155.52 MHz (STS-3/STM-1) or 622.08 MHz (STS-12/STM-4). This buffer is internally disabled when not in STS-48/STM-16 mode and channel D is disabled. This buffer is internally disabled through proper provisioning when the input is not active.
AB1	RxD[9]N/ RxCLK[D]N			

Pin Information (continued)

Table 3. Pin Descriptions—Line Interface Signals (continued)

Unused LVPECL outputs should not be terminated to minimize power consumption. Unused inputs are internally disabled whenever Core registers 0x0010 and 0x0011 are properly provisioned. The unused inputs can be considered to be NC (no connect).

Pin	Symbol	Type	I/O	Name/Description
AB4	RxD[10]P/ RxD[D]P	LVPECL	I	**Receive Line Data Input [10]/Receive Line Data Input Channel D.** In STS-48/STM-16 mode, these pins function as receive line data input [10] at 155.52 Mbits/s. In STS-3/STM-1 or STS-12/STM-4 mode, these pins function as receive line data input channel D at either 155.52 Mbits/s (STS-3/ STM-1) or 622.08 Mbits/s (STS-12/STM-4). This buffer is internally disabled when not in STS-48/STM-16 mode and channel D is disabled. This buffer is internally disabled through proper provisioning when the input is not active.
AB3	RxD[10]N/ RxD[D]N			
AA2	RxD[11]P/ RxCLK[C]P	LVPECL	I	**Receive Line Data Input [11]/Receive Line Clock Channel C.** In STS-48/STM-16 mode, these pins function as receive line data input [11] at 155.52 Mbits/s. In STS-3/STM-1 or STS-12/STM-4 mode, these pins function as receive line clock channel C at either 155.52 MHz (STS-3/STM-1) or 622.08 MHz (STS-12/STM-4). This buffer is internally disabled when not in STS-48/STM-16 mode and channel C is disabled. This buffer is internally disabled through proper provisioning when the input is not active.
AA1	RxD[11]N/ RxCLK[C]N			
AA4	RxD[12]P/ RxD[C]P	LVPECL	I	**Receive Line Data Input [12]/Receive Line Data Input Channel C.** In STS-48/STM-16 mode, these pins function as Receive Line Data Input [12] at 155.52 Mbits/s. In STS-3/STM-1 or STS-12/STM-4 mode, these pins function as receive line data input channel C at either 155.52 Mbits/s (STS-3/ STM-1) or 622.08 Mbits/s (STS-12/STM-4). This buffer is internally disabled when not in STS-48/STM-16 mode and channel C is disabled. This buffer is internally disabled through proper provisioning when the input is not active.
AA3	RxD[12]N/ RxD[C]N			
Y3	RxD[13]P/ RxCLK[B]P	LVPECL	I	**Receive Line Data Input [13]/Receive Line Clock Channel B.** In STS-48/STM-16 mode, these pins function as receive line data input [13] at 155.52 Mbits/s. In STS-3/STM-1 or STS-12/STM-4 mode, these pins function as receive line clock channel B at either 155.52 MHz (STS-3/STM-1) or 622.08 MHz (STS-12/STM-4). This buffer is internally disabled when not in STS-48/STM-16 mode and channel B is disabled. This buffer is internally disabled through proper provisioning when the input is not active.
Y2	RxD[13]N/ RxCLK[B]N			
W3	RxD[14]P/ RxCLK[A]P	LVPECL	I	**Receive Line Data Input [14]/Receive Line Clock Channel A.** In STS-48/STM-16 mode, these pins function as receive line data input [14] at 155.52 Mbits/s. In STS-3/STM-1 or STS-12/STM-4 mode, these pins function as receive line clock channel A at either 155.52 MHz (STS-3/STM-1) or 622.08 MHz (STS-12/STM-4). This buffer is internally disabled when not in STS-48/STM-16 mode and channel A is disabled. This buffer is internally disabled through proper provisioning when the input is not active.
W2	RxD[14]N/ RxCLK[A]N			

Pin Information (continued)

Table 3. Pin Descriptions—Line Interface Signals (continued)

Unused LVPECL outputs should not be terminated to minimize power consumption. Unused inputs are internally disabled whenever Core registers 0x0010 and 0x0011 are properly provisioned. The unused inputs can be considered to be NC (no connect).

Pin	Symbol	Type	I/O*	Name/Description
W5	RxD[15]P/ RxD[B]P	LVPECL	I	**Receive Line Data Input [15]/Receive Line Data Input Channel B.** In STS-48/STM-16 mode, these pins function as receive line data input [15] at 155.52 Mbits/s. In STS-3/STM-1 or STS-12/STM-4 mode, these pins function as receive line data input channel B at either 155.52 Mbits/s (STS-3/STM-1) or 622.08 Mbits/s (STS-12/STM-4). This buffer is internally disabled when not in STS-48/STM-16 mode and channel B is disabled. This buffer is internally disabled through proper provisioning when the input is not active.
W4	RxD[15]N/ RxD[B]N			
H4	CLKDIV	3.3 V (5 V tolerant)	I^u	**Clock Division.** This pin controls a divider in the line transmit block to create a 77.76 MHz clock from either the 155.52 MHz STS-3/STM-1 or STS-48/STM-16 transmit line clock, or the 622.08 MHz STS-12/STM-4 transmit line clock, TxCKP/N. CLKDIV = 1 for STS-12/STM-4 (divide by 8). CLKDIV = 0 for STS-3/STM-1 and STS-48 /STM-16 (divide by 2).
AG3	ECLREFLO	—	O	**Reference Voltage for LVPECL I/O Buffers.** ECLREFLO and ECLREFHI are buffer outputs which provide the reference for the output level of the LVPECL output buffers. ECLREFLO and ECLREFHI must be connected to a 50 Ω source of VDDD – 2 V.[†] No user-accessible signal is present on these pins.
AG4	ECLREFHI	—	O	

* I^u = internal pull-up resistance, I^d = internal pull-down resistance.

† This may be obtained from a passive voltage divider of a 130 Ω resistor connected from VDDD to one end of an 82 Ω resistor, the other end of which is connected to GNDD.

Pin Information (continued)

Table 3. Pin Descriptions—Line Interface Signals (continued)

Unused LVPECL outputs should not be terminated to minimize power consumption. Unused inputs are internally disabled whenever Core registers 0x0010 and 0x0011 are properly provisioned. The unused inputs can be considered to be NC (no connect).

Pin	Symbol	Type	I/O*	Name/Description
U4	TxCKP	LVPECL	I	**Transmit Line Clock.** When in STS-48/STM-16 mode, this clock is a 155.52 MHz input and clocks out TxD[15:0]P/N or TxD[D:A]. When in STS-12/STM-4 mode, this clock is a 622.08 MHz input and clocks out TxD[D:A]P/N. When in STS-3/STM-1 mode, this clock is a 155.52 MHz input and clocks out TxD[D:A]P/N.
U5	TxCKN			
U3	TxFSYNCP	LVPECL	I^u	**Transmit Line Frame Sync.** This input is the external 8 kHz transmit line frame sync. Driving this input is optional. If undriven from an external source, these pins must be no connects. When this input is used, it must be (1) synchronized to TxCKP/N, and (2) at least one TxCKP/N cycle wide, up to a maximum of 125 µs minus 2 TxCKP/N cycles wide.
U1	TxFSYNCN		I^d	
T2	TxD[0]P/ TxD[D]P	LVPECL	O	**Transmit Line Data Output [0]/Transmit Line Data Output Channel D.** In STS-48/STM-16 mode, the pins function as transmit line data output [0] at 155.52 Mbits/s. In STS-3/STM-1 or STS-12/STM-4 mode, the pins function as transmit data output channel D at either 155.52 Mbits/s or 622.08 Mbits/s. This buffer is internally disabled through proper provisioning when the input is not active.
U2	TxD[0]N/ TxD[D]N			
T4	TxD[1]P/ TxD[C]P	LVPECL	O	**Transmit Line Data Output [1]/Transmit Line Data Output Channel C.** In STS-48/STM-16 mode, the pins function as transmit line data output [1] at 155.52 Mbits/s. In STS-3/STM-1 or STS-12/STM-4 mode, the pins function as transmit data output channel C at either 155.52 Mbits/s or 622.08 Mbits/s. This buffer is internally disabled through proper provisioning when the input is not active.
T3	TxD[1]N/ TxD[C]N			
R3	TxD[2]P/ TxD[B]P	LVPECL	O	**Transmit Line Data Output [2]/Transmit Line Data Output Channel B.** In STS-48/STM-16 mode, the pins function as transmit line data output [2] at 155.52 Mbits/s. In STS-3/STM-1 or STS-12/STM-4 mode, the pins function as transmit data output channel B at either 155.52 Mbits/s or 622.08 Mbits/s. This buffer is internally disabled through proper provisioning when the input is not active.
R2	TxD[2]N/ TxD[B]N			
R4	TxD[3]P/ TxD[A]P	LVPECL	O	**Transmit Line Data Output [3]/Transmit Line Data Output Channel A.** In STS-48/STM-16 mode, the pins function as transmit line data output [3] at 155.52 Mbits/s. In STS-3/STM-1 or STS-12/STM-4 mode, the pins function as transmit data output channel A at either 155.52 Mbits/s or 622.08 Mbits/s. This buffer is internally disabled through proper provisioning when the input is not active.
R5	TxD[3]N/ TxD[A]N			

* I^u = internal pull-up resistance, I^d = internal pull-down resistance.

Pin Information (continued)

Table 3. Pin Descriptions—Line Interface Signals (continued)

Unused LVPECL outputs should not be terminated to minimize power consumption. Unused inputs are internally disabled whenever Core registers 0x0010 and 0x0011 are properly provisioned. The unused inputs can be considered to be NC (no connect).

Pin	Symbol	Type	I/O	Name/Description
H2	TxCKQP	LVPECL	O	**Transmit Line Clock Q.** This 155.52 MHz clock is used to clock out the data in the STS-48/STM-16 mode for forward-directional timing with the 155 Mbits/s 16-bit parallel-to-2.5 Gbits/s serial MUX. For an STS-48/STM-16 contra-clocking interface with the 155 Mbits/s parallel-to-2.5 Gbits/s serial MUX, this clock is not used. In the contra-clocking mode, a phase-locked version of TxCKP/N as supplied by the MUX, is used to clock out data. In the contra-clocking mode, the TxCKP/N PLL must be active (see Core register map 0x0010, bit 5 (PLL_ MODE). This clock is not used in the STS-3/STM-1 or STS-12/STM-4 modes.
J5	TxCKQN			
P2	TxD[4]P	LVPECL	O	**Transmit Line Data Outputs (STS-48/STM-16).** In STS-48/STM-16 mode, these pins function as Transmit Line Data Outputs [4:15]. The remaining transmit line data outputs [0:3] are listed below and are multiplexed for use in the STS-3/STM-1 or STS-12/STM-4 modes. The 155.52 Mbits/s 16-bit word parallel bus is converted to a 2.488 Gbits/s serial data stream external to TDAT042G5 by a multiplexer. All 32 differential data output pins, TxD[15:0]P/N, are used as the parallel data output bus in the STS-48/STM-16 mode. These pins constitute a 155.52 Mbyte/s parallel 16-bit word-aligned to the TxCKP/N and TxCKQP/N 155.52 MHz Transmit Line Clock. TxD[15] is the most significant bit and is the first bit transmitted. TxD[0] is the least significant bit and is the last bit transmitted. This buffer is internally disabled through proper provisioning when the input is not active.
P1	TxD[4]N			
P5	TxD[5]P	LVPECL		
P3	TxD[5]N			
N3	TxD[6]P	LVPECL		
N2	TxD[6]N			
N5	TxD[7]P	LVPECL		
N4	TxD[7]N			
M2	TxD[8]P	LVPECL		
M1	TxD[8]N			
M4	TxD[9]P	LVPECL		
M3	TxD[9]N			
L2	TxD[10]P	LVPECL		
L1	TxD[10]N			
L4	TxD[11]P	LVPECL		
L3	TxD[11]N			
K2	TxD[12]P	LVPECL		
K1	TxD[12]N			
K4	TxD[13]P	LVPECL		
K3	TxD[13]N			
J2	TxD[14]P	LVPECL		
J1	TxD[14]N			
J4	TxD[15]P	LVPECL		
J3	TxD[15]N			

Pin Information (continued)

Table 4. Pin Descriptions—TOH Interface Signals

Pin	Symbol	Type	I/O*	Name/Description
AK3	RxREF	3.3 V	O	**Receive Line Frame.** This output provides the receive 8 kHz frame reference for external timing needs. RxREF is derived from one of the received line clocks (user-selectable). It is a 50% duty cycle clock when TDAT042G5 is in frame. This signal may be used to implement line timing on a SONET ring. When not provisioned, this signal must not be used.
AL7 AL6 AL4 AK5	RxTOHCK[D] RxTOHCK[C] RxTOHCK[B] RxTOHCK[A]	3.3 V	O	**Receive TOH Interface Clock.** This clock is nominally a 5.184 MHz (STS-3/STM-1) or 20.736 MHz (STS-12/STM-4, STS-48/STM-16) clock which provides timing for circuitry that receives and externally processes the receive transport overhead bytes. The duty cycle of the clock is not 50% (see Figure 42, page 251). In STS-48/STM-16 mode, all four of these clocks are active.
AN7 AM6 AM5 AL2	RxTOHD[D] RxTOHD[C] RxTOHD[B] RxTOHD[A]	3.3 V	O	**Receive TOH Interface Data.** This 5.184 Mbits/s or 20.736 Mbits/s signal contains all the receive transport overhead bytes (A1, A2, J0/Z0, B1, E1, F1, D1—D3, H1—H3, K1, K2, D4—D12, S1/Z1, M0, and E2) for all 3/12/48 STS-1s. This signal can be used by external circuitry to process the TOH bytes. RxTOHD is updated on the falling edge of RxTOHCK. In STS-48/STM-16 mode, RxTOHD[A] contains all currently defined TOH bits except for M1, which is located in RxTOHD[C].
AP6 AN5 AL3 AK4	RxTOHF[D] RxTOHF[C] RxTOHF[B] RxTOHF[A]	3.3 V	O	**Receive TOH Interface Frame.** This 8 kHz framing signal is used to locate the individual receive transport overhead bits in the RxTOHD bit stream. RxTOHF is only high while bit 1 (MSB) of the first framing byte (A1 during parity time in first byte) is present on the RxTOHD output. RxTOHF is updated on the falling edge of RxTOHCK.
AJ2	TxTOHCK	3.3 V	O	**Transmit TOH Interface Clock.** This clock is nominally a 5.184 MHz (STS-3/STM-1), 20.736 MHz (STS-12/STM-4), or a 20.736 MHz (STS-48/STM-16) clock which provides timing for circuitry that externally generates and transmits the transmit transport overhead bytes for inclusion in the transmit data stream. The duty cycle of the clock is not 50% (see Figure 41, page 251).
AK2 AJ5 AJ4 AJ3	TxTOHD[D] TxTOHD[C] TxTOHD[B] TxTOHD[A]	3.3 V (5 V tolerant)	I^u	**Transmit TOH Interface Data.** This 5.184 Mbits/s or 20.736 Mbits/s signal contains all the transmit transport overhead bytes (A1, A2, J0/Z0, B1, E1, F1, D1—D3, H1—H3, K1, K2, D4—D12, S1/Z1, M0, and E2) for all 3/12/48 STS-1s. This signal is generated by external circuitry for custom TOH byte definitions. TxTOHD is sampled on the rising edge of TxTOHCK.
AH5	TxTOHF	3.3 V	O	**Transmit TOH Interface Frame.** This 8 kHz framing signal is used to align the individual transmit transport overhead bits in the TxTOHD bit stream. TxTOHF is only high while bit 1 (MSB) of the first framing byte (A1 during parity time in first byte) is expected on the TxTOHD input. TxTOHF is updated on the falling edge of TxTOHCK.

* I^u = internal pull-up resistance, I^d = internal pull-down resistance.

Pin Information (continued)

Note: An external pull-up resistor of 50 kΩ—100 kΩ is required on all input pins of a disabled UTOPIA port. Either an external pull-up resistor of 50 kΩ—100 kΩ or an external pull-down resistor of 0 Ω—1 kΩ is required on all unused inputs of an enabled UTOPIA port. Use of either a pull-up or pull-down resistor is selected to place the unused input pin into the inactive state.

Table 5. Pin Descriptions—Enhanced UTOPIA Interface Signals

Pin	Symbol	Type	I/O	Name/Description
AM31 Y34 W34 G33 G32	TxADDR[4] TxADDR[3] TxADDR[2] TxADDR[1] TxADDR[0]	3.3 V (5 V tolerant)	I	**Transmit Address.** The TxADDR is driven by the UTOPIA master to poll and select the appropriate PHY channel of TDAT042G5 to transmit data. **Note:** The PHY address (0x00 to 0x1E) for each of the four channels in TDAT042G5 is configured via software provisioning.
J34 J35 K31 K32 K33 K34 K35 L32 L33 L34 L35 M31 M32 M33 M34 M35	TxDATA[A][15] TxDATA[A][14] TxDATA[A][13] TxDATA[A][12] TxDATA[A][11] TxDATA[A][10] TxDATA[A][9] TxDATA[A][8] TxDATA[A][7] TxDATA[A][6] TxDATA[A][5] TxDATA[A][4] TxDATA[A][3] TxDATA[A][2] TxDATA[A][1] TxDATA[A][0]	3.3 V (5 V tolerant)	I	**Transmit Data Channel A.** Used to transport data into the UTOPIA PHY Tx block. TxDATA[A] is only valid when TxENB[A] is asserted, and is sampled on the rising edge of TxCLK[A]. Note that TxDATA[A] is used in various UTOPIA modes. In U2 or U2+, all 16 bits are valid. In U3 or U3+ (8-bit mode), only bits 15 to 8 are valid. In U3 or U3+ (32-bit mode), TxDATA[A][15:0] forms the most significant 16 bits of the combined data bus (bits 31 to 16), and TxDATA[B][15:0] forms the least significant 16 bits of the combined data bus (bits 15 to 0).
AB34 AB33 AB31 AB32 AC34 AC33 AC32 AC31 AD35 AD34 AD33 AD32 AD31 AE35 AE34 AE33	TxDATA[B][15] TxDATA[B][14] TxDATA[B][13] TxDATA[B][12] TxDATA[B][11] TxDATA[B][10] TxDATA[B][9] TxDATA[B][8] TxDATA[B][7] TxDATA[B][6] TxDATA[B][5] TxDATA[B][4] TxDATA[B][3] TxDATA[B][2] TxDATA[B][1] TxDATA[B][0]	3.3 V (5 V tolerant)	I	**Transmit Data Channel B.** Used to transport data into the UTOPIA PHY Tx block. TxDATA[B] is only valid when TxENB[B] is asserted (TxENB[A] for U3 or U3+ (32-bit mode)), and is sampled on the rising edge of TxCLK[B] (TxCLK[A] for U3 or U3+ (32-bit mode). Note that TxDATA[B] is used in various UTOPIA modes. In U2 or U2+, all 16 bits are valid. In U3 or U3+ (8-bit mode), only bits 15 to 8 are valid. In U3 or U3+ (32-bit mode), TxDATA[B][15:0] forms the lest significant 16 bits of the combined data bus (bits 15 to 0), and TxDATA[A][15:0] forms the most significant 16 bits of the combined data bus (bits 31 to 16). In this mode, channel B port must be provisioned to the idle (default) state.

Note: [15:0] refers to a 16-bit data bus (15 = MSB, 0 = LSB).

Pin Information (continued)

Table 5. Pin Descriptions—Enhanced UTOPIA Interface Signals (continued)

Pin	Symbol	Type	I/O	Name/Description
AP29 AL28 AM28 AN28 AP28 AL27 AM27 AN27 AP27 AR27 AL26 AM26 AN26 AP26 AR26 AM25	TxDATA[C][15] TxDATA[C][14] TxDATA[C][13] TxDATA[C][12] TxDATA[C][11] TxDATA[C][10] TxDATA[C][9] TxDATA[C][8] TxDATA[C][7] TxDATA[C][6] TxDATA[C][5] TxDATA[C][4] TxDATA[C][3] TxDATA[C][2] TxDATA[C][1] TxDATA[C][0]	3.3 V (5 V tolerant)	I	**Transmit Data Channel C.** Used to transport data into the UTOPIA PHY Tx block. TxDATA[C] is only valid when TxENB[C] is asserted, and is sampled on the rising edge of TxCLK[C]. Note that TxDATA[C] is used in various UTOPIA modes. In U2 or U2+, all 16 bits are valid. In U3 or U3+ (8-bit mode), only bits 15 to 8 are valid. In U3 or U3+ (32-bit mode), channel C port is considered disabled, and must be provisioned to the idle (default) state.
AP17 AP16 AN16 AM16 AR15 AP15 AN15 AL15 AM15 AR14 AP14 AN14 AL14 AM14 AP13 AN13	TxDATA[D][15] TxDATA[D][14] TxDATA[D][13] TxDATA[D][12] TxDATA[D][11] TxDATA[D][10] TxDATA[D][9] TxDATA[D][8] TxDATA[D][7] TxDATA[D][6] TxDATA[D][5] TxDATA[D][4] TxDATA[D][3] TxDATA[D][2] TxDATA[D][1] TxDATA[D][0]	3.3 V (5 V tolerant)	I	**Transmit Data Channel D.** Used to transport data into the UTOPIA PHY Tx block. TxDATA[D] is only valid when TxENB[D] is asserted, and is sampled on the rising edge of TxCLK[D] (TxCLK[A] for U3+, 32-bit mode). Note that TxDATA[D] is used in various UTOPIA modes. In U2 or U2+, all 16 bits are valid. In U3 or U3+ (8-bit mode), only bits 15 to 8 are valid. In U3 or U3+ (32-bit mode), channel D port is considered disabled, and must be provisioned to the idle (default) state.
AM17 AN29 AB35 J33	TxPRTY[D] TxPRTY[C] TxPRTY[B] TxPRTY[A]	3.3 V (5 V tolerant)	I	**Transmit Parity.** This signal indicates the parity on the TxDATA[D:A][15:0] bus. A parity error raises an alarm but does not cause the cell/packet to be dropped. Odd or even parity may be provisioned through a software register. TxPRTY[D:A] is considered valid only when TxENB[D:A] is asserted, and is sampled on the rising edge of TxCLK[D:A]. In U3 or U3+ (32-bit mode), the TxPRTY[A] parity pin of port A indicates the parity for the entire 32-bit data input.

Note: [15:0] refers to a 16-bit data bus (15 = MSB, 0 = LSB).

Pin Information (continued)

Table 5. Pin Descriptions—Enhanced UTOPIA Interface Signals (continued)

Pin	Symbol	Type	I/O	Name/Description
AL17 AM29 AA32 J32	TxSOP/C[D] TxSOP/C[C] TxSOP/C[B] TxSOP/C[A]	3.3 V (5 V tolerant)	I	**Transmit Start of Packet/Cell.** In ATM mode, the TxSOP/C[D:A] signal marks the start of a cell on the TxDATA[D:A][15:0] bus. When TxSOP/C[D:A] is active, the first word of the cell is present on the TxDATA[D:A][15:0] bus. In packet modes, the TxSOP/C[D:A] signal marks the start of a packet on the TxDATA[D:A][15:0] bus. When TxSOP/C[D:A] is active, the first word of the packet is present on the TxDATA[D:A][15:0] bus. TxSOP/C[D:A] is considered valid only when TxENB[D:A] is asserted, and is sampled on the rising edge of TxCLK[D:A]. In U3 or U3+ (32-bit mode), only the TxSOP/C[A] pin of port A is used to indicate a start of packet/cell for the 32-bit data input.
AP18 AN30 AA34 H33	TxPA[D] TxPA[C] TxPA[B] TxPA[A]	3.3 V	O	**Transmit Cell or Packet Available.** This signal indicates when the TDAT042G5 transmit FIFO can accept data from the master device. If the FIFO is empty or more than the provisioned space is available in the FIFO, TxPA[D:A] is set active. **TxPA[D:A] Assertion (High)** The TxPA[D:A] signal behavior relies on the UTOPIA provisionable watermarks. In packet mode, TxPA[D:A] goes high when the amount of data in the FIFO is less than the high watermark setting. In ATM mode, TxPA goes high when the FIFO has space to receive a complete ATM cell from the master. This requires the high threshold to be set appropriately by the user, i.e., set so that an entire cell can be received once TxPA[D:A] goes active. **TxPA[D:A] Deassertion (Low)** In packet mode, TxPA[D:A] goes low when the amount of data in the FIFO reaches or exceeds the high watermark. In ATM mode, TxPA[D:A] goes low when there is not enough space in the FIFO to receive an entire ATM cell. This requires the threshold values to be provisioned properly, i.e., set low enough such that when the high watermark is reached the transmission of the current cell can be completed without overflowing the FIFO. In ATM mode, TxPA[D:A] will be deasserted four cycles before the end of the current cell transfer if the FIFO cannot accept a complete ATM cell on the following transmission. TxPA[D:A] is updated on the rising edge of TxCLK[D:A]. In U3 or U3+ (32-bit mode), only the TxPA[A] pin of port A is used to indicate the packet/cell available status. When the TxPA signals are used for multi-PHY (MPHY) direct status, the corresponding TxCLK[B, C, and/or D] must be provided. This clock will be the same as TxCLK[A].

Note: [15:0] refers to a 16-bit data bus (15 = MSB, 0 = LSB).

Pin Information (continued)

Table 5. Pin Descriptions—Enhanced UTOPIA Interface Signals (continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>I/O</th><th>Name/Description</th></tr>
<tr><td>AP19
AP31
Y33
G34</td><td>TxCLK[D]
TxCLK[C]
TxCLK[B]
TxCLK[A]</td><td>3.3 V
(5 V tolerant)</td><td>I</td><td>Transmit Clock. This clock is used to write cells or packets into the transmit FIFO. TxCLK[D:A] can operate at speeds from dc to 104 MHz.
In U3 or U3+ (32-bit mode), only the TxCLK[A] input pin of port A is used to clock the data input.
If MPHY direct status is used, then all clocks TxCLK[D:A] must be provided.</td></tr>
<tr><td>AR17
AP30
AA33
H34</td><td>TxENB[D]
TxENB[C]
TxENB[B]
TxENB[A]</td><td>3.3 V
(5 V tolerant)</td><td>I</td><td>Transmit Data Enable (Active-Low). This signal is used to transfer data on the TxDATA[D:A][15:0] bus into the transmit FIFOs. If TxENB[D:A] is high, no operation is performed. If TxENB[D:A] is low, a write occurs.
TxENB[D:A] is sampled on the rising edge of TxCLK[D:A]. TxENB[D:A] has the same meaning as data valid.
In U3 or U3+ (32-bit mode), only the TxENB[A] input pin of port A is used to enable the transfer of data.</td></tr>
<tr><td>AN18
AL30
Y32
H31</td><td>TxSZ[D]
TxSZ[C]
TxSZ[B]
TxSZ[A]</td><td>3.3 V
(5 V tolerant)</td><td>I</td><td>Transmit Size. This signal defines the valid bytes transmitted and their packing within (1) TxDATA[D:A][15:0] for U2+ 16-bit mode, and (2) TxDATA[A][15:0] and TxDATA[B][15:0] for the U3 or U3+ (32-bit mode). The meaning of these bits may be inverted through UT register 0x0226 TxSZ/RxSZ mode.
In U2 and U3+ (8-bit modes), TxSZ[D:A] are unused.
For U2+ 16-bit mode,
TxSZ[D:A] = 0 defines the MSByte of TxDATA[D:A][15:0], i.e., TxDATA[D:A][15:8], to be the last byte of the packet transmitted when using the default configuration.
TxSZ[D:A] = 1 defines the LSByte of TxDATA[D:A][15:0], i.e. TxDATA[D:A][7:0], to be the last byte of the packet transmitted when using the default configuration.
For U3 or U3+ (32-bit mode), TxSZ[A] and TxSZ[B] are combined to define four states of the transmitted data stream. TxSZ[C] and TxSZ[D] are unused. The following states are assigned by TxSZ[A] and TxSZ[B] when TxEOP[A] is asserted when using the default configuration. TxSZ[D:A] is ignored when TxEOP[D:A] is not present.
<table>
<tr><th></th><th></th><th colspan="2">TxDATA[A]</th><th colspan="2">TxDATA[B]</th></tr>
<tr><th></th><th></th><th>TxDATA[A][15:8]</th><th>TxDATA[A][7:0]</th><th>TxDATA[B][15:8]</th><th>TxDATA[B][7:0]</th></tr>
<tr><th>TxSZ[A]</th><th>TxSZ[B]</th><th>DATA[31:24]</th><th>DATA[23:16]</th><th>DATA[15:8]</th><th>DATA[7:0]</th></tr>
<tr><td>0</td><td>0</td><td>Valid</td><td>Not valid</td><td>Not valid</td><td>Not valid</td></tr>
<tr><td>0</td><td>1</td><td>Valid</td><td>Valid</td><td>Not valid</td><td>Not valid</td></tr>
<tr><td>1</td><td>0</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Not valid</td></tr>
<tr><td>1</td><td>1</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td></tr>
</table>
There is no byte swapping and the data bytes are packed into the upper transmitted bytes first.</td></tr>
</table>

Note: [15:0] refers to a 16-bit data bus (15 = MSB, 0 = LSB).

Pin Information (continued)

Table 5. Pin Descriptions—Enhanced UTOPIA Interface Signals (continued)

Pin	Symbol	Type	I/O	Name/Description
AN17 AL29 AA31 J31	TxEOP[D] TxEOP[C] TxEOP[B] TxEOP[A]	3.3 V (5 V tolerant)	I	**Transmit End of Packet.** This signal indicates that the last word of a packet is on the TxDATA[D:A][15:0] bus. TxEOP[D:A] is valid only when TxENB[D:A] is asserted, and is sampled on the rising edge of TxCLK[D:A]. In U3 or U3+ (32-bit mode), only the TxEOP[A] input pin of port A is used to indicate the end of the incoming packet.
AM18 AM30 AA35 H32	TxERR[D] TxERR[C] TxERR[B] TxERR[A]	3.3 V (5 V tolerant)	I	**Transmit Error.** TxERR[D:A] is only used in packet modes, and indicates that the current packet is to be aborted and discarded, if possible. TxERR[D:A] is only valid when TxEOP[D:A] and TxENB[D:A] are asserted, and is sampled on the rising edge of TxCLK[D:A]. In U3 or U3+ (32-bit mode), only the TxERR[A] input pin of port A is used to indicate an error on the incoming packet.
AP20 AL32 AL33 W32 W31	RxADDR[4] RxADDR[3] RxADDR[2] RxADDR[1] RxADDR[0]	3.3 V (5 V tolerant)	I	**Receive Address.** Receive address is driven to the MPHY to poll and select the appropriate MPHY channel. **Note:** The address for each channel is configured by the microprocessor.
N31 N32 N33 N34 P31 P32 P33 P34 P35 R31 R32 R33 R34 R35 T32 T33	RxDATA[A][15] RxDATA[A][14] RxDATA[A][13] RxDATA[A][12] RxDATA[A][11] RxDATA[A][10] RxDATA[A][9] RxDATA[A][8] RxDATA[A][7] RxDATA[A][6] RxDATA[A][5] RxDATA[A][4] RxDATA[A][3] RxDATA[A][2] RxDATA[A][1] RxDATA[A][0]	3.3 V	O	**Receive Data Channel A.** Used to transport data out of the UTOPIA PHY Rx block. RxDATA[A][15:0] is only valid when RxENB[A] is asserted, and is updated on the rising edge of RxCLK[A]. Note that RxDATA[A][15:0] is used in various UTOPIA modes. In U2 or U2+, all 16 bits are valid. In U3 or U3+ (8-bit mode), only bits 15 to 8 are valid. In U3 or U3+ (32-bit mode), RxDATA[A][15:0] forms the most significant 16 bits of the combined data bus (bits 31 to 16), and RxDATA[B][15:0] forms the least significant 16 bits of the combined data bus (bits 15 to 0).

Note: [15:0] refers to a 16-bit data bus (15 = MSB, 0 = LSB).

Pin Information (continued)

Table 5. Pin Descriptions—Enhanced UTOPIA Interface Signals (continued)

Pin	Symbol	Type	I/O	Name/Description
AE32 AF35 AF34 AF33 AF32 AF31 AG35 AG34 AG33 AG32 AG31 AH34 AH33 AH32 AH31 AJ34	RxDATA[B][15] RxDATA[B][14] RxDATA[B][13] RxDATA[B][12] RxDATA[B][11] RxDATA[B][10] RxDATA[B][9] RxDATA[B][8] RxDATA[B][7] RxDATA[B][6] RxDATA[B][5] RxDATA[B][4] RxDATA[B][3] RxDATA[B][2] RxDATA[B][1] RxDATA[B][0]	3.3 V	O	**Receive Data Channel B.** Used to transport data out of the UTOPIA PHY Rx block. RxDATA[B][15:0] is only valid when RxENB[B] is asserted, and is updated on the rising edge of RxCLK[B]. Note that RxDATA[B][15:0] is used in various UTOPIA modes. In U2 or U2+, all 16 bits are valid. In U3 or U3+ (8-bit mode), only bits 15 to 8 are valid. In U3 or U3+ (32-bit mode), RxDATA[B][15:0] forms the least significant 16 bits of the combined data bus (bits 15 to 0), and RxDATA[A][15:0] forms the most significant 16 bits of the combined data bus (bits 31 to 16). In this mode, channel B port must be provisioned to idle. In this mode, RxDATA[B][15:0] is valid when RxENB[A] is asserted, and RxDATA[B][15:0] is updated on the rising edge of RxCLK[A].
AN25 AP25 AR25 AL24 AM24 AN24 AP24 AR24 AL23 AM23 AN23 AP23 AL22 AM22 AN22 AP22	RxDATA[C][15] RxDATA[C][14] RxDATA[C][13] RxDATA[C][12] RxDATA[C][11] RxDATA[C][10] RxDATA[C][9] RxDATA[C][8] RxDATA[C][7] RxDATA[C][6] RxDATA[C][5] RxDATA[C][4] RxDATA[C][3] RxDATA[C][2] RxDATA[C][1] RxDATA[C][0]	3.3 V	O	**Receive Data Channel C.** Used to transport data out of the UTOPIA PHY Rx block. RxDATA[C][15:0] is only valid when RxENB[C] is asserted, and is updated on the rising edge of RxCLK[C]. Note that RxDATA[C][15:0] is used in various UTOPIA modes. In U2 or U2+, all 16 bits are valid. In U3+ (8-bit mode), only bits 15 to 8 are valid. In U3 or U3+ (32-bit mode), channel C port must be provisioned to idle mode.

Note: [15:0] refers to a 16-bit data bus (15 = MSB, 0 = LSB).

Pin Information (continued)

Table 5. Pin Descriptions—Enhanced UTOPIA Interface Signals (continued)

Pin	Symbol	Type	I/O	Name/Description
AM13 AL13 AR12 AP12 AN12 AM12 AL12 AR11 AP11 AN11 AM11 AR10 AP10 AN10 AM10 AL10	RxDATA[D][15] RxDATA[D][14] RxDATA[D][13] RxDATA[D][12] RxDATA[D][11] RxDATA[D][10] RxDATA[D][9] RxDATA[D][8] RxDATA[D][7] RxDATA[D][6] RxDATA[D][5] RxDATA[D][4] RxDATA[D][3] RxDATA[D][2] RxDATA[D][1] RxDATA[D][0]	3.3 V	O	**Receive Data Channel D.** Used to transport data out of the UTOPIA PHY Rx block. RxDATA[D][15:0] is only valid when RxENB[D] is asserted, and is updated on the rising edge of RxCLK[D]. Note that RxDATA[D][15:0] is used in various UTOPIA modes. In U2 or U2+, all 16 bits are valid. In U3+ (8-bit mode), only bits 15 to 8 are valid. In U3 or U3+ (32-bit mode), channel D port must be provisioned to idle mode.
AR9 AR22 AJ33 T34	RxPRTY[D] RxPRTY[C] RxPRTY[B] RxPRTY[A]	3.3 V	O	**Receive Parity.** This signal indicates the parity on the RxDATA[D:A][15:0]. Odd or even parity may be provisioned through a software register. RxPRTY[D:A] is considered valid only when RxENB[D:A] is asserted, and is updated on the rising edge of RxCLK[D:A]. In U3 or U3+ (32-bit mode), the RxPRTY[A] parity pin of port A indicates the parity for the entire 32-bit data output.
AP9 AL21 AJ32 U31	RxSOP/C[D] RxSOP/C[C] RxSOP/C[B] RxSOP/C[A]	3.3 V	O	**Receive Start of Packet/Cell.** In ATM mode, RxSOP/C[D:A] signal marks the start of a cell on the RxDATA[D:A][15:0] bus. When RxSOP/C[D:A] is high on the clock cycle following the latching of an active RxENB[D:A] signal, the first word of the cell structure is present on the RxDATA[D:A][15:0] bus. In packet modes, the RxSOP/C[D:A] signal marks the start of a packet on the RxDATA[D:A][15:0] bus. When RxSOP/C[D:A] is high, the first word of the packet is present on the RxDATA[D:A][15:0] bus. RxSOP/C[D:A] is considered valid only when RxENB[D:A] is asserted, and is updated on the rising edge of RxCLK[D:A]. In U3 or U3+ (32-bit mode), only the RxSOP/C[A] pin of port A is used to indicate a start of packet/cell for the 32-bit data output.

Note: [15:0] refers to a 16-bit data bus (15 = MSB, 0 = LSB).

Pin Information (continued)

Table 5. Pin Descriptions—Enhanced UTOPIA Interface Signals (continued)

Pin	Symbol	Type	I/O	Name/Description
AL9 AP21 AK33 V33	RxPA[D] RxPA[C] RxPA[B] RxPA[A]	3.3 V	O	**Receive Cell/Packet Available.** This signal indicates when the receive FIFO can send data to the master device. The RxPA[D:A] signal behavior depends on the provisioned low watermark in the UTOPIA interface. **RxPA[D:A] Assertion (High)** RxPA[D:A] goes high (is asserted) when the amount of data in the receive FIFO has reached or exceeded the low watermark, or there is end of packet (EOP) resident in the FIFO. **RxPA[D:A] Deassertion (Low)** In ATM mode, the RxPA[D:A] signal goes low (is deasserted) when the FIFO has less than the low threshold amount of data and there is no EOP inside the FIFO (i.e., part of an ATM cell). Once the last byte of the current cell is transmitted, if the amount of data within the FIFO is less than the low threshold, then the RxPA[D:A] is deasserted. In packet mode, the RxPA[D:A] signal goes low (is deasserted) when the FIFO has less than the low threshold amount of data and there is no EOP inside the FIFO. Once the data transfer begins (since the amount of data has reached or exceeded the low watermark), if there is no EOP below the low threshold (i.e., a long packet), the RxPA signal is deasserted when the FIFO is drained by the UTOPIA master device. In this case, the master must closely monitor the RxPA[D:A] signals and use these signals as data valid indicators to ensure that bad data is not read. TDAT042G5 will deassert the RxPA[D:A], and the signal will be deasserted immediately when the FIFO is drained. (See further description on next page.)

Note: [15:0] refers to a 16-bit data bus (15 = MSB, 0 = LSB).

Pin Information (continued)

Table 5. Pin Descriptions—Enhanced UTOPIA Interface Signals (continued)

Pin	Symbol	Type	I/O	Name/Description
AL9 AP21 AK33 V33	RxPA[D] RxPA[C] RxPA[B] RxPA[A]	3.3 V	O	**Receive Cell/Packet Available** (continued). **Data Transfer** A TDAT042G5 ingress channel sends data when it has asserted RxPA[D:A] and the master device requests data (via RxENB[D:A]). In ATM mode, if the master device requests data using RxENB[D:A] and if the TDAT042G5 has less than the low watermark amount of data to send and there is no end of cell in the FIFO (RxPA[D:A] is deasserted), then the TDAT042G5 UTOPIA interface will send out data that should be ignored by the master, i.e., it does not send data from its internal FIFO. In ATM mode, once an ATM cell transfer starts, the Tx or Rx side must complete the transfer. If the transfer is not completed, then the cell will be corrupted. The transfer continues until either (1) the end of cell is reached, when the end of cell exists below the low watermark, or (2) the end of the FIFO is reached. If the end of the FIFO is reached, no underflow is flagged on the receive side. In ATM mode, the low watermark should be set so that at least one entire cell is in the FIFO prior to asserting RxPA[D:A]. In packet mode, once the data transfer begins, the RxPA[D:A] signal will remain asserted until the FIFO is drained if there is no EOP below the low watermark. During the time RxPA[D:A] is asserted, valid data is being transferred. RxPA[D:A] is updated on the rising edge of RxCLK[D:A]. In U3 or U3+ (32-bit mode), only the RxPA[A] pin of port A is used to indicate the packet/cell available status. When the RxPA signals are used for MPHY direct status, the corresponding RxCLK[B, C, and/or D] must be provided. This clock will be the same as RxCLK[A].
AM9 AN21 AK34 U34	RxENB[D] RxENB[C] RxENB[B] RxENB[A]	3.3 V (5 V tolerant)	I	**Receive Data Enable (Active-Low).** This signal is used to indicate to the UTOPIA PHY Rx block that it is selected. If RxENB[D:A] is high, no operation is performed. If RxENB[D:A] is low, the UTOPIA PHY Rx block sends data (not necessarily valid data). In U3 or U3+ (32-bit mode), only the RxENB[A] input pin of port A is used to enable the transfer of data.
AM8 AN20 AL34 W33	RxCLK[D] RxCLK[C] RxCLK[B] RxCLK[A]	3.3 V (5 V tolerant)	I^u/O	**Receive Clock.** This clock is used to read cells or packets from the receive FIFO. RxCLK[D:A] can operate at speeds from dc to 104 MHz. For clock rates above 52 MHz, the receive clock must be placed in source mode. RxCLK[D:A] sourcing from the respective TxCLK[D:A] may be provisioned by CLOCK_MODE_Rx (see register 0x020F). In U3 or U3+ (32-bit mode), only the RxCLK[A] input/output pin of port A is used to clock the data output. If MPHY direct status is used, then all clocks RxCLK[D:A] must be provided.

Note: [15:0] refers to a 16-bit data bus (15 = MSB, 0 = LSB).

Pin Information (continued)

Table 5. Pin Descriptions—Enhanced UTOPIA Interface Signals (continued)

<table>
<tr><th>Pin</th><th>Symbol</th><th>Type</th><th>I/O*</th><th>Name/Description</th></tr>
<tr><td>AN8
AM20
AK31
W35</td><td>RxSZ[D]
RxSZ[C]
RxSZ[B]
RxSZ[A]</td><td>3.3 V</td><td>O</td><td>Receive Size. This signal defines the valid bytes received and their packing within (1) RxDATA[D:A][15:0] for U2+ 16-bit mode, and (2) RxDATA[A][15:0] and RxDATA[B][15:0] for the U3 or U3+ (32-bit mode). The meaning of these bits may be inverted through UT register 0x0226 TxSZ/RxSZ mode.
In U2 and U3+ (8-bit modes), RxSZ[D:A] are unused.
For U2+ 16-bit mode,
RxSZ[D:A] = 0 defines the MSByte of RxDATA[D:A][15:0], i.e., RxDATA[D:A][15:8], to be the last byte of the packet received when using the default configuration.
RxSZ[D:A] = 1 defines the LSByte of RxDATA[D:A][15:0], i.e., RxDATA[D:A][7:0], to be the last byte of the packet received when using the default configuration.
In U3 or U3+ (32-bit mode), the MSByte must be placed on RxDATA[A], bits 15 to 8. In the 16-bit mode, the MSByte must be placed on RxDATA[D:A], bits 15 to 8.
For U3 or U3+ (32-bit mode), RxSZ[A] and RxSZ[B] are combined to define four states of the received data stream. RxSZ[C] and RxSZ[D] are unused. The following states are assigned by RxSZ[A] and RxSZ[B] when RxEOP[A] is asserted and the default configuration is provisioned.
<table>
<tr><th></th><th></th><th colspan="2">RxDATA[A]</th><th colspan="2">RxDATA[B]</th></tr>
<tr><th></th><th></th><th>RxDATA[A][15:8]</th><th>RxDATA[A][7:0]</th><th>RxDATA[B][15:8]</th><th>RxDATA[B][7:0]</th></tr>
<tr><th>RxSZ[A]</th><th>RxSZ[B]</th><th>DATA[31:24]</th><th>DATA[23:16]</th><th>DATA[15:8]</th><th>DATA[7:0]</th></tr>
<tr><td>0</td><td>0</td><td>Valid</td><td>Not valid</td><td>Not valid</td><td>Not valid</td></tr>
<tr><td>0</td><td>1</td><td>Valid</td><td>Valid</td><td>Not valid</td><td>Not valid</td></tr>
<tr><td>1</td><td>0</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Not valid</td></tr>
<tr><td>1</td><td>1</td><td>Valid</td><td>Valid</td><td>Valid</td><td>Valid</td></tr>
</table>
The data bytes are packed into the upper transmitted bytes first.</td></tr>
<tr><td>AN9
AM21
AJ31
U32</td><td>RxEOP[D]
RxEOP[C]
RxEOP[B]
RxEOP[A]</td><td>3.3 V</td><td>O</td><td>Receive End of Packet. This signal indicates that the last word of a packet is on the RxDATA[D:A][15:0] bus. RxEOP[D:A] is valid only when RxENB[D:A] is asserted, and is updated on the rising edge of RxCLK[D:A].
In U3 or U3+ (32-bit mode), only the RxEOP[A] output pin of port A is used to indicate the end of the outgoing packet.</td></tr>
<tr><td>AP8
AR21
AK32
V32</td><td>RxERR[D]
RxERR[C]
RxERR[B]
RxERR[A]</td><td>3.3 V</td><td>O</td><td>Receive Error. RxERR[D:A] is only used in POS mode, and indicates that the current packet is to be aborted and discarded, if possible. RxERR[D:A] is only valid when RxEOP[D:A] and RxENB[D:A] are asserted, and is updated on the rising edge of RxCLK[D:A]. If the Rx FIFO overflows, RxERR[D:A] and RxEOP[D:A] are asserted to indicate a corrupted packet.
In U3 or U3+ (32-bit mode), only the RxERR[A] output pin of port A is used to indicate an error on the outgoing packet.</td></tr>
</table>

*I^u = internal pull-up resistance, I^d = internal pull-down resistance.

Note: [15:0] refers to a 16-bit data bus (15 = MSB, 0 = LSB).

Pin Information (continued)

Table 6. Pin Descriptions—Microprocessor Interface Signals

Pin	Symbol	Type	I/O*	Name/Description
C7	$\overline{\text{RST}}$	3.3 V (5 V tolerant)	I^u	**Reset (Asynchronous) (Active-Low).** Reset must be held active-low for a minimum of 100 ns. After deassertion of reset, the device is reset and available for use after 8 µs.
E7	$\overline{\text{ICT}}$	3.3 V (5 V tolerant)	I^u	**3-State Control (Active-Low).** $\overline{\text{ICT}}$ has an internal 100 kΩ pull-up. This control 3-states the digital outputs. It does not control the LVPECL outputs.
D7	PMRST	3.3 V (5 V tolerant)	I/O	**1-Second Performance Monitor (PM) Clock.** PM clock can be generated on-chip. This signal will have a 50% duty cycle. When the PMRST is under software control (PM mode), it can be activated longer or shorter than once per second.
D8	MPMODE	3.3 V (5 V tolerant)	I^u	**MPU Mode Select.** This signal is set high for a synchronous microprocessor, or low for an asynchronous microprocessor.
C8	MPCLK	3.3 V (5 V tolerant)	I^u	**MPU Clock.** This clock can operate from 1 Hz to 66 MHz when in synchronous mode.
B8	$\overline{\text{CS}}$	3.3 V (5 V tolerant)	I^u	**Chip Select (Active-Low).** This signal must be low during register access.
B7	$\overline{\text{INT}}$	3.3 V (open drain)	O	**Interrupt (Active-Low).** This signal goes low when the device generates an unmasked interrupt.
A12	DATA[15]	3.3 V (5 V tolerant)	I^u/O	**Data Bus.** This bus is a bidirectional data bus for writing and reading software registers.
B12	DATA[14]			
C12	DATA[13]			
D12	DATA[12]			
E12	DATA[11]			
A11	DATA[10]			
B11	DATA[9]			
C11	DATA[8]			
D11	DATA[7]			
A10	DATA[6]			
B10	DATA[5]			
C10	DATA[4]			
D10	DATA[3]			
E10	DATA[2]			
A9	DATA[1]			
B9	DATA[0]			

* I^u = internal pull-up resistance, I^d = internal pull-down resistance.

Notes:
An overbar above symbol name indicates active-low.

[15:0] refers to a 16-bit data bus (15 = MSB, 0 = LSB).

Pin Information (continued)

Table 6. Pin Descriptions—Microprocessor Interface Signals (continued)

Pin	Symbol	Type	I/O*	Name/Description
B16 C16 D16 A15 B15 C15 E15 A14 B14 C14 D14 E14 B13 C13 D13 E13	ADDR[15] ADDR[14] ADDR[13] ADDR[12] ADDR[11] ADDR[10] ADDR[9] ADDR[8] ADDR[7] ADDR[6] ADDR[5] ADDR[4] ADDR[3] ADDR[2] ADDR[1] ADDR[0]	3.3 V (5 V tolerant)	I^u	**Address Bus.** This bus is used to address registers.
E9	$\overline{\text{ADS}}$	3.3 V (5 V tolerant)	I^u	**Address Strobe (Active-Low).** This signal indicates the address is valid for MPU access in the asynchronous mode, and transfer start for the synchronous mode.
D9	R/$\overline{\text{W}}$	3.3 V (5 V tolerant)	I^u	**Read/$\overline{\text{Write}}$.** This signal is low to indicate a write operation and is high to indicate a read operation.
C9	$\overline{\text{DS}}$	3.3 V (5 V tolerant)	I^u	**Data Strobe (Active-Low).** This signal used in the asynchronous mode (MPMODE = 0) indicates that the data is valid for MPU writes.
E8	$\overline{\text{DT}}$	3.3 V	O	**Data Transfer Acknowledge (Active-Low).** This signal acknowledges the data transfer cycle.

* I^u = internal pull-up resistance, I^d = internal pull-down resistance.

Notes:
An overbar above symbol name indicates active-low.

[15:0] refers to a 16-bit data bus (15 = MSB, 0 = LSB).

Table 7. Pin Descriptions—General-Purpose I/O Signals: Interface Signals

Pin	Symbol	Type	I/O*	Name/Description
AG5 AH2 AH3 AH4	GPIO[3] GPIO[2] GPIO[1] GPIO[0]	3.3 V (5 V tolerant)	I^u/O	**General-Purpose I/O.** These programmable I/O pins may be used to monitor or control external circuitry. These pins may also be provisioned to cause an interrupt upon a change in their values.

* I^u = internal pull-up resistance, I^d = internal pull-down resistance.

Pin Information (continued)

Table 8. Pin Descriptions—JTAG Interface Signals

Pin	Symbol	Type	I/O*	Name/Description
F2	TCK	3.3 V (5 V tolerant)	I^u	**JTAG Test Clock.** This 10 MHz signal provides timing for test operations.
F4	$\overline{\text{TMS}}$	3.3 V (5 V tolerant)	I^u	**JTAG Test Mode Select (Active-Low).** Controls test operations. $\overline{\text{TMS}}$ is sampled on the rising edge of TCK.
G5	TDI	3.3 V (5 V tolerant)	I^u	**JTAG Test Data In.** Provides a 10 Mbits/s test data input signal. TDI is sampled on the rising edge of TCK.
G2	TDO	3.3 V	O	**JTAG Test Data Out.** This 10 Mbits/s data output signal is updated on the falling edge of TCK. The TDO output is 3-stated except when scanning out test data.
G3	$\overline{\text{TRST}}$	3.3 V (5 V tolerant)	I^u	**JTAG Test Reset (Active-Low).** This signal provides an asynchronous reset for the TAP. Under normal device operations, $\overline{\text{TRST}}$ should be pulled low.

* I^u = internal pull-up resistance, I^d = internal pull-down resistance.

Notes:
An overbar above symbol name indicates active-low.

JTAG interface signals are used for test operations that are carried out using the *IEEE* P1149.1 test access port. *IEEE* is a registered trademark of the Institute of Electrical and Electronics Engineers, Inc.

Pin Information (continued)

Table 9. Pin Descriptions—Power Signals

Pin	Symbol	Type*	I/O	Name/Description
B6	VDDA	P	—	**Analog Power Supply.**
A1, A2, A5, A6, A17, A18, A30, A31, A34, A35, B1, B2, B34, B35, C3, C33, D4, D27, D32, E1, E5, E11, E16, E20, E25, E31, E35, F1, F35, K5, L5, L31, M5, P4, R1, T5, T31, U35, V1, V2, V35, W1, Y5, Y31, AB5, AD5, AE5, AE31, AF5, AK1, AK35, AL1, AL5, AL11, AL16, AL18, AL20, AL25, AL31, AL35, AM4, AM32, AN3, AN33, AP1, AP2, AP34, AP35, AR1, AR2, AR5, AR6, AR18, AR19, AR30, AR31, AR34, AR35	VDDD	P	—	**Digital Power Supply.**
E3	VDDD PLL	P	—	**Digital Power Supply PLL.**
C6	GNDA	P	—	**Analog Ground.**
A3, A4, A7, A8, A13, A16, A20, A23, A27, A28, A29, A32, A33, B3, B4, B32, B33, C1, C2, C4, C32, C34, C35, D1, D2, D3, D33, D34, D35, F3, G1, G35, H1, H3, H5, H35, N1, N35, T1, T35, V3, V31, Y1, Y4, Y35, AA5, AC1, AC35, AH1, AH35, AJ1, AJ35, AM1, AM2, AM3, AM33, AM34, AM35, AN1, AN2, AN4, AN6, AN32, AN34, AN35, AP3, AP4, AP32, AP33, AR3, AR4, AR7, AR8, AR13, AR16, AR20, AR23, AR28, AR29, AR32, AR33	GNDD	P	—	**Digital Ground.**
E4	GNDD PLL	P	—	**Digital Ground PLL.**

* P = power.

Pin Information (continued)

Table 10. Pin Descriptions—No Connect Pins

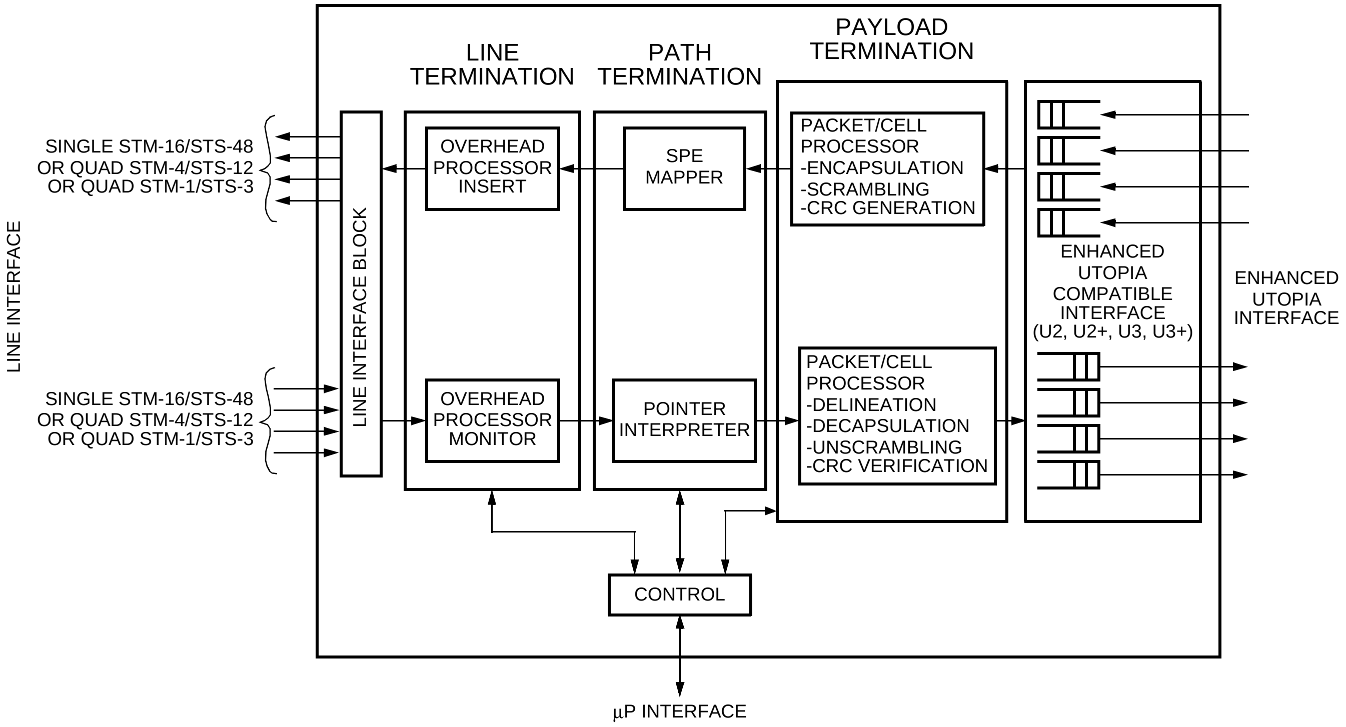
Pin	Symbol	Type	I/O	Name/Description
E6, D6	NC	—	—	**No Connection.** Has internal pull-up resistor. Do not connect to these pins.
A19, A21, A22, A24, A25, A26, B5, B17, B18, B19, B20, B21, B22, B23, B24, B25, B26, B27, B28, B29, B30, B31, C5, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26, C27, C28, C29, C30, C31, D5, D15, D17, D18, D19, D20, D21, D22, D23, D24, D25, D26, D28, D29, D30, D31, E2, E17, E18, E19, E21, E22, E23, E24, E26, E27, E28, E29, E30, E32, E33, E34, F5, F31, F32, F33, F34, G4, G31, U33, V34, AL8, AL19, AM7, AM19, AN19, AN31, AP5, AP7	NC	—	—	**No Connection.** Do not connect to these pins.

Overview

This device integrates the SONET/SDH interface termination functions with a generic cell/packet delineation circuit. It supports STS-48/STM-16, quad STS-12/STM-4, and quad STS-3/STM-1 interface rates. Up to four data channels transported within an STS-N payload are processed via the SONET/SDH termination blocks and the on-chip data encapsulation/decapsulation engine. Packet or ATM data are transmitted/received by this device on the equipment side via the enhanced UTOPIA interface. SONET/SDH streams are transmitted/received by this device on the network side via the line interface.

Concatenation levels supported by this device are from STS-1 to STS-48c, including non-standard modes (e.g., STS-5C). See Table 22 on page 61 for details.

This device supports mapping for ATM cells into SONET/SDH, mapping for packet data via all existing or currently proposed standards (e.g., PPP, SDL) into SONET/SDH streams. This device, via SDL mapping or cell-based UNI mapping, also supports packet over fiber or ATM over fiber, respectively. Figure 2 shows the overview block diagram, and Figure 3 shows the interface block diagram for this device.



5-6680(F).ar.15

Figure 2. Overview Block Diagram

Overview (continued)

Figure 3 shows the interface diagram of the IC.

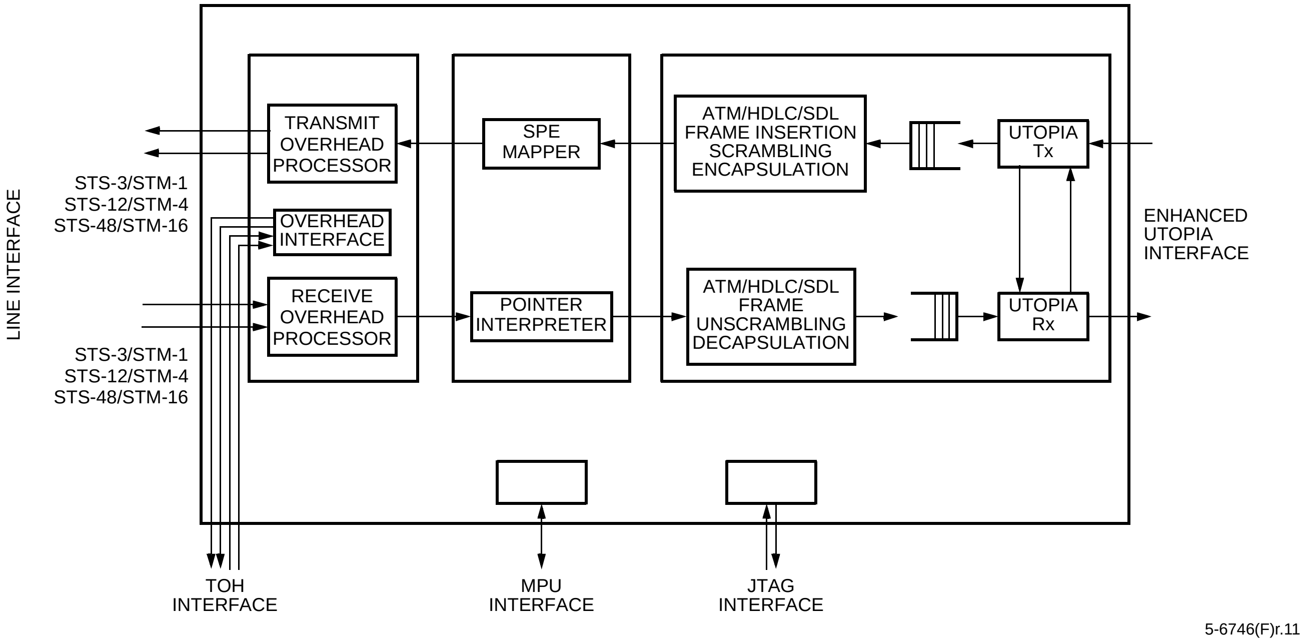


Figure 3. Interface Block Diagram

The receive path terminates and processes section, line, and path overhead. It performs framing (A1, A2), descrambling, detects alarm conditions, and monitors section, line, and path BIP-Ns (B1, B2, B3), accumulating error counts for each level for performance monitoring purposes. Line and path remote error indications (M1, G1) are also accumulated. The payload pointers (H1, H2) are interpreted and the synchronous payload envelope (SPE) is extracted.

The transmit path inserts section, line, and path overhead. It inserts the framing pattern (A1, A2), performs scrambling, inserts AIS (optionally), and calculates and inserts section, line, and path BIP-8s (B1, B2, B3). Line and path remote failure indications (M1, G1) are inserted based on received BIP-8 errors. The payload pointers (H1, H2) are generated and the SPE is inserted.

When used to implement an ATM UNI, ATM cells are written into an internal 4-cell FIFO buffer using a generic 8-/16-/32-bit wide UTOPIA 2/3 compliant interface. Idle/unassigned cells are automatically inserted when the internal FIFO is empty. The device provides generation of the header check sequence and optionally scrambles the ATM payload. The TDAT042G5 also supports cell-based UNI per I.432 (i.e., ATM over fiber).

Overview (continued)

When used to implement a POS UNI, the device writes packets into an internal 256-byte FIFO buffer using a generic 8-/16-/32-bit wide enhanced UTOPIA 2/3 compliant interface. HDLC framing performs the insertion of flags, control escape characters, and the FCS fields. Either the CRC-ITU or CRC-32 (in regular or reversed mode) can be computed and added to the frame. Counts of transmitted packets and errored/dropped packets are accumulated for performance monitoring purposes.

ATM/HDLC/HDLC-CRC/PPP Support

TDAT042G5 supports the transfer of ATM cells or variable-length packets. Support for 52- or 53-byte cell sizes is provided at the UTOPIA interface through register provisioning. The following three types of packet data can be sent and received with HLDC-like framing: transparent HDLC, CRC, and PPP. Transparent HDLC contains 0x7E framing but no CRC. CRC mode is HDLC with an attached CRC. PPP has 0x7E framing with provisionable attached header information and CRC.

When used to implement an ATM UNI, the device performs cell delineation on the SPE. HEC error correction is provided. Idle/unassigned cells may be dropped according to a programmable filter. Cells are also dropped upon detection of an uncorrectable header check sequence error. The ATM cell payloads are descrambled before being passed to a 4-cell FIFO buffer. The received cells are read from the FIFO using a generic 8-/16-/32-bit wide UTOPIA 2/3 compliant interface. Counts of received ATM cells, uncorrectable HEC errors, and correctable HEC errors are accumulated independently for performance monitoring purposes.

When used to implement a POS UNI, the device descrambles the SPE before extracting HDLC frames. The control escape characters are removed. Descrambling can be performed after control escape byte destuffing (or before to control malicious HDLC expansion). The optional 16- or 32-bit error check sequence is verified for correctness. The packets are placed into a 256-byte FIFO buffer.* The received packets are read from the FIFO using a generic 8-/16-/32-bit wide enhanced UTOPIA 2/3 compliant interface. Counts of received packets and errored/ dropped packets are accumulated independently for performance monitoring purposes. The device POS implementation also allows the optional attach/detach of a per-channel provisionable PPP header.

* FIFOs are 256 bytes per channel and cannot be re-allocated.

Overview (continued)

SDL Support

Supports the simplified data link (SDL) protocol, which is currently being reviewed in standards bodies. The implementation supports 4-byte modified SDL UNI including the following:

- CRC-16 based frame delineation with 2-byte packet field length
- Forty-eighth order scrambler
- No HDLC-like packet expansion
- Optional CRC-16/-32 payload check
- Capable of packet-over-fiber operation (i.e., no SONET frame)
- Two user-programmable 6-byte OAM messages
- Optional offset field from 0 to 32 bytes.

TDAT042G5 provides support for a provisionable offset to the packet to allow for the attachment of layer 2 routing information (e.g., MPLS tags). Table 11 defines the provisioned value for each offset.

Table 11. Optional Offset Field

Provisioned Value	Route Tag Length (Bytes)
0x0	0
0x1	1
0x2	2
0x3	3
0x4	4
0x5	5
0x6	6
0x7	7
0x8	8
0x9	10
0xA	12
0xB	14
0xC	16
0xD	20
0xE	24
0xF	32

The packet length value (header value that CRC is calculated over) shall account for the total length of the packet datagram as sell as the associated route tags.

Overview (continued)

Transparent Mode

Transparent mode is useful for packet delivery over fiber. No SONET overhead is added in this mode. Since no SONET overhead is added, the OHP and PT blocks must be configured for the bypass mode.

In transmitting from the TDAT042G5 to the line, the data engine maps the data payload into a full SONET frame starting at what normally would be the first A1 byte. The data engine continues to map payload into the full SONET frame until an end of packet or end of frame is reached, at which time the data engine halts the mapping of the incoming data stream into the SONET frame until the next start of frame.

When TDAT042G5 is receiving from the line, the data engine must be provisioned to receive the maximum packet size, unless the location of the last byte of the packet is known in advance. If the size of the packet is not known, one must program the data engine to receive the entire SONET frame. The external UTOPIA interface device must then be capable of extracting the variable length packets from the full SONET frame.

Details of the transparent mode are given in the Data Engine (DE) Block section, page 75.

Test and General-Purpose I/O Support

The device is provisioned, controlled, and monitored using a generic 16-bit microprocessor interface. A standard five-signal *IEEE* -1149.1 compliant JTAG test port is also provided for boundary scan purposes.

A 4-bit GPIO (general-purpose input/output) interface is provided to control and/or monitor other onboard devices.

External Interfaces

Figure 4 shows the external interfaces.

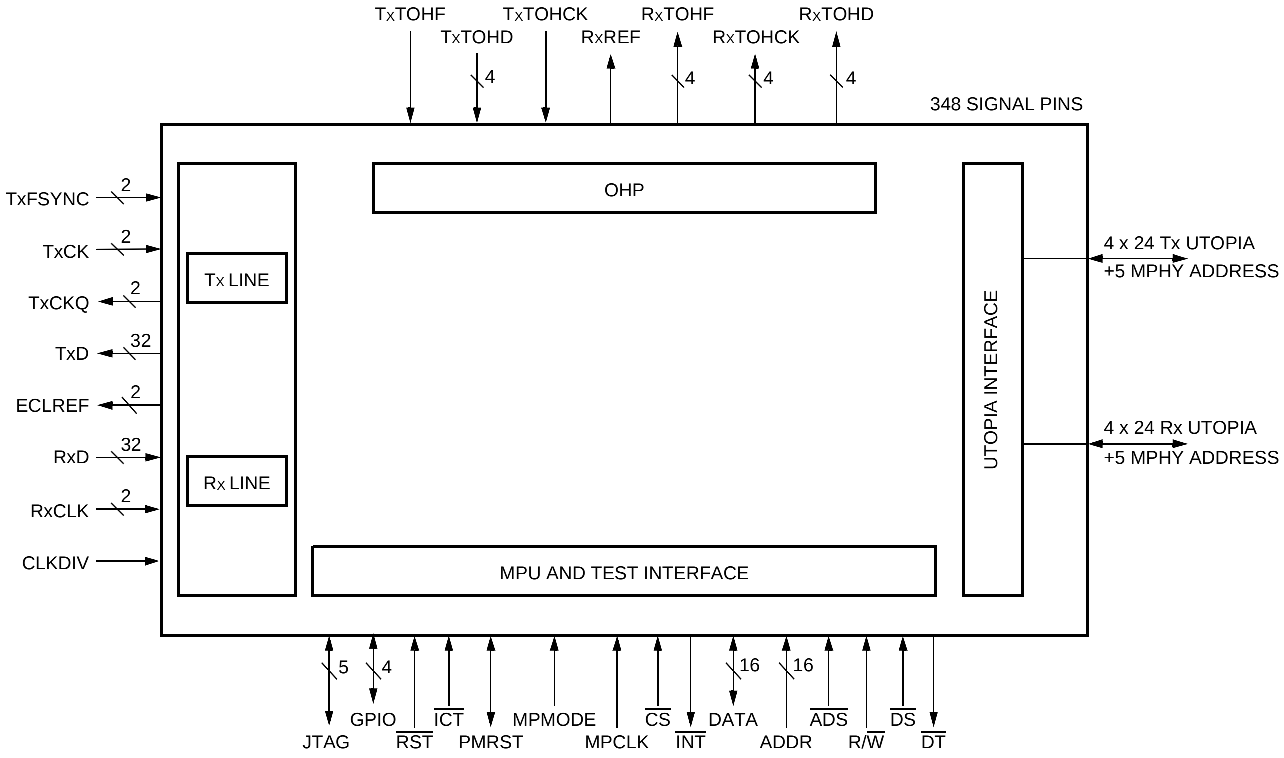


Figure 4. External Interface Summary Diagram

Functional Description

The block diagram for this device can be seen in Figure 5.

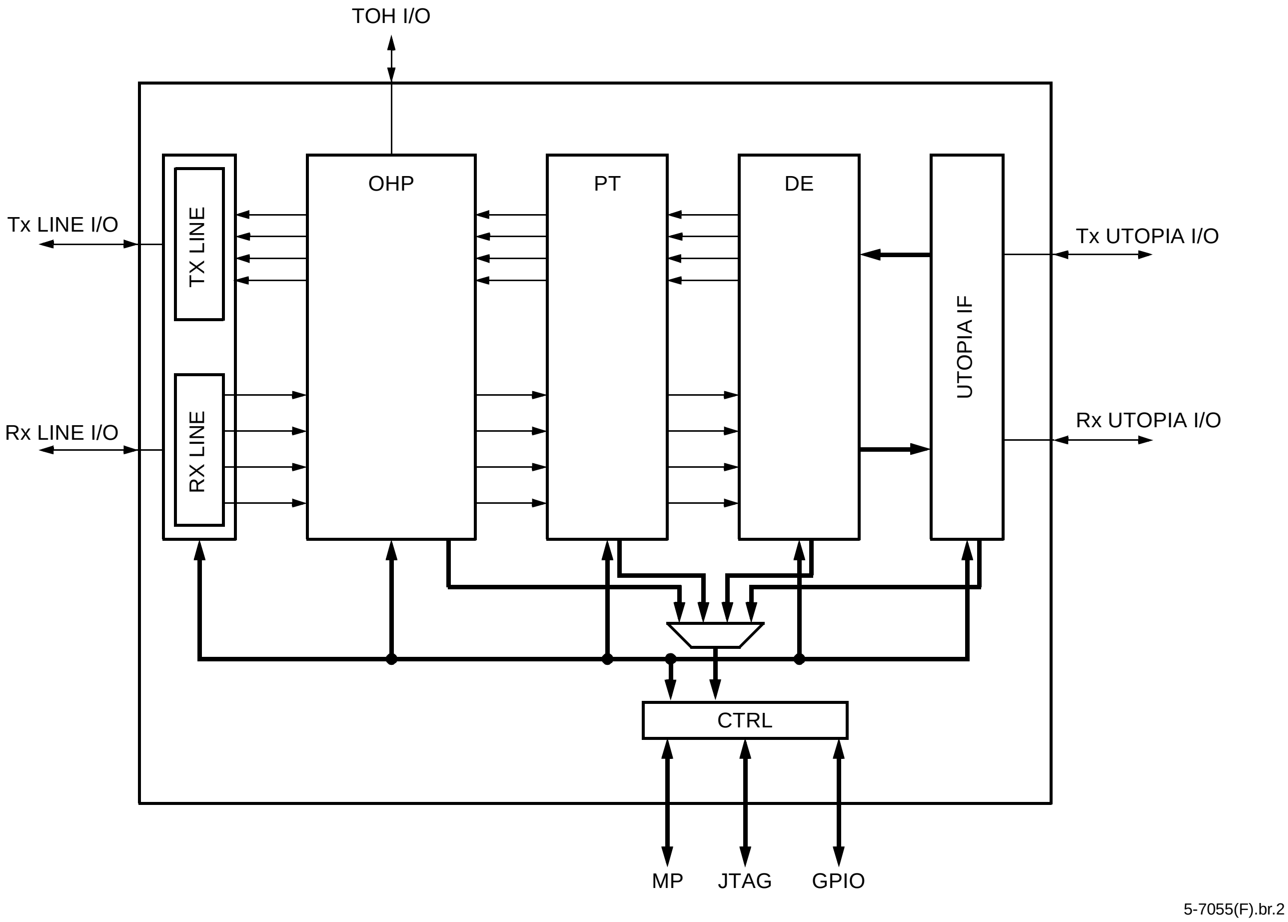


Figure 5. Functional Block Diagram

Functional Description (continued)

Line Interface Block

This device is designed to work with commonly available opto-electronic converters for OC-3, OC-12, and OC-48 line rates. It will also work with available multiplexer and demultiplexer chip sets for an STS-48/STM-16 line interface rate. The line interface will operate in one of three possible modes, and is provisioned through core register 0x0010 (mode), bits 4—0. These three values of the mode register are the only values allowed.

Table 12. Line Interface Modes

Mode[4:0] Core Register 0x0010	Interfaces	Line Interface Signals
10000	STS-48/STM-16	RxCKP/N, RxD[15:0]P/N, TxCKP/N, TxD[15:0]P/N
01111	STS-12/STM-4	RxCLK[D]P/N, RxD[D]P/N,TxCKP/N, TxD[D]P/N RxCLK[C]P/N, RxD[C]P/N,TxCKP/N, TxD[C]P/N RxCLK[B]P/N, RxD[B]P/N,TxCKP/N, TxD[B]P/N RxCLK[A]P/N, RxD[A]P/N,TxCKP/N, TxD[A]P/N
00000	STS-3/STM-1	RxCLK[D]P/N, RxD[DP/N, TxCKP/N, TxD[D]P/N RxCLK[C]P/N, RxD[C]P/N,TxCKP/N, TxD[C]P/N RxCLK[B]P/N, RxD[B]P/N,TxCKP/N, TxD[B]P/N RxCLK[A]P/N, RxD[A]P/N,TxCKP/N, TxD[A]P/N

This block provides the interface between the external SONET/SDH line components and the overhead processor (OHP) block. The line interface must provide transmit/receive functions for quad STS-3/STM-1, quad STS-12/STM-4, and STS-48/STM-16 applications. All external inputs and outputs for the TDAT042G5 line I/O block are referenced to the positive edge of the clock. When the external devices are referenced to the negative edge, the differential input clock will need to be reversed at the TDAT042G5 input.

Receive Line Interface Summary

The following list summarizes the receive line interface operations for each STS mode.

- In quad STS-3/STM-1 mode, the receive line interface provides four separate STS-3/STM-1 input pin groups. Each input group comprises a differential LVPECL 155.52 Mbits/s data input and a differential 155.52 MHz clock. Each input group provides data to only one of four (A, B, C, or D) OHP blocks. This interface is synchronous and requires an external CDR.
- In quad STS-12/STM-4 mode, the receive line interface provides four separate STS-12/STM-4 input pin groups. Each input group comprises a differential LVPECL 622.08 Mbits/s data input and a differential 622.08 MHz clock. Each input group provides data to only one of four (A, B, C, or D) OHP blocks. This interface is synchronous and requires an external CDR.
- In the STS-48/STM-16 mode, the device provides 16 differential LVPECL data inputs at 155.52 Mbits/s with a differential LVPECL 155.52 MHz clock. In this mode, an external 1:16 data demultiplexer with a 1/16 clock divider is required. External barrel shifter circuitry to byte align the data is not required.
- Multiplexers select between the terminal loopback data, the 32-bit parallel STS-48/STM-16 data bus, and the four STS-12/STM-4 or STS-3/STM-1 8-bit parallel data buses. The controls for these MUXes are mode (register 0x0010) and loopback (register 0x0012) provided by the control block (see Table 42 and Table 44 on pages 137—138).
- For STS-48 mode, the 155.52 MHz input clock is divided by two to 77.76 MHz and distributed to all four multiplexers. For the STS-12/STM-4 mode, each 622.08 MHz input clock is divided by eight to 77.76 MHz. Each 77.76 MHz clock is distributed to the appropriate clock multiplexer (A, B, C, or D). For the STS-3/STM-1 mode, each 155.52 MHz input clock is divided by eight to 19.44 MHz. Each 19.44 MHz clock is distributed to the appropriate clock multiplexer (A, B, C, or D).

Functional Description (continued)

Line Interface Block (continued)

Transmit Line Interface Summary

The following list summarizes the transmit line interface operations for each STS mode.

- In quad STS-3/STM-1 and STS-12/STM-4 modes, the transmit line interface receives 8 bits of data from each OHP block (A, B, C, and D) at 19.44 Mbits/s and 77.76 Mbits/s, respectively. An 8-to-1 parallel-to-serial conversion produces output data at 155.52 Mbits/s for STS-3/STM-1 mode and 622.08 Mbits/s for STS-12/STM-4 mode. For facility loopback, the outputs are multiplexed with the corresponding data from the STS-12/STS-3 (STM-4/STM-1) receive block and sent to four differential LVPECL buffers.
- In STS-48/STM-16 mode, a 32-bit data word at 77.76 Mbits/s is received from the OHP. Then a 2-to-1 parallel-to-parallel conversion is performed producing a 16-bit word at 155.52 Mbits/s. In this mode, an external 16:1 data demultiplexer is required. Facility loopback is not available for the STS-48/STM-16 mode.
- There is a single clock input, TxCKP/N, in the transmit case. The clock source rates are 622.08 MHz (STS-12/STM-4), 155.52 MHz (STS-3/STM-1), or 155.52 MHz (STS-48/STM-16).

  In the STS-48/STM-16 case, two transmit clock modes are available, contra* and forward clocking. In the contra clocking mode, the transmit data is sent out as commanded by TxCKP/N; in addition, an internal PLL must be activated, core register 0x0010 bit 5, to minimize the phase delay between TxCKP/N and the transmitted data. In the forward clocking mode, the transmit data and the clock, TxCKQ (used to clock out the data), are sent in parallel to the transmit multiplexer.

  In STS-12/STM-4 and STS-3/STM-1 modes, the input clock is divided by eight producing the internal clock at 77.76 MHz and 19.44 MHz, respectively. In STS-48/STM-16 mode, the input clock is divided by eight to produce an internal clock at 77.76 MHz. The CLKDIV pin (H4) controls this division. Table 13 shows the required value of CLKDIV.

Table 13. Clock Settings for CLKDIV Pin

CLKDIV Pin	Description
CLKDIV = 1	When in STS-12/STM-4 (622.08 MHz divide by 8).
CLKDIV = 0	When in STS-3/STM-1, STS-48/STM-16 (155.52 MHz divide by 2).

- TxFSYNCP/N is an optional external frame sync. This 8 kHz frame sync pulse must be synchronous with TxCKP/N. It is, at minimum, a one TxCKP/N clock cycle wide pulse that is latched in at the system rate (622.08 MHz or 155.52 MHz).
- The active edge of the transmit clock is the positive edge.
- When TDAT042G5 operates in asynchronous mode (MPMODE = 0), the line block provides the microprocessor clock to the microprocessor interface block. The CLKDIV pin must be set to ensure that the clock is always 77.76 MHz.

Line interface timing is given in the Interface Timing Specifications section (see Table 153—Table 155, pages 244—246).

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* Contra refers to a type of data transmission whereby a clock signal is received by a register **before** the register sends data.

Functional Description (continued)

Overhead Processor (OHP) Block

The OHP block terminates/generates the section and line overhead bytes of the line. The data rate of the TOH interface is given in Table 14.

Table 14. R/T TOH Interface Rates

Mode	R/T TOH Interface Rate
STS-48/STM-16	20.736* Mbits/s
STS-12/STM-4	20.736 Mbits/s
STS-3/STM-1	5.184 Mbits/s

* This STS-48/STM-16 interface is a four-line interface resulting in an effective interface rate of 82.944 Mbits/s.

All receive transport overhead bytes are output on the RTOH interface for external processing. Transmit transport overhead bytes can optionally be inserted from the TTOH interface.

The transmit transport overhead bytes can be inserted in one of three ways selected through software provisioning: (1) automatically by hardware, (2) via software provisioning, or (3) through the TOAC. Table 15 defines those overhead bytes that can be inserted via each of the three paths. In some cases, the user has the choice to insert the byte via software registers or through the TOAC. Superscripts in the table reference these insertion methods which are described in the footnotes.

Table 15. TOAC Byte Insertion: An STS-3/STM-1 Example

OH Parity[3] (1st bit of 1st byte)	X[6]	X[6]	X[6]	X[6]	X[6]	J0[5]	Z0[4]	Z0[4]
X[6]	B1-2[1]	B1-3[1]	E1[5]	E1-2[1]	E1-3[1]	F1[5]	F1-2[1]	F1-3[1]
D1[3]	D1-2[1]	D2-3[1]	D2[3]	D2-2[1]	D2-3[1]	D3[3]	D3-2[1]	D3-3[1]
X[6]	X[6]	X[6]	X[6]	X[6]	X[6]	X[6]	X[6]	X[6]
X[6]	X[6]	X[6]	K1[2]	K1-2[1]	K1-3[1]	K2[2]	K2-2[1]	K2-3[1]
D4[3]	D4-2[1]	D4-3[1]	D5[3]	D5-2[1]	D5-3[1]	D6[3]	D6-2[1]	D6-3[1]
D7[3]	D7-2[1]	D7-3[1]	D8[3]	D8-2[1]	D8-3[1]	D9[3]	D9-2[1]	D9-3[1]
D10[3]	D10-2[1]	D10-3[1]	D11[3]	D11-2[1]	D11-3[1]	D12[3]	D12-2[1]	D12-3[1]
S1[5]	Z1-2[3]	Z1-3[3]	Z2[3]	Z2-2[3]	X[6]	E2[3]	E2-2[1]	E2-3[1]

1. Inserted via TOAC, but not part of SONET standard.
2. Inserted via software or automatically via hardware.
3. Inserted via TOAC only.
4. Inserted via software register only.
5. Inserted via TOAC or software register.
6. Inserted via TOAC hardware; should be included in TOAC interface timing.

Timing for the TOH interface is given in the Interface Timing Specifications section (see Table 159 and Table 160, page 251).

Functional Description (continued)

Overhead Processor (OHP) Block (continued)

Receive OHP

Loss-of-Signal. The loss-of-signal block monitors the incoming scrambled data for the absence of transitions. When an absence of transitions is detected for a programmable length of time, a loss-of-signal (LOS) is declared. LOS is cleared when two valid framing patterns are detected, and during the intervening time, no LOS condition is detected.

Framer. The frame block finds and locks onto the incoming A1 and A2 bytes of the SONET transport overhead. Loss-of-frame (LOF) is declared when a defect persists for more than 3 ms. LOF is cleared when the defect is absent for more than 3 ms. To prevent intermittent out-of-frame/in-frame conditions, the 3 ms timer is not reset to zero until an in-frame (or out-of-frame) condition persists for 3 ms. The framer is also responsible for performing bit rotations on the incoming data stream to ensure that the rest of the IC receives byte-aligned data.

While in-frame, the A1/A2 framing bytes in each frame are compared against the expected pattern. Out-of-frame (OOF) is declared when five consecutive frames containing one or more framing pattern errors have been received.

While out-of-frame, this block will monitor the receive data stream for an occurrence of the framing pattern. When a framing pattern has been recognized, the framer performs the necessary bit rotation and verifies that an error-free framing pattern is present in the next frame before declaring in-frame.

J0 Section Trace. The section trace message is extracted and stored in a 16-byte memory for access by software. The first byte of the message can be provisioned to be either:

- The byte with the most significant bit (MSB) set high (for SDH), or
- The byte following a carriage return (0x0D) and line feed (0x0A) sequence (for SONET).
- J0 mismatch detection is provided using one of four methods (provisionable via J0MONMODE[A—D][1:0]; see register description, page 159).

Descrambler. The descrambler block implements the frame synchronous SONET descrambler with a generating polynomial of $1 + x^6 + x^7$. The framing bytes (A1, A2), the section trace bytes (J0), and the growth bytes (Z0) are not descrambled. The descrambler may be disabled through a software register.

B1 BIP-8 Check. The SBIP block counts section BIP-8 (B1) errors. The SBIP value is calculated over the scrambled data of the complete previous frame. The calculated value is compared against the received B1 byte and differences (errors) are counted. A theoretical maximum of 64,000 errors may be detected per second. The SBIP block accumulates these errors in a 16-bit saturating counter. This counter operates in latch and clear mode to ensure Bellcore and ITU compliance with regard to not missing any events (bit errors). It is intended that this counter be polled at least once per second so that no error events are missed. Optionally, a maximum of only one SBIP error per frame can be counted (provisionable via B1BITBLKCNT[A—D]; see register description, page 160). This causes the error counter to only increment by one when one or more errors are detected.

Functional Description (continued)

Overhead Processor (OHP) Block (continued)

Receive OHP (continued)

B2 BIP-N Check. The LBIP block counts line BIP-N errors. The LBIP value is calculated over the incoming frame and is compared to the received B2 bytes received in the next frame. The errors are counted. Optionally, a maximum of only one LBIP error per frame can be counted (B2BITBLKCNT[A—D]; see register description, page 160). This causes the block error counter to only increment by one when one or more errors are detected. A theoretical maximum of 3,072,000 errors may be detected per second. The LBIP block accumulates these errors in a 22-bit saturating counter. This counter is operated in latch and clear mode to ensure Bellcore and ITU compliance with regard to not missing any events (bit errors). It is intended that this counter be polled at least once per second so that no error events are missed.

BER Check. The OHP block also detects provisionable signal fail (SF) and signal degrade (SD) conditions. The SF and SD values are provisioned through a group of software registers. The operation of these registers is discussed in more detail in the OHP Registers section (see page 171). The SF alarm can be provisioned for a bit error rate (BER) of between 10^{-3} to 10^{-5}. The SD alarm can be provisioned for a bit error rate (BER) of between 10^{-5} to 10^{-9}. Table 16 shows the register settings for typical BER values.

Table 16. Values of SFNSSET[A—D][18:0], SFMSET[A—D][7:0], SFLSET[A—D][3:0], SFBSET[A—D][15:0] in Terms of Equivalent BER for BIP-24 Case

BER	SFNSSET [A—D][18:0]	SFMSET [A—D][7:0]	SFLSET [A—D][3:0]	SFBSET [A—D][15:0]
10^{-3}	0x00027	0x04	0xC	0x00EF
10^{-4}	0x00027	0xE5	0x1	0x012B
10^{-5}	0x00027	0x16	0x1	0x012B
10^{-6}	0x0018F	0x16	0x1	0x012B
10^{-7}	0x0018F	0x04	0x1	0x012B
10^{-8}	0x0018F	0x04	0x1	0x05DB
10^{-9}	0x61A7F	0x00	0x1	0x0001

Functional Description (continued)

Overhead Processor (OHP) Block (continued)

Receive OHP (continued)

Figure 6 illustrates the parameters used in determining the bit error detection rate.

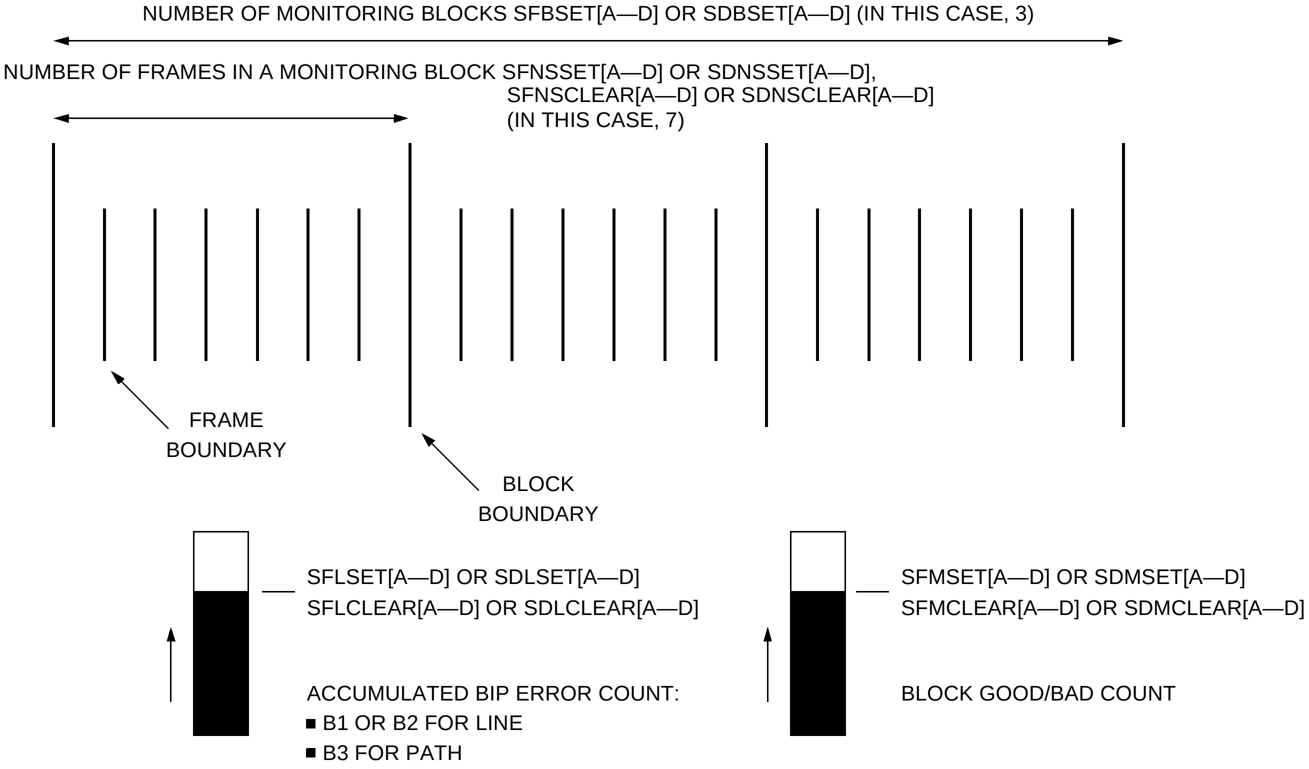

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Figure 6. Signal Degrade and Failure Parameters for BER

TDAT042G5 provides a method to monitor the BER at the line and path layers. The following explains the algorithm for this method to set and clear the BER. The algorithm for this method is the same for setting and clearing the BER, the only difference is the programmed values. TDAT042G5 includes two complete sets of identical counters, one used to determine signal fail (SF) and one used to determine signal degrade (SD). The only difference between SF and SD is the provisioned values. The same algorithm is used for both the line and path layers of SONET.

The algorithm uses four sets of counters: labelled Ns (number of frames), L (number of errors), M (number of errored blocks), and B (total number of blocks). Each of these counters has different values that are provisioned to either set the BER high or clear the BER indication. The algorithm works by counting blocks, i.e., a preset number of SONET/SDH frames (Ns). If the number of errors in the block exceeds the provisioned level (L), then the errored block counter is incremented by 1; otherwise, the number of blocks in error stays at its current level. At this point, the frame counter and the error counter are reset back to 0 and start counting again. At the end of a preset number of blocks (B), the count in the errored block counter is compared against a provisioned threshold (M). If the total number of blocks in error equals or exceeds the provisioned threshold (M), then the BER alarm is raised. If the total number of blocks in error is less than the provisioned amount (M), then the BER alarm is cleared.

The values used by the counters are determined by the state of the algorithm. If the BER state is low, then the SET parameters are used. If the BER state is high, then the CLEAR parameters are used.

Functional Description (continued)

Overhead Processor (OHP) Block (continued)

Receive OHP (continued)

Table 17 shows values of Ns, L, M, and B for OC-3, OC-12, and OC-48 to set and clear the BER indicator.

Table 17. Ns, L, M, and B Values to Set and Clear the BER Indicator

Mode	BER	SF/SD Set Values				SF/SD Clear Values			
		Ns*	L*	M*	B*	Ns*	L*	M*	B*
OC-3	1.00E-03	0	7	61	61	0	4	4	6
	1.00E-04	5	10	3	7	5	3	3	7
	1.00E-05	47	8	3	7	47	3	3	7
	1.00E-06	479	8	3	7	479	3	3	7
	1.00E-07	4724	8	4	9	4724	3	4	9
	1.00E-08	46499	8	3	9	46499	3	3	9
	1.00E-09	259999	5	5	15	259999	3	2	15
OC-12	1.00E-03	0	32	63	63	0	6	4	6
	1.00E-04	1	12	6	10	1	3	8	10
	1.00E-05	12	9	3	8	12	3	3	8
	1.00E-06	127	9	3	8	127	3	3	8
	1.00E-07	1274	9	3	8	1274	3	3	8
	1.00E-08	12749	9	3	8	12749	3	3	8
	1.00E-09	127499	9	3	8	127499	3	3	8
OC-48	1.00E-03	0	75	63	63	0	75	63	63
	1.00E-04	0	15	63	63	0	3	13	14
	1.00E-05	4	11	53	63	4	3	7	11
	1.00E-06	31	8	8	14	31	3	8	14
	1.00E-07	313	8	8	14	313	3	8	14
	1.00E-08	3099	8	7	14	3099	3	7	14
	1.00E-09	30299	7	6	10	30299	3	4	10

* These are the numbers to be provisioned in TDAT042G5. The actual values of the BER algorithm are 1 greater than the actual values shown.

Overhead (OH) Extract. All transport overhead (TOH) bytes are extracted and sent over the RxTOH interface for possible external processing. The number of bits sent are:

- STS-3/STM-1: 5,184,000 bits/s per interface
- STS-12/STM-4: 20,736,000 bits/s per interface
- STS-48/STM-16: 82,944,000 bits/s (over 4 serial lines (20,736 kbits/s each))

The OH interface consists of clock, data, and frame. The data and frame signals update on the falling edge of the clock. The frame pulse is high for the most significant bit (MSB) of the first bit of the frame. Bytes J0, Z0, and F1 (current and previous), K1, K2, and S1 can also be extracted via software registers.

Functional Description (continued)

Overhead Processor (OHP) Block (continued)

Receive OHP (continued)

Table 18 shows the ordering of the bytes for the allowed TOAC configurations.

Table 18. TOAC Channel I/O vs. STS Number/Time Slot

Output Rate	TOAC Channel Input vs. Input STS Number/Time Slot ◄—— Time
STS-3/STM-1	3 2 1 (Channel A)
	3 2 1 (Channel B)
	3 2 1 (Channel C)
	3 2 1 (Channel D)
STS-12/STM-4	12 9 6 3 11 8 5 2 10 7 4 1 (Channel A)
	12 9 6 3 11 8 5 2 10 7 4 1 (Channel B)
	12 9 6 3 11 8 5 2 10 7 4 1 (Channel C)
	12 9 6 3 11 8 5 2 10 7 4 1 (Channel D)
STS-48/STM-16	39 27 15 3 38 26 14 2 37 25 13 1 (Channel A)
	42 30 18 6 41 29 17 5 40 28 16 4 (Channel B)
	45 33 21 9 44 32 20 8 43 31 19 7 (Channel C)
	48 36 24 12 47 35 23 11 46 34 22 10 (Channel D)

The overhead extract block also performs the following functions:

- **Error Monitors.** The REI_L block counts remote error indication block errors. The M1 byte is extracted and counted. This represents the number of LBIP errors detected by the far-end equipment. Optionally, a maximum of only one REI-L error per frame may be counted (provisionable via M1BITBLKCNT[A—D]; register description, page 161). This causes the block error counter to only increment by one when one or more errors are detected.
- **Automatic Protection Switch Signaling.** The APS block filters the K1 and K2 bytes (automatic protection switching channel) and stores the validated message in software-accessible registers. The K bytes are validated after a programmable number of consecutive frames contain identical K1 (and K2[7:3] or K2[7:0]) values. APS protection switching byte failure is detected within this block when a programmable number of frames have passed without valid K bytes. The protection switching byte failure is removed upon detection of a programmable number of frames with identical K1 (and K2[7:3] or K2[7:0]) bytes. The use of K2[7:3] or K2[7:0] is provisionable via the K1K2_2_OR_1 register bit (see register description, page 155).
- **Line Remote Defect Indicator.** Bits 2, 1, and 0 of the K2 byte are monitored for the pattern 110. If this pattern appears for 3—15 (provisionable by OHP register CNTDK2) consecutive frames, RDI-L is asserted. RDI-L is removed when any pattern other than 110 is detected for 3—15 (provisionable by OHP register CNTDK2) consecutive frames. (See page 157 for register description of CNTDK2[A—D][3:0].)
- **Line Alarm Indication Signal.** Bits 6, 7, and 8 of the K2 byte are monitored for the pattern 111. If this pattern appears for 3—15 (provisionable by OHP register CNTDK2) consecutive frames, AIS-L is asserted. AIS-L is removed when any pattern other than 111 is detected for 3—15 (provisionable by OHP register CNTDK2) consecutive frames. (See page 157 for register description of CNTDK2[A—D][3:0].)
- **Rx Synchronization Message.** The S1 block filters the synchronization message (S1) byte and stores the validated message in a software-accessible register. The synchronization message will be validated if a programmable number (in OHP register CNTDS1) of consecutive frames contain identical S1 values. An inconsistent synchronization message alarm will be reported if a provisional number (by OHP register CNTDS1FRAME) of consecutive frames pass without a validated message occurring. (See page 158 for register descriptions of CNTDS1[A—D][3:0] and CNTDS1FRAME [A—D][3:0].)

Functional Description (continued)

Overhead Processor (OHP) Block (continued)

Receive OHP (continued)

- **F1 User Channel.** The F1 byte is extracted by the OHP. The F1 user channel is monitored for change of state using OHP registers 0x0402, 0x0404, 0x0406, 0x0408 (see register map, page 103). The previous and current F1 values are stored in F1DMON1[A—D][7:0] and F1DMON0[A—D][7:0], respectively (see page 109 for register map, page 174 for register descriptions).
- **DCC and Orderwire Bytes.** The data communication channel (D1—D3, D4—D12) and orderwire bytes (E1, E2) can only be extracted via the TOAC.
- **D1/D2/D3 Section Data Communications Channels (DCC).** DCC outputs are taken from the TOAC.
- **D4—D12 Line Data Communications Channels (DCC).** DCC outputs are taken from the TOAC.
- **M1 REI-L.** REI-L is extracted by the OHP.
- **Support for ATM/Packet-Over-Fiber.** The transport overhead must be bypassed when operating in data-over-fiber mode. In this mode, the TOH_BYPASS and ROH_BYPASS register bits must be set to 1. No overhead insertion/extraction is done when in bypass mode.

Transmit OHP

Overhead Insertion. Some transport overhead (TOH) bytes can optionally be inserted via the TxTOH interface and inserted into the TOH bytes (see Table 15, page 49). Certain bytes can be either inserted from values stored in registers or automatically generated. The TxTOH interface controls the insertion mechanism. Software insertion takes precedence over TOAC insertion. The number of bits received are as follows:

- STS-3/STM-1: 5,184,000 bits/s per interface
- STS-12/STM-4: 20,736,000 bits/s per interface
- STS-48/STM-16: 82,944,000 bits/s (over four serial lines (20,736 kbits/s each))

S1 Synchronization Message. The S1 block controls the insertion of the S1 byte. The byte ordering is the same as the RxTOAC and is shown in Table 18 (see page 54). The S1 byte can be provisioned to come from the TxTOH interface or from a software-settable register. Control for message insertion is from software control register TS1INS[A—D] (see register description, page 165 and page 169).

K1K2 APS Signaling. The APS block controls the insertion of the K bytes based on software provisioned K bytes, and alarm conditions (AIS-L, RDI-L). Inconsistent APS bytes can be inserted via register provisioning by TAPSBABBLEINS[A—D] (see register description, page 164 and page 169).

RDI_L Generation. The following six alarms contribute to RDI_L generation: LOF, OOF, LOS, LOC, AIS_L, and SF. They can be inhibited from contributing to RDI-L via transmit control registers (addresses 0x042F, 0x0431, 0x0433, 0x0435; see register description, page 166).

BIP-8 Generation. The SBIP block calculates the B1 value according to Bellcore and ITU standards. Insertion of SBIP errors is possible through the use of software control register TB1ERRINS[A—D] (see register description, page 166).

The LBIP block calculates the B2 values according to Bellcore and ITU standards. Insertion of LBIP errors is possible through the use of software control register TB2ERRINS[A—D] (see register description, page 166).

The REI_L block controls the insertion of the remote error indication block error count.

Functional Description (continued)

Overhead Processor (OHP) Block (continued)

Transmit OHP (continued)

J0 Section Trace. The section trace message is inserted either from the TxTOH interface or from a message stored in a 16-byte software-accessible memory. Control for message insertion is from software control register TJ0INS[A—D] (see register description, page 163 and page 167).

SONET Scrambler. The scrambler block implements the frame synchronous SONET scrambler with a generating polynomial of $1 + x^6 + x^7$. The scrambler may be disabled through a software register.

A1/A2 Framing Bytes. A1 and A2 are automatically placed on the line. Errors can be inserted into A2 by setting OHP register TA1A2ERRINS[A—D][4:0] (see register description, page 166).

E1/E2 Orderwire Bytes. The orderwire bytes for section and line are taken from the TOAC.

D1/D2/D3 Section Data Communications Channels (DCC). DCC inputs are taken from the TOAC.

D4—D12 Line Data Communications Channels (DCC). DCC inputs are taken from the TOAC.

F1 User Channel. The F1 byte can be optionally inserted from stored values in OHP register TF1INS[A—D] (addresses 0x047E, 0x0480, 0x0482, 0x0484; see register description, page 165 and page 169).

M1 REI-L. REI-L can be automatically generated and inserted into the outgoing SONET frame, or can optionally be inhibited. Errors can be inserted into M1 via OHP register TM1_ERR_INS[A—D] (addresses 0x042E, 0x0430, 0x0432, 0x0434; see register description, page 165 and page 169).

Support for ATM/Packet-Over-Fiber. The transport overhead must be bypassed when operating in data-over-fiber mode. In this mode, the TOH_BYPASS and ROH_BYPASS register bits must be set to 1. No overhead insertion/extraction is done when in bypass mode.

Path Terminator (PT) Block

The path terminator performs path overhead (POH) termination and extracts the payload for further processing by the downstream circuitry. The path terminator block interprets the incoming H1/H2 pointer of each incoming STS channel. The pointer interpreter supports up to four channels and performs path overhead termination on each channel. Each channel may be either an STS-1, STS-3c, STS-6c, STS-9c, . . . , STS-45c, or STS-48c.

The pointer is validated according to Bellcore and ITU specifications. The H1/H2 pointers are used to determine the location of the first path overhead (POH) byte (J1). The pointer interpreter consists of a finite state machine (FSM) with four steady states. These states are defined as follows:

- Normal state
- Loss-of-pointer (LOP)
- Alarm indication signal (AIS)
- Concatenation

Functional Description (continued)

Path Terminator (PT) Block (continued)

The transition between states will require several consecutive events to protect against transient conditions caused by bit errors during high BER conditions. The state machine is shown below in Figure 7.

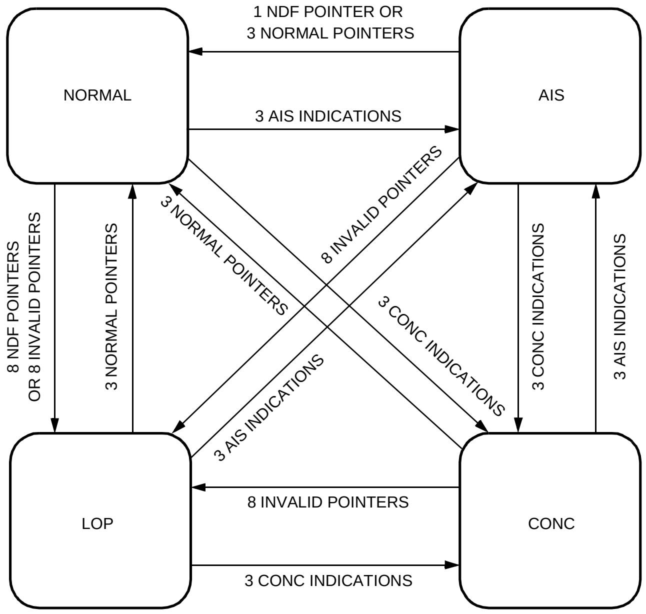

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Figure 7. Pointer Interpreter State Diagram

The PT block monitors for the following conditions and takes appropriate actions:

- **Pointer Increment.** TDAT042G5 uses an 11-bit counter to count the number of pointer increments and updates the associated counter holding register on the occurrence of PMRST (RPI_INC[A—D][10:0]; see register description, page 182). A pointer increment can occur when in the normal pointer mode. The following two methods can be used to determine if the pointer increment operation should be performed: 6-of-10 or 8-of-10 majority matching (selectable via software provisioning of register RINCDEC_6OR8MAJ [A—D]; see register description, page 183).
- **Pointer Decrement.** TDAT042G5 uses an 11-bit counter to count the number of pointer decrements and updates the associated counter holding register on the occurrence of PMRST (RPI_DEC[A—D][10:0]; see register description, page 182). A pointer decrement can occur when in the normal pointer mode. The following two methods can be used to determine if the pointer decrement operation should be performed: 6-of-10 or 8-of-10 majority matching (selectable via software provisioning of register RINCDEC_6OR8MAJ [A—D]; see register description, page 183).
- **Loss-of-Pointer.** LOP-P is declared as shown in the above state diagram. In an LOP-P state, none of the path overhead bytes are extracted.
- **AIS-P.** The AIS-P is declared when the H1 and H2 bytes are set to all ones. In an AIS-P state, none of the path overhead bytes are extracted.
- **Concatenated Pointer.** A concatenated pointer is detected when the new data flag is set and the pointer offset value is all ones.

Functional Description (continued)

Path Terminator (PT) Block (continued)

- **New Pointer.** TDAT042G5 uses a 13-bit counter to count the number of new data flags that occur and updates the associated counter holding register on the occurrence of PMRST (RNDFCNT[A—D][12:0]; see register description, page 182). TDAT042G5 uses a 3-of-4 majority voting scheme to determine if the new data flag is set. Valid new data flags occur when the NDF bits are either 1001, 0001, 1101, 1011, or 1000.
- **Normal Pointer.** A normal pointer occurs when all of the following conditions are true simultaneously.
  (1) NDF is not set (NDF bits are either 0110, 0111, 0100, or 0010),
  (2) There is no invalid pointer value,
  (3) There is a valid offset (0 to 782),
  (4) There is either a match of the SS bits (RSSDRP[A—D][1:0] (addresses 0x0836, 0x0888, 0x08DA, 0x092C)) with the expected values (RSSEXP[1:0] (address 0x0AC7)), or RSSPTRNORM[A—D] (addresses 0x0AA6, 0x0AAE, 0x0AB6, 0x0ABE) is not set.
- **Invalid Pointer.** An invalid pointer is declared when neither a new data flag nor a normal pointer is detected.

SPE Terminate

Receive Path Trace. The path trace message is extracted and stored in a 16-byte (SDH) or 64-byte (SONET) memory for access by software. The first byte of the message can be provisioned to be either of the following:

- For SDH mode, the byte with the most significant bit (MSB) set high (for SDH)
- For SONET mode, the byte following a carriage return (0x0D) and line feed (0x0A) sequence.

The framing can also be disabled.

Receive Error Monitor. The PBIP block counts path BIP-8 errors. A theoretical maximum of 64,000 errors may be detected per second. The PBIP block accumulates these errors in a 16-bit saturating counter. This counter is operated in latch and clear mode to ensure Bellcore and ITU compliance with regard to not missing any events (bit errors). It is intended that this counter be polled at least once per second in order that no error events are missed. The REI_P block counts remote error indication block errors.

Receive Signal Label. The C2 block will extract and validate the signal label byte (C2) and store it in a software-accessible register. The signal label is updated when a provisionable number of consecutive detections of a new C2 value occur (CNTDC2[A—D][3:0]; see register description, page 187). All monitoring is disabled when the pointer is in an LOP-P or an AIS-P state. Commonly used values of C2 with their signal labels are listed below in Table 19.

Table 19. Types of Signal Labels

C2 Value	Signal Label
0x00	Unequipped STS SPE
0x01	Equipped nonspecific payload
0x13	Mapping for ATM
0x16	Mapping for HDLC-PPP

Any value of C2 may be provisioned. If the provisioned value is not matched by the detected value, then data is not passed to the DE. If the provisioned value does match the detected value, then data is passed to the DE.

TDAT042G5 will detect unequipped payloads (UNEQ-P) when a provisionable number of consecutive monitored C2 bytes match the 0x00 unequipped STS SPE state. TDAT042G5 will detect mismatched payloads (PLM-P) when a provisionable number of consecutive monitored C2 bytes do not match the provisioned expected payload label (RC2EXPVAL[7:0]; see register description, page 188).

Functional Description (continued)

Path Terminator (PT) Block (continued)

SPE Terminate (continued)

Receive Path Status. The G1 block extracts the path remote error indication (REI-P) bits of G1[7:4] and accumulates the REI-P errors in a 16-bit saturating counter. This counter is operated in latch and clear mode to ensure Bellcore and ITU compliance. It is intended that this counter be polled at least once per second in order that no error events are missed.

RDI-P. This block will also validate the path remote defect indication (RDI-P) bits and store the result in a software-accessible register. The receive path can monitor remote defect indications in either enhanced or single bit RDI-P modes (provisionable via software bit RDIPMON_ENH_OR1B [A—D]; see register description, page 183). The interpretation of the G1 byte is as follows.

Table 20. 1-bit Mode

G1 Bytes	Description
G1[3:1] = 0xx	No RDI-P defects
G1[3:1] = 1xx	AIS-P, LOP-P

Table 21. 3-bit Mode (Enhanced RDI)

G1 Bytes	Description
G1[3:1] = 001	No RDI-P defects
G1[3:1] = 010	PLM-P or LCD-P
G1[3:1] = 101	AIS-P or LOP-P
G1[3:1] = 110	UNEQ-P or TIM-P (TIM-P is J1 mismatch*)

* TIM-P must be accomplished through (microprocessor) software by reading the transmit RDI-P state and inserting the G1 bit.

Z5/N1, Z4/K4, Z3/F3, H4, F2 Monitoring. TDAT042G5 monitors the F2 user channel byte, the H4 VT multiframe indicator byte, Z3/F3 growth/user byte, Z4/K4 growth/APS path byte, and the Z5/N1 tandem connection byte. These bytes are stored in software registers. These registers are updated when a provisionable number of detections of new values occur on the associated incoming byte. All monitoring is disabled when the pointer is in an LOP-P or an AIS-P state.

Signal Failure and Signal Degrade Monitoring. The path overhead processor also detects/clears provisionable signal fail (SF) and signal degrade (SD) conditions. The SF and SD values are provisionable through a group of software registers in the PT register map. The provisioning is the same as that shown in Table 16, page 51 and Table 17, page 53 of the Overhead Processor (OHP) Block section.

Functional Description (continued)

Path Terminator (PT) Block (continued)

SPE Generate

Transmit Pointer Generation. The pointer generation block generates the outgoing H1 and H2 pointer values. The first H1 and H2 bytes will contain a valid pointer value. The remaining H1 and H2 bytes of the channel will have their pointer values set to indicate concatenation. The remaining unequipped channels will have their H1 and H2 pointers set to a fixed pointer value.

For proper pointer generation, the appropriate values must be provisioned in the H-byte transmit state register THx_STATE (see register description, page 185 and page 186). For example, Figure 8 illustrates the provisioning of the THx_STATE register for the case of an STS-48c payload contained in an STS-48 signal. In this case, the first STS (STS-1) is marked with a normal pointer value while all the remaining STS signals are marked with concatenated pointers. Figure 9 shows another example for the case of four STS-12c payloads in an STS-48 signal (see page 61). TDAT042G5 restricts the available mappings allowed for STS-Mc payloads into STS-N signals (M ≤ N). Table 22 illustrates some of these restrictions (see page 61).

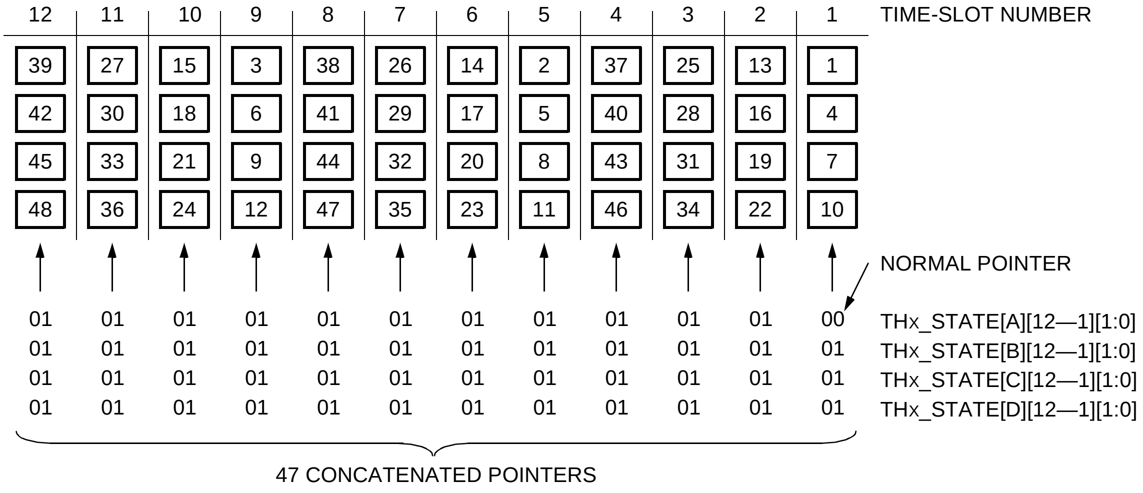

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Figure 8. STS-48 Configuration Carrying STS-48c Payload

Functional Description (continued)

Path Terminator (PT) Block (continued)

SPE Generate (continued)

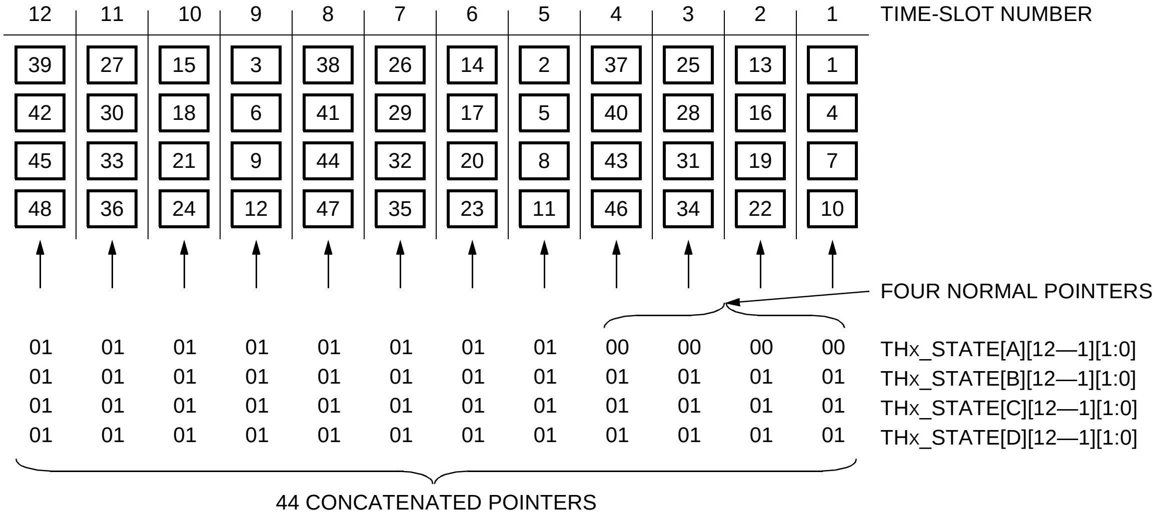

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Figure 9. STS-48 Configuration Carrying Four STS-12c Payloads

The general rule for mapping STS-Mc payloads in STS-N signals (M ≤ N) is that TDAT042G5 allows a maximum of four normal pointers. For M ≤ 12, the valid starting locations for mapping into an STS-48 signal are 1, 13, 25, and 37. For M >12, only one normal pointer is permitted and it must start at the first location, STS #1.

Table 22. Valid Concatenation Starting Locations: STS-Mc into an STS-48c

STS-1 Number	STS-3c	STS-6c	STS-9c	STS-12c	STS-15c	STS-18c	STS-48c
1	Y	Y	Y	Y	Y	Y	Y
4	No	No	No	No	No	No	No
7	No	No	No	No	No	No	No
10	No	No	No	No	No	No	No
13	Y	Y	Y	Y	No	No	No
16	No	No	No	No	No	No	No
19	No	No	No	No	No	No	No
22	No	No	No	No	No	No	No
25	Y	Y	Y	Y	No	No	No
28	No	No	No	No	No	No	No
31	No	No	No	No	No	No	No
34	No	No	No	No	No	No	No
37	Y	Y	Y	Y	No	No	No
40	No	No	No	No	No	No	No
43	No	No	No	No	No	No	No
46	No	No	No	No	No	No	No

Functional Description (continued)

Path Terminator (PT) Block (continued)

SPE Generate (continued)

BIP-8. The PBIP block calculates the B3 value according to Bellcore and ITU standards. Insertion of PBIP errors is possible through the use of a software control register.

REI Generation. The REI_P block controls the insertion of the remote error indication block error count. The received PBIP error counts are inserted into the path status (G1) byte.

RDI-P Generation. The transmit path can insert remote defect indications using either single-bit or enhanced RDI-P modes (provisionable via software register bit TRDIP_ENH_OR1B[A—D]; see register description, page 185). The highest to lowest priority of the defect code insertion is as follows:

(1) AIS-P, LOP-P (applies only to the single-bit version of RDI-P),

(2) UNEQ-P,

(3) PLM-P, LCD-P,

(4) No defects

TIM-P can be inserted using software through TRDIPSINS (registers 0x0AAA, 0x0AB2, 0x0ABA, or 0x0AC2, bits 15—11; see register description, page 184). The LCD-P defect is observed in the data engine and passed to the pointer block for transmission. Each particular defect can be inhibited from contributing to the transmitted RDI-P insertion value via software registers 0x0AAA, 0x0AB2, 0x0ABA, and 0x0AC2. RDI_P can either be inserted by software or automatically through hardware.

Z5/N1, Z4/K4, Z3/F3, H4, F2 Insertion. TDAT042G5 inserts the F2 user channel byte, the H4 VT multiframe indicator byte, Z3/F3 growth/user byte, Z4/K4 growth/APS path byte, and the Z5/N1 tandem connection byte via software provisioning.

Error Insertion Mechanisms. TDAT042G5 provides a method to inject via software REI-P (TREIPERRINS[A—D]) and B3 (TB3ERRINS[A—D]) errors into the transmitted SONET frame (see register descriptions, page 185).

Insertion of J1, F2, C2, Z3, H4, Z4, Z5, SS Values. TDAT042G5 provides paged provisionable registers to insert the path overhead bytes into the outgoing SONET frame. The paging is done by first writing to the page provisioning register at location 0x0AC6 to set the port number and time slot to be provisioned, then writing to the appropriate insertion registers. Available time-slot values for TDAT042G5 are time slot 1 for STS-48c mode; time slots 1, 2, 3, and 4 for STS-48 consisting of four STS-Mc (M ≤ 12) signals; and time slot 1 for quad STS-12c and quad STS-3c modes (ports A, B, C, and D configured for quad STS-3c and quad STS-12c).

Functional Description (continued)

Data Engine (DE) Block

The DE block processes the ATM, SDL, PPP, and HDLC cells/packets at rates up to 2.488 Gbits/s. The DE block behaves like four independent logical data channels, one for each of the four STS-12/STM-4 or STS-3/STM-1 channels, or like a separate single channel for STS-48/STM-16. The following description is for each one of these data engines. Each of the functional elements to be described are independently provisioned. The ATM processor functions with 52-byte, 53-byte, and 56-byte ATM cells. The block diagram for the data engine is shown in Figure 10.

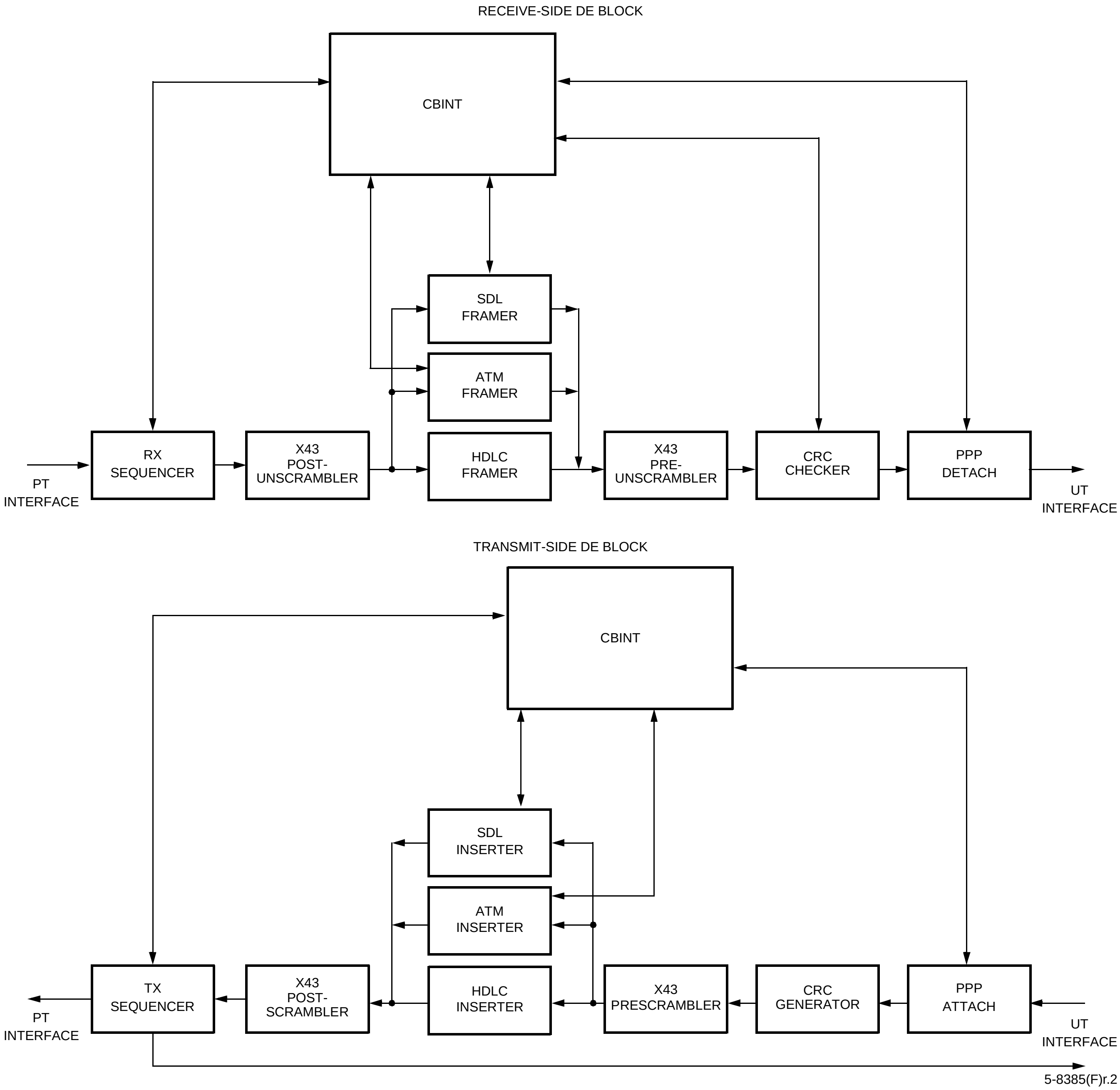


Figure 10. Block Diagram of Date Engine (DE)

Functional Description (continued)

Data Engine (DE) Block (continued)

Receive Data Engine

Receive Sequencer. The receive sequencer demaps SONET framing to four logical channels, performs the physical channel byte alignment and packing, and performs appropriate payload clock domain transfer. The receive sequencer must be provisioned properly for correct operation. There are six registers that are fixed for each particular mode of operation (STS-3/STM-1, STS-12/STM-4, or STS-48/STM-16) and must not be modified (SEQ_CTRL, INIT_CNTS, OH_MARKER_LO, OH_MARKER_HI, SOH_MARKER_LO, SOH_MARKER_HI). See the register descriptions for details, page 195. Also, the appropriate time slots must be provisioned for the rate of the payload expected for each channel. This is done via the registers Rx_TS[0—11] (see register descriptions, page 200). An example of how to configure this for STS-48c mode is shown in the section on configuring the transmit/receive sequencer (see Transmit Data Engine section, page 70).

ATM Cell Processor. The cell processor performs ATM cell delineation using the ATM header error correction (HEC) field found in the cell header. The HEC is a CRC-8 calculation over the first four octets (total of 32 bits) of the ATM cell header. If the TDAT042G5 is in bit-synchronous mode (data is not byte-aligned), 32 separate HEC calculations are performed to delineate an ATM cell. If the TDAT042G5 is in byte-synchronous mode (data is byte-aligned), 4 separate HEC calculations are performed to delineate an ATM cell. An alpha-delta counter is used to track the processor's ability to frame the ATM cells consistently. When a certain level of confidence is reached (defined by the programmable delta counter threshold), the frame is declared in **sync** state, and data is passed to subsequent blocks. If the framer is unable to frame ATM cells over a few cell periods (defined by the programmable delta counter threshold), the framer resumes **hunt** state.

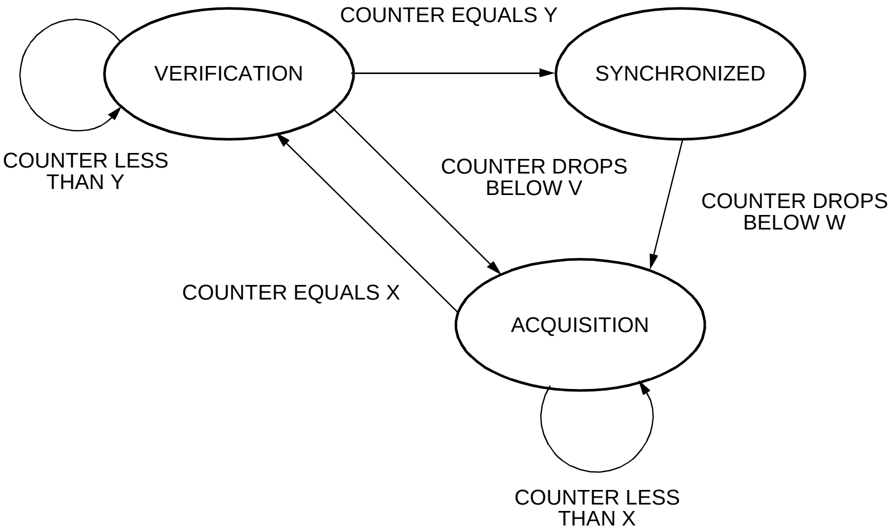
In SONET mode, the processor performs optional X^{43} unscrambling of the payload. Because the X^{43} scrambler is self-synchronizing, the framer needs no assistance from the data in order to synchronize the scrambler. The TDAT042G5 also supports an X^{31} scrambler, compliant with I.432, which is mainly used for packet-over-fiber applications. The state diagram for the X^{31} scrambler is shown in Figure on page 65. The X^{31} scrambler uses an $x^{31} + x^{28} + 1$ polynomial to scramble the data. Unlike the X^{43} scrambler, the X^{31} scrambler does not self-synchronize based upon the data it receives. Thus, one-bit samples of the scrambler output are sent on the transmit side and compared with the scrambler samples on the receive side every 212 bits. If the samples do not match, the receive-side scrambler is adjusted to converge with the transmit-side scrambler. This process continues until a certain level of confidence in the scrambler synchronization is achieved. In the X^{31} mode, the ATM cell processor does not send out any output until both the framer and the scrambler are synchronized, whereas in X^{31} mode, only the framer needs to be synchronized.

Idle ATM cells, which contain no real data, can be either left in or removed from the bitstream. The idle cell header description can be configured, though it is set to a default value (0x00000001). ATM cells can also be filtered if the header contents match a provisioned match register after masking with a provisionable mask register. This allows filtering based on the contents of the GFC, PTI, and CLP fields of the header. Optionally, ATM cells may be dropped if uncorrectable HEC errors are detected. Incoming single-bit ATM header errors can be corrected and the cells may be passed through or dropped, depending on the software configuration.

Functional Description (continued)

Data Engine (DE) Block (continued)

Receive Data Engine (continued)



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Note: Even in synchronized mode, the confidence counter can continue to increase up to the Z value.

Figure 11. State Diagram for the X^{31} Scrambler Synchronization Process

SDL Frame Processor. The SDL frame processor consists of an SDL framer, which detects the start of SDL packets, and an (optional) X^{48} unscrambler, which is used to unscramble payload data. SDL packets can also arrive unscrambled, in which case the unscrambler is disabled. The SDL frame processor can frame packets in SDL form which contain a data length between 4 and 65,535 bytes.

The SDL framer uses a CRC-16 check upon 2 bytes sequences used to determine packet length in order to frame SDL packets. Since the framer is designed to support data that is not byte-aligned, 32 separate framers may be used to search for the CRC-16 pattern. If the data is byte-synchronized, only four framers are needed. A confidence counter is used to gauge the framer's ability to frame SDL packets consistently. Wen the confidence counters reaches a certain level (defined by the programmable SDL delta counter register), the framer is in sync state. Single-bit error correction for the SDL headers is also supported. Shown below in Figure 12 is the general structure of the SDL packets. In this figure, there is no interpacket fill.

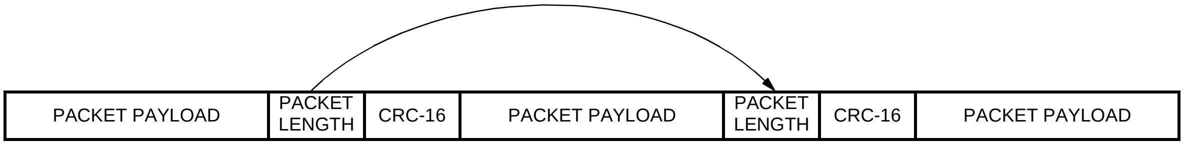

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Figure 12. General Structure of SDL Packets

Functional Description (continued)

Data Engine (DE) Block (continued)

Receive Data Engine (continued)

Interpacket fill separating packets always contains a multiple of 4 bytes. The SDL framer is able to detect interpacket fill since its value is fixed. (It has 4 bytes equal to 0x0000000, i.e., a packet length of 0x0000 with a CRC-16 of 0x0000.) Given that the framer knows the length of a particular packet and can detect interpacket fill, it should be able to predict the start of the next frame and frame on it. The SDL frame processor supports SDL and SDL CRC modes. When operating in SDL CRC mode, a 2-byte or 4-byte CRC for the packet payload is attached to the end of the packet payload prior to the next packet length. When operating in SDL mode, there is no 2-byte or 4-byte CRC for the packet payload.

The SDL frame processor supports X^{48} scrambling of the packet payload, which is accomplished by using a primitive polynomial of $x^{48} + x^{28} + x^{27} + x + 1$. The X^{48} scrambler is not self-synchronizing. Thus the side transmitting SDL packets will periodically send its 48-bit scrambler state within the data stream such that the receive side can synchronize its scrambler. Whenever the SDL frame processor receives a scrambler state, it is immediately put into sync state, which allow it to send data out. Upon receiving additional scrambler states, the scrambler will compare its own state with the state received. If the scrambler states match, then the scrambler remains in sync state. However, if there is a mismatch, the scrambler is put into postsync state. In postsync state, if an additional scrambler state mismatch occurs, the X^{48} scrambler is resynchronized with the scrambler state it has received. The SDL frame processor detects scrambler state data since the packet length field of 0x001 and the length of time separating scrambler state transmissions is programmable. Single-bit error correction for the SDL scrambler state is incorporated within the TDAT042G5.

Both the SDL framer and the X^{48} scrambler must be synchronized before the SDL frame processor will send data.

Besides the SDL scrambler state being transmitted, the SDL framer will also extract special A and B messages used by the upstream device to send link layer 1 messages to the downstream hardware. The packet length headers used to detect A and B messages are 0x0002 and 0x0003, respectively.

In addition to scrambling the data, the SDL data steam coming into the SDL frame processor is dc balanced wit the 32-bit value 0xB6AB31E0.

Table 23 below is used to describe the packet length field.

Table 23. Packet Length Field

Packet Length Field	SDL Data Type
0x0000	Interpacket fill
0x0001	SDL scrambler state
0x0002	A message
0x0003	B message
0x0004—0xFFFF	Length of payload region for current packets (in bytes)

Pre-descrambler. The pre-descrambler block descrambles the payload using a self-synchronous descrambler with a generator polynomial of $1 + x^{43}$. For ATM cell traffic, only the 48-byte cell payload (and not the cell overhead) is descrambled. For HDLC and PPP packets, the entire frame (including header and trailer) is descrambled. Predescrambling, post-descrambling, or no descrambling may be selected through a provisionable register.

Functional Description (continued)

Data Engine (DE) Block (continued)

Receive Data Engine (continued)

HDLC Framer. The packet processor frame aligns to HDLC packets using the HDLC flag character (0x7E). Flags are also used to fill interpacket spaces. The flags are removed and control escape destuffing is performed. The control escape character (0x7D) is searched for and when it is found, the control escape character is removed, i.e., 0x7D5D is unescaped to 0x7D and 0x7D5E is unescaped to 0x7E. If dry mode is enabled, then 0x7D20 is unescaped to a value of 0x00, which represents dry data (FIFO underflow in the middle of a packet). Any other unescaped sequence of 0x7D results in an errored packet.

CRC Check. An optional CRC-ITU or CRC-32 calculation on the whole POS frame is performed after byte destuffing and data descrambling. The CRC-ITU generating polynomial is $1 + x^5 + x^{12} + x^{16}$. The CRC-32 generating polynomial is $1 + x + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$. The computation over the whole packet, including the FCS field, should result in all zeros. A different value indicates an error. Packets with FCS errors are marked as such and are discarded. CRC field stripping is optional. Both normal and reversed CRC modes are supported.

Post-descrambler. The descrambler block descrambles the payload using a self-synchronous descrambler with a generator polynomial of $1 + x^{43}$. For ATM cell traffic, this block is bypassed. For HDLC frames, the entire frame (including header and trailer) is descrambled. The descrambler may be disabled through the use of a software register.

Functional Description (continued)

Data Engine (DE) Block (continued)

Receive Data Engine (continued)

PPP Header Detach. The PPP detach function matches the PPP header (corresponding to the first 4 bytes of the PPP uncompressed frame or first 2 bytes of the PPP compressed frame) to a set of fixed or provisionable values for each channel and outputs frames in accordance with payload control register settings. The address and control field bytes are assumed to be 0xFF03. The block supports two fixed protocol fields (0x0021 corresponding to the IP protocol field and 0x8021, corresponding to the IP control protocol). Additionally, 12 provisionable registers, PPP_Rx_HDRmn (mn = 00, 01, 02, . . . , 11), are supported on-chip to allow a large number of protocols to be recognized in the receive (ingress) data path of the chip (see register descriptions, page 216).

The PPP detach function supports compressed or uncompressed header fields, optionally matching two fixed (one corresponding to IP protocol) 16-bit protocol fields. This optional PPP header check allows PPP (normal or compressed (i.e., no FF03)) to be checked and the header optionally stripped. Packets that fail to match one of the provisioned headers or the two default headers can optionally be discarded. This function supports optionally matching 12 programmable 16-bit protocol fields. The PPP detach function provides bad PPP header counts through a pair of 28-bit counters per channel. The function can optionally discard frames if header fields do not match on a per-channel basis. It can also optionally strip header fields only if they do match on a per-channel basis.

A PPP packet has the following two formats:

Uncompressed PPP Packet

1 byte	1 byte	1 byte	2 bytes	≤64 kbytes	2 or 4 bytes	1 byte
0x7E	address field 0xFF	control field 0x03	protocol field	data	CRC field	0x7E

Compressed PPP Packet

1 byte	2 bytes	≤64 kbytes	2 or 4 bytes	1 byte
0x7E	protocol field	data	CRC field	0x7E

Each channel has a 16-bit register, PPP_Rx_CHK_CHn (n = 0, 1, 2, or 3), that can be provisioned (see register descriptions, page 217).

If the header bytes do not match and payload control bit 7 = 0, the entire PPP packet is discarded for a given channel. Otherwise, if the header bytes do not match and payload control bit 7 = 1, the PPP packet is marked as bad and not discarded for a given channel.

If payload control bit 6 = 0, the header is stripped, provided it matches a provisionable value; otherwise, it is left on for a given channel.

The bad packet counting is based upon the following criteria:

- **Header Fields.** The PPP bad header counter, PM_BHC_n (n = 0, 1, 2, 3), counts for PPP packets with various header errors/mismatches as provisioned in the registers.
- **CRC Field.** The CRC bad packet counter, PM_BPC_n (n = 0, 1, 2, 3), increments if a CRC error is found in channel n.

Each PPP packet not counted as a bad packet in PM_BHC_n counter or PM_BPC_n counter increments the PPP good packet counter, PM_GPC_n (n = 0, 1, 2, 3), for channel n. (See register descriptions, page 222.)

Note that each channel only has a single pair of good and bad packet counters.

Functional Description (continued)

Data Engine (DE) Block (continued)

Transmit Data Engine

ATM Cell Inserter. The ATM cell inserter provides X^{43} or X^{31} scrambling of the payload for transport of ATM cells over SONET. X^{31} scrambling is suitable for the transport of ATM cells over fiber where bit-level cell delineation is required. The state diagram for the X^{31} scrambler is shown in Figure 11, page 65. The ATM cell inserter will generate idle cells/bytes to fill the SONET/SDH payload when cells/packets are not available in the transmit direction FIFO of the UTOPIA block. For ATM cells, the GFC, PTI, and CLP fields of the idle cell header and the idle cell payload are provisionable via software registers. The idle generator generates idle cells/bytes to fill the SONET/SDH payload when cells/packets are not available in the transmit FIFO. Idle cell HCS is automatically calculated and inserted.

Header Check Sequence (HCS) Generator. The HCS generator performs a CRC-8 calculation over the first four header octets of the ATM cell. The generator inserts the result into the fifth octet of the ATM header.

SDL Frame Inserter. The SDL inserter performs SDL frame generation and X^{48} scrambling of the payload field. An optional CRC-16/32 field can be attached (SDL-CRC mode) and is calculated over the payload. The SDL inserter also periodically transmits scrambler state updates through a special 6-byte message. The time between scrambler state updates can be provisioned by software using register SDLFI_INT (see register description, page 231). The packet length header of scrambler state updates is the 16-bit word, 0x0001. Special A and B messages can be software-provisioned to send link layer 1 messages to downstream hardware. The packet length headers for the special A and B messages are 0x0002 and 0x0003, respectively.

Prescrambler. The prescrambler block optionally scrambles the payload using a self-synchronizing scrambler with a generator polynomial of $1 + x^{43}$ for HDLC and PPP packets. For HDLC frames, the entire frame, including header and trailer, is scrambled; however, HDLC flags are not scrambled. The scrambler may be disabled through the use of a software register. This scrambler removes excessive 0x7D and 0x7E bytes. For ATM cell and SDL packet traffic, this block is not used. (By randomizing the data, the scrambler prevents malicious use of the channel due to escaping 7D and 7E sequences.)

CRC-16/-32 Generator. An optional CRC-16/-32 generator on the whole packet frame can be performed. The generating polynomial for CRC-16 is $1+ x^5 + x^{12} + x^{16}$. The generating polynomial for CRC-32 is $1+ x + x^2 + x^4 + x^5 + x^7 + x^8 + x^{10} + x^{11} + x^{12} + x^{16} + x^{22} + x^{23} + x^{26} + x^{32}$.

HDLC Inserter. The HDLC framer provides frame check sequence (FCS) generation and insertion using either the CRC-ITU or CRC-32 generation polynomials. After optional CRC generation, the HDLC framer performs control escape (0x7D) stuffing, flag character (0x7E) or abort character (0x7D7E) insertion, and dry mode insertion (0x7D20, where the bits 20 are provisionable).

Postscrambler. The postscrambler block optionally scrambles the payload using a self-synchronizing scrambler with a generator polynomial of $1 + x^{43}$ for HDLC and PPP packets, in accordance with RFC1619. For HDLC and PPP packets, the entire frame, including header and trailer, is scrambled. The scrambler may be disabled through the use of a software register. For ATM cell and SDL packet traffic, this block is not used.*

* The ATM and SDL framer inserters have their own dedicated scramblers.

Functional Description (continued)

Data Engine (DE) Block (continued)

Transmit Data Engine (continued)

PPP Header Attach. The PPP attach function inserts the provisionable 4-byte PPP header if payload control bit 7 = 1 (addresses 0x10E0—0x10E3). The first and second bytes are set to 0xFF03, and the third and fourth bytes are set to a value defined by a software register in PPP_Tx_CHAN[0—3] (see register description, page 215).

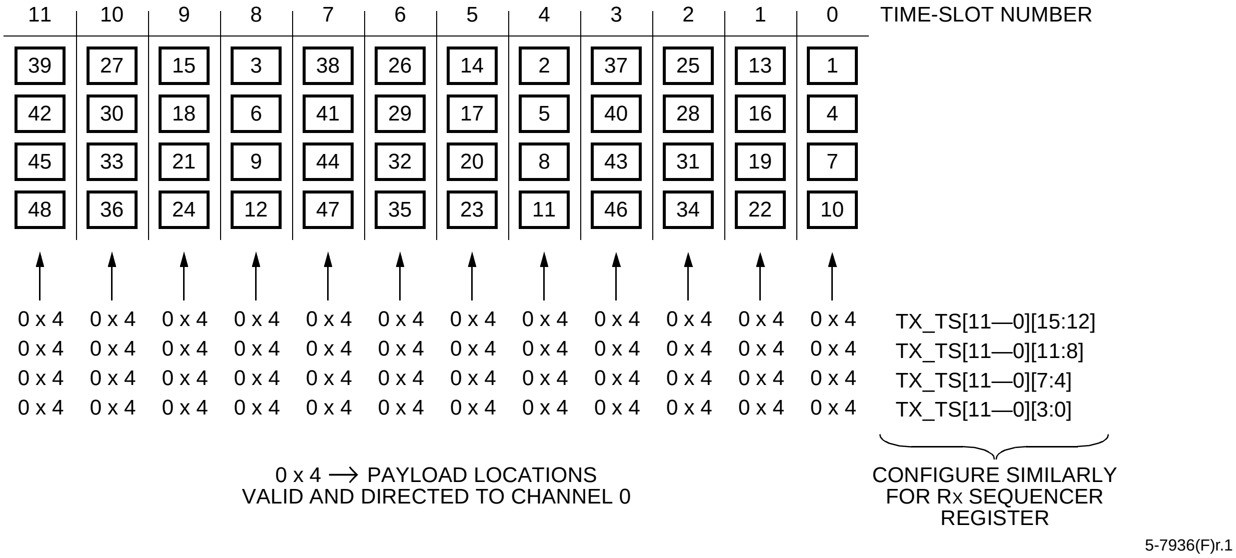
If payload control bit 7 = 0 (addresses 0x10E0—0x10E3) (compressed PPP header mode), only the two provisionable bytes defined by the software register PPP_Tx_CHAN[0—3] can be attached. Note that there is only one software register-defined protocol value for each channel.

The PPP attach function provides good packet count through a pair of 28-bit counters, PM_GPC_TX_[0—3] [27:0], per channel (see register description, page 224).

Tx Sequencer. The transmit sequencer maps logical channels into SONET frames, and must be provisioned properly for correct operation. The appropriate time slots must be provisioned for the rate of the payload expected for each channel. This is done via the registers Tx_TS[0—11] (see page 196 for register descriptions).

TDAT042G5 provides 12 time slots and four channels to define how data is mapped into the 48 synchronous transport signals (STS-1) of an STS-48 frame or into the 12/3 STS signals of an STS-12/3 SONET frame.

Figure 13 illustrates the mapping of the 48 STS-1 signals into an STS-48 signal and their assigned time slots. Each STS-1 block in the figure represents a byte of data for the specific STS-1 signal. The STS signals within the 12 time slots are ordered such that the SONET multiplexing requirements of lower rate signals into higher rate signals are satisfied. A value of 0x4 indicates that valid data is contained in the specific byte (STS) and the data is being received/transmitted from/to channel 0.



11	10	9	8	7	6	5	4	3	2	1	0	TIME-SLOT NUMBER
39	27	15	3	38	26	14	2	37	25	13	1	
42	30	18	6	41	29	17	5	40	28	16	4	
45	33	21	9	44	32	20	8	43	31	19	7	
48	36	24	12	47	35	23	11	46	34	22	10	
0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	TX_TS[11—0][15:12]
0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	TX_TS[11—0][11:8]
0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	TX_TS[11—0][7:4]
0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	0 x 4	TX_TS[11—0][3:0]

Figure 13. Example of Tx/Rx Sequencer Configuration: STS-48c into Single OC-48 Signal

Functional Description (continued)

Data Engine (DE) Block (continued)

Transmit Data Engine (continued)

Figure 14 illustrates the configuration of the time-slot registers for four independent STS-12 signals. In this case, there are 12 STS-1 signals that comprise each STS-12 signal.

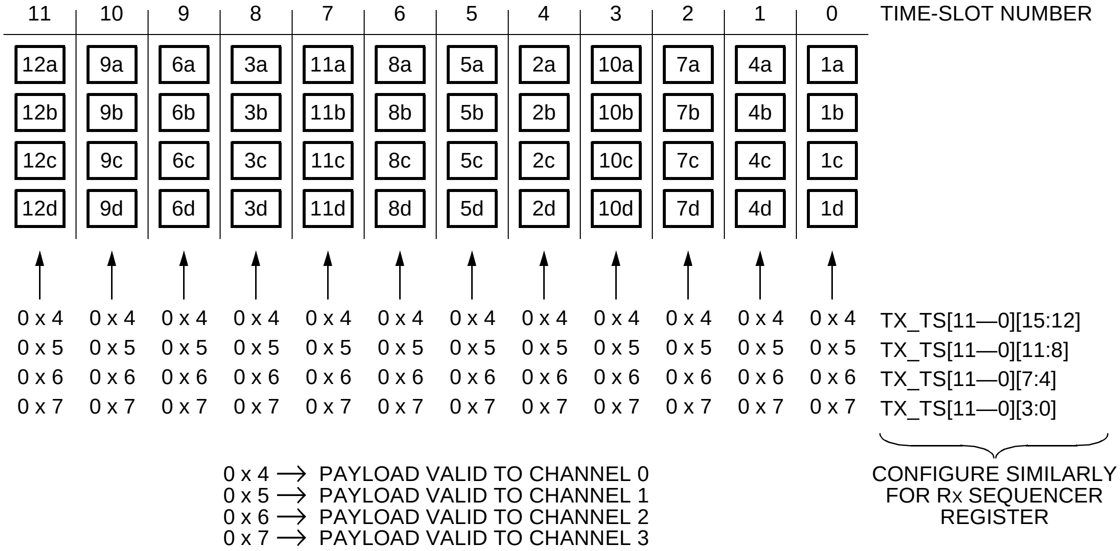


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Figure 14. Example of Tx/Rx Sequencer Configuration: 4xSTS-12c into Four Independent OC-12 Signals

Functional Description (continued)

Data Engine (DE) Block (continued)

Transmit Data Engine (continued)

The multiplexing rules of SONET are illustrated in Figure 15, and are shown for the case of two-stage byte interleaving of 12 STS-1 signals into an STS-12 signal. The values provisioned in the time-slot registers should obey the SONET multiplexing rules. In Figure 14, time slots 0 through 11 of channel A represent the interleaved bytes of the multiplexed STS-12 signal being received/transmitted in logical channel 0 (0x4). Channels B, C, and D are configured similarly, however, data is being received/transmitted from logical channels 1, 2, and 3, respectively.

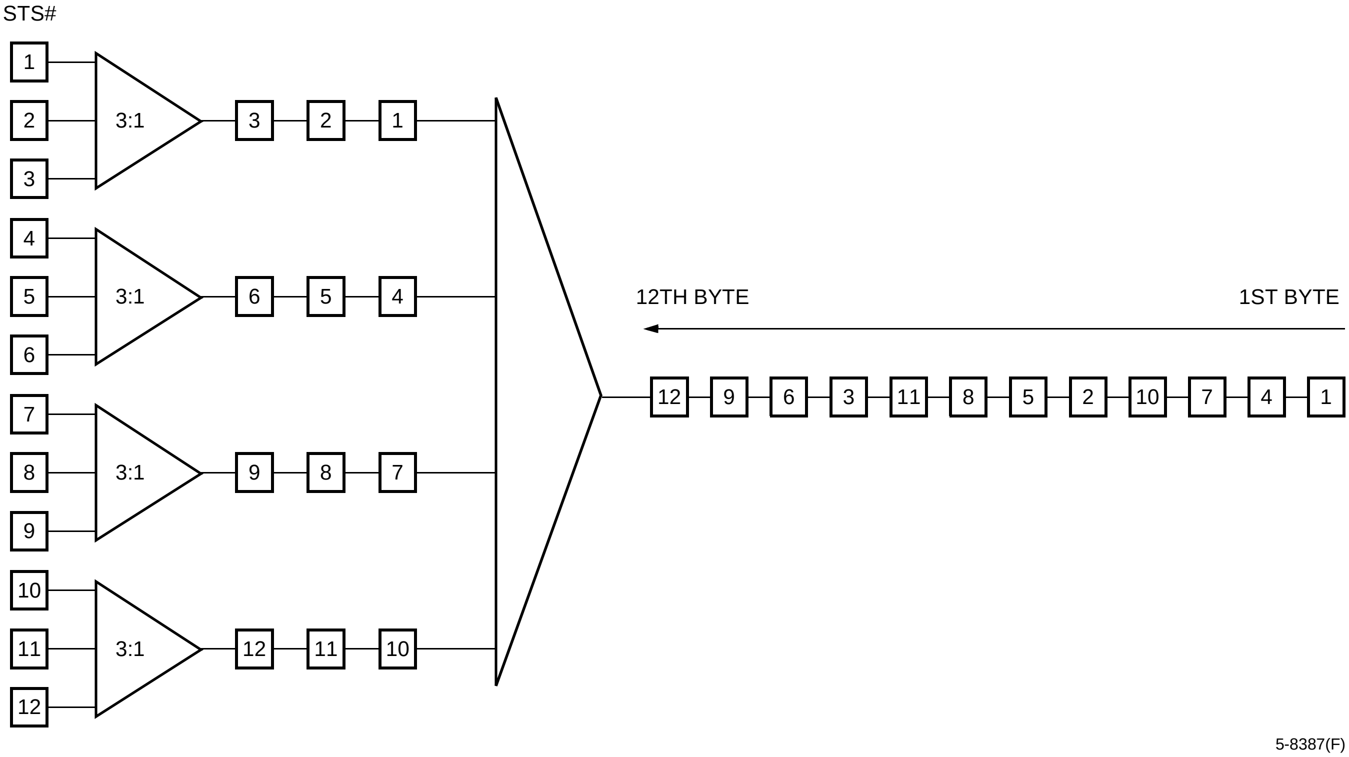

Figure 15. SONET Multiplexing: 2-Stage Byte Interleaving Example

Functional Description (continued)

Data Engine (DE) Block (continued)

Transmit Data Engine (continued)

Figure 16 illustrates the configuration of the time-slot registers for four independent STS-3 signals. In this case, there are three STS-1 signals that comprise each STS-3 signal. Since there are 12 time slots and only three are actually required, the values in time slots 3—11 can be repetitively configured as shown in the figure or can be configured as invalid, i.e., 0x0, 0x1, 0x2, and 0x3 for channels A, B, C, and D, respectively.

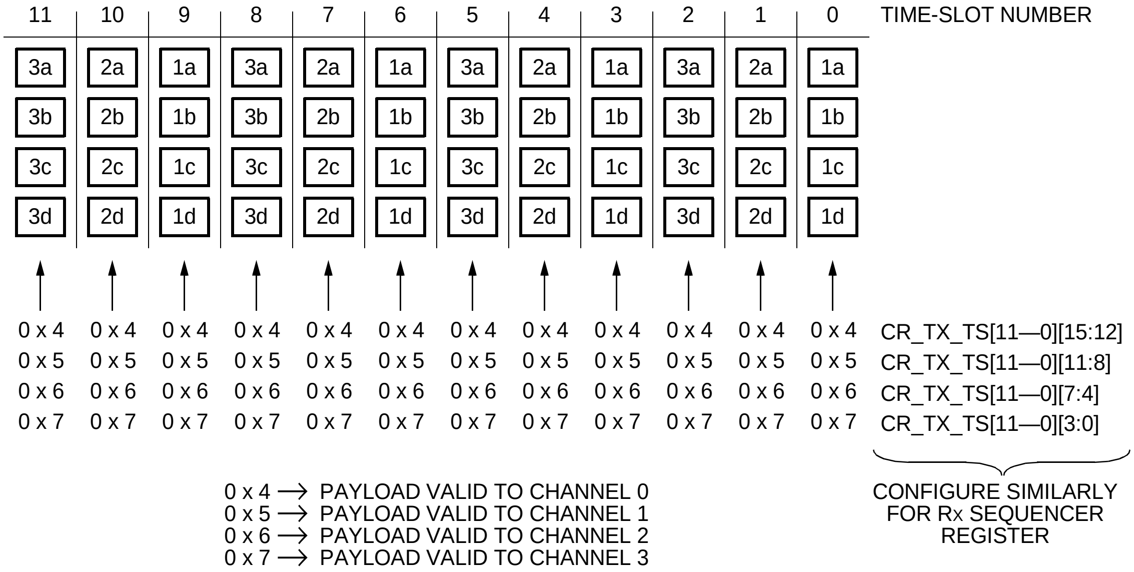

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Figure 16. Example of Tx/Rx Sequencer Configuration: 4xSTS-3c into Four Independent OC-12 Signals

Performance Monitoring

This block contains several cell/packet counters for receive/transmit data traffic. Two 28-bit saturating counters count the number of good packets/cells that are sent out and received by the enhanced UTOPIA interface. There are 28-bit counters used to count the number of corrected ATM HCS single bit errors, HDLC invalid sequences, and SDL corrected headers. Also, 28-bit counters are used to count the number of uncorrectable HCS errored ATM cells (discarded cells), HDLC short packets, SDL errored headers, packets with bad CRC checks, and bad PPP headers. These counters are operated in latch and clear mode (using PMRST) to ensure GR256 standards compliance. It is intended that these counters be polled at least once per second so that no error events are missed.

Functional Description (continued)

Data Engine (DE) Block (continued)

Over-Fiber Modes

In addition to the support of the normal SONET/SDH modes for different payload types such as HDLC, PPP, ATM (X^{43} or X^{31}), SDL as shown in Figure 2 on page 41, this device is capable of supporting the over-fiber modes for two payload types, SDL or ATM X^{31}. In the over-fiber mode, the data stream contains no SONET/SDH overhead bytes, and us it results in a 3% savings.

In other words, it is possible to utilize the whole bandwidth (155 Mbits/s for OC-3, 622 Mbits/s for OC-12, or 2.5 Gbits/s for OC-48) of the optical fiber for SDL packets or ATM cells.

As can be seen in Figure 17, for over-fiber modes the device is provisioned as follows.

- The line termination (OHP) and path termination (PT) blocks of the device need to be provisioned in the passthrough mode.
- The payload termination (DE) block needs to be set to the bit synchronization mode in the payload control register.
- The transparent mode in the transmit and receive sequencers (addresses 0x102E and 0x102F; see register description, page 204).
- The 12th bit of the mode register (address 0x0010) needs to be set to 0 so that the received clock drives the entire receive data path. In this way, there is no need to cross the clock domain boundary. As a result, only a single channel is allowed for OC-3, OC-12, or OC-48 when the device is operated in the over-fiber modes. In contrast, the device is capable of supporting four OC-3/OC-12 channels or one OC-8 channel in the SONET/SDH modes.

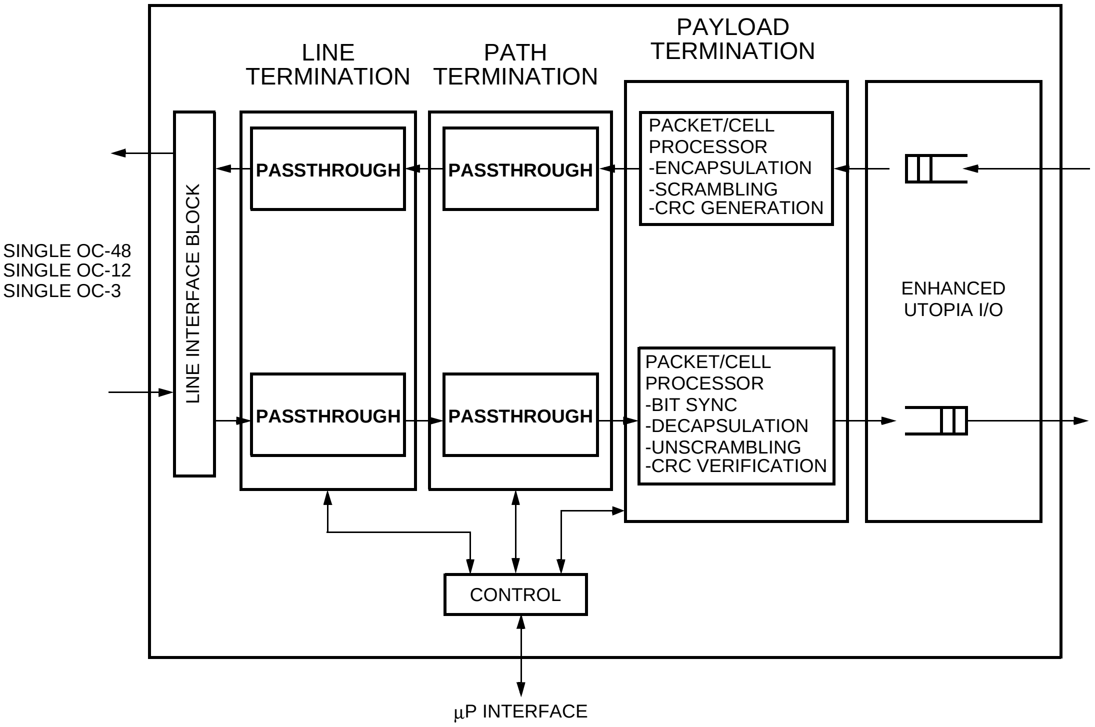

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Figure 17. TDAT042G5 Over-Fiber Modes: SDL, ATM (X^{31})

Functional Description (continued)

Data Engine (DE) Block (continued)

Transparent Payload Mode

The transparent payload mode in the payload termination data engine (DE) block is one of seven basic payload type modes in the payload control registers and allows data to pass directly through the DE. In this mode, no framing is done on the data, and the data in the SONET frame is treated as raw data. The transparent payload mode basically disables all the functions of the framers. In contrast, the transparent mode of the sequencer disables the conversion function of the sequencer between the SONET/SDH framing structure and the logical channel structure. If the device is set in both the transparent payload mode in the payload control registers and the transparent mode in the sequencer, then the whole SONET/SDH frame (overhead bytes will be overwritten with zeros) will appear at the receive UTOPIA interface as one packet. At the transmit UTOPIA side, the whole SONET/SDH frame needs to be supplied.

Transparent Receive Mode Control. In receiving from the line, provisioning must specify the time slot and SONET frame byte location where the last byte in the packet will occur. The following registers are used to indicate this location.

- Rx_CHCD_FM (address 0x1030; see register description, page 205) specifies the time slot where the last byte of a packet exists in channels C and D.
- Rx_CHAB_FM (address 0x1031; see register description, page 205) specifies the time slot where the last byte of a packet exists in channels A and B.
- Rx_CELLA_FM (address 0x1032), Rx_CELLB_FM (address 0x1033), Rx_CELLC_FM (address 0x1034), and Rx_CELLD_FM (address 0x1035) specify in which SONET location (0 to 809) the last byte in a packet exists in channel A, B, C, or D, respectively. (See register descriptions, page 206.)

  In the case where the location of the last byte in the frame is not known, the last byte should be provisioned for location 809 and time slot 12, and external UTOPIA hardware must perform packet delineation on the data stream.

Transparent Transmit Mode Control. In transmitting to the line, provisioning must specify the time slot and SONET frame alignment. This is done through Tx_TRANS_CTRL (address 0x102F; see register description, page 204) used in conjunction with Tx_TS[0—11] (addresses 0x1016—0x1021; see register descriptions, page 196).

Functional Description (continued)

UTOPIA (UT) Interface Block

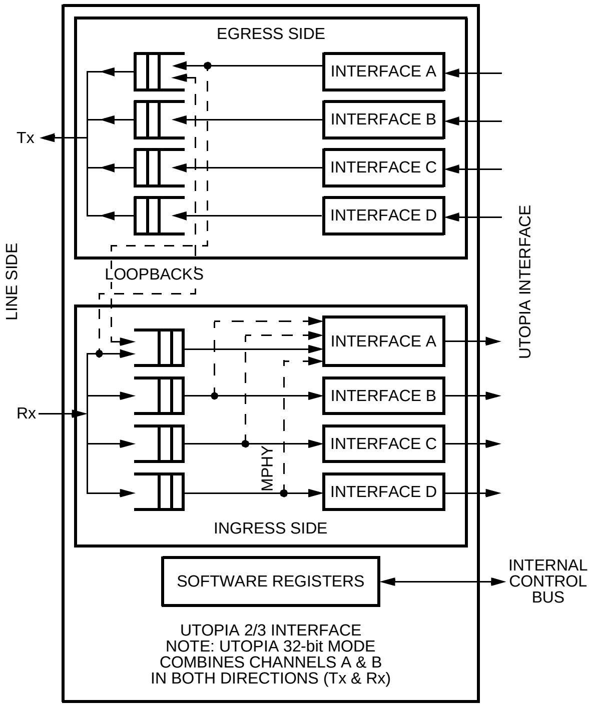
The UT core provides buffering and UTOPIA interface functionality. This enhanced UTOPIA interface will pass U2, U2+, U3, and U3+ protocols. In the receive direction, data is buffered from the line side, and sent out of the device via a UTOPIA/packet-over-SONET-PHY interface. In the transmit direction, data is received by the device via a UTOPIA/packet-over-SONET-PHY interface, and buffered before being sent to the line side. Data that is sent or received can be either packet or ATM traffic, and is configurable on a per-channel basis. The UTOPIA slave interface is designed to accommodate back-to-back ATM cell and packet data transfers in point-to-point or multi-PHY modes.

Level-2 physical interfaces (transmit and receive) support four logical data channels as shown in Figure 18. Each of these interfaces is independently configurable for cell or packet transfers, and can support up to STS-12/STM-4 bandwidth. Optionally, two of the interfaces, specifically A and B, can be grouped together to support a 32-bit UTOPIA level-3 interface supporting up to STS-48/STM-16 of bandwidth. The aggregate traffic that can be carried over these interfaces is limited to STS-48/STM-16 bandwidth.

In addition to operating as separate point-to-point streams, MPHY capabilities for up to four channels can be provided from the A interface in either 16-bit or 32-bit modes. For example, when operating as a 32-bit interface, the A interface can support either a single STS-48c channel or four STS-12c channels. As a 16-bit interface, the MPHY interface can support either a single STS-12c channel or four STS-3c channels.

Since each channel can be configured independently, each one can carry different traffic types at different rates, provided that the capabilities of the active interfaces and the data engine are not exceeded.

There are two basic data paths: receive side, defined to be data going from the line side to the UTOPIA side, and transmit side, defined to be data going from the UTOPIA side to the line side as shown in Figure 18.



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Note: For MPHY support, channels are mapped to interface A only.

Figure 18. UT Block Diagram

Functional Description (continued)

UTOPIA (UT) Interface Block (continued)

Enhanced refers to the extensions that have been added to support packet transfers. These extensions are indications of: (1) an end of packet (TxEOP/RxEOP), (2) the byte on which packet ends in last word (TxSZ/RxSZ), and (3) the signal to abort a packet early (TxERR/RxERR). An abort occurs for example, if the check sum at the end of a packet is bad, or the end of a packet is reached prematurely. If the receive FIFO overflows because the master cannot process packet data fast enough, an RxERR will also be generated.

UTOPIA Loopbacks

TDAT042G5 can be placed in loopback on a channel-by-channel basis. When the TDAT042G5 is placed in far-end loopback (FELB), data from the DE is sent to and processed by the UTOPIA interface. Instead of sending it to the UTOPIA master, however, the data is sent to the corresponding egress channel and back to the line interface.

When the TDAT042G5 is placed in near-end loopback (NELB), data from the egress channel is transferred to the corresponding ingress channel, instead of the DE. This data is then processed by the ingress channel and is returned to the UTOPIA master.

UTOPIA Modes

Each UTOPIA interface mode is capable of supporting various types of traffic with different bandwidth capabilities as summarized in Table 24. In a point-to-point operational mode, any interface can be configured independently in any of the defined modes (e.g., channel A passes ATM cells using STS-12c, channel B passes packets, etc.).

It should be noted that the U3 or U3+ (32-bit mode) can only be supported by overloading channel A and B interface pins. Only the control signals from channel A are used. The channel B size and data bits are combined with the channel A size and data bits to form the 2-bit size and the 32-bit data words. when 32-bit mode is selected, channels B, C, and D must be configured to be idle (so that channel B will be under the control of channel A in 32-bit mode).

Multi-channel multi-PHY (MPHY) capabilities are only supported on interface A by grouping the internal FIFOs and data paths of channels B, C, and D as needed. This operational mode is described in a later section.

Table 24. UTOPIA Traffic Types

UTOPIA Name	Interface Width	Maximum Speed	Aggregate Bandwidth	Traffic Type	Maximum Number of Interfaces
U2 (sinking clock)	16 bits	52 MHz*	622 Mbits/s (STS-12)	ATM cells only	4
U2+	16 bits	52 MHz*	622 Mbits/s (STS-12)	ATM cells/packets	4
U3, 8-bit mode (sinking clock)	8 bits	104 MHz	622 Mbits/s (STS-12)	ATM cells only	4
U3+, 8-bit mode	8 bits	104 MHz	622 Mbits/s (STS-12)	ATM cells/packets	4
U3, 32-bit mode (sinking clock)	32 bits	104 MHz	2.5 Gbits/s (STS-48)	ATM cells only	1
U3+, 32-bit mode	32 bits	104 MHz	2.5 Gbits/s (STS-48)	ATM cells/packets	1

* Maximum speed may be exceeded if non-standard load conditions are used and the clock is sourced.

Functional Description (continued)

UTOPIA (UT) Interface Block (continued)

UT Receive Input Path (Ingress)

The UTOPIA Rx interface is designed to accommodate ATM cells as well as packet traffic. While the standard UTOPIA interface transmits and receives ATM cells, this interface has been enhanced to carry non-ATM traffic. The interfaces supported include the following: UTOPIA Level 2 (U2), enhanced UTOPIA Level 2 (U2+), UTOPIA Level 3 (U3) in 8-bit mode or 32-bit mode, and enhanced UTOPIA Level 3 (U3+) in 8-bit mode or 32-bit mode.

In the receive direction, data arrives and is sent to one of four channels (A through D). Each channel buffers data independently, and when sufficient data has been stored in its FIFO, sends the data out of the channel via its UTOPIA interface. There are four paths inside the UT core, corresponding to one path per channel. These paths are labeled A to D. When using 32-bit modes, only the control signals of interface A and size signals of interfaces A and B are used.

Note: 32-bit mode is supported using channels A and B only. When 32-bit mode is selected, channels B, C, and D must be configured to be idle (channel B will be under the control of channel A in 32-bit mode).

In normal mode, data arrives into the ingress channel, and control and data information are written into the FIFO. The data is extracted from the FIFO, and word-aligned on the first byte of data. After word alignment, the data is sent out of the device via the UTOPIA interface.

Note: The start of packets must be word-aligned and there can only be one packet per word, as this is required by the definition of the UTOPIA interface.

FIFO. The 256-byte UTOPIA Rx FIFO is responsible for buffering data from the DE block to be sent to the UTOPIA interface. The FIFO accommodates four ATM cells or 256 bytes of packet data. In STS-48/STM-16, only one 256-byte FIFO is used. The FIFO is required to manage the asynchronous nature of the UTOPIA interface. Overflow will only occur if the master device connected to the UTOPIA interface is having congestion problems. When overflow occurs and head of line discard is performed, it is possible that part of one packet may be appended to another (if for example, an end of packet is discarded along with the data at the head of the FIFO). Because this is not a desirable operation, it is necessary to discard until the start of the next packet is observed. Data is read from the FIFO when there is sufficient data in the FIFO. Upon overflow, the RxERR and RxEOP signals are asserted to indicate to the master the corruption of the current packet.

Sufficient data is defined to be a minimum amount of data in the FIFO (a programmable threshold, low watermark), or at least one end of packet stored in the FIFO. If the FIFO overflows, the block is responsible for discarding data until the next start of packet. When this occurs, an alarm is raised. Underflow in the receive direction can occur when there is no data, or if only part of a packet has arrived and has been transmitted, and is normal behavior.

Functional Description (continued)

UTOPIA (UT) Interface Block (continued)

UT Receive Input Path (Ingress) (continued)

Receive Cell/Packet Available (RxPA). This signal indicates when the TDAT042G5 receive FIFO can send data to the master device. The RxPA[D:A] signal behavior depends on the provisioned low watermark in the UTOPIA interface.

- **One-Cycle Delay Mode.** This mode follows the UTOPIA Level-2 Standard. The RxPA response occurs one cycle after the address is polled. RxENB is asserted to activate the selected PHY. RxDATA and RxSOP are output one cycle after RxENB is sampled active by the PHY device.
- **Two-Cycle Delay Mode.** This mode follows the UTOPIA Level-3 Baselined Text. The RxPA response occurs two cycles after the address is polled. RxENB is asserted to activate the selected PHY. RxDATA and RxSOP are output two cycles after RxENB is sampled active by the PHY device.
- **RxPA[D:A] Assertion.** RxPA[D:A] goes high (is asserted) when the amount of data in the receive FIFO has reached or exceeded the low watermark **or** there is end of packet (EOP) resident in the FIFO.
- **RxPA[D:A] Deassertion.** In ATM mode, the RxPA[D:A] signal goes low (is deasserted) when the FIFO has less than the low threshold amount of data **and** there is no EOP inside the FIFO (i.e., part of an ATM cell). Once the last byte of the current cell is transmitted, and if the amount of data within the FIFO is still less than the low threshold, RxPA[D:A] is deasserted.

  In packet mode, the RxPA[D:A] signal goes low (is deasserted) when the FIFO has less than the low threshold amount of data and there is no EOP inside the FIFO.

  Once the data transfer begins (since the amount of data has reached or exceeded the low watermark), and if there is no EOP below the low threshold (i.e., a long packet), the RxPA signal is deasserted when the FIFO is drained by the UTOPIA master device. In this case, the master must closely monitor the RxPA[D:A] signals and use these signals as data valid indicators to ensure that bad data is not read from the TDAT042G5. TDAT042G5 will deassert the RxPA[D:A] signal immediately when the FIFO is drained.
- **Data Transfer.** A TDAT042G5 ingress channel sends data when it has asserted RxPA[D:A] and the master device requests data (via RxENB[D:A]). In ATM mode, if the master device requests data using RxENB[D:A] and if the TDAT042G5 has less than the low watermark amount of data to send and there is no end of cell in the FIFO (RxPA[D:A] is deasserted), then the TDAT042G5 UTOPIA interface will send out data that should be ignored by the master, i.e., it does not send data from its internal FIFO.

  In ATM mode, once an ATM cell transfer starts, the Tx or Rx side must complete the transfer. If the transfer is not completed, then the cell will be corrupted. The transfer continues until either (1) the end of cell is reached, when the end of cell exists below the low watermark, or (2) the end of the FIFO is reached. If the end of the FIFO is reached, no underflow is flagged on the receive side. In ATM mode, the low watermark should be set so that at least one entire cell is in the FIFO prior to asserting RxPA[D:A].

  In packet mode, once the data transfer begins, the RxPA[D:A] signal will remain asserted until the FIFO is drained if there is no EOP below the low watermark. During the time RxPA[D:A] is asserted, valid data is being transferred.

  RxPA[D:A] is updated on the rising edge of RxCLK[D:A].

  In 32-bit mode, only the RxPA[A] pin of port A is used to indicate the packet/cell available status.

Functional Description (continued)

UTOPIA (UT) Interface Block (continued)

UT Receive Input Path (Ingress) (continued)

Figure 19 illustrates the receive side interface handshaking when operating in point-to-point mode with the RxPA response provisioned to be a single cycle. In two-cycle mode, the RxSOP, RxDATA, and RxPA signals are delayed an additional cycle. In the figure, the master device initiates the transfer after observing an asserted packet available for the channel. The TDAT042G5 samples RxENB low on the first cycle and then asserts RxSOP/C and RxDATA on the second cycle. RxDATA is sampled on the rising edge of the second cycle by the master device.

In this example, the master stops transfer in the middle of the packet. Data with value 'c' is valid on the cycle that RxENB goes inactive, and when RxENB returns, data is again valid on the first cycle after the slave observes an active RxENB (data value d).

The packet transfer is complete when the slave asserts the RxEOP signal. If an error occurs in the packet, then the RxERR signal is asserted simultaneously with the RxEOP. RxERR is ignored if it is not asserted when RxEOP is active.

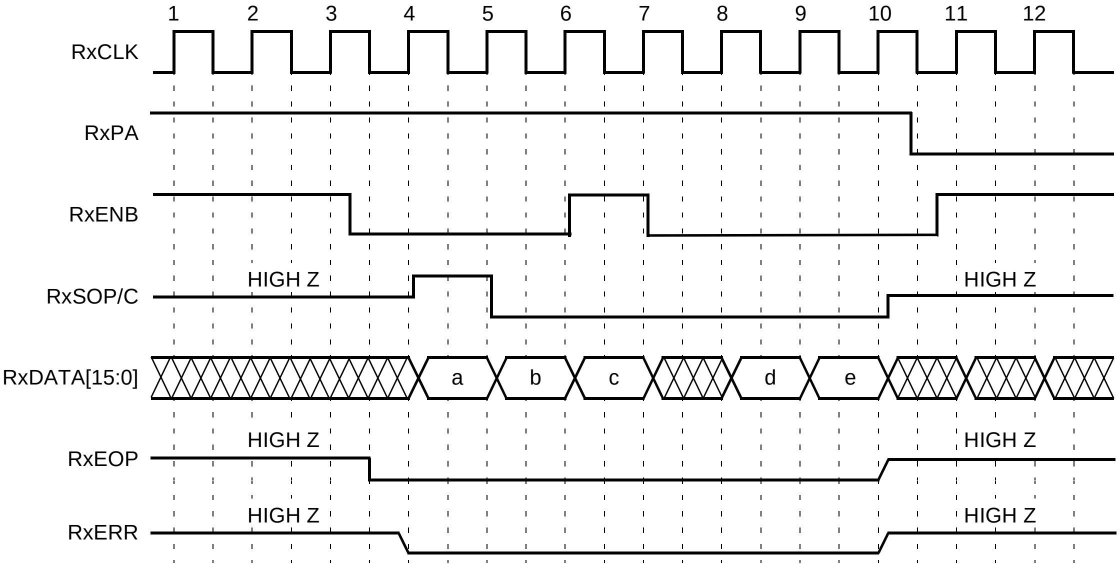

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Figure 19. Receive-Side Interface Handshaking in Point-to-Point Mode (RxPA as Single Cycle)

Clocks

In the receive direction, the receive UTOPIA clock, RxCLK, can be provisioned to be either sourced by the TDAT042G5 or received from the UTOPIA master. For RxCLK rates greater than 52 MHz, the clock must be sourced by TDAT042G5. In this mode, the RxCLK is derived from the corresponding transmit UTOPIA clock, TxCLK.

Functional Description (continued)

UTOPIA (UT) Interface Block (continued)

UT Transmit Input Path (Egress)

In the transmit direction, data arrives from the various UTOPIA interfaces, and is stored in a 256-byte FIFO, one per channel. After sufficient data has been stored into the FIFO, it is made available to be sent to the DE.

Like the UTOPIA Rx interface, the UTOPIA Tx interface is designed to accommodate ATM cells as well as packet traffic. While the traditional UTOPIA interface only transfers ATM cells, this interface has been enhanced to carry packet traffic. The interfaces supported include the following: UTOPIA Level 2 (U2), enhanced UTOPIA Level 2 (U2+), UTOPIA Level 3 (U3) in 4 x 8-bit mode or 32-bit mode, and enhanced UTOPIA Level 3 (U3+) in 4 x 8-bit mode or 32-bit mode.

The UTOPIA Tx side can indicate to the ATM side to suspend the transfer, by deasserting TxPA, when necessary. When the amount of data in the FIFO exceeds its programmable high watermark, it deasserts TxPA. This signal causes the deassertion of TxPA on the next clock. At this point, the ATM side knows that the UTOPIA Tx block can only accept a limited number of words, after which it will overflow. In this case, the ATM device must not exceed writing this limited number of words before suspending the transfer. Transfer is resumed once again when the FIFO falls below the high watermark. When transferring ATM cells, TxPA must be deasserted four clocks before the end of cell, or else it must be prepared to accept an entire new cell. When transferring ATM cells, deasserting TxPA does not immediately suspend the transfer of the current cell because the entire cell can be transmitted without interruption.

Transmit Cell/Packet Available (TxPA). The TxPA[D:A] signal behavior relies on the UTOPIA provisionable watermarks.

- High Watermark. In packet mode, TxPA goes high when the amount of data in the FIFO is less than the high watermark setting. In ATM mode, TxPA goes high when the FIFO has space to receive a complete ATM cell from the master (this requires the thresholds to be set appropriately by the user, i.e., set so that an entire cell can be received once TxPA goes inactive).

  In packet mode, TxPA goes low when the amount of data in the FIFO reaches or exceeds the high watermark. In ATM mode, TxPA goes low when there is not enough space in the FIFO to receive an entire ATM cell (this requires the threshold values to be provisioned properly, i.e., set low enough such that when the high watermark is reached, the transmission of the current cell can be completed without overflowing the FIFO). In ATM mode, TxPA will be deasserted four cycles before the end of the current cell transfer if the FIFO cannot accept a complete ATM cell on the following transmission.

- Low Watermark. The low watermark in the Tx direction is relevant for defining when data is sent from the UTOPIA block to the data engine. A particular egress channel will send data upon a request from the data engine if (1) there is greater than or equal to low threshold amount of data in the TxFIFO **or** (2) there is an end of packet (EOP) currently residing in the FIFO. This implies that if there is a complete ATM cell inside the FIFO, the corresponding egress channel will send this data to the data engine because an ATM will have an EOP within the FIFO.

  Once data transmission to the data engine begins, it continues until it reaches the EOP, which exists below the low watermark, **or** until it reaches the end of the FIFO, where it is flagged as an underflow. The UTOPIA side notifies the data engine that it has run dry. The data engine can either insert a dry escape character into the data stream (dry mode, user-provisionable value, 0x7D20 default) or it can insert an abort character into the data stream (0x7D7E).

  In ATM mode, the low watermark should be set to a value greater than 0xE so that at least one ATM cell is in the FIFO before the data can be sent to the data engine; otherwise, the egress channel will start to send data, and could possibly dry the FIFO in the middle of an ATM cell. This can occur in the case where the low watermark is set lower than a complete ATM cell size and the transmit clock is slower than the system clock.

Functional Description (continued)

UTOPIA (UT) Interface Block (continued)

UT Transmit Path (Egress) (continued)

FIFO. The UTOPIA Tx FIFO is used to create an elastic store that can buffer bursts of data received via the UTOPIA Tx, faster than can be transmitted out of the path. After the FIFO exceeds a programmable watermark, it indicates to the UTOPIA Tx master to stop sending data. The master can choose to ignore this request causing the risk of an overflow. The FIFO block buffers 256 bytes of cell/packet data. The FIFO accommodates four ATM cells or 256 bytes of packet data. The FIFO is required to manage the asynchronous nature of the UTOPIA interface.

Optionally, in the case of FIFO underflow, a 0x7D207D207D20 . . . will be inserted by the data engine into the middle of the packet if dry mode is provisioned and the default dry escape sequence is used (0x7D20, where the bits 20 are provisionable). This will be removed at the far end by the device (provided the link is comprised of two devices and both sides of the link support dry mode).

Note: When carrying ATM cell traffic, this threshold, while measured in words, should be set at least one cell's length from end of FIFO. The UTOPIA Tx interface, by definition, must be able to accept an entire ATM cell after the current ATM cell, unless TxPA is deasserted at least four clock cycles before the end of the current cell transfer.

When carrying packet traffic, however, the threshold can be set higher, as the UTOPIA Tx interface only needs to accept a limited number of words after deasserting TxPA. The number of words is a programmable value for the sender, and should be assumed to be at least 2 words for the purposes of setting the threshold.

Figure 20 illustrates the transmit side interface handshaking when operating in point-to-point mode with the TxPA response provisioned to be a single cycle. In two-cycle mode, the TxPA signal is delayed an additional cycle. In the figure, the master device initiates the transfer after observing an asserted packet available for the channel by asserting the TxENB signal. The master places data and start of packet on the bus the same cycle as TxENB, and the TDAT042G5 samples the TxSOP and TxDATA on the following clock cycle (rising edge).

In this example, the master stops transfer in the middle of the packet. Data with value ‘c' is valid on the cycle that TxENB goes inactive, and when TxENB returns, data is again valid on the first cycle (data value d).

The packet transfer is complete when the master asserts the TxEOP signal. If an error occurs in the packet, then the TxERR signal is asserted simultaneously with the TxEOP. TxERR is ignored if it is not asserted when TxEOP is active.

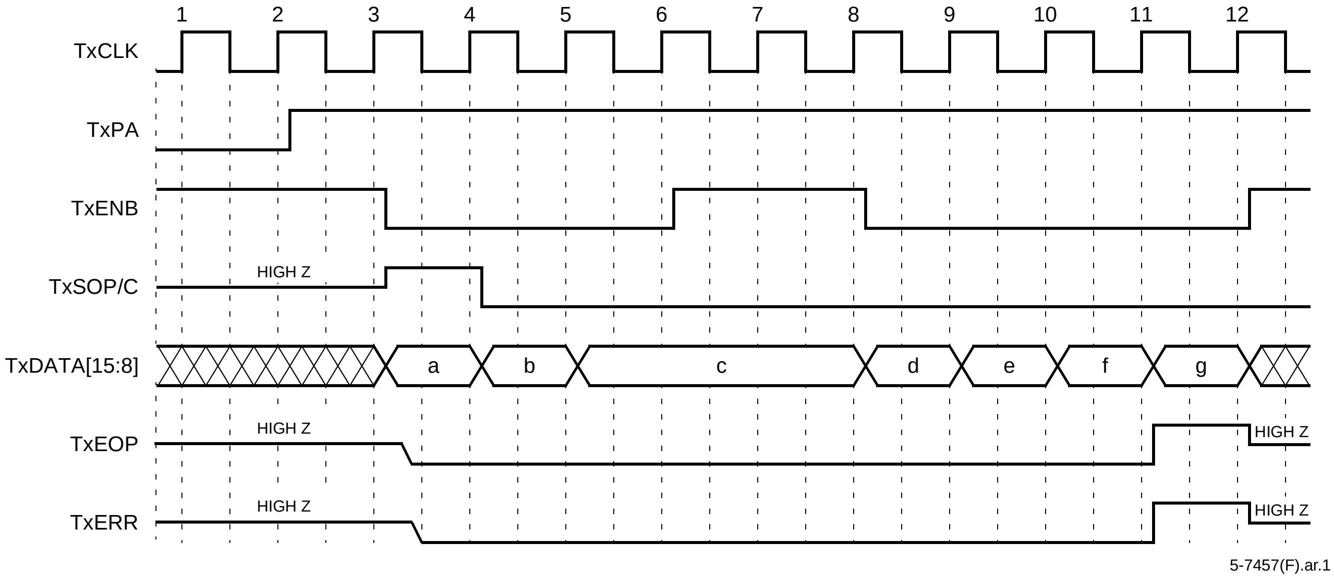

Figure 20. Transmit-Side Interface Handshaking in Point-to-Point Mode (TxPA as Single Cycle)

Functional Description (continued)

UTOPIA (UT) Interface Block (continued)

Multi-PHY Support

In addition to point-to-point UTOPIA mode, the TDAT042G5, as the slave device, can also be configured to support the polled multi-PHY mode. To operate in the polled mode, channel A must be configured in the polled mode, since the control signals of channel A are used for all channels. Any combination of B, C, or D can be included in the polling group, in which case they provide control information to channel A. Channels not configured for polling can be operated as point-to-point connections. When configuring the point-to-point 32-bit mode, only channel A is active and channels B, C, and D must be set as idle. However, in polling mode, channels B, C, and D also can be configured in any of the UTOPIA modes. In this case, the output is transferred through the channel A interface (channel A and B interfaces for 32-bit mode). If channel A is in 32-bit polling mode, channel B can not be in point-to-point mode since its interface is controlled by channel A, while channels C and D may be provisioned as point-to-point connections. Figure 21 shows a multi-PHY mode when all four channels of the UT are in polling mode.

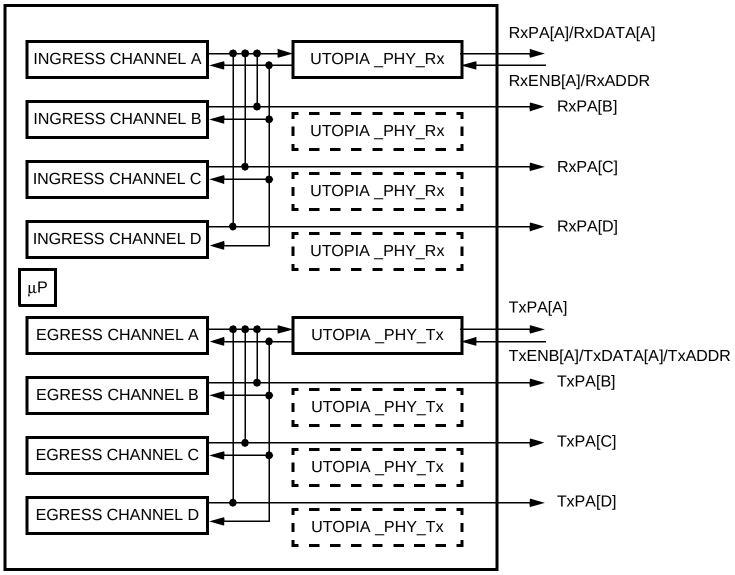

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Figure 21. Multi-PHY Configuration of All Four Channels

Mixed mode polling is also possible. For example, for those channels operated in polling mode, it is legitimate for some of the channels to be in packet mode while others are in ATM mode. However, if one or more of the channels are in packet mode, channel A should be configured as packet mode to activate control signals for packet transfer.

Multi-PHY operation can be configured by asserting the polling mode enable bit and Tx/Rx address in the respective port provisioning registers (see port provisioning registers, pages 144—147). Microprocessor provisionable registers in each channel include a polling mode enable bit, and 5-bit Rx address or 5-bit Tx address. The value for the Tx and Rx address of an MPHY channel must be identical. Both the Rx and Tx directions have a 5-pin address input to poll and select the appropriate PHY.

In 8-bit or 16-bit multi-PHY mode, only the data bus and the control signals (except the RxPA or TxPA signal) of channel A are active for the polled group. RxPA[A] indicates the packet/cell availability of the selected or polled channel. Similarly, TxPA[A] indicates transmit FIFO availability for a selected or polled channel. The remaining RxPA/TxPA signals for the polled channels are activated and indicate instantaneous or direct status of the particular channel. In 32-bit multi-PHY mode, the data bus and size control signals of channel B are also active.

Functional Description (continued)

UTOPIA (UT) Interface Block (continued)

Multi-PHY Support (continued)

TDAT042G5 does not provide a selected packet available (SPA) signal to monitor the status of the current channel sending/receiving data to or from the master. To prevent the FIFOs from running dry or overflowing in the middle of a packet transfer, the user must design the UT TDAT042G5 slave-to-master interface with direct status mode rather than address polling. The direct status of each channel is provided on the associated SPA pin for that channel. In this mode, the user must guarantee that when channels are switched to receive data from a channel other than channel A, they immediately reapply the address of channel A to the address bus after the new channel is selected. The user then gets the direct status SPA signal from channel A. Channels B, C, and D are always directly sent out of the TDAT042G5. In either receive or transmit, when direct status is used in addition to the direct status pin for a given interface, its corresponding interface clock pin must be driven by the clock of the A interface.

During the cycle when the selected channel is being changed, the address of the new channel is placed on the address bus. The user must ignore the RxPA response of the initial channel during the expected response time (one or two cycles later, depending on the PA response bit when the address of the newly selected channel was applied).

Figure 22 illustrates the transmit interface timing for the case when the direct status of packet available of channels A, B, C, and D is present. In this example, channels A and C indicate they can receive data. When the SPA signal for C is observed, a channel switch is performed by the master by deasserting TxENB and placing the address of channel C on the address bus. On the following cycle, data is placed on the bus along with the start of packet. In this example, the TxPA response is configured for two cycles so that the PA response of address ‘02’ results in the PA of channel C to appear on channel A’s output two clock cycles later. Subsequent data sent to the slave will go to channel C (i.e., data values I, J, etc.).

Functional Description (continued)

UTOPIA (UT) Interface Block (continued)

Multi-PHY Support (continued)

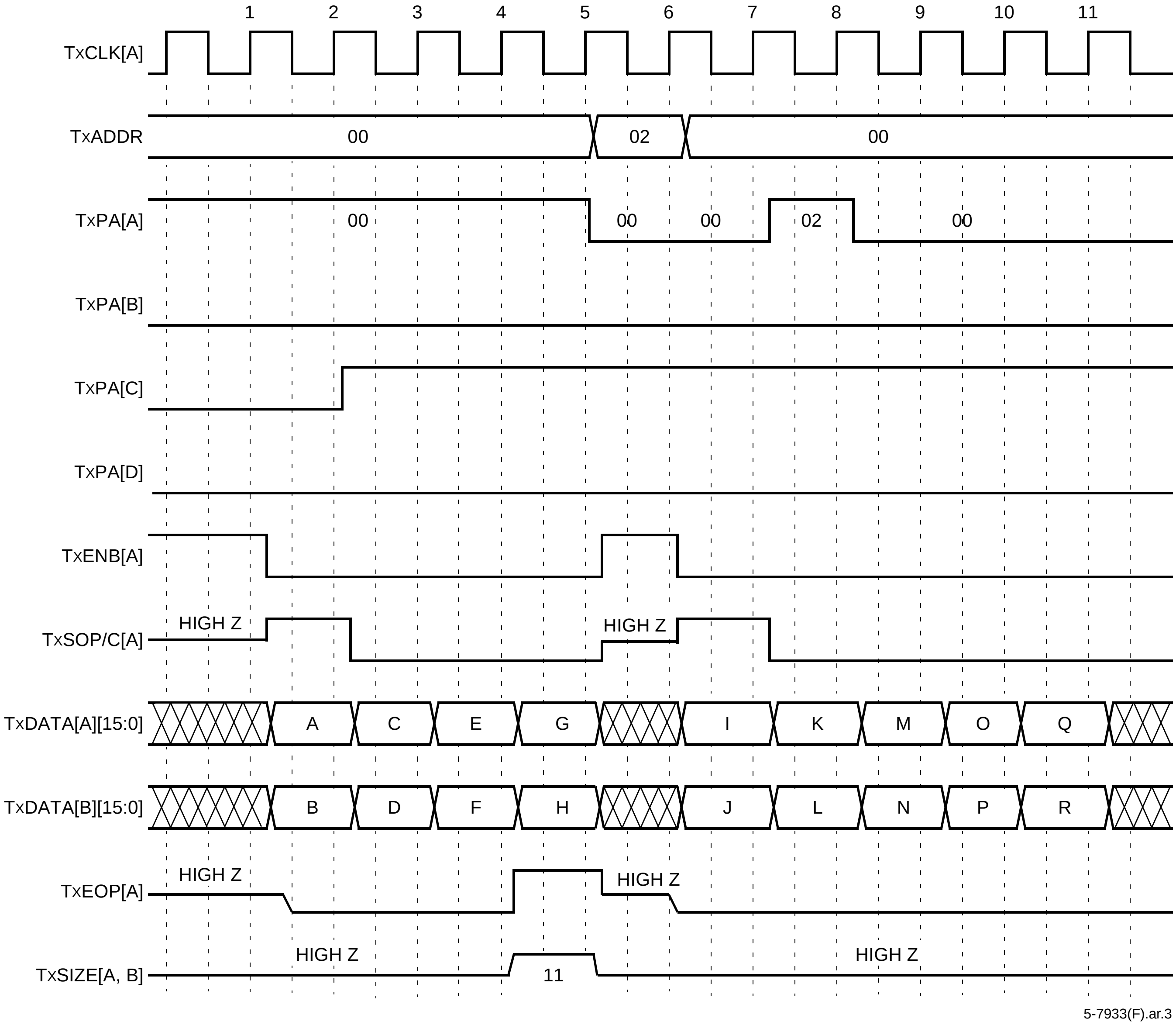

Figure 22. TxPA Two-Cycle Responses of a Multi-PHY for All Four Channels

Functional Description (continued)

UTOPIA (UT) Interface Block (continued)

Multi-PHY Support (continued)

The ATM side sends one RxENB (TxENB) signal to channel A for the grouped channels to select a channel which has ATM cells/packets (or room) available. An MPHY channel is selected using the following procedures. First, the ATM layer polls the RxPA (TxPA) status of a channel by placing its address on the RxADDR (TxADDR) lines. Second, in the following cycle, the MPHY channel gives its status by driving RxPA (TxPA) of channel A. Third, the ATM side selects the MPHY channel by placing the desired MPHY address, (at the current cycle, the RxENB or TxENB is deasserted). Finally, during the next cycle, the ATM side asserts RxENB (TxENB), and the selection of an MPHY channel is made. Only one MPHY channel at a time is selected for a cell/packet transfer when ATM drives RxENB (TxENB) for channel A from high to low. However, another MPHY channel can be polled for its RxPA (TxPA) status while the selected channel transfers data.

Figure 23 shows an example of the single-cycle RxPA response of each channel. In this figure, channels A, B, C, and D have Rx addresses 00, 01, 02, and 03, respectively. RxPA[A] shows the packet availability of all four channels. Channels A and C have available packets to send, and channels B and D do not have packets to send. By driving RxENB[A] low at clock edge 1, the ATM side selects channel A, and packet transfer is started at clock edge 2. The master samples this data at clock edge 3. At clock edge 4, RxPA[C] shows that channel C also has a packet to send, and this is reflected to RxPA[A] at clock edge 5. RxPA[B] and RxPA[D] show the direct status of channels B and D, indicating that they do not have packets to send.

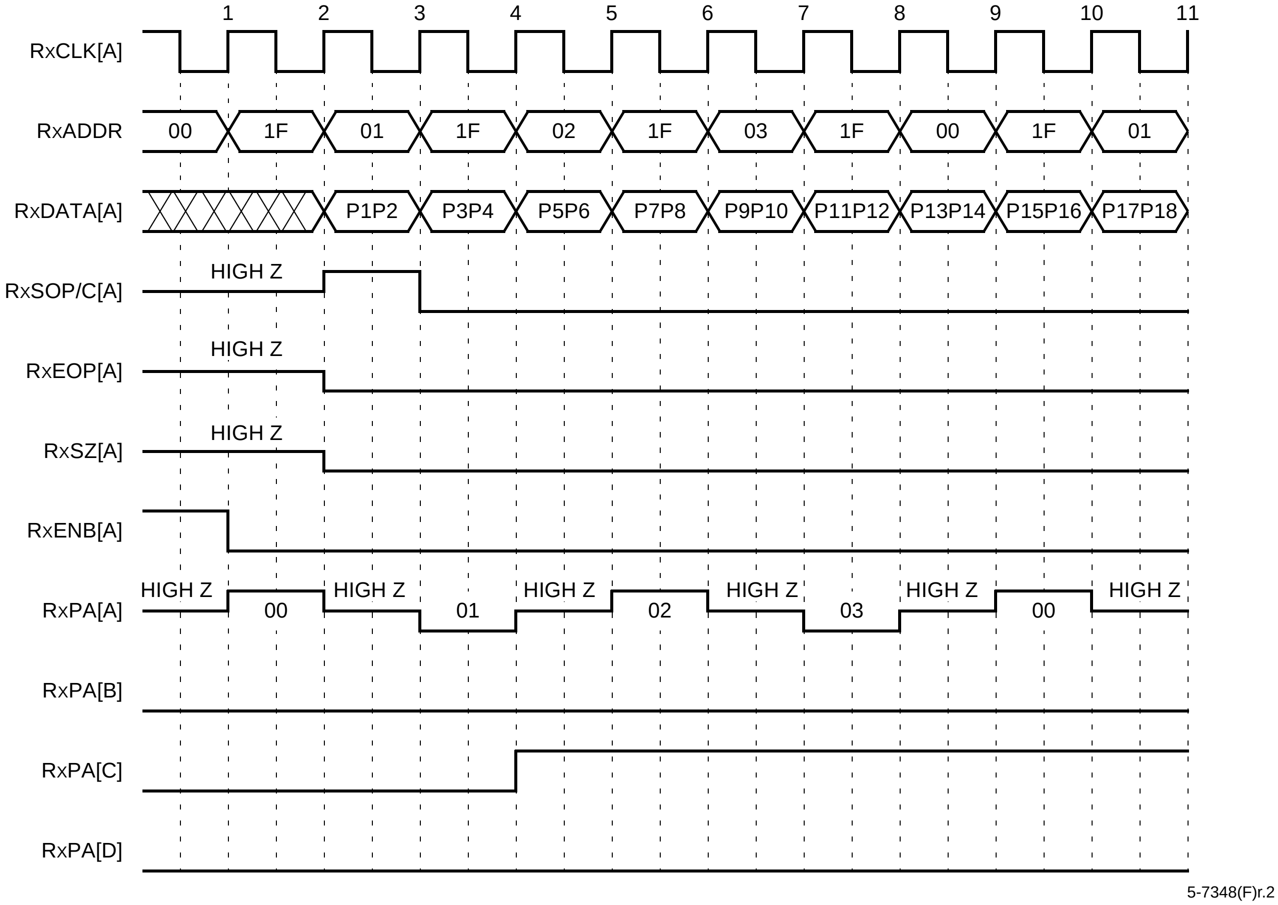

Figure 23. RxPA Responses of a Multi-PHY for All Four Channels (PA Response Configured for One Cycle)

Functional Description (continued)

JTAG (Boundary-Scan) Test Block

The JTAG test block provides an *IEEE* 1149.1 JTAG controller interface for memory BIST, boundary scan, and 32-bit ID register instructions. Details about JTAG (boundary-scan) functionality and interface timing specifications can be found in MN98-060ASIC-02, *HL250C 3.3 Volt 0.25 µm CMOS Standard-Cell Library* Manual, pages 8-1 through 8-31.

Interface Description

Microprocessor Interface

This device is equipped with a generic 16-bit microprocessor interface that allows operation with most commercially available microprocessors. Input MPMODE is used to configure this interface into one of two possible modes (synchronous or asynchronous). In synchronous mode, the microprocessor interface can operate at speeds from 1 MHz up to 66 MHz.* In asynchronous mode, the internal 78 MHz system clock is used to operate this interface.

Table 25. MPU Modes

MPMODE	Mode	Microprocessor Interface Signals
0	Async	$\overline{CS}$, $\overline{INT}$, D[15:0], A[15:0], $\overline{ADS}$, R/$\overline{W}$, $\overline{DS}$, $\overline{DT}$
1	Sync	MPCLK, $\overline{CS}$, $\overline{INT}$, D[15:0], A[15:0], $\overline{ADS}$, R/$\overline{W}$, $\overline{DT}$

The host interface is designed to connect directly to a commonly used asynchronous or synchronous host bus. The interface to this block includes a separate clock, MPCLK, which is used in the synchronous interface mode. The interface is only a slave on the host bus. There is no posting of writes in the host interface; all registers are directly accessible.

The microprocessor interface pins use 3.3 V (5 V, TTL-tolerant) CMOS I/O levels. The microprocessor interface timing specifications are given in the Interface Timing Specifications section (see Table 149—Table 152, pages 236—242).

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*All status counters must be read within the 1-second time window of the PMRST. If this is not the case, counter values will be lost.

Interface Description (continued)

General-Purpose I/O Bus (GPIO)

GPIO[3:0] are bi-directional pins. They can be configured individually as input or output by writing to GPIO mode register (address 0x0013; see register description, page 139). The value to be output is written into the GPIO output register (address 0x000F; see register description, page 137). The input value is read from the GPIO input register (address 0x000A; see register description, page 135). GPIO pins can also be used to generate an interrupt upon a change in value. An interrupt can be generated on either the input level or edge, depending on the GPIO mode register. Figure 24 shows how the GPIO functions.

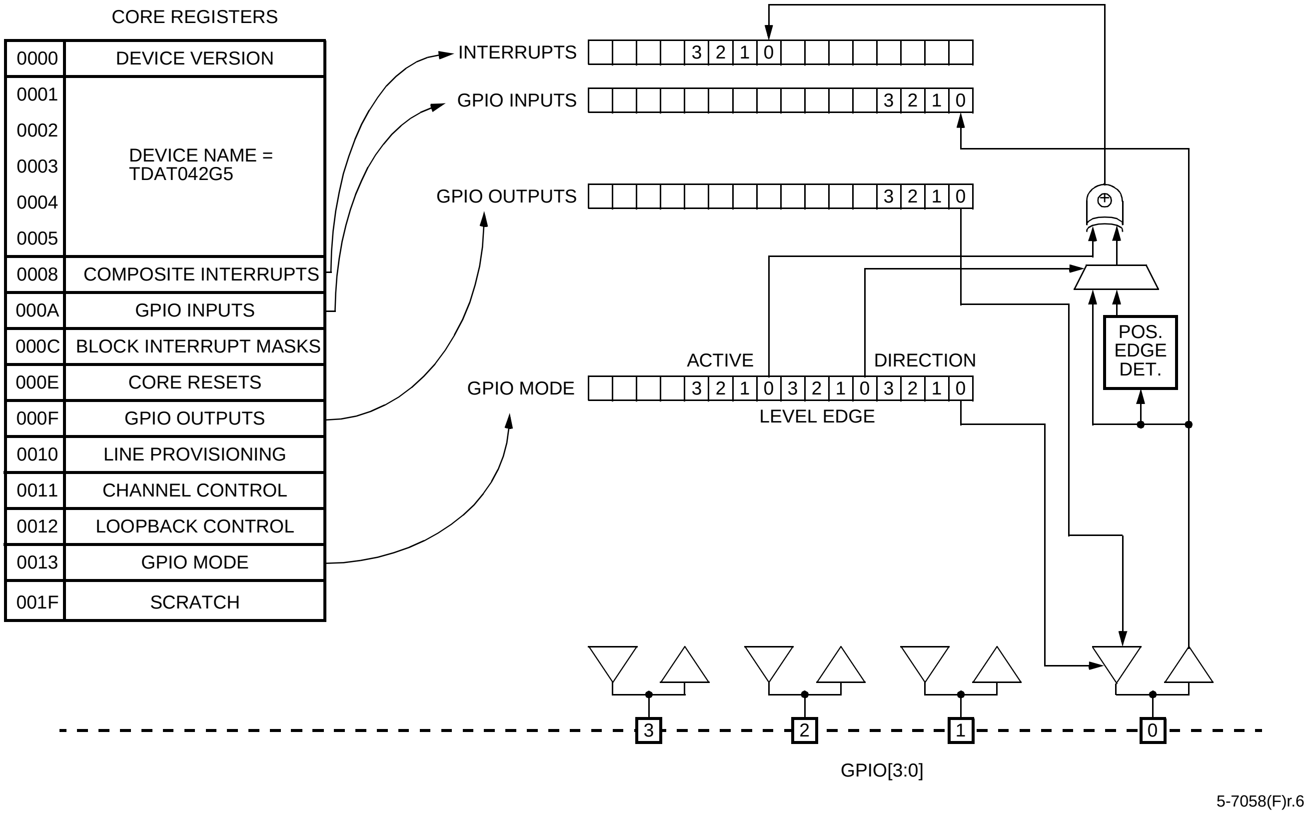


Figure 24. GPIO Functionality

If a GPIO pin is an input, the logic value on the pin can be read from a software register. The GPIO pin can also be programmed to generate a level-sensitive interrupt or a positive edge-triggered interrupt contributing to the external interrupt pin.

If a GPIO pin is an output, the value provisioned will appear on the device pin immediately.

Interface Description (continued)

Interrupts

Interrupt requests can be read from the composite interrupts register (0x0008; see register description, page 135). There is also a corresponding block interrupt masks register (0x000C; see register description, page 136). Any unmasked request will cause the INT pin to go low. GPIO interrupt functionality is shown in Figure 25.

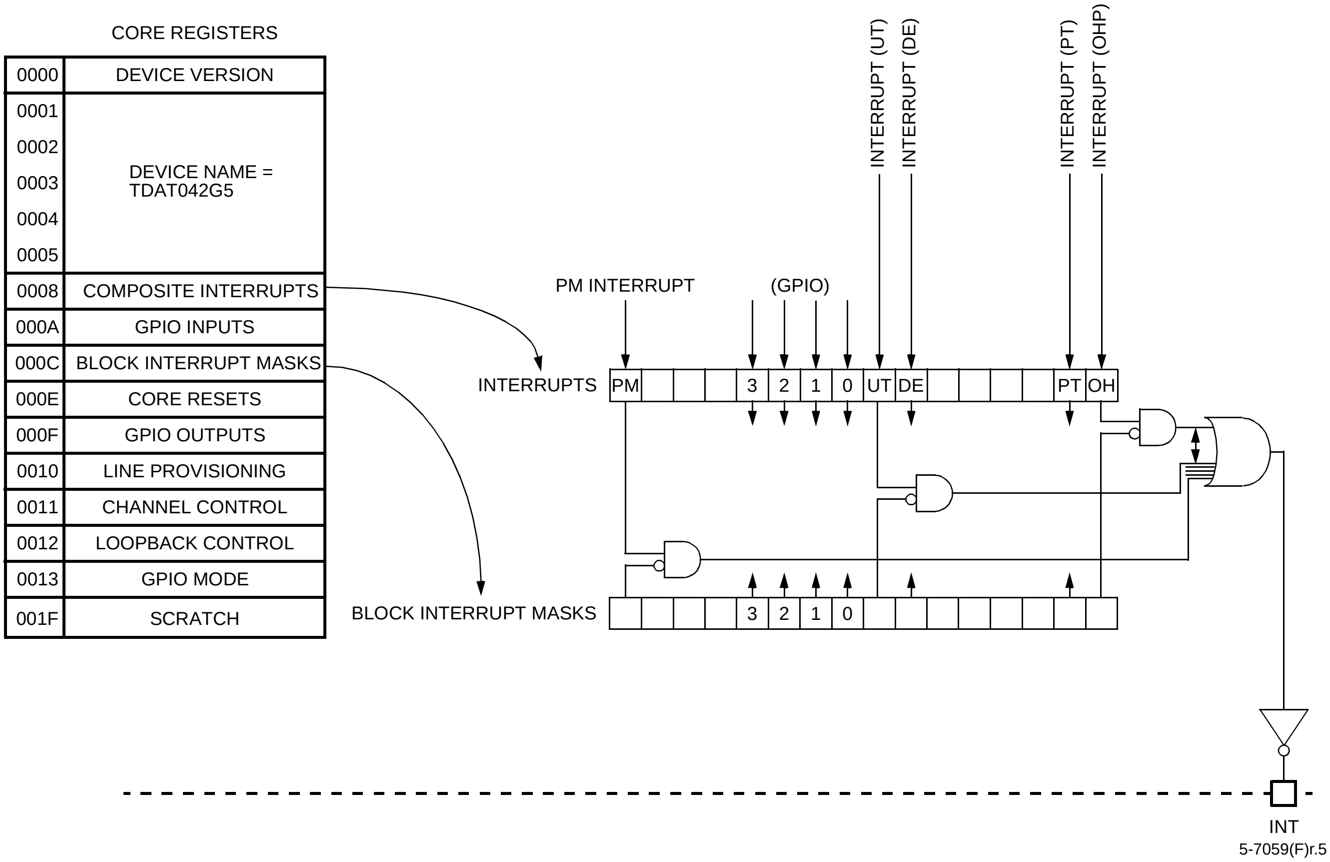


Figure 25. Interrupt Functionality

Interface Description (continued)

Reset (RST)

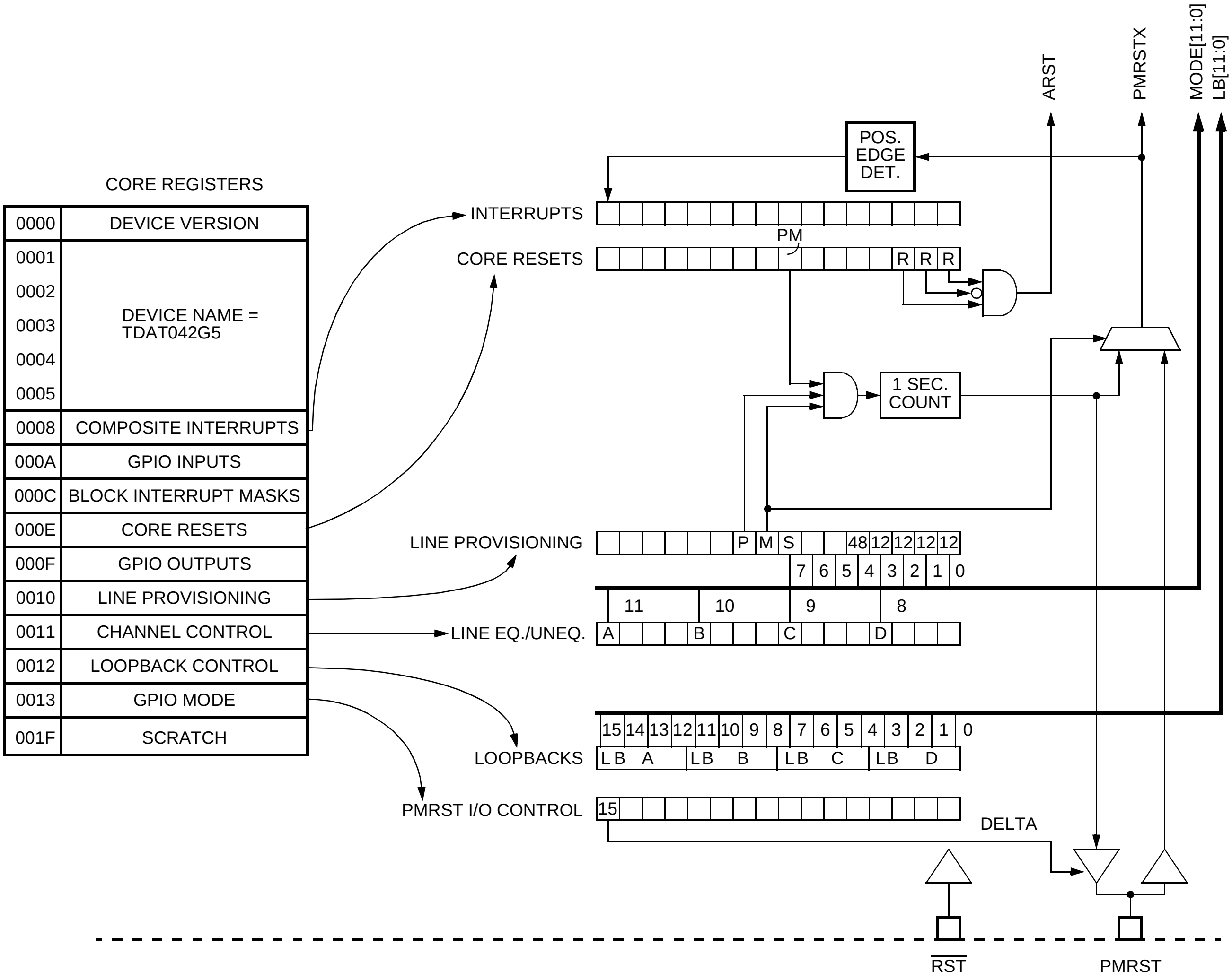
If RST is forced low, the software registers will be placed in their default powerup state. The device will lose its previous state and data path continuity will be lost. An internal 100 kΩ pull-up and a Schmitt-trigger input is provided for this pin. Reset can be generated from software by writing 0x0005 to the core resets register (0x000E; see register description on page 136).

Performance Monitor Reset (PMRST)

A 1 Hz clock (PMRST) is provided to all internal macrocells. This clock is used to control the 1-second binning of coding violations (CVs) and alarms. The source of this clock is selectable from one of the three following sources:

- The PMRST pin (D7)
- A software controllable register (0x000E; see register description on page 136)
- An internal 1-second counter (sourced from the 77.76 MHz transmit clock).

This is configured by the line provisioning register (address 0x0010). When under software control, writing 0x0080 to core resets register (address 0x000E) will generate a PMRSTX pulse.



5-7060(F)r.4

Figure 26. Miscellaneous Functionality

Interface Description (continued)

Performance Monitor Reset (PMRST) (continued)

Address 0x0010, bits 8 and 9 of the core register set defines the mode of operation for PMRST. Address 0x000E, bit 7 provides the software controllable reset function (see Register Maps section, page 98). When this bit is set to 1, the PMRST signal goes high. The register will automatically be reset to 0 and the PMRST signal will go low after 500 ms.

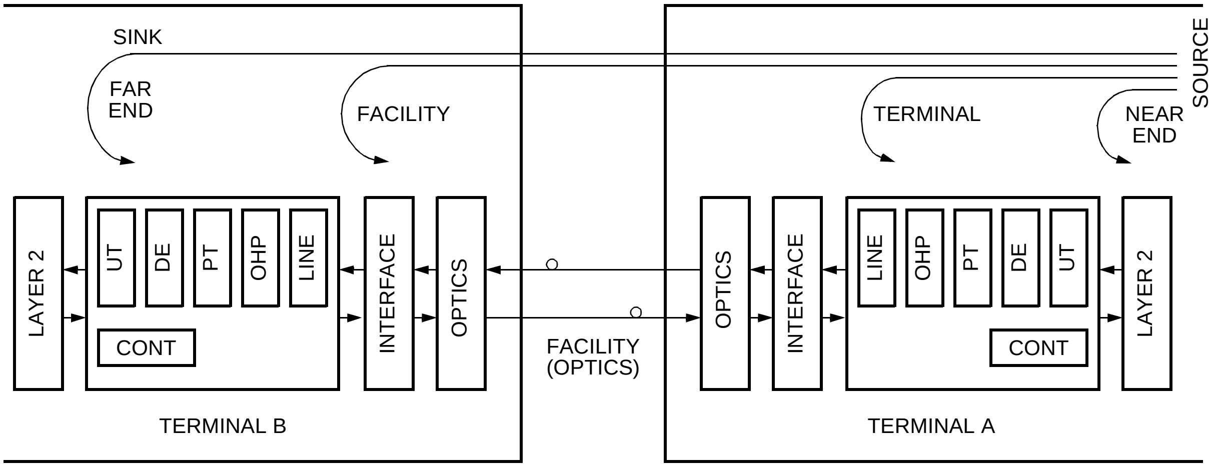
Table 26. PMRST Provisioning

Core Register ADDR 0x0010, Bits 9, 8	Description
00	PMRST comes from external pin (1 Hz, 50% duty cycle signal).
01	PMRST comes from internal 1-second counter (1 Hz, 50% duty cycle signal). Writing a logic 1 to the PMRST bit (Core register 0x000E, bit 7) in this mode will reset the counter so that a 0→1 transition occurs on the PMRST within 10 clock cycles of the 77.76 MHz clock.
11	PMRST is software controlled. Writing a logic 1 to the PMRST bit (core register 0x000E, bit 7) will cause a 0→1 transition on the internal PMRST signal. This pulse will be high for 100 cycles of the 77.76 MHz clock and low for 100 cycles of the 77.76 MHz clock. Writing the PMRST bit to a logic 1 during this 200 clock cycle interval will have no effect (2.57 µs). The PMRST rising edge must occur within 10 clock cycles of writing the PMRST bit.

Interface Description (continued)

Loopback Operation

Figure 27 illustrates the different types of loopback provided in the device. Loopback is controlled by core register 0x0012, loopback control (see register description on page 138).



5-7061(F)r.4

Figure 27. Loopback Operation

In the following description, only the data path from Terminal A to B is discussed, but the same terms apply to the reverse direction.

Near-End Loopback

The packet/cell payload is looped back to the data source (Layer 2 device) as soon as it crosses the Layer 1 to Layer 2 boundary (UTOPIA block).

Far-End Loopback

The packet/cell payload is looped back to the facility (optical) data source as soon as it enters the UTOPIA block of Terminal B. The data does not enter the Layer 2 device.

Terminal Loopback

The SONET/SDH signal is looped back at the terminal (line interface) block, and is returned to the Layer 2 device.

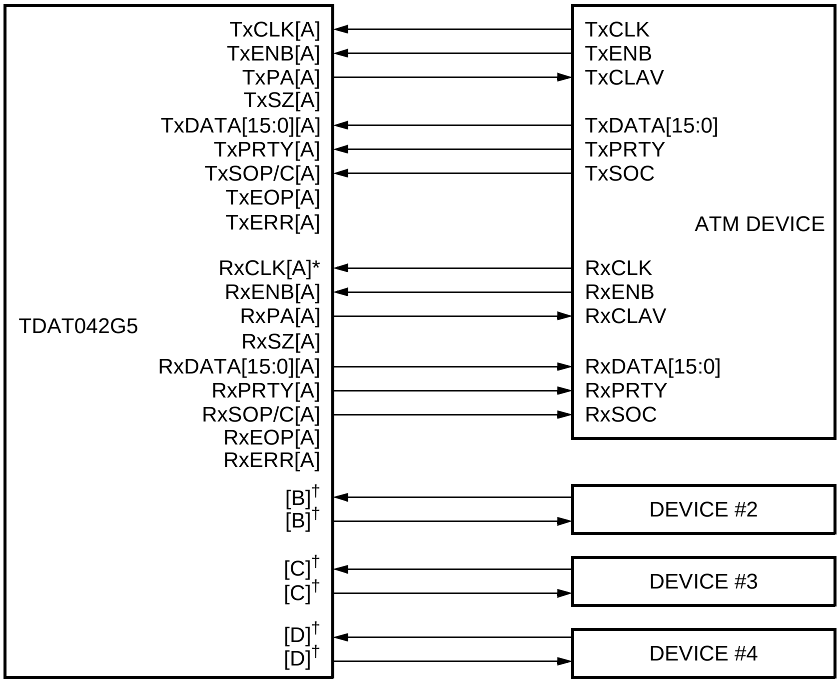
Facility Loopback

The facility (optical) data signal is looped back to the facility as soon as it enters the Terminal B line interface block.

Interface Description (continued)

System Interfaces

ATM Interfaces



5-6750(F)r.3

* RxCLK may be either sunk or sourced, depending upon the application.

† The transmit and receive signals for channels B, C, and D of the TDAT042G5 device are mapped to the remaining three ATM devices as shown above.

Figure 28. Quad ATM UTOPIA 2

For the quad ATM UTOPIA 3 eight-bit interface mode, where the ATM device has only an 8-bit interface, the RxDATA[15:0] and TxDATA[15:0] words are replaced with RxDATA[15:8] and TxDATA[15:8] in each channel of the TDAT042G5. This is shown in the following table.

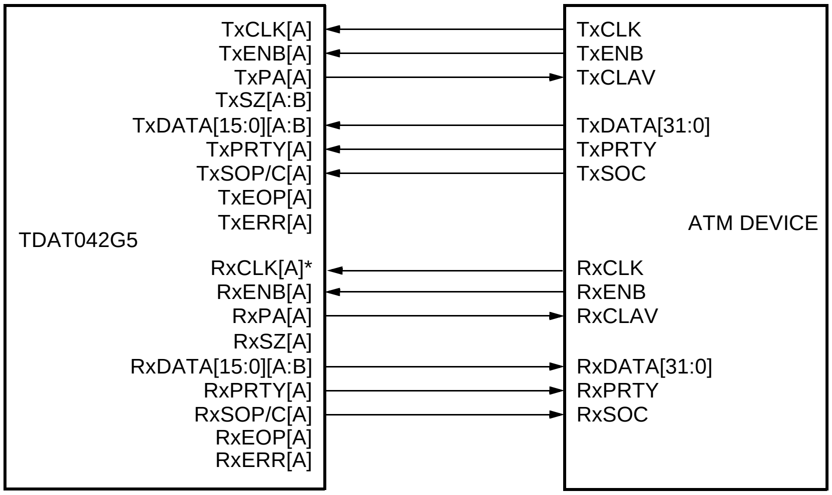
Table 27. Quad ATM UTOPIA 3 Interface

TDAT042G5 Channel	ATM Device
TxDATA[15:8][A] RxDATA[15:8][A]	TxDATA[7:0] RxDATA[7:0]
Same signals for channel [B]	Same signals for device #2
Same signals for channel [C]	Same signals for device #3
Same signals for channel [D]	Same signals for device #4

Interface Description (continued)

System Interfaces (continued)

ATM Interfaces (continued)



5-6740(F)r.5

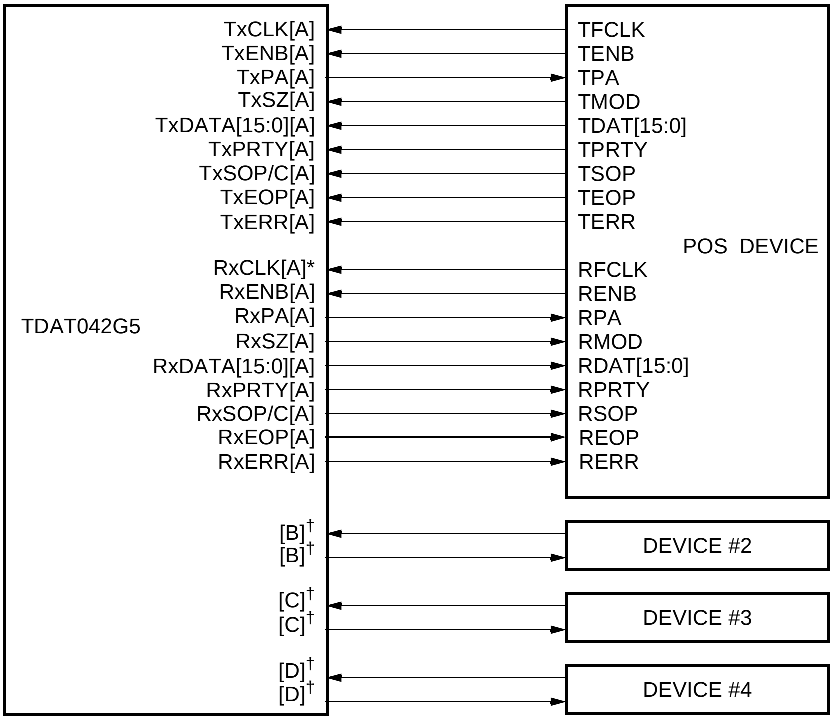
* RxCLK may be either sunk or sourced, depending upon the application.

Figure 29. Single ATM UTOPIA 3

Interface Description (continued)

System Interfaces (continued)

POS Interfaces



5-6741(F)r.7

* RxCLK may be either sunk or sourced, depending upon the application.

† The transmit and receive signals for channels B, C, and D of the TDAT042G5 device are mapped to the remaining three POS devices as shown above.

Figure 30. Quad POS UTOPIA 2

For the quad POS UTOPIA 3 eight-bit interface mode, where the POS device has only an 8-bit interface, the RxDATA and TxDATA words are replaced with RxDATA[15:8] and TxDATA[15:8] in each channel of the TDAT042G5. This is shown in the following table.

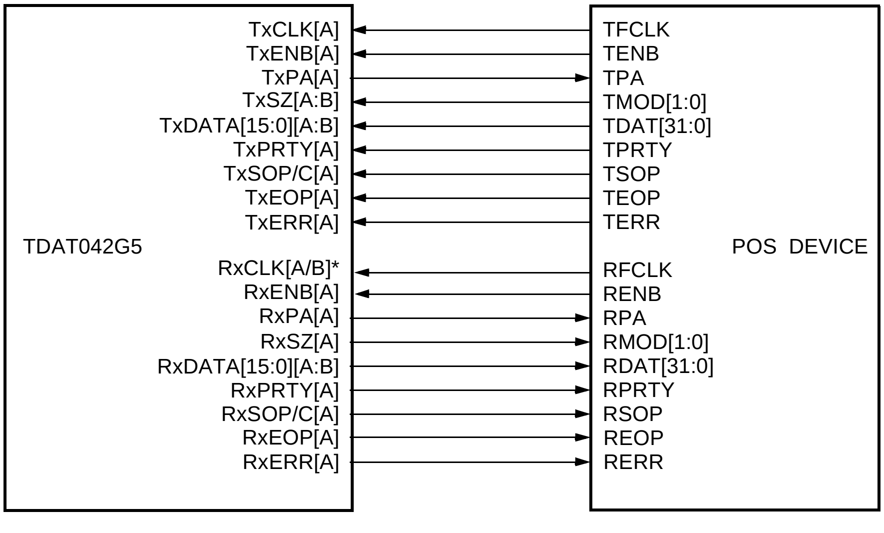
Table 28. Quad POS UTOPIA 3 Interface

TDAT042G5 Channel	POS Device
TxDATA[15:8][A] RxDATA[15:8][A]	TxDATA[7:0] RxDATA[7:0]
Same signals for channel [B]	Same signals for device #2
Same signals for channel [C]	Same signals for device #3
Same signals for channel [D]	Same signals for device #4

Interface Description (continued)

System Interfaces (continued)

POS Interfaces (continued)



* RxCLK may be either sunk or sourced, depending upon the application.

Figure 31. Single POS UTOPIA 3

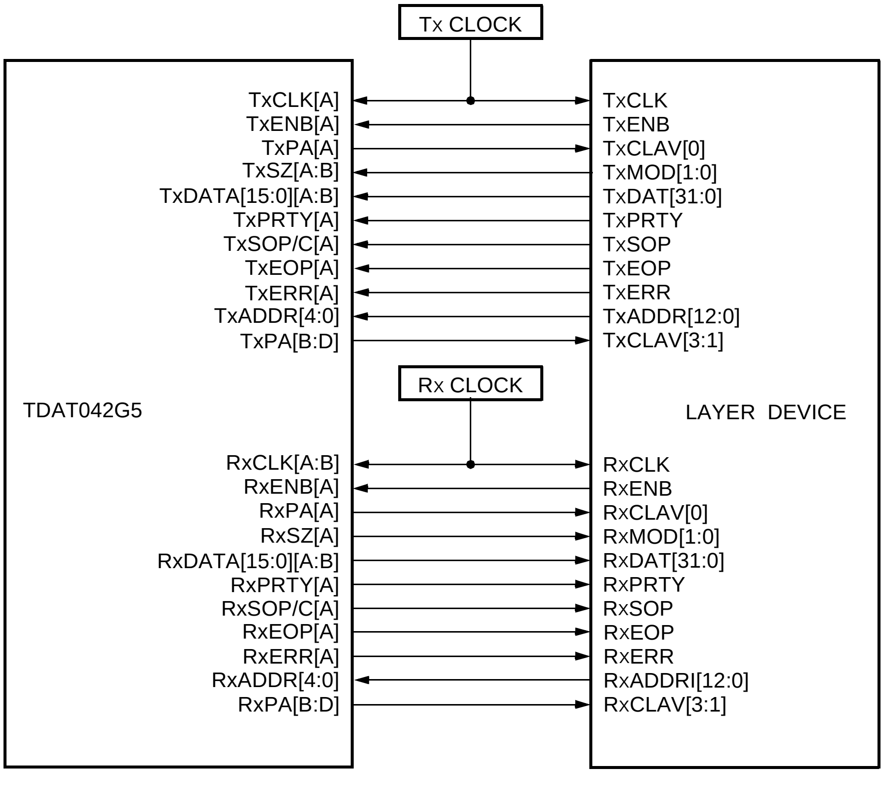


Figure 32. 32-bit MPHY UTOPIA 3

Register Access Description

Register address space is defined by the 16-bit address word of ADDR[15:0] (see pin description, page 36). Bits 15 through 13 must be 0. Bits 12 through 9 map to the major functional blocks as shown in Table 29. The usable address space is also shown in Table 29.

Table 29. Register Address Space

Functional Block	Address Range (Hex)
Core	0x0000—0x001F
UT	0x0200—0x0226
OHP	0x0400—0x05C2
PT	0x0800—0x0AF8
DE	0x1000—0x1607

Register addresses outside of the space defined in Table 29 must not be addressed, i.e., written or read.

Table 30—Table 34 is the register map. Details of the register functions are given in the following register description tables. Note that the usable register address space is not contiguous. Register addresses not specifically identified in the following tables are reserved and must not be addressed, i.e., written or read. Registers and bits that are reserved must not be written or must be written to the indicated default value. In Table 30—Table 34, the registers may be read only (RO), read/write (R/W), write only (WO), or clear-on-read or clear-on-write (COR/W).

The core registers must be written prior to provisioning any other registers (1) to establish the internal clock rates for the device, and (2) because writing to certain core registers resets the remainder of the device. Certain clocks must be present to read/write registers prior to provisioning the device.

Core register 0x0010 (mode) must be provisioned first, followed immediately by provisioning core register 0x0011 (channel (A—D) control). The remainder of the core registers must then be provisioned (order does not matter).

It is recommended, but not required, that the remainder of the device be provisioned in the following order: OHP, PT, and DE blocks (order does not matter); UT block to turn on the data source to the master and slave.

One of the following clocks must be present prior to provisioning to enable register access.

- TxCKP and TxCKN
- MPU clock (microprocessor interface synchronous mode only)

Register Maps

Core Registers

Table 30. Map of Core Registers

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Version Control																		
0000	RO	DEVICE_VERSION[7:0]								Reserved								0100
0001	RO	ASCII_NAME_TD																5444
0002	RO	ASCII_NAME_AT																4154
0003	RO	ASCII_NAME_04																3034
0004	RO	ASCII_NAME_2G																3247
0005	RO	ASCII_NAME_5CR																350D
0006—0007	—	Reserved																0000
Composite Interrupts																		
0008	RO or COR/W	PMRST (COR/W)	Reserved			GPIO[3:0]I (COR/W)				UTI (RO)	DEI (RO)	Reserved				PTI (RO)	OHPI (RO)	0000
General-Purpose Input																		
0009	—	Reserved																0000
000A	RO	Reserved												GPIO[3:0]_INPUT_VALUE				—
Block Interrupt Masks																		
000B	Reserved																	0000
000C	R/W	PMRSTM	Reserved			GPIO[3:0]IM				UTIM	DEIM	Reserved				PTIM	OHPIM	FFFF
Core Resets																		
000D	Reserved																	0000
000E	WO	Reserved								PMRST	Reserved				SWRST			—
General-Purpose Output																		
000F	R/W	Reserved												GPIO[3:0]_OUTPUT_VALUE				0000
Provisioning																		
0010	R/W	Reserved			POF_ POS	Reserved		PMMODE[1:0]		SDH/ SONET	COR/ COW	PLL_ MODE	STS48	STS12[A]	STS12[B]	STS12[C]	STS12[D]	1070
0011	R/W	EQ_CH_A	Reserved			EQ_CH_B	Reserved			EQ_CH_C	Reserved			EQ_CH_D	Reserved			0000
0012	R/W	LOOPBACKS[3:0]_CH_A				LOOPBACKS[3:0]_CH_B				Loopbacks[3:0]_CH_C				LOOPBACKS[3:0]_CH_D				0000
0013	R/W	PMRST_ IO_CTRL	Reserved			GPIO[3:0]_INTERRUPT_ACTIVE_H/L				GPIO[3:0]_INTERRUPT_LEVEL/EDGE				GPIO[3:0]_DIRECTION_I/O				0000
0014—001E	—	Reserved																0000
001F	R/W	CORE_SCRATCH[15:0]																0000

Register Maps (continued)

UT Registers

Table 31. Map of UT Registers

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
UT Version Control																		
0200	RO	Reserved								UT_VERSION[7:0]								0000
UT Interrupt																		
0201	RO	Reserved												UT_INT [D]	UT_INT [C]	UT_INT [B]	UT_INT [A]	0000
Delta & Event Parameters																		
Channel A																		
0202	COR/W	Reserved												FIFO_OVERFLOW TxA	FIFO_UNDERFLOW_TxA	FIFO_OVERFLOW RxA	PARITY_ERROR_TxA	0000
Channel B																		
0203	COR/W	Reserved												FIFO_OVERFLOW TxB	FIFO_UNDERFLOW_TxB	FIFO_OVERFLOW RxB	PARITY_ERROR_TxB	0000
Channel C																		
0204	COR/W	Reserved												FIFO_OVERFLOW TxC	FIFO_UNDERFLOW_TxC	FIFO_OVERFLOW RxC	PARITY_ERROR_TxC	0000
Channel D																		
0205	COR/W	Reserved												FIFO_OVERFLOW TxD	FIFO_UNDERFLOW_TxD	FIFO_OVERFLOW RxD	PARITY_ERROR_TxD	0000
Interrupt Mask Parameters																		
0206	R/W	Reserved												INTM[D]	INTM[C]	INTM[B]	INTM[A]	000F
Channel A																		
0207	R/W	Reserved												FIFO_OVERFLOW_Tx_MASK[A]	FIFO_UNDERFLOW_Tx_MASK[A]	FIFO_OVERFLOW_Rx_MASK[A]	PARITY_ERROR_Tx_MASK[A]	000F
Channel B																		
0208	R/W	Reserved												FIFO_OVERFLOW_Tx_MASK[B]	FIFO_UNDERFLOW_Tx_MASK[B]	FIFO_OVERFLOW_Rx_MASK[B]	PARITY_ERROR_Tx_MASK[B]	000F

Register Maps (continued)

UT Registers (continued)

Table 31. Map of UT Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Channel C																		
0209	R/W	Reserved												FIFO_OVER-FLOW_Tx_MASK[C]	FIFO_UNDER-FLOW_Tx_MASK[C]	FIFO_OVER-FLOW_Rx_MASK[C]	PARITY_ERROR_Tx_MASK[C]	000F
Channel D																		
020A	R/W	Reserved												FIFO_OVER-FLOW_Tx_MASK[D]	FIFO_UNDER-FLOW_Tx_MASK[D]	FIFO_OVER-FLOW_Rx_MASK[D]	PARITY_ERROR_Tx_MASK[D]	000F
Error Counters in PMRST Mode																		
Channel A																		
020B	RO	PMRST_PECTxA																0000
Channel B																		
020C	RO	PMRST_PECTxB																0000
Channel C																		
020D	RO	PMRST_PECTxC																0000
Channel D																		
020E	RO	PMRST_PECTxD																0000
UT Provisioning Registers																		
Channel A																		
020F	R/W	POLLING_ENB_RxA	Reserved		RxADDR_A[4:0]					Reserved	CLOCK_MODE_RxA	PARITY_RxA	ATM_SIZE_RxA	TRAFFIC_TYPE_RxA	UTOPIA_MODE_RxA[2:0]			0020
0210	R/W	POLLING_ENB_TxA	Reserved		TxADDR_A[4:0]					Reserved		PARITY_TxA	ATM_SIZE_TxA	TRAFFIC_TYPE_TxA	UTOPIA_MODE_TxA[2:0]			0000
0211	R/W	Reserved		INGRESS_WATERMARK_HIGH_A[6:0]						Reserved		INGRESS_WATERMARK_LOW_A[6:0]						361F
0212	R/W	Reserved		EGRESS_WATERMARK_HIGH_A[6:0]						Reserved		EGRESS_WATERMARK_LOW_A[6:0]						361F
Channel B																		
0213	R/W	POLLING_ENB_RxB	Reserved		RxADDR_B[4:0]					Reserved	CLOCK_MODE_RxB	PARITY_RxB	ATM_SIZE_RxB	TRAFFIC_TYPE_RxB	UTOPIA_MODE_RxB[2:0]			0120
0214	R/W	POLLING_ENB_TxB	Reserved		TxADDR_B[4:0]					Reserved		PARITY_TxB	ATM_SIZE_TxB	TRAFFIC_TYPE_TxB	UTOPIA_MODE_TxB[2:0]			0120
0215	R/W	Reserved		INGRESS_WATERMARK_HIGH_B[6:0]						Reserved		INGRESS_WATERMARK_LOW_B[6:0]						361F
0216	R/W	Reserved		EGRESS_WATERMARK_HIGH_B[6:0]						Reserved		EGRESS_WATERMARK_LOW_B[6:0]						361F

Register Maps (continued)

UT Registers (continued)

Table 31. Map of UT Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Channel C																		
0217	R/W	POLLING_ ENB_RxC	Reserved		RxADDR_C[4:0]					Reserved	CLOCK_ MODE_ RxC	PARITY_ RxC	ATM_ SIZE_ RxC	TRAFFIC _TYPE_ RxC	UTOPIA_MODE_RxC[2:0]			0220
0218	R/W	POLLING_ ENB_TxC	Reserved		TxADDR_C[4:0]					Reserved		PARITY_ TxC	ATM_ SIZE_ TxC	TRAFFIC _TYPE_ TxC	UTOPIA_MODE_TxC[2:0]			0220
0219	R/W	Reserved		INGRESS_WATERMARK_HIGH_C[6:0]						Reserved		INGRESS_WATERMARK_LOW_C[6:0]						361F
021A	R/W	Reserved		EGRESS_WATERMARK_HIGH_C[6:0]						Reserved		EGRESS_WATERMARK_LOW_C[6:0]						361F
Channel D																		
021B	R/W	POLLING_ ENB_RxD	Reserved		RxADDR_D[4:0]					Reserved	CLOCK_ MODE_ RxD	PARITY_ RxD	ATM_ SIZE_ RxD	TRAFFIC _TYPE_ RxD	UTOPIA_MODE_RxD[2:0]			0320
021C	R/W	POLLING_ ENB_TxD	Reserved		TxADDR_D[4:0]					Reserved		PARITY_ TxD	ATM_ SIZE_ TxD	TRAFFIC _TYPE_ TxD	UTOPIA_MODE_TxD[2:0]			0320
021D	R/W	Reserved		INGRESS_WATERMARK_HIGH_D[6:0]						Reserved		INGRESS_WATERMARK_LOW_D[6:0]						361F
021E	R/W	Reserved		EGRESS_WATERMARK_HIGH_D[6:0]						Reserved		EGRESS_WATERMARK_LOW_D[6:0]						361F
Reset Register																		
021F	R/W	Reserved								UT_Tx ARST_D	UT_Tx ARST_C	UT_Tx ARST_B	UT_Tx ARST_A	UT_Rx ARST_D	UT_Rx ARST_C	UT_Rx ARST_B	UT_Rx ARST_A	00FF
Error Counters																		
Channel A																		
0220	RO	PECTxA																0000
Channel B																		
0221	RO	PECTxB																0000
Channel C																		
0222	RO	PECTxC																0000
Channel D																		
0223	RO	PECTxD																0000
Scratch Register																		
0224	R/W	UT_SCRATCH[15:0]																0000
PA Response Register																		
0225	R/W	Reserved								TxPAD	TxPAC	TxPAB	TxPAA	RxPAD/ RxDATAD/ RxSOP/CD	RxPAC/ RxDATAC/ RxSOP/CC	RxPAB/ RxDATAB/ RxSOP/CB	RxPAA/ RxDATAA/ RxSOP/CA	0000

Register Maps (continued)

UT Registers (continued)

Table 31. Map of UT Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
Size Mode Register																		
0226	R/W	Reserved								TxSIZE_D	TxSIZE_C	TxSIZE_B	TxSIZE_A	RxSIZE_D	RxSIZE_C	RxSIZE_B	RxSIZE_A	0000

Register Maps (continued)

OHP Registers

Table 32. Map of OHP Registers

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
OHP Version Control																		
0400	RO	OHP_VERSION[15:0]																0000
OHP Interrupts																		
0401	RO	Reserved												OHP_INT[D]	OHP_INT[C]	OHP_INT[B]	OHP_INT[A]	0000
Delta & Event Parameters																		
0402	COR/W	LRDI-MOND[A]	LAIS-MOND[A]	RAPS-BABLEE[A]	S1DMON4D[A]	S1DMON8D[A]	K2DMOND[A]	K1K2DMOND[A]	F1DMOND[A]	TTOAC_PERRE[A]	S1BABBLEE[A]	SFD[A]	SDD[A]	OOFD[A]	LOFD[A]	LOSD[A]	LOCD[A]	0000
0403	COR/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	J0MISE[A]	0000
0404	COR/W	LRDI-MOND[B]	LAIS-MOND[B]	RAPS-BABLEE[B]	S1DMON4D[B]	S1DMON8D[B]	K2DMOND[B]	K1K2DMOND[B]	F1DMOND[B]	TTOAC_PERRE[B]	S1BABBLEE[B]	SFD[B]	SDD[B]	OOFD[B]	LOFD[B]	LOSD[B]	LOCD[B]	0000
0405	COR/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	J0MISE[B]	0000
0406	COR/W	LRDI-MOND[C]	LAIS-MOND[C]	RAPS-BABLEE[C]	S1DMON4D[C]	S1DMON8D[C]	K2DMOND[C]	K1K2DMOND[C]	F1DMOND[C]	TTOAC_PERRE[C]	S1BABBLEE[C]	SFD[C]	SDD[C]	OOFD[C]	LOFD[C]	LOSD[C]	LOCD[C]	0000
0407	COR/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	J0MISE[C]	0000
0408	COR/W	LRDI-MOND[D]	LAIS-MOND[D]	RAPS-BABLEE[D]	S1DMON4D[D]	S1DMON8D[D]	K2DMOND[D]	K1K2DMOND[D]	F1DMOND[D]	TTOAC_PERRE[D]	S1BABBLEE[D]	SFD[D]	SDD[D]	OOFD[D]	LOFD[D]	LOSD[D]	LOCD[D]	0000
0409	COR/W	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	J0MISE[D]	0000
Receive/Transmit State & Value Parameters																		
040A	RO	LRDI-MON[A]	LAIS-MON[A]	Reserved							TLRDI-INT[A]	SF[A]	SD[A]	OOF[A]	LOF[A]	LOS[A]	LOC[A]	000C
040B	RO	LRDI-MON[B]	LAIS-MON[B]	Reserved							TLRDI-INT[B]	SF[B]	SD[B]	OOF[B]	LOF[B]	LOS[B]	LOC[B]	000C
040C	RO	LRDI-MON[C]	LAIS-MON[C]	Reserved							TLRDI-INT[C]	SF[C]	SD[C]	OOF[C]	LOF[C]	LOS[C]	LOC[C]	000C
040D	RO	LRDI-MON[D]	LAIS-MON[D]	Reserved							TLRDI-INT[D]	SF[D]	SD[D]	OOF[D]	LOF[D]	LOS[D]	LOC[D]	000C
Interrupt Mask Parameters																		
040E	R/W	LRDI-MONM[A]	LAIS-MONM[A]	RAPS-BABLEM[A]	S1DMON4M[A]	S1DMON8M[A]	K2DMONM[A]	K1K2DMONM[A]	F1DMONM[A]	TTOAC_PERRM[A]	S1BABBLEM[A]	SFM[A]	SDM[A]	OOFM[A]	LOFM[A]	LOSM[A]	LOCM[A]	FFFF
040F	R/W	INTM[A]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	J0MISM[A]	8001

Register Maps (continued)

OHP Registers (continued)

Table 32. Map of OHP Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0410	R/W	LRDI-MONM[B]	LAIS-MONM[B]	RAPS-BABLEM [B]	S1DMON 4M[B]	S1DMON 8M[B]	K2DMON M[B]	K1K2DM ONM[B]	F1DMON M[B]	TTOAC_P ERRM [B]	S1BABB LEM[B]	SFM[B]	SDM[B]	OOFM[B]	LOFM[B]	LOSM[B]	LOCM[B]	FFFF
0411	R/W	INTM[B]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	J0MISM [B]	8001
0412	R/W	LRDI-MONM[C]	LAIS-MONM[C]	RAPS-BABLEM [C]	S1DMON 4M[C]	S1DMON 8M[C]	K2DMON M[C]	K1K2DM ONM[C]	F1DMON M[C]	TTOAC_P ERRM [C]	S1BABB LEM[C]	SFM[C]	SDM[C]	OOFM[C]	LOFM[C]	LOSM[C]	LOCM[C]	FFFF
0413	R/W	INTM[C]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	J0MISM [C]	8001
0414	R/W	LRDI-MONMD]	LAIS-MONM[D]	RAPS-BABLEM [D]	S1DMON 4M[D]	S1DMON 8M[D]	K2DMON M[D]	K1K2DM ONM[D]	F1DMON M[D]	TTOAC_P ERRM [D]	S1BABB LEM[D]	SFM[D]	SDM[D]	OOFM[D]	LOFM[D]	LOSM[D]	LOCM[D]	FFFF
0415	R/W	INTM[D]	0	0	0	0	0	0	0	0	0	0	0	0	0	0	J0MISM [D]	8001
Toggles																		
0416	R/W	Reserved											TA1A2ER REN[A]	SF CLEAR[A]	SFSET [A]	SD CLEAR[A]	SDSET [A]	—
0417	R/W	Reserved											TA1A2ER REN[B]	SF CLEAR[B]	SFSET [B]	SD CLEAR[B]	SDSET [B]	—
0418	R/W	Reserved											TA1A2ER REN[C]	SF CLEAR[C]	SFSET [C]	SD CLEAR[C]	SDSET [C]	—
0419	R/W	Reserved											TA1A2ER REN[D]	SF CLEAR[D]	SFSET [D]	SD CLEAR[D]	SDSET [D]	—
Continuous N Times Detect Values																		
041A	R/W	CNTDK2[A][3:0]				CNTDK1K2[A][3:0]				CNTDF1[A][3:0]				CNTDJ0Z0[A][3:0]				3333
041B	R/W	Reserved				CNTDS1FRAME[A][3:0]				CNTDS1[A][3:0]				CNTDK1K2FRAME[A][3:0]				053C
041C	R/W	CNTDK2[B][3:0]				CNTDK1K2[B][3:0]				CNTDF1[B][3:0]				CNTDJ0Z0[B][3:0]				3333
041D	R/W	Reserved				CNTDS1FRAME[B][3:0]				CNTDS1[B]3:0]				CNTDK1K2FRAME[B][3:0]				053C
041E	R/W	CNTDK2[C][3:0]				CNTDK1K2[C][3:0]				CNTDF1[C][3:0]				CNTDJ0Z0[C][3:0]				3333
041F	R/W	Reserved				CNTDS1FRAME[C][3:0]				CNTDS1[C]3:0]				CNTDK1K2FRAME[C][3:0]				053C
0420	R/W	CNTDK2[D][3:0]				CNTDK1K2[D][3:0]				CNTDF1[D][3:0]				CNTDJ0Z0[D][3:0]				3333
0421	R/W	Reserved				CNTDS1FRAME[D][3:0]				CNTDS1[D]3:0]				CNTDK1K2FRAME[D][3:0]				053C
Receive Control Parameters																		
0422	R/W	J0MONMODE[A] [1:0]		M1B7IGN ORE[A]	LAISINS [A]	LOF_AISI NH[A]	OOF_AIS INH[A]	LOS_AIS INH[A]	SFB1B2S EL[A]	SDB1B2 SEL[A]	CNTDB1 SEL[A]	S1MON8 _OR_4C TL[A]	K1K2_2 _OR_1 [A]	B2BITBL KCNT[A]	DSCRIN H[A]	B1BITBL KCNT[A]	ROH_BY PASS[A]	0000
0423	R/W	M1BITBLK CNT[A]	Reserved		LOSDETCNT[A][12:0]													0000

Register Maps (continued)

OHP Registers (continued)

Table 32. Map of OHP Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
0424	R/W	J0MONMODE[B][1:0]		M1B7IGNORE[B]	LAISINS[B]	LOF_AISINH[B]	OOF_AISINH[B]	LOS_AISINH[B]	SFB1B2SEL[B]	SDB1B2SEL[B]	CNTDB1SEL[B]	S1MON8_OR_4CTL[B]	K1K2_2_OR_1[B]	B2BITBLKCNT[B]	DSCRINH[B]	B1BITBLKCNT[B]	ROH_BYPASS[B]	0000
0425	R/W	M1BITBLKCNT[B]	Reserved		LOSDETCNT[B][12:0]													0000
0426	R/W	J0MONMODE[C][1:0]		M1B7IGNORE[C]	LAISINS[C]	LOF_AISINH[C]	OOF_AISINH[C]	LOS_AISINH[C]	SFB1B2SEL[C]	SDB1B2SEL[C]	CNTDB1SEL[C]	S1MON8_OR_4CTL[C]	K1K2_2_OR_1[C]	B2BITBLKCNT[C]	DSCRINH[C]	B1BITBLKCNT[C]	ROH_BYPASS[C]	0000
0427	R/W	M1BITBLKCNT[C]	Reserved		LOSDETCNT[C][12:0]													0000
0428	R/W	J0MONMODE[D][1:0]		M1B7IGNORE[D]	LAISINS[D]	LOF_AISINH[D]	OOF_AISINH[D]	LOS_AISINH[D]	SFB1B2SEL[D]	SDB1B2SEL[D]	CNTDB1SEL[D]	S1MON8_OR_4CTL[D]	K1K2_2_OR_1[D]	B2BITBLKCNT[D]	DSCRINH[D]	B1BITBLKCNT[D]	ROH_BYPASS[D]	0000
0429	R/W	M1BITBLKCNT[D]	Reserved		LOSDETCNT[D][12:0]													0000
042A	R/W	RREFSEL[1:0]		RREF_EN	Reserved									RTOAC-SINH[A]	RTOAC-CINH[A]	RTOACDINH[A]	RTOAC_OEPINS[A]	0000
042B	R/W	Reserved												RTOAC-SINH[B]	RTOAC-CINH[B]	RTOACDINH[B]	RTOAC_OEPINS[B]	0000
042C	R/W	Reserved												RTOAC-SINH[C]	RTOAC-CINH[C]	RTOACDINH[C]	RTOAC_OEPINS[C]	0000
042D	R/W	Reserved												RTOAC-SINH[D]	RTOAC-CINH[D]	RTOACDINH[D]	RTOAC_OEPINS[D]	0000
Transmit Control Parameters																		
042E	R/W	TTOACINH	TJ0INS[A]	TTOAC_J0[A]	TTOAC_OEPMON[A]	TTOAC_INS[A]	TTOAC_E2[A]	TTOAC_S1[A]	TTOAC_D4TO12[A]	TTOAC_D1TO3[A]	TTOAC_F1[A]	TTOAC_E1[A]	TAPS-BAB-BLEINS[A]	TM1_ERR_INS[A]	TM1_REIL_INH[A]	TF1INS[A]	TS1INS[A]	0003
042F	R/W	TA1A2ERRINS[A][4:0]					TOH_BYPASS[A]	SCRINH[A]	TB1ERRINS[A]	TB2ERRINS[A]	TIMER_LRDIINH[A]	TSF_LRDIINH[A]	TLAISMON_LRDIINH[A]	TLOF_LRDIINH[A]	TOOF_LRDIINH[A]	TLOS_LRDIINH[A]	TLOC_LRDIINH[A]	0000
0430	R/W	Reserved	TJ0INS[B]	TTOAC_J0[B]	TTOAC_OEPMON[B]	TTOAC_INS[B]	TTOAC_E2[B]	TTOAC_S1[B]	TTOAC_D4TO12[B]	TTOAC_D1TO3[B]	TTOAC_F1[B]	TTOAC_E1[B]	TAPS-BAB-BLEINS[B]	TM1_ERR_INS[B]	TM1_REIL_INH[B]	TF1INS[B]	TS1INS[B]	0003

Register Maps (continued)

OHP Registers (continued)

Table 32. Map of OHP Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0431	R/W	TA1A2ERRINS[B][4:0]					TOH_BYPASS[B]	SCRINH[B]	TB1ERRINS[B]	TB2ERRINS[B]	TIMER_LRDIINH[B]	TSF_LRDIINH[B]	TLAISMON_LRDIINH[B]	TLOF_LRDIINH[B]	TOOF_LRDIINH[B]	TLOS_LRDIINH[B]	TLOC_LRDIINH[B]	0000
0432	R/W	Reserved	TJ0INS[C]	TTOAC_J0[C]	TTOAC_OEPMON[C]	TTOAC_INS[C]	TTOAC_E2[C]	TTOAC_S1[C]	TTOAC_D4TO12[C]	TTOAC_D1TO3[C]	TTOAC_F1[C]	TTOAC_E1[C]	TAPSBABBLEINS[C]	TM1_ERR_INS[C]	TM1_REIL_INH[C]	TF1INS[C]	TS1INS[C]	0003
0433	R/W	TA1A2ERRINS[C][4:0]					TOH_BYPASS[C]	SCRINH[C]	TB1ERRINS[C]	TB2ERRINS[C]	TIMER_LRDIINH[C]	TSF_LRDIINH[C]	TLAISMON_LRDIINH[C]	TLOF_LRDIINH[C]	TOOF_LRDIINH[C]	TLOS_LRDIINH[C]	TLOC_LRDIINH[C]	0000
0434	R/W	Reserved	TJ0INS[D]	TTOAC_J0[D]	TTOAC_OEPMON[D]	TTOAC_INS[D]	TTOAC_E2[D]	TTOAC_S1[D]	TTOAC_D4TO12[D]	TTOAC_D1TO3[D]	TTOAC_F1[D]	TTOAC_E1[D]	TAPSBABBLEINS[D]	TM1_ERR_INS[D]	TM1_REIL_INH[D]	TF1INS[D]	TS1INS[D]	0003
0435	R/W	TA1A2ERRINS[D][4:0]					TOH_BYPASS[D]	SCRINH[D]	TB1ERRINS[D]	TB2ERRINS[D]	TIMER_LRDIINH[D]	TSF_LRDIINH[D]	TLAISMON_LRDIINH[D]	TLOF_LRDIINH[D]	TOOF_LRDIINH[D]	TLOS_LRDIINH[D]	TLOC_LRDIINH[D]	0000
0436	R/W	TAPSINS[A]	TK2SINS[A]	Reserved		TAISLINS[A][11:0]												C000
0437	R/W	TAPSINS[B]	TK2SINS[B]	Reserved		TAISLINS[B][11:0]												C000
0438	R/W	TAPSINS[C]	TK2SINS[C]	Reserved		TAISLINS[C][11:0]												C000
0439	R/W	TAPSINS[D]	TK2SINS[D]	Reserved		TAISLINS[D][11:0]												C000
Signal Degrade Set/Clear Control Registers																		
043A	R/W	SDNSSET[A][18:3]																0000
043B	R/W	Reserved	SDMSET[A][7:0]								SDLSET[A][3:0]				SDNSSET[A][2:0]			0000
043C	R/W	SDNSSET[B][18:3]																0000
043D	R/W	Reserved	SDMSET[B][7:0]								SDLSET[B][3:0]				SDNSSET[B][2:0]			0000
043E	R/W	SDNSSET[C][18:3]																0000
043F	R/W	Reserved	SDMSET[C][7:0]								SDLSET[C][3:0]				SDNSSET[C][2:0]			0000
0440	R/W	SDNSSET[D][18:3]																0000
0441	R/W	Reserved	SDMSET[D][7:0]								SDLSET[D][3:0]				SDNSSET[D][2:0]			0000
0442	R/W	SDBSET[A][15:0]																0000
0443	R/W	SDBSET[B][15:0]																0000
0444	R/W	SDBSET[C][15:0]																0000

Register Maps (continued)

OHP Registers (continued)

Table 32. Map of OHP Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0445	R/W	SDBSET[D][15:0]																0000
0446	R/W	SDNSCLEAR[A][18:3]																0000
0447	R/W	Reserved	SDMCLEAR[A][7:0]								SDLCLEAR[A][3:0]				SDNSCLEAR[A][2:0]			0000
0448	R/W	SDNSCLEAR[B][18:3]																0000
0449	R/W	Reserved	SDMCLEAR[B][7:0]								SDLCLEAR[B][3:0]				SDNSCLEAR[B][2:0]			0000
044A	R/W	SDNSCLEAR[C][18:3]																0000
044B	R/W	Reserved	SDMCLEAR[C][7:0]								SDLCLEAR[C][3:0]				SDNSCLEAR[C][2:0]			0000
044C	R/W	SDNSCLEAR[D][18:3]																0000
044D	R/W	Reserved	SDMCLEAR[D][7:0]								SDLCLEAR[D][3:0]				SDNSCLEAR[D][2:0]			0000
044E	R/W	SDBCLEAR[A][15:0]																0000
044F	R/W	SDBCLEAR[B][15:0]																0000
0450	R/W	SDBCLEAR[C][15:0]																0000
0451	R/W	SDBCLEAR[D][15:0]																0000
Signal Fail Set/Clear Control Registers																		
0452	R/W	SFNSSET[A][18:3]																0000
0453	R/W	Reserved	SFMSET[A][7:0]								SFLSET[A][3:0]				SFNSSET[A][2:0]			0000
0454	R/W	SFNSSET[B][18:3]																0000
0455	R/W	Reserved	SFMSET[B][7:0]								SFLSET[B][3:0]				SFNSSET[B][2:0]			0000
0456	R/W	SFNSSET[C][18:3]																0000
0457	R/W	Reserved	SFMSET[C][7:0]								SFLSET[C][3:0]				SFNSSET[C][2:0]			0000
0458	R/W	SFNSSET[D][18:3]																0000
0459	R/W	Reserved	SFMSET[D][7:0]								SFLSET[D][3:0]				SFNSSET[D][2:0]			0000
045A	R/W	SFBSET[A][15:0]																0000
045B	R/W	SFBSET[B][15:0]																0000
045C	R/W	SFBSET[C][15:0]																0000
045D	R/W	SFBSET[D][15:0]																0000
045E	R/W	SFNSCLEAR[A][18:3]																0000
045F	R/W	Reserved	SFMCLEAR[A][7:0]								SFLCLEAR[A][3:0]				SFNSCLEAR[A][2:0]			0000
0460	R/W	SFNSCLEAR[B][18:3]																0000
0461	R/W	Reserved	SFMCLEAR[B][7:0]								SFLCLEAR[B][3:0]				SFNSCLEAR[B][2:0]			0000
0462	R/W	SFNSCLEAR[C][18:3]																0000
0463	R/W	Reserved	SFMCLEAR[C][7:0]								SFLCLEAR[C][3:0]				SFNSCLEAR[C][2:0]			0000
0464	R/W	SFNSCLEAR[D][18:3]																0000
0465	R/W	Reserved	SFMCLEAR[D][7:0]								SFLCLEAR[D][3:0]				SFNSCLEAR[D][2:0]			0000

Register Maps (continued)

OHP Registers (continued)

Table 32. Map of OHP Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0466	R/W	SFBCLEAR[A][15:0]																0000
0467	R/W	SFBCLEAR[B][15:0]																0000
0468	R/W	SFBCLEAR[C][15:0]																0000
0469	R/W	SFBCLEAR[D][15:0]																0000
B1, B2, and M1 Error Counts																		
046A	RO	B1ECNT[A][15:0]																0000
046B	RO	B1ECNT[B][15:0]																0000
046C	RO	B1ECNT[C][15:0]																0000
046D	RO	B1ECNT[D][15:0]																0000
046E	RO	Reserved										B2ECNT[A][21:16]						0000
046F	RO	B2ECNT[A][15:0]																0000
0470	RO	Reserved										B2ECNT[B][21:16]						0000
0471	RO	B2ECNT[B][15:0]																0000
0472	RO	Reserved										B2ECNT[C][21:16]						0000
0473	RO	B2ECNT[C][15:0]																0000
0474	RO	Reserved										B2ECNT[D][21:16]						0000
0475	RO	B2ECNT[D][15:0]																0000
0476	RO	Reserved											M1ECNT[A][20:16]					0000
0477	RO	M1ECNT[A][15:0]																0000
0478	RO	Reserved											M1ECNT[B][20:16]					0000
0479	RO	M1ECNT[B][15:0]																0000
047A	RO	Reserved											M1ECNT[C][20:16]					0000
047B	RO	M1ECNT[C][15:0]																0000
047C	RO	Reserved											M1ECNT[D][20:16]					0000
047D	RO	M1ECNT[D][15:0]																0000
Transmit F1, S1, K2, K1 OH Insert Value																		
047E	R/W	TF1DINS[A][7:0]								TS1DINS[A][7:0]								0000
047F	R/W	TK2DINS[A][7:0]								TK1DINS[A][7:0]								0000
0480	R/W	TF1DINS[B][7:0]								TS1DINS[B][7:0]								0000
0481	R/W	TK2DINS[B][7:0]								TK1DINS[B][7:0]								0000
0482	R/W	TF1DINS[C][7:0]								TS1DINS[C][7:0]								0000
0483	R/W	TK2DINS[C][7:0]								TK1DINS[C][7:0]								0000
0484	R/W	TF1DINS[D][7:0]								TS1DINS[D][7:0]								0000
0485	R/W	TK2DINS[D][7:0]								TK1DINS[D][7:0]								0000

Register Maps (continued)

OHP Registers (continued)

Table 32. Map of OHP Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
Receive F1, S1, K2, K1 Monitor Value																		
0486	RO	F1DMON1[A][7:0]								F1DMON0[A][7:0]								0000
0487	RO	K2DMON[A][7:0]								K1DMON[A][7:0]								0000
0488	RO	Reserved								S1DMON[A][7:0]								0000
0489	RO	F1DMON1[B][7:0]								F1DMON0[B][7:0]								0000
048A	RO	K2DMON[B][7:0]								K1DMON[B][7:0]								0000
048B	RO	Reserved								S1DMON[B][7:0]								0000
048C	RO	F1DMON1[C][7:0]								F1DMON0[C][7:0]								0000
048D	RO	K2DMON[C][7:0]								K1DMON[C][7:0]								0000
048E	RO	Reserved								S1DMON[C][7:0]								0000
048F	RO	F1DMON1[D][7:0]								F1DMON0[D][7:0]								0000
0490	RO	K2DMON[D][7:0]								K1DMON[D][7:0]								0000
0491	RO	Reserved								S1DMON[D][7:0]								0000
Receive J0 Monitor Value																		
0492	RO	RJ0DMON[A][2][7:0]								RJ0DMON[A][1][7:0]								0000
0493	RO	RJ0DMON[A][4][7:0]								RJ0DMON[A][3][7:0]								0000
0494	RO	RJ0DMON[A][6][7:0]								RJ0DMON[A][5][7:0]								0000
0495	RO	RJ0DMON[A][8][7:0]								RJ0DMON[A][7][7:0]								0000
0496	RO	RJ0DMON[A][10][7:0]								RJ0DMON[A][9][7:0]								0000
0497	RO	RJ0DMON[A][12][7:0]								RJ0DMON[A][11][7:0]								0000
0498	RO	RJ0DMON[A][14][7:0]								RJ0DMON[A][13][7:0]								0000
0499	RO	RJ0DMON[A][16][7:0]								RJ0DMON[A][15][7:0]								0000
049A—04B1	—	Reserved																0000
04B2	RO	RJ0DMON[B][2][7:0]								RJ0DMON[B][1][7:0]								0000
04B3	RO	RJ0DMON[B][4][7:0]								RJ0DMON[B][3][7:0]								0000
04B4	RO	RJ0DMON[B][6][7:0]								RJ0DMON[B][5][7:0]								0000
04B5	RO	RJ0DMON[B][8][7:0]								RJ0DMON[B][7][7:0]								0000
04B6	RO	RJ0DMON[B][10][7:0]								RJ0DMON[B][9][7:0]								0000
04B7	RO	RJ0DMON[B][12][7:0]								RJ0DMON[B][11][7:0]								0000
04B8	RO	RJ0DMON[B][14][7:0]								RJ0DMON[B][13][7:0]								0000
04B9	RO	RJ0DMON[B][16][7:0]								RJ0DMON[B][15][7:0]								0000
04BA—04D1	—	Reserved																0000

Register Maps (continued)

OHP Registers (continued)

Table 32. Map of OHP Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
04D2	RO	RJ0DMON[C][2][7:0]								RJ0DMON[C][1][7:0]								0000
04D3	RO	RJ0DMON[C][4][7:0]								RJ0DMON[C][3][7:0]								0000
04D4	RO	RJ0DMON[C][6][7:0]								RJ0DMON[C][5][7:0]								0000
04D5	RO	RJ0DMON[C][8][7:0]								RJ0DMON[C][7][7:0]								0000
04D6	RO	RJ0DMON[C][10][7:0]								RJ0DMON[C][9][7:0]								0000
04D7	RO	RJ0DMON[C][12][7:0]								RJ0DMON[C][11][7:0]								0000
04D8	RO	RJ0DMON[C][14][7:0]								RJ0DMON[C][13][7:0]								0000
04D9	RO	RJ0DMON[C]16[7:0]								RJ0DMON[C][15][7:0]								0000
04DA—04F1	—	Reserved																0000
04F2	RO	RJ0DMON[D][2][7:0]								RJ0DMON[D][1][7:0]								0000
04F3	RO	RJ0DMON[D][4][7:0]								RJ0DMON[D][3][7:0]								0000
04F4	RO	RJ0DMON[D][6][7:0]								RJ0DMON[D][5][7:0]								0000
04F5	RO	RJ0DMON[D][8][7:0]								RJ0DMON[D][7][7:0]								0000
04F6	RO	RJ0DMON[D][10][7:0]								RJ0DMON[D][9][7:0]								0000
04F7	RO	RJ0DMON[D][12][7:0]								RJ0DMON[D][11][7:0]								0000
04F8	RO	RJ0DMON[D][14][7:0]								RJ0DMON[D][13][7:0]								0000
04F9	RO	RJ0DMON[D]16[7:0]								RJ0DMON[D][15][7:0]								0000
04FA—0511	—	Reserved																0000
J0 Byte Transmit Insert (16 Bytes)																		
0512	R/W	TJ0DINS[A][2][7:0]								TJ0DINS[A][1][7:0]								0000
0513	R/W	TJ0DINS[A][4][7:0]								TJ0DINS[A][3][7:0]								0000
0514	R/W	TJ0DINS[A][6][7:0]								TJ0DINS[A][5][7:0]								0000
0515	R/W	TJ0DINS[A][8][7:0]								TJ0DINS[A][7][7:0]								0000
0516	R/W	TJ0DINS[A][10][7:0]								TJ0DINS[A][9][7:0]								0000
0517	R/W	TJ0DINS[A][12][7:0]								TJ0DINS[A][11][7:0]								0000
0518	R/W	TJ0DINS[A][14][7:0]								TJ0DINS[A][13][7:0]								0000
0519	R/W	TJ0DINS[A][16][7:0]								TJ0DINS[A][15][7:0]								0000
051A—0531	—	Reserved																0000
0532	R/W	TJ0DINS[B][2][7:0]								TJ0DINS[B][1][7:0]								0000
0533	R/W	TJ0DINS[B][4][7:0]								TJ0DINS[B][3][7:0]								0000
0534	R/W	TJ0DINS[B][6][7:0]								TJ0DINS[B][5][7:0]								0000

Register Maps (continued)

OHP Registers (continued)

Table 32. Map of OHP Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0535	R/W	TJ0DINS[B][8][7:0]								TJ0DINS[B][7][7:0]								0000
0536	R/W	TJ0DINS[B][10][7:0]								TJ0DINS[B][9][7:0]								0000
0537	R/W	TJ0DINS[B][12][7:0]								TJ0DINS[B][11][7:0]								0000
0538	R/W	TJ0DINS[B][14][7:0]								TJ0DINS[B][13][7:0]								0000
0539	R/W	TJ0DINS[B][16][7:0]								TJ0DINS[B][15][7:0]								0000
053A—0551	—	Reserved																0000
0552	R/W	TJ0DINS[C][2][7:0]								TJ0DINS[C][1][7:0]								0000
0553	R/W	TJ0DINS[C][4][7:0]								TJ0DINS[C][3][7:0]								0000
0554	R/W	TJ0DINS[C][6][7:0]								TJ0DINS[C][5][7:0]								0000
0555	R/W	TJ0DINS[C][8][7:0]								TJ0DINS[C][7][7:0]								0000
0556	R/W	TJ0DINS[C][10][7:0]								TJ0DINS[C][9][7:0]								0000
0557	R/W	TJ0DINS[C][12][7:0]								TJ0DINS[C][11][7:0]								0000
0558	R/W	TJ0DINS[C][14][7:0]								TJ0DINS[C][13][7:0]								0000
0559	R/W	TJ0DINS[C][16][7:0]								TJ0DINS[C][15][7:0]								0000
055A—0571	—	Reserved																0000
0572	R/W	TJ0DINS[D][2][7:0]								TJ0DINS[D][1][7:0]								0000
0573	R/W	TJ0DINS[D][4][7:0]								TJ0DINS[D][3][7:0]								0000
0574	R/W	TJ0DINS[D][6][7:0]								TJ0DINS[D][5][7:0]								0000
0575	R/W	TJ0DINS[D][8][7:0]								TJ0DINS[D][7][7:0]								0000
0576	R/W	TJ0DINS[D][10][7:0]								TJ0DINS[D][9][7:0]								0000
0577	R/W	TJ0DINS[D][12][7:0]								TJ0DINS[D][11][7:0]								0000
0578	R/W	TJ0DINS[D][14][7:0]								TJ0DINS[D][13][7:0]								0000
0579	R/W	TJ0DINS[D][16][7:0]								TJ0DINS[D][15][7:0]								0000
057A—05A9	—	Reserved																0000
Z0 Byte Transmit Insert																		
05AA	R/W	TZ0DINS[A][2][7:0]								TZ0DINS[A][1][7:0]								0000
05AB	R/W	TZ0DINS[A][4][7:0]								TZ0DINS[A][3][7:0]								0000
05AC	R/W	TZ0DINS[A][6][7:0]								TZ0DINS[A][5][7:0]								0000
05AD	R/W	TZ0DINS[A][8][7:0]								TZ0DINS[A][7][7:0]								0000
05AE	R/W	TZ0DINS[A][10][7:0]								TZ0DINS[A][9][7:0]								0000
05AF	R/W	TZ0DINS[A][12][7:0]								TZ0DINS[A][11][7:0]								0000

Register Maps (continued)

OHP Registers (continued)

Table 32. Map of OHP Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
05B0	R/W	TZ0DINS[B][2][7:0]								TZ0DINS[B][1][7:0]								0000
05B1	R/W	TZ0DINS[B][4][7:0]								TZ0DINS[B][3][7:0]								0000
05B2	R/W	TZ0DINS[B][6][7:0]								TZ0DINS[B][5][7:0]								0000
05B3	R/W	TZ0DINS[B][8][7:0]								TZ0DINS[B][7][7:0]								0000
05B4	R/W	TZ0DINS[B][10][7:0]								TZ0DINS[B][9][7:0]								0000
05B5	R/W	TZ0DINS[B][12][7:0]								TZ0DINS[B][11][7:0]								0000
05B6	R/W	TZ0DINS[C][2][7:0]								TZ0DINS[C][1][7:0]								0000
05B7	R/W	TZ0DINS[C][4][7:0]								TZ0DINS[C][3][7:0]								0000
05B8	R/W	TZ0DINS[C][6][7:0]								TZ0DINS[C][5][7:0]								0000
05B9	R/W	TZ0DINS[C][8][7:0]								TZ0DINS[C][7][7:0]								0000
05BA	R/W	TZ0DINS[C][10][7:0]								TZ0DINS[C][9][7:0]								0000
05BB	R/W	TZ0DINS[C][12][7:0]								TZ0DINS[C][11][7:0]								0000
05BC	R/W	TZ0DINS[D][2][7:0]								TJ0DINS[D][1][7:0]								0000
05BD	R/W	TZ0DINS[D][4][7:0]								TZ0DINS[D][3][7:0]								0000
05BE	R/W	TZ0DINS[D][6][7:0]								TZ0DINS[D][5][7:0]								0000
05BF	R/W	TZ0DINS[D][8][7:0]								TZ0DINS[D][7][7:0]								0000
05C0	R/W	TZ0DINS[D][10][7:0]								TZ0DINS[D][9][7:0]								0000
05C1	R/W	TZ0DINS[D][12][7:0]								TZ0DINS[D][11][7:0]								0000
OHP Scratch Register																		
05C2	R/W	OHP_SCRATCH[15:0]																0000

Register Maps (continued)

PT Registers

Table 33. Map of Path Terminator Registers

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
PT Version Control																		
0800	RO	Reserved								PT_VERSION[7:0]								0000
PT Interrupt																		
0801	RO	Reserved												PT_INT[D]	PT_INT[C]	PT_INT[B]	PT_INT[A]	0000
PT Delta & Event Parameters																		
Port A																		
0802	COR/W	RJ1DMONMIS[A]E	Reserved			RPIHD[A][1—12]												0000
0803	COR/W	TRDIPD [A]	Reserved				RZ5DMOND[A]	RZ4DMOND[A]	RZ3DMOND[A]	RH4DMOND[A]	RF2DMOND[A]	RRDIPDMOND[A]	RC2DMOND[A]	RUC2D [A]	RPPLMD [A]	RSDD[A]	RSFD[A]	0000
0804—080E	—	Reserved																0000
Port B																		
080F	COR/W	RJ1DMONMIS[B]E	Reserved			RPIHD[B][1—12]												0000
0810	COR/W	TRDIPD [B]	Reserved				RZ5DMOND[B]	RZ4DMOND[B]	RZ3DMOND[B]	RH4DMOND[B]	RF2DMOND[B]	RRDIPDMOND[B]	RC2DMOND[B]	RUC2D [B]	RPPLMD [B]	RSDD[B]	RSFD[B]	0000
0811—081B	—	Reserved																0000
Port C																		
081C	COR/W	RJ1DMONMIS[C]E	Reserved			RPIHD[C][1—12]												0000
081D	COR/W	TRDIPD [C]	Reserved				RZ5DMOND[C]	RZ4DMOND[C]	RZ3DMOND[C]	RH4DMOND[C]	RF2DMOND[C]	RRDIPDMOND[C]	RC2DMOND[C]	RUC2D [C]	RPPLMD [C]	RSDD[C]	RSFD[C]	0000
081E—0828	—	Reserved																0000
Port D																		
0829	COR/W	RJ1DMONMIS[D]E	Reserved			RPIHD[D][1—12]												0000
082A	COR/W	TRDIPD [D]	Reserved				RZ5DMOND[D]	RZ4DMOND[D]	RZ3DMOND[D]	RH4DMOND[D]	RF2DMOND[D]	RRDIPDMOND[D]	RC2DMOND[D]	RUC2D [D]	RPPLMD [D]	RSDD[D]	RSFD[D]	0000
082B—0835	—	Reserved																0000
PT State Registers																		
Port A State Registers																		
0836	RO	RSSDRP[A][1:0]		Reserved		RPIH_STATE[A][1][1:0]		RPIH_STATE[A][2][1:0]		RPIH_STATE[A][3][1:0]		RPIH_STATE[A][4][1:0]		RPIH_STATE[A][5][1:0]		RPIH_STATE[A][6][1:0]		0AAA

Register Maps (continued)

PT Registers (continued)

Table 33. Map of Path Terminator Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0837	RO	Reserved				RPIH_STATE[A][7] [1:0]		RPIH_STATE[A][8] [1:0]		RPIH_STATE[A][9] [1:0]		RPIH_STATE[A][10] [1:0]		RPIH_STATE[A][11] [1:0]		RPIH_STATE[A][12] [1:0]		0AAA
0838	RO	TRDIPINT[A][2:0]			Reserved						RRDIPDMON[A][2:0]			RUC2VS [A]	RPPLMS [A]	RSDS[A]	RSF[A]	0000
0839	RO	RF2DMON[A][7:0]								RC2DMON[A][7:0]								0000
083A	RO	RZ3DMON[A][7:0]								RH4DMON[A][7:0]								0000
083B	RO	RZ5DMON[A][7:0]								RZ4DMON[A][7:0]								0000
083C—0867	—	Reserved																0000
0868	RO	RJ1DMON[A][1][7:0]								RJ1DMON[A][2][7:0]								0000
0869	RO	RJ1DMON[A][3][7:0]								RJ1DMON[A][4][7:0]								0000
086A	RO	RJ1DMON[A][5][7:0]								RJ1DMON[A][6][7:0]								0000
086B	RO	RJ1DMON[A][7][7:0]								RJ1DMON[A][8][7:0]								0000
086C	RO	RJ1DMON[A][9][7:0]								RJ1DMON[A][10][7:0]								0000
086D	RO	RJ1DMON[A][11][7:0]								RJ1DMON[A][12][7:0]								0000
086E	RO	RJ1DMON[A][13][7:0]								RJ1DMON[A][14][7:0]								0000
086F	RO	RJ1DMON[A][15][7:0]								RJ1DMON[A][16][7:0]								0000
0870	RO	RJ1DMON[A][17][7:0]								RJ1DMON[A][18][7:0]								0000
0871	RO	RJ1DMON[A][19][7:0]								RJ1DMON[A][20][7:0]								0000
0872	RO	RJ1DMON[A][21][7:0]								RJ1DMON[A][22][7:0]								0000
0873	RO	RJ1DMON[A][23][7:0]								RJ1DMON[A][24][7:0]								0000
0874	RO	RJ1DMON[A][25][7:0]								RJ1DMON[A][26][7:0]								0000
0875	RO	RJ1DMON[A][27][7:0]								RJ1DMON[A][28][7:0]								0000
0876	RO	RJ1DMON[A][29][7:0]								RJ1DMON[A][30][7:0]								0000
0877	RO	RJ1DMON[A][31][7:0]								RJ1DMON[A][32][7:0]								0000
0878	RO	RJ1DMON[A][33][7:0]								RJ1DMON[A][34][7:0]								0000
0879	RO	RJ1DMON[A][35][7:0]								RJ1DMON[A][36][7:0]								0000
087A	RO	RJ1DMON[A][37][7:0]								RJ1DMON[A][38][7:0]								0000
087B	RO	RJ1DMON[A][39][7:0]								RJ1DMON[A][40][7:0]								0000
087C	RO	RJ1DMON[A][41][7:0]								RJ1DMON[A][42][7:0]								0000
087D	RO	RJ1DMON[A][43][7:0]								RJ1DMON[A][44][7:0]								0000
087E	RO	RJ1DMON[A][45][7:0]								RJ1DMON[A][46][7:0]								0000
087F	RO	RJ1DMON[A][47][7:0]								RJ1DMON[A][48][7:0]								0000
0880	RO	RJ1DMON[A][49][7:0]								RJ1DMON[A][50][7:0]								0000
0881	RO	RJ1DMON[A][51][7:0]								RJ1DMON[A][52][7:0]								0000

Register Maps (continued)

PT Registers (continued)

Table 33. Map of Path Terminator Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0882	RO	RJ1DMON[A][53][7:0]								RJ1DMON[A][54][7:0]								0000
0883	RO	RJ1DMON[A][55][7:0]								RJ1DMON[A][56][7:0]								0000
0884	RO	RJ1DMON[A][57][7:0]								RJ1DMON[A][58][7:0]								0000
0885	RO	RJ1DMON[A][59][7:0]								RJ1DMON[A][60][7:0]								0000
0886	RO	RJ1DMON[A][61][7:0]								RJ1DMON[A][62][7:0]								0000
0887	RO	RJ1DMON[A][63][7:0]								RJ1DMON[A][64][7:0]								0000
Port B State Registers																		
0888	RO	RSSDRP[B][1:0]		Reserved		RPIH_STATE[B][1] [1:0]		RPIH_STATE[B][2] [1:0]		RPIH_STATE[B][3] [1:0]		RPIH_STATE[B][4] [1:0]		RPIH_STATE[B][5] [1:0]		RPIH_STATE[B][6] [1:0]		0AAA
0889	RO	Reserved				RPIH_STATE[B][7] [1:0]		RPIH_STATE[B][8] [1:0]		RPIH_STATE[B][9] [1:0]		RPIH_STATE[B][10] [1:0]		RPIH_STATE[B][11] [1:0]		RPIH_STATE[B][12] [1:0]		0AAA
088A	RO	TRDIPINT[B][2:0]			Reserved						RRDIPDMON[B][2:0]			RUC2VS [B]	RPPLMS [B]	RSDS[B]	RSF[B]	0000
088B	RO	RF2DMON[B][7:0]								RC2DMON[B][7:0]								0000
088C	RO	RZ3DMON[B][7:0]								RH4DMON[B][7:0]								0000
088D	RO	RZ5DMON[B][7:0]								RZ4DMON[B][7:0]								0000
088E—08B9	—	Reserved																0000
08BA	RO	RJ1DMON[B][1][7:0]								RJ1DMON[B][2][7:0]								0000
08BB	RO	RJ1DMON[B][3][7:0]								RJ1DMON[B][4][7:0]								0000
08BC	RO	RJ1DMON[B][5][7:0]								RJ1DMON[B][6][7:0]								0000
08BD	RO	RJ1DMON[B][7][7:0]								RJ1DMON[B][8][7:0]								0000
08BE	RO	RJ1DMON[B][9][7:0]								RJ1DMON[B][10][7:0]								0000
08BF	RO	RJ1DMON[B][11][7:0]								RJ1DMON[B][12][7:0]								0000
08C0	RO	RJ1DMON[B][13][7:0]								RJ1DMON[B][14][7:0]								0000
08C1	RO	RJ1DMON[B][15][7:0]								RJ1DMON[B][16][7:0]								0000
08C2	RO	RJ1DMON[B][17][7:0]								RJ1DMON[B][18][7:0]								0000
08C3	RO	RJ1DMON[B][19][7:0]								RJ1DMON[B][20][7:0]								0000
08C4	RO	RJ1DMON[B][21][7:0]								RJ1DMON[B][22][7:0]								0000
08C5	RO	RJ1DMON[B][23][7:0]								RJ1DMON[B][24][7:0]								0000
08C6	RO	RJ1DMON[B][25][7:0]								RJ1DMON[B][26][7:0]								0000
08C7	RO	RJ1DMON[B][27][7:0]								RJ1DMON[B][28][7:0]								0000
08C8	RO	RJ1DMON[B][29][7:0]								RJ1DMON[B][30][7:0]								0000
08C9	RO	RJ1DMON[B][31][7:0]								RJ1DMON[B][32][7:0]								0000
08CA	RO	RJ1DMON[B][33][7:0]								RJ1DMON[B][34][7:0]								0000

Register Maps (continued)

PT Registers (continued)

Table 33. Map of Path Terminator Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
08CB	RO	RJ1DMON[B][35][7:0]								RJ1DMON[B][36][7:0]								0000
08CC	RO	RJ1DMON[B][37][7:0]								RJ1DMON[B][38][7:0]								0000
08CD	RO	RJ1DMON[B][39][7:0]								RJ1DMON[B][40][7:0]								0000
08CE	RO	RJ1DMON[B][41][7:0]								RJ1DMON[B][42][7:0]								0000
08CF	RO	RJ1DMON[B][43][7:0]								RJ1DMON[B][44][7:0]								0000
08D0	RO	RJ1DMON[B][45][7:0]								RJ1DMON[B][46][7:0]								0000
08D1	RO	RJ1DMON[B][47][7:0]								RJ1DMON[B][48][7:0]								0000
08D2	RO	RJ1DMON[B][49][7:0]								RJ1DMON[B][50][7:0]								0000
08D3	RO	RJ1DMON[B][51][7:0]								RJ1DMON[B][52][7:0]								0000
08D4	RO	RJ1DMON[B][53][7:0]								RJ1DMON[B][54][7:0]								0000
08D5	RO	RJ1DMON[B][55][7:0]								RJ1DMON[B][56][7:0]								0000
08D6	RO	RJ1DMON[B][57][7:0]								RJ1DMON[B][58][7:0]								0000
08D7	RO	RJ1DMON[B][59][7:0]								RJ1DMON[B][60][7:0]								0000
08D8	RO	RJ1DMON[B][61][7:0]								RJ1DMON[B][62][7:0]								0000
08D9	RO	RJ1DMON[B][63][7:0]								RJ1DMON[B][64][7:0]								0000
Port C State Registers																		
08DA	RO	RSSDRP[C][1:0]		Reserved		RPIH_STATE[C][1] [1:0]		RPIH_STATE[C][2] [1:0]		RPIH_STATE[C][3] [1:0]		RPIH_STATE[C][4] [1:0]		RPIH_STATE[C][5] [1:0]		RPIH_STATE[C][6] [1:0]		0AAA
08DB	RO	Reserved				RPIH_STATE[C][7] [1:0]		RPIH_STATE[C][8] [1:0]		RPIH_STATE[C][9] [1:0]		RPIH_STATE[C][10] [1:0]		RPIH_STATE[C][11] [1:0]		RPIH_STATE[C][12] [1:0]		0AAA
08DC	RO	TRDIPINT[C][2:0]			Reserved						RRDIPDMON[C][2:0]			RUC2VS [C]	RPPLMS [C]	RSDS[C]	RSF[C]	0000
08DD	RO	RF2DMON[C][7:0]								RC2DMON[C][7:0]								0000
08DE	RO	RZ3DMON[C][7:0]								RH4DMON[C][7:0]								0000
08DF	RO	RZ5DMON[C][7:0]								RZ4DMON[C][7:0]								0000
08E0—090B	—	Reserved																0000
090C	RO	RJ1DMON[C][1][7:0]								RJ1DMON[C][2][7:0]								0000
090D	RO	RJ1DMON[C][3][7:0]								RJ1DMON[C][4][7:0]								0000
090E	RO	RJ1DMON[C][5][7:0]								RJ1DMON[C][6][7:0]								0000
090F	RO	RJ1DMON[C][7][7:0]								RJ1DMON[C][8][7:0]								0000
0910	RO	RJ1DMON[C][9][7:0]								RJ1DMON[C][10][7:0]								0000
0911	RO	RJ1DMON[C][11][7:0]								RJ1DMON[C][12][7:0]								0000
0912	RO	RJ1DMON[C][13][7:0]								RJ1DMON[C][14][7:0]								0000
0913	RO	RJ1DMON[C][15][7:0]								RJ1DMON[C][16][7:0]								0000

Register Maps (continued)

PT Registers (continued)

Table 33. Map of Path Terminator Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0914	RO	RJ1DMON[C][17][7:0]								RJ1DMON[C][18][7:0]								0000
0915	RO	RJ1DMON[C][19][7:0]								RJ1DMON[C][20][7:0]								0000
0916	RO	RJ1DMON[C][21][7:0]								RJ1DMON[C][22][7:0]								0000
0917	RO	RJ1DMON[C][23][7:0]								RJ1DMON[C][24][7:0]								0000
0918	RO	RJ1DMON[C][25][7:0]								RJ1DMON[C][26][7:0]								0000
0919	RO	RJ1DMON[C][27][7:0]								RJ1DMON[C][28][7:0]								0000
091A	RO	RJ1DMON[C][29][7:0]								RJ1DMON[C][30][7:0]								0000
091B	RO	RJ1DMON[C][31][7:0]								RJ1DMON[C][32][7:0]								0000
091C	RO	RJ1DMON[C][33][7:0]								RJ1DMON[C][34][7:0]								0000
091D	RO	RJ1DMON[C][35][7:0]								RJ1DMON[C][36][7:0]								0000
091E	RO	RJ1DMON[C][37][7:0]								RJ1DMON[C][38][7:0]								0000
091F	RO	RJ1DMON[C][39][7:0]								RJ1DMON[C][40][7:0]								0000
0920	RO	RJ1DMON[C][41][7:0]								RJ1DMON[C][42][7:0]								0000
0921	RO	RJ1DMON[C][43][7:0]								RJ1DMON[C][44][7:0]								0000
0922	RO	RJ1DMON[C][45][7:0]								RJ1DMON[C][46][7:0]								0000
0923	RO	RJ1DMON[C][47][7:0]								RJ1DMON[C][48][7:0]								0000
0924	RO	RJ1DMON[C][49][7:0]								RJ1DMON[C][50][7:0]								0000
0925	RO	RJ1DMON[C][51][7:0]								RJ1DMON[C][52][7:0]								0000
0926	RO	RJ1DMON[C][53][7:0]								RJ1DMON[C][54][7:0]								0000
0927	RO	RJ1DMON[C][55][7:0]								RJ1DMON[C][56][7:0]								0000
0928	RO	RJ1DMON[C][57][7:0]								RJ1DMON[C][58][7:0]								0000
0929	RO	RJ1DMON[C][59][7:0]								RJ1DMON[C][60][7:0]								0000
092A	RO	RJ1DMON[C][61][7:0]								RJ1DMON[C][62][7:0]								0000
092B	RO	RJ1DMON[C][63][7:0]								RJ1DMON[C][64][7:0]								0000
Port D State Registers																		
092C	RO	RSSDRP[D][1:0]		Reserved		RPIH_STATE[D][1] [1:0]		RPIH_STATE[D][2] [1:0]		RPIH_STATE[D][3] [1:0]		RPIH_STATE[D][4] [1:0]		RPIH_STATE[D][5] [1:0]		RPIH_STATE[D][6] [1:0]		0AAA
092D	RO	Reserved				RPIH_STATE[D][7] [1:0]		RPIH_STATE[D][8] [1:0]		RPIH_STATE[D][9] [1:0]		RPIH_STATE[D][10] [1:0]		RPIH_STATE[D][11] [1:0]		RPIH_STATE[D][12] [1:0]		0AAA
092E	RO	TRDIPINT[D][2:0]			Reserved						RRDIPDMON[D][2:0]			RUC2VS [D]	RPPLMS [D]	RSDS[D]	RSF[D]	0000
092F	RO	RF2DMON[D][7:0]								RC2DMON[D][7:0]								0000
0930	RO	RZ3DMON[D][7:0]								RH4DMON[D][7:0]								0000
0931	RO	RZ5DMON[D][7:0]								RZ4DMON[D][7:0]								0000

Register Maps (continued)

PT Registers (continued)

Table 33. Map of Path Terminator Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0932—095D	—	Reserved																0000
095E	RO	RJ1DMON[D][1][7:0]								RJ1DMON[D][2][7:0]								0000
095F	RO	RJ1DMON[D][3][7:0]								RJ1DMON[D][4][7:0]								0000
0960	RO	RJ1DMON[D][5][7:0]								RJ1DMON[D][6][7:0]								0000
0961	RO	RJ1DMON[D][7][7:0]								RJ1DMON[D][8][7:0]								0000
0962	RO	RJ1DMON[D][9][7:0]								RJ1DMON[D][10][7:0]								0000
0963	RO	RJ1DMON[D][11][7:0]								RJ1DMON[D][12][7:0]								0000
0964	RO	RJ1DMON[D][13][7:0]								RJ1DMON[D][14][7:0]								0000
0965	RO	RJ1DMON[D][15][7:0]								RJ1DMON[D][16][7:0]								0000
0966	RO	RJ1DMON[D][17][7:0]								RJ1DMON[D][18][7:0]								0000
0967	RO	RJ1DMON[D][19][7:0]								RJ1DMON[D][20][7:0]								0000
0968	RO	RJ1DMON[D][21][7:0]								RJ1DMON[D][22][7:0]								0000
0969	RO	RJ1DMON[D][23][7:0]								RJ1DMON[D][24][7:0]								0000
096A	RO	RJ1DMON[D][25][7:0]								RJ1DMON[D][26][7:0]								0000
096B	RO	RJ1DMON[D][27][7:0]								RJ1DMON[D][28][7:0]								0000
096C	RO	RJ1DMON[D][29][7:0]								RJ1DMON[D][30][7:0]								0000
096D	RO	RJ1DMON[D][31][7:0]								RJ1DMON[D][32][7:0]								0000
096E	RO	RJ1DMON[D][33][7:0]								RJ1DMON[D][34][7:0]								0000
096F	RO	RJ1DMON[D][35][7:0]								RJ1DMON[D][36][7:0]								0000
0970	RO	RJ1DMON[D][37][7:0]								RJ1DMON[D][38][7:0]								0000
0971	RO	RJ1DMON[D][39][7:0]								RJ1DMON[D][40][7:0]								0000
0972	RO	RJ1DMON[D][41][7:0]								RJ1DMON[D][42][7:0]								0000
0973	RO	RJ1DMON[D][43][7:0]								RJ1DMON[D][44][7:0]								0000
0974	RO	RJ1DMON[D][45][7:0]								RJ1DMON[D][46][7:0]								0000
0975	RO	RJ1DMON[D][47][7:0]								RJ1DMON[D][48][7:0]								0000
0976	RO	RJ1DMON[D][49][7:0]								RJ1DMON[D][50][7:0]								0000
0977	RO	RJ1DMON[D][51][7:0]								RJ1DMON[D][52][7:0]								0000
0978	RO	RJ1DMON[D][53][7:0]								RJ1DMON[D][54][7:0]								0000
0979	RO	RJ1DMON[D][55][7:0]								RJ1DMON[D][56][7:0]								0000
097A	RO	RJ1DMON[D][57][7:0]								RJ1DMON[D][58][7:0]								0000
097B	RO	RJ1DMON[D][59][7:0]								RJ1DMON[D][60][7:0]								0000
097C	RO	RJ1DMON[D][61][7:0]								RJ1DMON[D][62][7:0]								0000
097D	RO	RJ1DMON[D][63][7:0]								RJ1DMON[D][64][7:0]								0000

Register Maps (continued)

PT Registers (continued)

Table 33. Map of Path Terminator Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
PT Interrupt Mask Control																		
097E	R/W	PT_FUNCMODE		Reserved										PTINTM[D—A]				000F
Port A Interrupt Mask Control																		
097F	R/W	RJ1DMON MISM[A]	Reserved			RPIH_STATEM[A][1—12]												8FFF
0980	R/W	TRDIP-INTM[A]	Reserved				RZ5DMO NM[A]	RZ4DMO NM[A]	RZ3DMO NM[A]	RH4DMO NM[A]	RF2DMO NM[A]	RRDIPD-MONM[A]	RC2MON M[A]	RUC2VM [A]	RPPLMM [A]	RSDM[A]	RSFM[A]	FFFF
0981—098B	—	Reserved																0000
Port B Interrupt Mask Control																		
098C	R/W	RJ1DMON MISM[B]	Reserved			RPIH_STATEM[B][1—12]												8FFF
098D	R/W	TRDIP-INTM[B]	Reserved				RZ5DMO NM[B]	RZ4DMO NM[B]	RZ3DMO NM[B]	RH4DMO NM[B]	RF2DMO NM[B]	RRDIPD-MONM[B]	RC2MON M[B]	RUC2VM [B]	RPPLMM [B]	RSDM[B]	RSFM[B]	FFFF
098E—0998	R/W	Reserved																0000
Port C Interrupt Mask Control																		
0999	R/W	RJ1DMON MISM[C]	Reserved			RPIH_STATEM[C][1—12]												8FFF
099A	R/W	TRDIP-INTM[C]	Reserved				RZ5DMO NM[C]	RZ4DMO NM[C]	RZ3DMO NM[C]	RH4DMO NM[C]	RF2DMO NM[C]	RRDIPD-MONM[C]	RC2MON M[C]	RUC2VM [C]	RPPLMM [C]	RSDM[C]	RSFM[C]	FFFF
099B—09A5	—	Reserved																0000
Port D Interrupt Mask Control																		
09A6	R/W	RJ1DMON MISM[D]	Reserved			RPIH_STATEM[D][1—12]												8FFF
09A7	R/W	TRDIP-INTM[D]	Reserved				RZ5DMO NM[D]	RZ4DMO NM[D]	RZ3DMO NM[D]	RH4DMO NM[D]	RF2DMO NM[D]	RRDIPD-MONM[D]	RC2MON M[D]	RUC2VM [D]	RPPLMM [D]	RSDM[D]	RSFM[D]	FFFF
09A8—09B2	—	Reserved																0000
Error Counters																		
Port A																		
09B3	RO	Reserved					RPI_INC[A][10:0]											0000
09B4—09BE	—	Reserved																0000
09BF	RO	Reserved					RPI_DEC[A][10:0]											0000
09C0—09CA	—	Reserved																0000

Register Maps (continued)

PT Registers (continued)

Table 33. Map of Path Terminator Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
09CB	RO	Reserved			RNDFCNT[A][12:0]													0000
09CC—09D6	—	Reserved																0000
09D7	RO	RB3ERRCNT[A][15:0]																0000
09D8—09E2	—	Reserved																0000
09E3	RO	RREIPERRCNT[A][15:0]																0000
09E4—09EE	—	Reserved																0000
Port B																		
09EF	RO	Reserved					RPI_INC[B][10:0]											0000
09F0—09FA	—	Reserved																0000
09FB	RO	Reserved					RPI_DEC[B][10:0]											0000
09FC—0A06	—	Reserved																0000
0A07	RO	Reserved			RNDFCNT[B][12:0]													0000
0A08—0A13	—	Reserved																0000
0A14	RO	RB3ERRCNT[B][15:0]																0000
0A15—0A1F	—	Reserved																0000
0A20	RO	RREIPERRCNT[B][15:0]																0000
0A21—0A2B	—	Reserved																0000
Port C																		
0A2C	RO	Reserved					RPI_INC[C][10:0]											0000
0A2D—0A37	—	Reserved																0000
0A38	RO	Reserved					RPI_DEC[C][10:0]											0000
0A39—0A43	—	Reserved																0000
0A44	RO	Reserved			RNDFCNT[C][12:0]													0000
0A45—0A4F	—	Reserved																0000
0A50	RO	RB3ERRCNT[C][15:0]																0000

Register Maps (continued)

PT Registers (continued)

Table 33. Map of Path Terminator Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0A51—0A5B	—	Reserved																0000
0A5C	RO	RREIPERRCNT[C][15:0]																0000
0A5D—0A67	—	Reserved																0000
Port D																		
0A68	RO	Reserved					RPI_INC[D][10:0]											0000
0A69—0A73	—	Reserved																0000
0A74	RO	Reserved					RPI_DEC[D][10:0]											0000
0A75—0A7F	—	Reserved																0000
0A80	RO	Reserved			RNDFCNT[D][12:0]													0000
0A81—0A8B	—	Reserved																0000
0A8C	RO	RB3ERRCNT[D][15:0]																0000
0A8D—0A97	—	Reserved																0000
0A98	RO	RREIPERRCNT[D][15:0]																0000
0A99—0AA3	—	Reserved																0000
PT One-Shot Control																		
0AA4	WO	SDCLEAR[A—D]				SDSET[A—D]				SFCLEAR[A—D]				SFSET[A—D]				—
0AA5	—	Reserved																0000
PT Control Parameters																		
Port A																		
0AA6	R/W	Reserved							RJ1FRAMEA[A][1:0]		RJ1DMPC[A]	RSSP-TRNORM[A]	RB3BITBLKCNT[A]	RIINCDEC_6OR8MAJ[A]	Reserved		RDIPMON_ENH_OR1B[A]	F200
0AA7	R/W	RFORCE_LOP[A][1—4]				CONCATI_EXPECTED[A][1—12]												0000
0AA8	R/W	RFORCE_LOP[A][5—8]				MASK_CONCAT[A][1—12]												0FFF
0AA9	R/W	RFORCE_LOP[A][9—12]				RFORCE_AIS[A][1—12]												0000
0AAA	R/W	Tx_REIP_VALUE[A][3:0]				TRDIPSINS[A]	Reserved	TRDIP_PLMP-INH[A]	TRDIP_UNEQUIPINH[A]	TRDIP_LCDINH[A]	TRDIP_LOPPINH[A]	TRDIP_AISINH[A]	TRDIP_ENH_OR1B[A]	TREIPER-RINS[A]	TB3ERRINS[A]	TJ1INS[A]	Reserved	0000
0AAB	R/W	TPOHINSSEL[A][3:0]				THx_STATE[A][1—6][1:0]												1AAA

Register Maps (continued)

PT Registers (continued)

Table 33. Map of Path Terminator Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0AAC	R/W	CNTDH4Z3Z4[A][3:0]				THx_STATE[A][7—12][1:0]												3AAA
0AAD	R/W	CNTDZ5[A][3:0]				CNTDF2[A][3:0]				CNTDRDIP[A][3:0]				CNTDC2[A][3:0]				3333
Port B																		
0AAE	R/W	Reserved							RJ1FRAMEA[B][1:0]		RJ1DMPC[B]	RSSP-TRNORM[B]	RB3BITBLKCNT[B]	RIINCDEC_6OR8MAJ[B]	Reserved		RDIPMON_ENH_OR1B[B]	F200
0AAF	R/W	RFORCE_LOP[B][1—4]				CONCATI_EXPECTED[B][1—12]												0000
0AB0	R/W	RFORCE_LOP[B][5—8]				MASK_CONCAT[B][1—12]												0FFF
0AB1	R/W	RFORCE_LOP[B][9—12]				RFORCE_AIS[B][1—12]												0000
0AB2	R/W	Tx_REIP_VALUE[B][3:0]				TRDIPSINS[B]	Reserved	TRDIP_PLMP-INH[B]	TRDIP_UNEQUIPINH[B]	TRDIP_LCDINH[B]	TRDIP_LOPPINH[B]	TRDIP_AISINH[B]	TRDIP_ENH_OR1B[B]	TREIPER-RINS[B]	TB3ERRINS[B]	TJ1INS[B]	Reserved	0000
0AB3	R/W	TPOHINSSEL[B][3:0]				THx_STATE[B][1—6][1:0]												1AAA
0AB4	R/W	CNTDH4Z3Z4[B][3:0]				THx_STATE[B][7—12][1:0]												3AAA
0AB5	R/W	CNTDZ5[B][3:0]				CNTDF2[B][3:0]				CNTDRDIP[B][3:0]				CNTDC2[B][3:0]				3333
Port C																		
0AB6	R/W	Reserved							RJ1FRAMEA[C][1:0]		RJ1DMPC[C]	RSSP-TRNORM[C]	RB3BITBLKCNT[C]	RIINCDEC_6OR8MAJ[C]	Reserved		RDIPMON_ENH_OR1[C]	F200
0AB7	R/W	RFORCE_LOP[C][1—4]				CONCATI_EXPECTED[C][1—12]												0000
0AB8	R/W	RFORCE_LOP[C][5—8]				MASK_CONCAT[C][1—12]												0FFF
0AB9	R/W	RFORCE_LOP[C][9—12]				RFORCE_AIS[C][1—12]												0000
0ABA	R/W	Tx_REIP_VALUE[C][3:0]				TRDIPSINS[C]	Reserved	TRDIP_PLMP-INH[C]	TRDIP_UNEQUIPINH[C]	TRDIP_LCDINH[C][C]	TRDIP_LOPPINH[C]	TRDIP_AISINH[C]	TRDIP_ENH_OR1B[C]	TREIPER-RINS[C]	TB3ERRINS[C]	TJ1INS[C]	Reserved	0000
0ABB	R/W	TPOHINSSEL[C][3:0]				THx_STATE[C][1—6][1:0]												1AAA
0ABC	R/W	CNTDH4Z3Z4[C][3:0]				THx_STATE[C][7—12][1:0]												3AAA
0ABD	R/W	CNTDZ5[C][3:0]				CNTDF2[C][3:0]				CNTDRDIP[C][3:0]				CNTDC2[C][3:0]				3333
Port D																		
0ABE	R/W	Reserved							RJ1FRAMEA[D][1:0]		RJ1DMPC[D]	RSSP-TRNORM[D]	RB3BITBLKCNT[D]	RIINCDEC_6OR8MAJ[D]	Reserved		RDIPMON_ENH_OR1[D]	F200
0ABF	R/W	RFORCE_LOP[D][1—4]				CONCATI_EXPECTED[D][1—12]												0000
0AC0	R/W	RFORCE_LOP[D][5—8]				MASK_CONCAT[D][1—12]												0FFF
0AC1	R/W	RFORCE_LOP[D][9—12]				RFORCE_AIS[D][1—12]												0000

Register Maps (continued)

PT Registers (continued)

Table 33. Map of Path Terminator Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
0AC2	R/W	Tx_REIP_VALUE[D][3:0]				TRDIPSINS[D]	Reserved	TRDIP_PLMP-INH[D]	TRDIP_UNEQUIPINH[D]	TRDIP_LCDINH[D]	TRDIP_LOPPINH[D]	TRDIP_AISINH[D]	TRDIP_ENH_OR1B[D]	TREIPERRINS[D]	TB3ERRINS[D]	TJ1INS[D]	Reserved	0000
0AC3	R/W	TPOHINSSEL[D][3:0]				THx_STATE[D][1—6][1:0]												1AAA
0AC4	R/W	CNTDH4Z3Z4[D][3:0]				THx_STATE[D][7—12][1:0]												3AAA
0AC5	R/W	CNTDZ5[D][3:0]				CNTDF2[D][3:0]				CNTDRDIP[D][3:0]				CNTDC2[D][3:0]				3333
PT Provisioning Registers																		
0AC6	R/W	Reserved										PG_PROV_PNUM[1:0]		PG_PROV_TNUM[3:0]				0001
0AC7	R/W	TRDIPDINS[2:0]			TSS[1:0]		Reserved									RSSEXP[1:0]		0000
0AC8	R/W	Reserved								RC2EXPVAL[7:0]								0000
0AC9	R/W	TF2DINS[7:0]								TC2DINS[7:0]								0000
0ACA	R/W	TZ3DINS[7:0]								TH4DINS[7:0]								0000
0ACB	R/W	TZ5DINS[7:0]								TZ4DINS[7:0]								0000
Signal Fail (SF) B3 BER Algorithm Control Signals																		0000
0ACC	R/W	SFMSET[7:0]								Reserved				SFLSET[3:0]				0000
0ACD	R/W	SFNSSET[18:16]			Reserved	SFBSET[11:0]												0000
0ACE	R/W	SFNSSET[15:0]																0000
0ACF	R/W	SFMCLEAR[7:0]								Reserved				SFLCLEAR[3:0]				0000
0AD0	R/W	SFNSCLEAR[18:16]			Reserved	SFBCLEAR[11:0]												0000
0AD1	R/W	SFNSCLEAR[15:0]																0000
Signal Degrade (SD) B3 BER Algorithm Control Signals																		0000
0AD2	R/W	SDM__SET[7:0]								Reserved				SDLSET[3:0]				0000
0AD3	R/W	SDNSSET[18:16]			Reserved	SDBSET[11:0]												0000
0AD4	R/W	SDNSSET[15:0]																0000
0AD5	R/W	SDMCLEAR[7:0]								Reserved				SDLCLEAR[3:0]				0000
0AD6	R/W	SDNSCLEAR[18:16]			Reserved	SDBCLEAR[11:0]												0000
0AD7	R/W	SDNSCLEAR[15:0]																0000
Transmit J1 Data Insert Registers																		
0AD8	R/W	TJ1DINS[1][7:0]								TJ1DINS[2][7:0]								0000
0AD9	R/W	TJ1DINS[3][7:0]								TJ1DINS[4][7:0]								0000
0ADA	R/W	TJ1DINS[5][7:0]								TJ1DINS[6][7:0]								0000
0ADB	R/W	TJ1DINS[7][7:0]								TJ1DINS[8][7:0]								0000
0ADC	R/W	TJ1DINS[9][7:0]								TJ1DINS[10][7:0]								0000
0ADD	R/W	TJ1DINS[11][7:0]								TJ1DINS[12][7:0]								0000

Register Maps (continued)

PT Registers (continued)

Table 33. Map of Path Terminator Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**	
0ADE	R/W	TJ1DINS[13][7:0]								TJ1DINS[14][7:0]								0000
0ADF	R/W	TJ1DINS[15][7:0]								TJ1DINS[16][7:0]								0000
0AE0	R/W	TJ1DINS[17][7:0]								TJ1DINS[18][7:0]								0000
0AE1	R/W	TJ1DINS[19][7:0]								TJ1DINS[20][7:0]								0000
0AE2	R/W	TJ1DINS[21][7:0]								TJ1DINS[22][7:0]								0000
0AE3	R/W	TJ1DINS[23][7:0]								TJ1DINS[24][7:0]								0000
0AE4	R/W	TJ1DINS[25][7:0]								TJ1DINS[26][7:0]								0000
0AE5	R/W	TJ1DINS[27][7:0]								TJ1DINS[28][7:0]								0000
0AE6	R/W	TJ1DINS[29][7:0]								TJ1DINS[30][7:0]								0000
0AE7	R/W	TJ1DINS[31][7:0]								TJ1DINS[32][7:0]								0000
0AE8	R/W	TJ1DINS[33][7:0]								TJ1DINS[34][7:0]								0000
0AE9	R/W	TJ1DINS[35][7:0]								TJ1DINS[36][7:0]								0000
0AEA	R/W	TJ1DINS[37][7:0]								TJ1DINS[38][7:0]								0000
0AEB	R/W	TJ1DINS[39][7:0]								TJ1DINS[40][7:0]								0000
0AEC	R/W	TJ1DINS[41][7:0]								TJ1DINS[42][7:0]								0000
0AED	R/W	TJ1DINS[43][7:0]								TJ1DINS[44][7:0]								0000
0AEE	R/W	TJ1DINS[45][7:0]								TJ1DINS[46][7:0]								0000
0AEF	R/W	TJ1DINS[47][7:0]								TJ1DINS[48][7:0]								0000
0AF0	R/W	TJ1DINS[49][7:0]								TJ1DINS[50][7:0]								0000
0AF1	R/W	TJ1DINS[51][7:0]								TJ1DINS[52][7:0]								0000
0AF2	R/W	TJ1DINS[53][7:0]								TJ1DINS[54][7:0]								0000
0AF3	R/W	TJ1DINS[55][7:0]								TJ1DINS[56][7:0]								0000
0AF4	R/W	TJ1DINS[57][7:0]								TJ1DINS[58][7:0]								0000
0AF5	R/W	TJ1DINS[59][7:0]								TJ1DINS[60][7:0]								0000
0AF6	R/W	TJ1DINS[61][7:0]								TJ1DINS[62][7:0]								0000
0AF7	R/W	TJ1DINS[63][7:0]								TJ1DINS[64][7:0]								0000
Scratch Register																		
0AF8	R/W	PT_SCRATCH[15:0]																0000

Register Maps (continued)

DE Registers

Table 34. Map of DE Registers

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
DE Version Control																		
1000	RO	DE_VERSION[15:0]																0001
DE Interrupts																		
1001	RO	Reserved											DEINT_SDLMS	DEINTCH[3:0]				0000
1002	RO	DEINT_SDLRxFS				DEINT_ATMRxAC				DEINT_ATMRxS				DEINT_ATMRxF				0000
1003	—	Reserved																0000
Miscellaneous Registers																		
1004	R/W	Reserved								DRYESCAPE[7:0]								0020
1005—100F	—	Reserved																0000
Sequencer Provisioning Registers (R/W)																		
1010	R/W	Reserved														SEQ_RATE	SEQ_MODE	0002
1011	R/W	INIT_CNTS																2210
1012	R/W	OH_MARKER_LO																0435
1013	R/W	OH_MARKER_HI																0025
1014	R/W	SOH_MARKER_LO																0435
1015	R/W	SOH_MARKER_HI																0025
Egress/Ingress Configuration Registers (R/W)																		
1016	R/W	Tx_TS0[15:0] (Bits 15, 11, 7, 3 are reserved)																4444
1017	R/W	Tx_TS1[15:0] (Bits 15, 11, 7, 3 are reserved)																5555
1018	R/W	Tx_TS2[15:0] (Bits 15, 11, 7, 3 are reserved)																6666
1019	R/W	Tx_TS3[15:0] (Bits 15, 11, 7, 3 are reserved)																7777
101A	R/W	Tx_TS4[15:0] (Bits 15, 11, 7, 3 are reserved)																4444
101B	R/W	Tx_TS5[15:0] (Bits 15, 11, 7, 3 are reserved)																5555
101C	R/W	Tx_TS6[15:0] (Bits 15, 11, 7, 3 are reserved)																6666
101D	R/W	Tx_TS7[15:0] (Bits 15, 11, 7, 3 are reserved)																7777
101E	R/W	Tx_TS8[15:0] (Bits 15, 11, 7, 3 are reserved)																4444
101F	R/W	Tx_TS9[15:0] (Bits 15, 11, 7, 3 are reserved)																5555
1020	R/W	Tx_TS10[15:0] (Bits 15, 11, 7, 3 are reserved)																6666
1021	R/W	Tx_TS11[15:0] (Bits 15, 11, 7, 3 are reserved)																7777
1022	R/W	Rx_TS0[15:0] (Bits 15, 11, 7, 3 are reserved)																4444
1023	R/W	Rx_TS1[15:0] (Bits 15, 11, 7, 3 are reserved)																5555
1024	R/W	Rx_TS2[15:0] (Bits 15, 11, 7, 3 are reserved)																6666

Register Maps (continued)

DE Registers (continued)

Table 34. Map of DE Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1025	R/W	Rx_TS3[15:0] (Bits 15, 11, 7, 3 are reserved)																7777
1026	R/W	Rx_TS4[15:0] (Bits 15, 11, 7, 3 are reserved)																4444
1027	R/W	Rx_TS5[15:0] (Bits 15, 11, 7, 3 are reserved)																5555
1028	R/W	Rx_TS6[15:0] (Bits 15, 11, 7, 3 are reserved)																6666
1029	R/W	Rx_TS7[15:0] (Bits 15, 11, 7, 3 are reserved)																7777
102A	R/W	Rx_TS8[15:0] (Bits 15, 11, 7, 3 are reserved)																4444
102B	R/W	Rx_TS9[15:0] (Bits 15, 11, 7, 3 are reserved)																5555
102C	R/W	Rx_TS10[15:0] (Bits 15, 11, 7, 3 are reserved)																6666
102D	R/W	Rx_TS11[15:0] (Bits 15, 11, 7, 3 are reserved)																7777
Transparent Mode Control																		
102E	R/W	Rx_OF_CTRL[15:0] (Bits 15, 13, 12, 11, 9, 8, 7, 5, 4, 3 are reserved)																0000
102F	R/W	Tx_OF_CTRL[15:0] (Bits 15, 13, 12, 11, 9, 8, 7, 5, 4, 3 are reserved)																0000
1030	R/W	Rx_CHCD_FM[15:0] (Bits 15, 14, 7 6 are reserved)																0000
1031	R/W	Rx_CHAB_FM[15:0] (Bits 15, 14, 7 6 are reserved)																0000
Sequencer Cell State																		
1032	R/W	Reserved						Rx_CELL[A]_FM[9:0]										0000
1033	R/W	Reserved						Rx_CELL[B]_FM[9:0]										0000
1034	R/W	Reserved						Rx_CELL[C]_FM[9:0]										0000
1035	R/W	Reserved						Rx_CELL[D]_FM[9:0]										0000
1036	R/W	Reserved												Tx_SEQ_DISABLE[3:0]				000F
1037—103F	—	Reserved																0000
Ingress Type/Mode Control Registers																		
1040	R/W	Reserved					Rx_PCTL_0[10:0]											0700
1041	R/W	Reserved					Rx_PCTL_1[10:0]											0700
1042	R/W	Reserved					Rx_PCTL_2[10:0]											0700
1043	R/W	Reserved					Rx_PCTL_3[10:0]											0700
1044—107F	—	Reserved																0000
ATM Framer Registers																		
Idle Cell Match Mask																		
1080	R/W	ATM_IDM_0[31:16]																FFFF
1081	R/W	ATM_IDM_0[15:0]																FFFF
1082	R/W	ATM_IDM_1[31:16]																FFFF
1083	R/W	ATM_IDM_1[15:0]																FFFF

Register Maps (continued)

DE Registers (continued)

Table 34. Map of DE Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1084	R/W	ATM_IDM_2[31:16]																FFFF
1085	R/W	ATM_IDM_2[15:0]																FFFF
1086	R/W	ATM_IDM_3[31:16]																FFFF
1087	R/W	ATM_IDM_3[15:0]																FFFF
Idle Cell Register																		
1088	R/W	ATM_IDC_0[31:16]																0000
1089	R/W	ATM_IDC_0[15:0]																0001
108A	R/W	ATM_IDC_1[31:16]																0000
108B	R/W	ATM_IDC_1[15:0]																0001
108C	R/W	ATM_IDC_2[31:16]																0000
108D	R/W	ATM_IDC_2[15:0]																0001
108E	R/W	ATM_IDC_3[31:16]																0000
108F	R/W	ATM_IDC_3[15:0]																0001
Unassigned Cell Match Mask																		
1090	R/W	ATM_USM_0[31:16]																FFFF
1091	R/W	ATM_USM_0[15:0]																FFFF
1092	R/W	ATM_USM_1[31:16]																FFFF
1093	R/W	ATM_USM_1[15:0]																FFFF
1094	R/W	ATM_USM_2[31:16]																FFFF
1095	R/W	ATM_USM_2[15:0]																FFFF
1096	R/W	ATM_USM_3[31:16]																FFFF
1097	R/W	ATM_USM_3[15:0]																FFFF
Unassigned Cell Register																		
1098	R/W	ATM_USG_0[31:16]																0000
1099	R/W	ATM_USG_0[15:0]																0000
109A	R/W	ATM_USG_1[31:16]																0000
109B	R/W	ATM_USG_1[15:0]																0000
109C	R/W	ATM_USG_2[31:16]																0000
109D	R/W	ATM_USG_2[15:0]																0000
109E	R/W	ATM_USG_3[31:16]																0000
109F	R/W	ATM_USG_3[15:0]																0000

Register Maps (continued)

DE Registers (continued)

Table 34. Map of DE Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
ATM Scrambler Framer State																		
10A0	RO	Reserved												ATM_ST_0[3:0]				0000
10A1	RO	Reserved												ATM_ST_1[3:0]				0000
10A2	RO	Reserved												ATM_ST_2[3:0]				0000
10A3	RO	Reserved												ATM_ST_3[3:0]				0000
ATM Control Registers																		
ATM Receive Configuration Registers																		
10A4	R/W	Reserved				ATM_X43[11:0]												01C6
10A5	R/W	Reserved				ATM_X31[11:0]												01C8
10A6	R/W	Reserved				ATM_X31VW[11:0]												0210
10A7	R/W	Reserved				ATM_X31XY[11:0]												0418
10A8	R/W	Reserved										ATM_X31Z[5:0]						0018
10A9	R/W	Reserved												FS_INT_MASK[3:0]				000F
10AA	R/W	Reserved												SS_INT_MASK[3:0]				000F
10AB	R/W	Reserved										ATM_Rx_DEBUG_REG[5:0]						003C
10AC—10AF	—	Reserved																0000
ATM Transmit Control Registers																		
PPP Attach Registers																		
10B0	R/W	PPP_Tx_CHAN[0][15:0]																0000
10B1	R/W	PPP_Tx_CHAN[1][15:0]																0000
10B2	R/W	PPP_Tx_CHAN[2][15:0]																0000
10B3	R/W	PPP_Tx_CHAN[3][15:0]																0000
10B4—10DF	—	Reserved																0000
Egress Type/Mode Control Registers																		
10E0	R/W	Reserved					Tx_PCTL_[0][10:0]											0700
10E1	R/W	Reserved					Tx_PCTL_[1][10:0]											0700
10E2	R/W	Reserved					Tx_PCTL_[2][10:0]											0700
10E3	R/W	Reserved					Tx_PCTL_[3][10:0]											0700
10E4—10EF	—	Reserved																0000
PPP Detach Registers																		
10F0	R/W	PPP_Rx_HDR0[0][15:0]																0000
10F1	R/W	PPP_Rx_HDR0[1][15:0]																0000

Register Maps (continued)

DE Registers (continued)

Table 34. Map of DE Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
10F2	R/W	PPP_Rx_HDR0[2][15:0]																0000
10F3	R/W	PPP_Rx_HDR0[3][15:0]																0000
10F4	R/W	PPP_Rx_HDR0[4][15:0]																0000
10F5	R/W	PPP_Rx_HDR0[5][15:0]																0000
10F6	R/W	PPP_Rx_HDR0[6][15:0]																0000
10F7	R/W	PPP_Rx_HDR0[7][15:0]																0000
10F8	R/W	PPP_Rx_HDR0[8][15:0]																0000
10F9	R/W	PPP_Rx_HDR0[9][15:0]																0000
10FA	R/W	PPP_Rx_HDR0[10][15:0]																0000
10FB	R/W	PPP_Rx_HDR0[11][15:0]																0000
10FC	R/W	PPP_Rx_CHK_CH[0][15:0]																C001
10FD	R/W	PPP_Rx_CHK_CH[1][15:0]																C002
10FE	R/W	PPP_Rx_CHK_CH[2][15:0]																C004
10FF	R/W	PPP_Rx_CHK_CH[3][15:0]																C008
ATM/HDLC/SDL—Counter 1 (PMRST Update)																		
1100	RO	Reserved				PM_FC1_0[27:16]												0000
1101	RO	PM_FC1_0[15:0]																0000
1102	RO	Reserved				PM_FC1_1[27:16]												0000
1103	RO	PM_FC1_1[15:0]																0000
1104	RO	Reserved				PM_FC1_2[27:16]												0000
1105	RO	PM_FC1_2[15:0]																0000
1106	RO	Reserved				PM_FC1_3[27:16]												0000
1107	RO	PM_FC1_3[15:0]																0000
ATM/HDLC/SDL—Counter 2 (PMRST Update)																		
1108	RO	Reserved				PM_FC2_0[27:16]												0000
1109	RO	PM_FC2_0[15:0]																0000
110A	RO	Reserved				PM_FC2_1[27:16]												0000
110B	RO	PM_FC2_1[15:0]																0000
110C	RO	Reserved				PM_FC2_2[27:16]												0000
110D	RO	PM_FC2_2[15:0]																0000
110E	RO	Reserved				PM_FC2_3[27:16]												0000
110F	RO	PM_FC2_3[15:0]																0000
CRC Checker—Bad Packet Counter (PMRST Update)																		
1110	RO	Reserved				PM_BPC_0[27:16]												0000

Register Maps (continued)

DE Registers (continued)

Table 34. Map of DE Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1111	RO	PM_BPC_0[15:0]																0000
1112	RO	Reserved				PM_BPC_1[27:16]												0000
1113	RO	PM_BPC_1[15:0]																0000
1114	RO	Reserved				PM_BPC_2[27:16]												0000
1115	RO	PM_BPC_2[15:0]																0000
1116	RO	Reserved				PM_BPC_3[27:16]												0000
1117	RO	PM_BPC_3[15:0]																0000
PPP Detach—Mismatched Header Counter (PMRST Update)																		
1118	RO	Reserved				PM_BHC_0[27:16]												0000
1119	RO	PM_BHC_0[15:0]																0000
111A	RO	Reserved				PM_BHC_1[27:16]												0000
111B	RO	PM_BHC_1[15:0]																0000
111C	RO	Reserved				PM_BHC_2[27:16]												0000
111D	RO	PM_BHC_2[15:0]																0000
111E	RO	Reserved				PM_BHC_3[27:16]												0000
111F	RO	PM_BHC_3[15:0]																0000
PPP Detach—Rx Good Packet/Cell Counter (PMRST Update)																		
1120	RO	Reserved				PM_GPC_Rx_0[27:16]												0000
1121	RO	PM_GPC_Rx_0[15:0]																0000
1122	RO	Reserved				PM_GPC_Rx_1[27:16]												0000
1123	RO	PM_GPC_Rx_1[15:0]																0000
1124	RO	Reserved				PM_GPC_Rx_2[27:16]												0000
1125	RO	PM_GPC_Rx_2[15:0]																0000
1126	RO	Reserved				PM_GPC_Rx_3[27:16]												0000
1127	RO	PM_GPC_Rx_3[15:0]																0000
PPP Attach—Tx Good Packet/Cell Counter (PMRST Update)																		
1128	RO	Reserved				PM_GPC_Tx_0[27:16]												0000
1129	RO	PM_GPC_Tx_0[15:0]																0000
112A	RO	Reserved				PM_GPC_Tx_1[27:16]												0000
112B	RO	PM_GPC_Tx_1[15:0]																0000
112C	RO	Reserved				PM_GPC_Tx_2[27:16]												0000
112D	RO	PM_GPC_Tx_2[15:0]																0000
112E	RO	Reserved				PM_GPC_Tx_3[27:16]												0000
112F	RO	PM_GPC_Tx_3[15:0]																0000

Register Maps (continued)

DE Registers (continued)

Table 34. Map of DE Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1130—117F	RO	Reserved																0000
Interrupts and Mask Control																		
1180	R/W	Reserved											DEDINTM[0]					001F
1181	COR/W	Reserved											DEDINT[0]					0000
1182	R/W	Reserved											DEDINTM[1]					001F
1183	COR/W	Reserved											DEDINT[1]					0000
1184	R/W	Reserved											DEDINTM[2]					001F
1185	COR/W	Reserved											DEDINT[2]					0000
1186	R/W	Reserved											DEDINTM[3]					001F
1187	COR/W	Reserved											DEDINT[3]					0000
1188—11FF	—	Reserved																0000
ATM Transmit Registers																		
1200	R/W	NULLCELL1[0][15:0]																0000
1201	R/W	NULLCELL1[1][15:0]																0000
1202	R/W	NULLCELL1[2][15:0]																0000
1203	R/W	NULLCELL1[3][15:0]																0000
1204—120F	—	Reserved																0000
1210	R/W	NULLCELL2[0][15:0]																0001
1211	R/W	NULLCELL2[1][15:0]																0001
1212	R/W	NULLCELL2[2][15:0]																0001
1213	R/W	NULLCELL2[3][15:0]																0001
1214—12EF	—	Reserved																0000
12F0	R/W	Reserved								ATM_HEADER_ERROR[7:0]								0000
12F1—13FF	—	Reserved																0000
SDL Receive Registers																		
1400	RO	Reserved												SDL_ST[0][3:0]				0000
1401	RO	Reserved												SDL_ST[1][3:0]				0000
1402	RO	Reserved												SDL_ST[2][3:0]				0000
1403	RO	Reserved												SDL_ST[3][3:0]				0000

Register Maps (continued)

DE Registers (continued)

Table 34. Map of DE Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
1404—146F	—	Reserved																0000
1470	RO	SDL_AMM1[0][15:0]																0000
1471	RO	SDL_AMM1[1][15:0]																0000
1472	RO	SDL_AMM1[2][15:0]																0000
1473	RO	SDL_AMM1[3][15:0]																0000
1474—147F	—	Reserved																0000
1480	RO	SDL_AMM2[0][15:0]																0000
1481	RO	SDL_AMM2[1][15:0]																0000
1482	RO	SDL_AMM2[2][15:0]																0000
1483	RO	SDL_AMM2[3][15:0]																0000
1484—148F	—	Reserved																0000
1490	RO	SDL_AMM3[0][15:0]																0000
1491	RO	SDL_AMM3[1][15:0]																0000
1492	RO	SDL_AMM3[2][15:0]																0000
1493	RO	SDL_AMM3[3][15:0]																0000
1494—149F	—	Reserved																0000
14A0	RO	SDL_BMM1[0][15:0]																0000
14A1	RO	SDL_BMM1[1][15:0]																0000
14A2	RO	SDL_BMM1[2][15:0]																0000
14A3	RO	SDL_BMM1[3][15:0]																0000
14A4—14AF	—	Reserved																0000
14B0	RO	SDL_BMM2[0][15:0]																0000
14B1	RO	SDL_BMM2[1][15:0]																0000
14B2	RO	SDL_BMM2[2][15:0]																0000
14B3	RO	SDL_BMM2[3][15:0]																0000
14B4—14BF	—	Reserved																0000
14C0	RO	SDL_BMM[0]_3[15:0]																0000
14C1	RO	SDL_BMM[1]_3[15:0]																0000
14C2	RO	SDL_BMM[2]_3[15:0]																0000

Register Maps (continued)

DE Registers (continued)

Table 34. Map of DE Registers (continued)

Address (Hex)	(RO), (R/W), (WO), (COR/W)	Bit Number																Default Value (Hex)
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
14C3	RO	SDL_BMM[3]_3[15:0]																0000
14C4—14CF	—	Reserved																0000
14D0	R/W	Reserved								SDLINTM[0][7:0] (Bit 3 is reserved)								00FF
14D1	R/W	Reserved								SDLINTM[1][7:0] (Bit 3 is reserved)								00FF
14D2	R/W	Reserved								SDLINTM[2][7:0] (Bit 3 is reserved)								00FF
14D3	R/W	Reserved								SDLINTM[3][7:0] (Bit 3 is reserved)								00FF
14D4—14DF	—	Reserved																0000
14E0	R/W	Reserved								SDLINT[0][7:0] (Bit 3 is reserved)								0000
14E1	R/W	Reserved								SDLINT[1][7:0] (Bit 3 is reserved)								0000
14E2	R/W	Reserved								SDLINT[2][7:0] (Bit 3 is reserved)								0000
14E3	R/W	Reserved								SDLINT[3][7:0] (Bit 3 is reserved)								0000
14E4—14EF	—	Reserved																0000
14F0	R/W	Reserved									SDL_DELTA[6:0]							0001
14F1—15FF	—	Reserved																0000
SDL Transmit Registers																		
1600	R/W	SDLFI_MSG1[15:0]																0000
1601	R/W	SDLFI_MSG2[15:0]																0000
1602	R/W	SDLFI_MSG3[15:0]																0000
1603	R/W	SDLMTB	Reserved													SDLCHID[1:0]		0000
1604	R/W	SDLFI_INT[15:0]																0008
1605	R/W	SDLSMIE	Reserved													SDLSC	SDLSSTMS	8000
1606	R/W	Reserved														SDLFDO	SDLMSI	0000
1607	R/W	Reserved										SDLHE[1:0]		SDLPE[1:0]		SDLECID[1:0]		0000

Register Descriptions

Core Registers

This section gives a brief description of each register bit and its functionality. All algorithms are described in the main text of the document. The abbreviations after each register indicate if the register is read only (RO), read/write (R/W), write only (WO), or clear-on-read or clear-on-write (COR/W).

0x indicates a hexadecimal value in the Reset Default column. Otherwise, the entry is binary. This is true for every register table in the document.

Table 35. Register 0x0000: Device Version (RO)

Reset default of register = 0x0100.

Address (Hex)	Bit #	Name	Function	Reset Default
0000	15—8	DEVICE_VERSION[7:0]	**Device Version Number.** Device version register will change each time the device is changed.	0x01
	7—0	—	**Reserved.** These bits must be written to their reset default value (0x00).	0x00

Table 36. Registers 0x0001—0x0005: Device Name (RO)

Reset default of each register is shown below.

Address (Hex)	Bit #	Name	Function	Reset Default
0001	15—0	ASCII_NAME_TD	**Device ASCII Name.** Value = T, D.	0x5444
0002	15—0	ASCII_NAME_AT	**Device ASCII Name.** Value = A, T.	0x4154
0003	15—0	ASCII_NAME_04	**Device ASCII Name.** Value = 0, 4.	0x3034
0004	15—0	ASCII_NAME_2G	**Device ASCII Name.** Value = 2, G.	0x3247
0005	15—0	ASCII_NAME_5CR	**Device ASCII Name.** Value = 5, CR.	0x350D

Register Descriptions (continued)

Core Registers (continued)

Table 37. Register 0x0008: Composite Interrupts (RO or COR/W)

Reset default of register = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0008	15	PMRSTI	**Performance Monitor Reset Interrupt.** Active-high signal indicating a 1 second event has occurred. This bit is COR/W.	0
	14—12	—	**Reserved.** These bits must be written to their reset default value (000).	000
	11—8	GPIO[3:0]I	**General-Purpose Interrupt.** Signal indicating the associated input is active. When the GPIO are outputs, this signal will be forced low. These interrupts are COR/W when the interrupt is programmed to the positive edge mode; otherwise, this is a read-only (RO) location.	0x0
	7	UTI	**UTOPIA Composite Interrupt**. Active-high signal indicating an unmasked delta or event is active in the UTOPIA block. This bit is RO.	0
	6	DEI	**Data Engine Composite Interrupt.** Active-high signal indicating an unmasked delta or event is active in the data engine block. This bit is RO.	0
	5—2	—	**Reserved.** These bits must be written to their reset default value (0000).	0000
0008	1	PTI	**Path Terminator Composite Interrupt.** Active-high signal indicating an unmasked delta or event is active in the path terminator block. This bit is RO.	0
	0	OHPI	**Overhead Processor Composite Interrupt.** Active-high signal indicating an unmasked delta or event is active in the overhead processor block. This bit is RO.	0

Table 38. Register 0x000A: GPIO Input (RO)

Reset default of register = 0x000x (x not determined).

Address (Hex)	Bit #	Name	Function	Reset Default
000A	15—4	—	**Reserved.** These bits must be written to their reset default value (0x000).	0x000
	3—0	GPIO[3:0]_INPUT_VALUE	**General-Purpose Input Value.** These are the logical values of the GPIO[3:0] I/O pins.	Pin value

Register Descriptions (continued)

Core Registers (continued)

Table 39. Register 0x000C: Block Interrupt Masks (R/W)

Reset default of register = 0xFFFF.

Address (Hex)	Bit #	Name	Function	Reset Default
000C	15	PMRSTM	**Performance Monitor Reset Mask.** When set to 1, the associated composite interrupt bit will be inhibited (masked) from contributing to the interrupt pin ($\overline{\text{INT}}$).	1
	14—12	—	**Reserved.** These bits must be written to their reset default value (111).	111
	11—8	GPIO[3:0]IM	**General-Purpose Interrupt Mask.** When set to 1, the associated composite interrupt bits will be inhibited (masked) from contributing to the interrupt pin ($\overline{\text{INT}}$).	0xF
	7	UTIM	**UTOPIA Composite Interrupt Mask**. When set to 1, the associated composite interrupt bit will be inhibited (masked) from contributing to the interrupt pin ($\overline{\text{INT}}$).	1
	6	DEIM	**Data Engine Composite Interrupt Mask.** When set to 1, the associated composite interrupt bit will be inhibited (masked) from contributing to the interrupt pin ($\overline{\text{INT}}$).	1
	5—2	—	**Reserved.** These bits must be written to their reset default value (1111).	1111
	1	PTIM	**Path Terminator Composite Interrupt Mask.** When set to 1, the associated composite interrupt bit will be inhibited (masked) from contributing to the interrupt pin ($\overline{\text{INT}}$).	1
	0	OHPIM	**Overhead Processor Composite Interrupt Mask.** When set to 1, the associated composite interrupt bit will be inhibited (masked) from contributing to the interrupt pin ($\overline{\text{INT}}$).	1

Table 40. Register 0x000E: Core Resets (WO)

Address (Hex)	Bit #	Name	Function	Reset Default
000E	15—8	—	**Reserved.**	NA
	7	PMRST	**Performance Monitor Reset.** When this bit is set to 1, the PMRST signal goes high. The register will automatically be reset to 0 and the PMRST signal will go low after 500 ms.	NA
	6—3	—	**Reserved.**	NA
000E	2—0	SWRST	**Software Reset.** When a binary value of 101 is written to this register, it will create a software reset of the device. This reset has the same effect as the hardware reset. All microprocessor registers are reset to their default states and all internal data path state machines are reset.	NA

Register Descriptions (continued)

Core Registers (continued)

Table 41. Register 0x000F: GPIO Output (R/W)

Reset default of register = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
000F	15—4	—	**Reserved.** These bits must be written to their reset default value (0x000).	0x000
	3—0	GPIO[3:0]_OUTPUT_VALUE	**General-Purpose Output Values.** The value written into these bits will appear on the GPIO[3:0] pins.	0x0

Provisioning Registers

Table 42. Register 0x0010: Line Provisioning/Mode (R/W)

Reset default of register = 0x1070.

Address (Hex)	Bit #	Name	Function	Reset Default
0010	15—13	—	**Reserved.** These bits must be written to their reset default value (000).	000
	12	POF_POS	**Packet/ATM Over Fiber/SONET.** 0 = packet or ATM over fiber (POF); 1 = packet or ATM over SONET (POS).	1
	11—10	—	**Reserved.** These bits must be written to their reset default value (00).	00
	9—8	PMMODE[1:0]	**Performance Monitoring Mode.** 00 or 10 = PMRST comes from external pin 01 = PMRST comes from internal 1-second counter 11 = PMRST is software controlled	00
	7	SDH/SONET	**SDH or SONET Mode.** 1 = SDH; 0 = SONET.	0
	6	COR/W	**Clear-on-Read or Clear-on-Write Control.** This bit sets the functionality of the COR/W registers. 1 = COR. Clear on read; read register to clear. 0 = COW. Clear on write; write 0 to clear.	1
	5	PLL_MODE	**PLL Mode.** Set this bit to 1 to turn off the phase-locked loop.	1
	4	STS48	**STS-48/STM-16 Control.** 1 = STS-48/STM-16 mode; 0 = STS-3/STS-12 (STM-1/STM-4) mode.	1
	3—0	STS12[A—D]	**STS-12/STS-3 (STM-4/STM-1) Mode Control.** The only values permitted are the following: 1111 = STS-12/STM-4 0000 = STS-3/STM-1	0x0

Register Descriptions (continued)

Core Registers (continued)

Provisioning Registers (continued)

Table 43. Register 0x0011: Channel (A—D) Control (R/W)

Reset default of register = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0011	15	EQ_CH_A	**Equip Channel A.** 1 = enable; 0 = disable, i.e., turns off clock in Rx direction, except in the STS-48/ STM-16 mode. This function is valid only for STS-12/STM-4 and STS-3/STM-1 modes (no effect in Tx direction).	0
	14—12	—	**Reserved.** These bits must be written to their reset default value (000).	000
	11	EQ_CH_B	**Equip Channel B.** 1 = enable; 0 = disable, i.e., turns off clock in Rx direction, except in the STS-48/ STM-16 mode. This function is valid only for STS-12/STM-4 and STS-3/STM-1 modes (no effect in Tx direction).	0
	10—8	—	**Reserved.** These bits must be written to their reset default value (000).	000
	7	EQ_CH_C	**Equip Channel C.** 1 = enable; 0 = disable, i.e., turns off clock in Rx direction, except in the STS-48/ STM-16 mode. This function is valid only for STS-12/STM-4 and STS-3/STM-1 modes (no effect in Tx direction).	0
	6—4	—	**Reserved.** These bits must be written to their reset default value (000).	000
	3	EQ_CH_D	**Equip Channel D.** 1 = enable; 0 = disable, i.e., turns off clock in Rx direction, except in the STS-48/ STM-16 mode. This function is valid only for STS-12/STM-4 and OSTS-3/STM-1 modes (no effect in Tx direction).	0
	2—0	—	**Reserved.** These bits must be written to their reset default value (000).	000

Table 44. Register 0x0012: Loopback Control (R/W)

Reset default of register = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0012	15—12	LOOPBACK[3:0]_CH_A	**Loopback Control**. In the following, x = don't care: 0000 = no loopbacks xxx1 = SONET facility loopback xx1x = SONET terminal loopback x1xx = UTOPIA far-end loopback 1xxx = UTOPIA near-end loopback SONET facility loopback is only available in STS-3/ STM-1 and STS-12/STM-4 modes.	0x0
	11—8	LOOPBACK[3:0]_CH_B		0x0
	7—4	LOOPBACK[3:0]_CH_C		0x0
	3—0	LOOPBACK[3:0]_CH_D		0x0

Register Descriptions (continued)

Core Registers (continued)

Provisioning Registers (continued)

Table 45. Register 0x0013: GPIO Mode (R/W)

Reset default of register = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0013	15	PMRST_I/O_CTRL	**PMRST I/O Control.** This bit is set to 1 to make PMRST an output.	0
	14—12	—	**Reserved.** These bits must be written to their reset default value (000).	000
	11—8	GPIO[3:0]_INTERRUPT_ ACTIVE_H/L	**GPIO Interrupt Active State.** 0 = report received value unchanged (level = input pin value, positive edge = 1 when signal rises). 1 = invert received value (level = invert input pin value, positive edge = 0 when detected).	0x0
	7—4	GPIO[3:0]_INTERRUPT_ LEVEL/EDGE	**GPIO Interrupt Type.** 0 = positive edge; 1 = level.	0x0
	3—0	GPIO[3:0]_DIRECTION_I/O	**GPIO Direction Control.** 0 = input; 1 = output.	0x0

Table 46. Register 0x001F: Scratch (R/W)

Reset default of register = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
001F	15—0	CORE_SCRATCH[15:0]	**Core Scratch Register.** A read/write register used to verify functionality of the microprocessor interface. No internal action will occur when written data is written to this location.	0x0000

Register Descriptions (continued)

UT Registers

This section gives a brief description of each register bit and its functionality. All algorithms are described in the main text of the document. The abbreviations after each register indicate if the register is read only (RO), read/write (R/W), write only (WO), or clear-on-read or clear-on-write (COR/W).

0x indicates a hexadecimal value in the Reset Default column. Otherwise, the entry is binary. This is true for every register table in the document.

Version Control

Table 47. Register 0x0200: UT Macrocell Version Number (RO)

Reset default of register = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0200	15—8	—	**Reserved.** These bits must be written to their reset default value (0x00).	0x00
	7—0	UT_VERSION[7:0]	**UT Macrocell Version Number.** The version of the macrocell will increment each time a change occurs to the macrocell functionality.	0x00

Interrupt

Table 48. Register 0x0201: UT Interrupt (RO)

Reset default of register = 0x0000.

Note: These registers are cleared by accessing registers 0x0202, 0x0203, 0x0204, 0x0205.

Address (Hex)	Bit #	Name	Function	Reset Default
0201	15—4	—	**Reserved.** These bits must be written to their reset default value (0x000).	0x000
	3	UT_INT[D]	**UT Interrupt for Channel D.** If this bit is set to 1, it indicates one of the interrupt conditions for channel D occurred.	0x0
	2	UT_INT[C]	**UT Interrupt for Channel C.** If this bit is set to 1, it indicates one of the interrupt conditions for channel C occurred.	
	1	UT_INT[B]	**UT Interrupt for Channel B.** If this bit is set to 1, it indicates one of the interrupt conditions for channel B occurred.	
	0	UT_INT[A]	**UT Interrupt for Channel A.** If this bit is set to 1, it indicates one of the interrupt conditions for channel A occurred.	

Register Descriptions (continued)

UT Registers (continued)

Delta and Event Parameters (COR)

Table 49. Registers 0x0202, 0x0203, 0x0204, 0x0205: Channel [A—D] (COR)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0202, 0203, 0204, 0205	15—4	—	**Reserved.** These bits must be written to their reset default value (0x000).	0x000
	3	FIFO_OVERFLOW_Tx[A—D]	**FIFO Overflow Transmit Channel [A—D].** If set, indicates that an overflow occurred in the Tx FIFO of channel [A—D].	0x0
	2	FIFO_UNDERFLOW_Tx[A—D]	**FIFO Underflow Transmit Channel [A—D].** If set, indicates that an underflow occurred in the Tx FIFO of channel [A—D].	
	1	FIFO_OVERFLOW_Rx[A—D]	**FIFO Overflow Receive Channel [A—D].** If set, indicates that an overflow occurred in the Rx FIFO of channel [A—D].	
	0	PARITY_ERROR_Tx[A—D]	**Parity Error Transmit Channel [A—D].** If set, indicates that a parity error was detected on the Tx channel of channel [A—D].	

Register Descriptions (continued)

UT Registers (continued)

Interrupt Mask Parameters (R/W)

Table 50. Register 0x0206: Interrupt Mask (R/W)

Reset default of register = 0x000F.

Address (Hex)	Bit #	Name	Function	Reset Default
0206	15—4	—	**Reserved.** These bits must be written to their reset default value (0x000).	0x000
	3	INTM[D]	**Interrupt Mask D.** If set to 1, masks any interrupts from channel D.	0xF
	2	INTM[C]	**Interrupt Mask C.** If set to 1, masks any interrupts from channel C.	
	1	INTM[B]	**Interrupt Mask B.** If set to 1, masks any interrupts from channel B.	
	0	INTM[A]	**Interrupt Mask A.** If set to 1, masks any interrupts from channel A.	

Table 51. Registers 0x0207, 0x0208, 0x0209, 0x020A: Interrupt Mask—Channel [A—D] (R/W)

Reset default of registers = 0x000F.

Address (Hex)	Bit #	Name	Function	Reset Default
0207, 0208, 0209, 020A	15—4	—	**Reserved.** These bits must be written to their reset default value (0x000).	0x000
	3	FIFO_OVERFLOW_Tx_MASK[A—D]	**FIFO Overflow Transmit Mask [A—D].** If set, masks this interrupt from setting Int[A—D].	0xF
	2	FIFO_UNDERFLOW_Tx_MASK[A—D]	**FIFO Underflow Transmit Mask [A—D].** If set, masks this interrupt from setting Int[A—D].	
	1	FIFO_OVERFLOW_Rx_MASK[A—D]	**FIFO Overflow Receive Mask [A—D].** If set, masks this interrupt from setting Int[A—D].	
	0	PARITY_ERROR_Tx_MASK[A—D]	**Parity Error Transmit Mask [A—D].** If set, masks this interrupt from setting Int[A—D].	

Error Count Registers in PMRST Mode (RO)

Table 52. Register 0x020B: Channel [A—D] Error Count in PMRST Mode (RO)

Reset default of register = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
020B—020E	15—0	PMRST_PECTx[A—D]	**PMRST Parity Error Count Transmit Channel [A—D].** Counts the number of parity errors that occur for Tx channel [A—D], based upon the PMRST interval.	0x0000

Register Descriptions (continued)

UT Registers (continued)

UT Provisioning Registers (R/W)

The fields of the UT provisioning registers in Table 54—Table 57 are summarized in Table 53. Following the table are the provisioning registers for the four channels.

Note: The default value depends on the channel. Defaults are as follows:

Channel A = 00000
Channel B = 00001
Channel C = 00010
Channel D = 00011

Table 53. Fields of the Provisioning Registers

Field Name	Function	Bit Value	Default
POLLING_ENB_Rx POLLING_ENB_Tx	Enabled	Bit 15 = 1	0
	Disabled	Bit 15 = 0	
RxADDR_[4:0] TxADDR_[4:0]	MPHY Address Value	Bits [12:8]	See note above.
CLOCK_MODE_Rx	Source	Bit 6 = 1	0
	Sink	Bit 6 =0	
PARITY_Rx PARITY_Tx	Odd	Bit 5 = 1	1
	Even	Bit 5 = 0	
ATM_SIZE_Rx ATM_SIZE_Tx	52 Bytes	Bit 4 = 1	0
	53 Bytes	Bit 4 = 0	
TRAFFIC_TYPE_Rx TRAFFIC_TYPE_Tx	ATM Cells	Bit 3 = 1	0
	Packets	Bit 3 = 0	
UTOPIA_MODE_Rx UTOPIA_MODE_Tx	Disabled (Idle)	Bits[2:0] = 000	000
	U2	Bits[2:0] = 001	
	U2+	Bits[2:0] = 010	
	U3, 8-bit	Bits[2:0] = 011	
	U3, 32-bit	Bits[2:0] = 100	
	U3+, 8-bit	Bits[2:0] = 101	
	U3+, 32-bit	Bits[2:0] = 110	
	Invalid	Bits[2:0] = 111	

Register Descriptions (continued)

UT Registers (continued)

UT Provisioning Registers (R/W) (continued)

Table 54. Registers 0x020F, 0213, 0217, 021B: Channel [A—D] Receive Provisioning Register (R/W)

Reset default of register 0x020F = 0x0020.
Reset default of register 0x0213 = 0x0120.
Reset default of register 0x0217 = 0x0020.
Reset default of register 0x021B = 0x0320.

Address (Hex)	Bit #	Name	Function	Reset Default
020F, 0213, 0127, 021B	15	POLLING_ENB_Rx [A—D]	**Polling Enable Receive Channel [A—D].** If set to 1, receive polling mode is enabled.	0
	14—13	—	**Reserved.** These bits must be written to their reset default value (00).	00
	12—8	RxADDR_A[4:0]	**Polling Receive Address Channel [A—D].** Receive polling address.	00000
		RxADDR_B[4:0]		00001
		RxADDR_C[4:0]		00010
		RxADDR_D[4:0]		00011
	7	—	**Reserved.** This bit must be written to its reset default value (0).	0
	6	CLOCK_MODE_Rx [A—D]	**Clock Mode Receive Channel [A—D].** Defines if the RxCLK[A—D] is sourced or sunk. If this bit = 1, the clock is sourced, and then (1) the corresponding Tx clock is used as RxCLK[A—D], and (2) this clock is also sent out of the device via RxCLK[A—D]. If this bit = 0, CLOCK_MODE_Rx[A—D] is sunk, and then RxCLK[A—D] acts as an input. Default is sink.	0
	5	PARITY_Rx[A—D]	**Parity Receive Channel [A—D].** Defines if odd (bit = 1) or even (bit = 0) parity is generated for the data transmitted across the UTOPIA PHY Rx interface. Default is odd.	1
	4	ATM_SIZE_Rx[A—D]	**ATM Packet Size Receive Channel [A—D].** If traffic type is ATM cells, this bit indicates if UDF fields are transmitted across the UTOPIA PHY Rx interface. Default is true.	0
	3	TRAFFIC_TYPE_Rx [A—D]	**Traffic Type Receive Channel [A—D].** Configures channel to receive either ATM cells or packets. Bit Value — Traffic Type 0 — packets (default) 1 — ATM cells	0

Register Descriptions (continued)

UT Registers (continued)

UT Provisioning Registers (R/W) (continued)

Table 54. Registers 0x020F, 0213, 0217, 021B: Channel [A—D] Receive Provisioning Register (R/W) (continued)

Reset default of register 0x020F = 0x0020.
Reset default of register 0x0213 = 0x0120.
Reset default of register 0x0217 = 0x0020.
Reset default of register 0x021B = 0x0320.

Address (Hex)	Bit #	Name	Function	Reset Default
020F, 0213, 0127, 021B	2—0	UTOPIA_MODE_Rx [A—D][2:0]	**UTOPIA Mode Receive Channel [A—D].** Configures the Rx channel mode. Mode Bit Value disabled (idle) bits[2:0] = 000 U2 bits[2:0] = 001 U2+ bits[2:0] = 010 U3, 8-bit bits[2:0] = 011 U3, 32-bit bits[2:0] = 100 U3+, 8-bit bits[2:0] = 101 U3+, 32-bit bits[2:0] = 110 invalid bits[2:0] = 111 U3 configuration also requires the appropriate setting of register 0x0225 (PA response) to be set for a two-cycle response.	000

Register Descriptions (continued)

UT Registers (continued)

UT Provisioning Registers (R/W) (continued)

Table 55. Registers 0x0210, 0214, 0218, 021C: Channel [A—D] Transmit Provisioning Register (R/W)

Reset default of register 0x0210 = 0x0000.
reset default of register 0x0214 = 0x0120.
Reset default of register 0x0218 = 0x0020.
reset default of register 0x021C = 0x0320.

Address (Hex)	Bit #	Name	Function	Reset Default
0210, 0214, 0218, 021C	15	POLLING_ENB_Tx [A—D]	**Polling Enable Transmit Channel [A—D].** If set, transmit polling mode is enabled.	0
	14—13	—	**Reserved.** These bits must be written to their reset default value (00).	00
	12—8	TxADDR_A[4:0]	**Polling Transmit Address Channel [A—D].** Transmit polling address.	00000
		TxADDR_B[4:0]		0001
		TxADDR_C[4:0]		0010
		TxADDR_D[4:0]		00011
	7—6	—	**Reserved.** These bits must be written to their reset default value (00).	00
	5	PARITY_Tx[A—D]	**Parity Transmit Channel [A—D].** Defines if odd or even parity is generated for the data transmitted across the UTOPIA PHY Tx interface. Default is odd.	0
	4	ATM_SIZE_Tx[A—D]	**ATM Packet Size Transmit Channel [A—D].** Defines how many bytes are received per ATM cell. Default is 53 bytes. Valid only when traffic type is ATM cells.	0
	3	TRAFFIC_TYPE_Tx [A—D]	**Traffic Type Transmit Channel [A—D].** Configures channel to transmit either ATM cells or packets. Bit Value Traffic Type 0 packets (default) 1 ATM cells	0
	2—0	UTOPIA_MODE_Tx [A—D][2:0]	**UTOPIA Mode Transmit Channel [A—D].** Configures the Tx channel mode. Mode Bit Value disabled (idle) bits[2:0] = 000 U2 bits[2:0] = 001 U2+ bits[2:0] = 010 U3, 8-bit bits[2:0] = 011 U3, 32-bit bits[2:0] = 100 U3+, 8-bit bits[2:0] = 101 U3+, 32-bit bits[2:0] = 110 invalid bits[2:0] = 111 U3 configuration also requires appropriate setting of register 0x0225 (PA response) to be set for a two-cycle response.	000

Register Descriptions (continued)

UT Registers (continued)

UT Provisioning Registers (R/W) (continued)

Table 56. Registers 0x0211, 0x0215, 0x0219, 0x021D: Channel [A—D] Ingress Provisioning Register (R/W)

Reset default of registers = 0x361F.

Address (Hex)	Bit #	Name	Function	Reset Default
0211, 0215, 0219, 021D	15—14	—	**Reserved.** These bits must be written to their reset default value (00).	00
	13—8	INGRESS_WATERMARK_HIGH_[A—D][6:0]	**Ingress Water Mark High for Channel [A—D].** Defines threshold before which overflow is detected.	110110
	7—6	—	**Reserved.** These bits must be written to their reset default value (00).	00
	5—0	INGRESS_WATERMARK_LOW_[A—D][6:0]	**Ingress Water Mark Low for Channel [A—D].** Defines how many words must be stored in the ingress FIFO before transmission out of the UTOPIA port, if an end of packet is not received.	011111

Table 57. Registers 0x0212, 0x0216, 0x021A, 0x021E: Channel [A—D] Egress Provisioning Register (R/W)

Reset default of registers = 0x361F.

Address (Hex)	Bit #	Name	Function	Reset Default
0212, 0216, 021A, 021E	15—14	—	**Reserved.** These bits must be written to their reset default value (00).	00
	13—8	EGRESS_WATERMARK_HIGH_[A—D][6:0]	**Egress Water Mark High for Channel [A—D].** Defines how many words can be stored into the egress FIFO before backpressure is applied to the UTOPIA PHY Tx port to stop acceptance of more traffic. Default value is set for packet transfer. For ATM transfer, the value should be configured as 0x29. For packet mode, this value depends upon the specific user-interface characteristics. The default value (110110) will work for packet mode.	110110
	7—6	—	**Reserved.** These bits must be written to their reset default value (00).	00
	5—0	EGRESS_WATERMARK_LOW_[A—D][6:0]	**Egress Water Mark Low for Channel [A—D].** Defines how many words must be stored in the egress FIFO before transmission to the data engine, if an end of packet is not received.	011111

Register Descriptions (continued)

UT Registers (continued)

Reset Register (R/W)

Table 58. Register 0x021F: Reset Register (R/W)

Reset default of register = 0x00FF.

Address (Hex)	Bit #	Name	Function	Reset Default
021F	—	UT_ARST	**UTOPIA Asynchronous Reset.** Active-high signal. This must be the last signal written to the UTOPIA interface during configuration and must be written to the value 0x00 to enable the particular channels.	0x00FF
	15—8	—	**Reserved.** These bits must be written to their reset default value (0x00).	0x00
	7	UT_TxARST_D	**Transmit ARST for Transmit Channel D.**	1
	6	UT_TxARST_C	**Transmit ARST for Transmit Channel C.**	1
	5	UT_TxARST_B	**Transmit ARST for Transmit Channel B.**	1
	4	UT_TxARST_A	**Transmit ARST for Transmit Channel A.**	1
	3	UT_RxARST_D	**Receive ARST for Receive Channel D.**	1
	2	UT_RxARST_C	**Receive ARST for Receive Channel C.**	1
	1	UT_RxARST_B	**Receive ARST for Receive Channel B.**	1
	0	UT_RxARST_A	**Receive ARST for Receive Channel A.**	1

Error Count Registers (RO)

Table 59. Register 0x0220: Channel [A—D] Error Count (RO)

Reset default of register = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0220—0223	15—0	PECTx[A—D]	**Parity Error Count Transmit Channel [A—D].** Counts the instantaneous (real-time) number of parity errors that occur for Tx channel [A—D].	0x0000

Scratch Register (R/W)

Table 60. Register 0x0224: UT_Scratch Register (R/W)

Reset default of register = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0224	15—0	UT_SCRATCH	**UT Scratch Register.** Read/write register with no other internal UT connections.	0x0000

Register Descriptions (continued)

UT Registers (continued)

PA Response Register (R/W)

Table 61. Register 0x0225: PA Response Register (R/W)

Reset default of register = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0225	—	PA/DATA	**Packet Available (PA).** In MPHY mode, when this bit is 0, the PA response follows placement of a valid address on the address bus by the ATM master device by one UTOPIA interface clock period. The RxDATA response follows the RxENB assertion. If this bit is 1, then the PA response and RxDATA response follow the address by two clock periods. Two-cycle response is provided for U3-compatible operation.	0x0000
	15—8	—	**Reserved.** These bits must be written to their reset default value (0x00).	0x00
	7	TxPAD	**TxPA Response for Transmit Channel D.**	0
	6	TxPAC	**TxPA Response for Transmit Channel C.**	0
	5	TxPAB	**TxPA Response for Transmit Channel B.**	0
	4	TxPAA	**TxPA Response for Transmit Channel A.**	0
	3	RxPAD/RxDATAD/ RxSOP/CD	**RxPA Response for Receive Channel D.**	0
	2	RxPAC/RxDATAC/ RxSOP/CC	**RxPA Response for Receive Channel C.**	0
	1	RxPAB/RxDATAB/ RxSOP/CB	**RxPA Response for Receive Channel B.**	0
	0	RxPAA/RxDATAA/ RxSOP/CA	**RxPA Response for Receive Channel A.**	0

Register Descriptions (continued)

UT Registers (continued)

Size Mode Register (R/W)

Table 62. Register 0x0226: Size Mode Register (R/W)

Reset default of register = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0226	—	—	**Size Mode.** Size mode for each channel. If this mode bit = 0 (default mode): ■ TxSize (or RxSize) set to 0 means the most significant byte is the last byte of the current packet, and ■ TxSize (or RxSize) set to 1 means the least significant byte is the last byte. ■ TxSIZE or RxSIZE are defined as per Pin Information section, page 29. If this mode bit = 1: ■ TxSize (or RxSize) set to 1 means the most significant byte is the last byte of the current packet, and ■ TxSize (or RxSize) set to 0 means the least significant byte is the last byte. ■ TxSIZE or RxSIZE definitions are inverted as per Table 5, page 29.	0x0000
	15—8	—	**Reserved.** These bits must be written to their reset default value (0x00).	0x00
	7	TxSIZE_D	**TxSIZE_MODE for Transmit Channel D.**	0
	6	TxSIZE_C	**TxSIZE_MODE for Transmit Channel C.**	0
	5	TxSIZE_B	**TxSIZE_MODE for Transmit Channel B.**	0
	4	TxSIZE_A	**TxSIZE_MODE for Transmit Channel A.**	0
	3	RxSIZE_D	**RxSIZE_MODE for Receive Channel D.**	0
	2	RxSIZE_C	**RxSIZE_MODE for Receive Channel C.**	0
	1	RxSIZE_B	**RxSIZE_MODE for Receive Channel B.**	0
	0	RxSIZE_A	**RxSIZE_MODE for Receive Channel A.**	0

Register Descriptions (continued)

OHP Registers

This section gives a brief description of each register bit and its functionality. All algorithms are described in the main text of the document. The abbreviations after each register indicate if the register is read only (RO), read/write (R/W), write only (WO), or clear-on-read or clear-on-write (COR/W).

0x indicates a hexadecimal value in the Reset Default column. Otherwise, the entry is binary. This is true for every register table in the document.

Table 63. Register 0x0400: OHP Macrocell Version Number (RO)

Reset default of register = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0400	15—0	OHP_VERSION[15:0]	**OHP Macrocell Version Number.** The version of the macrocell will increment each time a change occurs to the macrocell functionality.	0x0000

Table 64. Register 0x0401: OHP Interrupt (RO)

Reset default of register = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0401	15—4	—	**Reserved.** These bits must be written to their reset default value (0x000).	0x000
	3	OHP_INT[D]	**OHP Interrupt.** Active-high interrupt bits for channels D to A. Each bit is the ORing of all event and delta bits of that channel. In STS-48/STM-16 mode, INT[A] is valid.	0x0
	2	OHP_INT[C]		0x0
	1	OHP_INT[B]		0x0
	0	OHP_INT[A]		0x0

Table 65. Registers 0x0402—0x0409: Delta/Event (COR/W)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0402, 0404, 0406, 0408	15	LRDIMOND[A—D]	**Line/Multiplex RDI Delta.** Delta bits indicate a change of state for the line/multiplex RDI state bits (LRDIMON[A—D]). Their mask bits are LRDIMONM[A—D]. Only LRDIMOND[A] is valid for STS-48/STM-16.	0
	14	LAISMOND[A—D]	**Line/Multiplex AIS Delta.** Delta bits indicate a change of state for the line/multiplex AIS state bits (LAISMON[A—D]). The delta bits clear when read. Their mask bits are LAISMONM[A—D]. Only LAISMOND[A] is valid for STS-48/STM-16.	0
	13	RAPSBABLEE[A—D]	**APS Babble Event.** Each bit is active-high to indicate the inconsistence in K1 byte of that channel. Their mask bits are RAPSBABLEM[A—D]. Only RAPSBABLEE[A] is valid for STS-48/STM-16.	0

Register Descriptions (continued)

OHP Registers (continued)

Table 65. Registers 0x0402—0x0409: Delta/Event (COR/W) (continued)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0402, 0404, 0406, 0408	12	S1DMON4D[A—D]	**Delta Register for S1DMON[3:0] When S1MON8or4CTL = 1.** Each delta bit indicates a change of state for S1DMON[3:0] in its channel. The delta bits clear when read. Their mask bits are S1DMON4M[A—D]. In STS-48/STM-16 mode, S1DMON4D[A] is valid.	0
	11	S1DMON8D[A—D]	**Delta Register for S1DMON[7:4] When S1MON8or4CTL = 1 or S1DMON[7:0] When S1MON8or4CTL = 0.** Each delta bit indicates a change of state for S1DMON[7:4]/ S1DMON[7:0] in its channel. The delta bits clear when read. Their mask bits are S1DMON8M[A—D]. In STS-48/STM-16 mode, S1DMON8D[A] is valid.	0
	10	K2DMOND[A—D]	**K2[2:0] Data Monitor Delta.** Each bit is active-high to indicate a change in K2DMON[A—D] for that channel. These bits will clear when read or written. Their mask bits are K2DMONM[A—D]. Only K2DMOND[A] is valid for STS-48/STM-16.	0
	9	K1K2DMOND[A—D]	**K1K2 Data Monitor Delta.** Each bit is active-high to indicate a change in (K1[7:0] and K2[7:3]) or (K1[7:0] and K2[7:0]) for that channel depending on K1K2_2_OR_1. Their mask bits are K1K2DMONM[A—D]. Only K1K2DMOND[A] is valid for STS-48/STM-16.	0
	8	F1DMOND[A—D]	**F1 Data Monitor Delta.** Their mask bits are F1DMONM[A—D]. Only F1DMOND[A] is valid for STS-48/STM-16.	0
	7	TTOAC_PERRE[A—D]	**Transmit TOAC Parity Error Event.** Event bit indicates a parity error was detected on the incoming TOAC.	0
	6	S1BABBLEE[A—D]	**Receive S1 Byte Babbling Event.** Event bit will be set if CNTDS1FRAME[A—D][3:0] consecutive frames pass without a validated S1 byte.	0
	5	SFD[A—D]	**Signal Fail BER Algorithm Delta.** Delta bits indicate a change of state for the signal fail BER algorithm state bits (SF[A—D]). The delta bits clear when read. Their mask bits are SFM[A—D]. Only SFD[A] is valid for STS-48/ STM-16.	0

Register Descriptions (continued)

OHP Registers (continued)

Table 65. Registers 0x0402—0x0409: Delta/Event (COR/W) (continued)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0402, 0404, 0406, 0408	4	SDD[A—D]	**Signal Degrade BER Algorithm Delta.** Delta bit indicates a change of state for the signal degrade BER algorithm state bits (SD[A—D]). The delta bits clear when read. Their mask bits are SDM[A—D]. Only SDD[A] is valid for STS-48/STM-16.	0
	3	OOFD[A—D]	**Receive Out-of-Frame Delta.** Delta bit indicates a change of state for the out-of-frame (OOF[A—D]). The delta bits clear when read. Their mask bits are OOFM[A—D]. In STS-48/STM-16 mode, only OOFD[A] is valid.	0
	2	LOFD[A—D]	**Receive Loss-of-Frame Delta.** Delta bit indicates a change of state for the loss-of-frame (LOF[A—D]) . The delta bits clear when read. Their mask bits are LOFM[A—D]. In STS-48/STM-16 mode, only LOFD[A] is valid.	0
	1	LOSD[A—D]	**Receive Loss-of-Signal Delta.** Delta bit indicates a change of state for the loss-of-signal (LOS[A—D]). The delta bits clear when read. Their mask bits are LOSM[A—D]. In STS-48/STM-16 mode, only LOSD[A] is valid.	0
	0	LOCD[A—D]	**Receive Loss-of-Clock Delta.** Delta bit indicates a change of state for the loss-of-clock (LOC[A—D]). The delta bits clear when read. Their mask bits are LOCM[A—D]. In STS-48/STM-16 mode, only LOCD[A] is valid.	0
0403, 0405, 0407, 0409	15—1	—	**Reserved.** These bits must be written to their reset default value (000000000000000).	000 0000 0000 0000
	0	J0MISE[A—D]	**J0 Mismatch Event.** Their mask bits are J0MISM[A—D]. In STS-48/STM-16 mode, only J0MISE[A] is valid for J0 byte while J0MISE[B—D] are used for Z0 bytes.	0

Register Descriptions (continued)

OHP Registers (continued)

Table 66. Registers 0x040A—0x040D: Receive/Transmit State (RO)

Reset default of registers = 0x000C.

Address (Hex)	Bit #	Name	Function	Reset Default
040A—040D	15	LRDIMON[A—D]	**Line/Multiplex RDI State.** In STS-48/ STM-16 mode, only LRDIMON[A] is valid.	0
	14	LAISMON[A—D]	**Line/Multiplex AIS State.** In STS-48/ STM-16 mode, only LAISMON[A] is valid.	0
	13—7	—	**Reserved.** These bits must be written to their reset default value (0000000).	000 0000
	6	TLRDIINT[A—D]	**Transmit Line RDI Insert State.** State bits for inserting line RDI value into the K2[2:0] bits. In STS-48/STM-16 mode, only TLRDIINT[A] is valid.	0
	5	SF[A—D]	**Signal Fail State.** In STS-48/STM-16 mode, only SF[A] is valid.	0
	4	SD[A—D]	**Signal Degrade State.** In STS-48/STM-16 mode, only SD[A] is valid.	0
	3	OOF[A—D]	**Out-of-Frame.** Active-high out-of-frame state bits. In STS-48/STM-16 mode, only OOF[A] is valid.	1
	2	LOF[A—D]	**Loss-of-Frame.** Active-high loss-of-frame state bits. In STS-48/STM-16 mode, only LOF[A] is valid.	1
	1	LOS[A—D]	**Loss-of-Signal.** Active-high loss-of-signal state bits. In STS-48/STM-16 mode, only LOS[A] is valid.	0
	0	LOC[A—D]	**Loss-of-Clock.** Active-high loss-of-clock state bits. In STS-48/STM-16 mode, only LOC[A] is valid.	0

Register Descriptions (continued)

OHP Registers (continued)

Table 67. Registers 0x040 E, 0x0410, 0x0412, 0x0414: Mask Bits (R/W)

Reset default of registers = 0xFFFF.

Address (Hex)	Bit #	Name	Function	Reset Default
040E, 0410, 0412, 0414	15	LRDIMONM[A—D]	**Line/Multiplex RDI Mask.** A 1 masks the corresponding occurrence of the alarm to the interrupt. In STS-48/STM-16 mode, only LRDIMONM[A] is valid.	1
	14	LAISMONM[A—D]	**Line/Multiplex AIS Mask.** A 1 masks the corresponding occurrence of the alarm to the interrupt. In STS-48/STM-16 mode, only LAISMONM[A] is valid.	1
	13	RAPSBABLEM[A—D]	**APS Babble Mask.** A 1 masks the corresponding occurrence of the alarm to the interrupt. In STS-48/STM-16 mode, only RAPSBABLEM[A] is valid.	1
	12	S1DMON4M[A—D]	**Mask Bits for S1DMON4D When S1MON8 or 4CTL = 1.** A 1 masks the corresponding occurrence of the alarm to the interrupt. In STS-48/STM-16 mode, only S1DMON4LSNM[A] is valid.	1
	11	S1DMON8M[A—D]	**Mask Bits for S1DMON8D.** A 1 masks the corresponding occurrence of the alarm to the interrupt. In STS-48/STM-16 mode, only S1DMON8M[A] is valid.	1
	10	K2DMONM[A—D]	**K2[2:0] Data Monitor Mask.** A 1 masks the corresponding occurrence of the alarm to the interrupt. In STS-48/STM-16 mode, only K2DMONM[A] is valid.	1
	9	K1K2DMONM[A—D]	**K1K2 Data Monitor Mask.** A 1 masks the corresponding occurrence of the alarm to the interrupt. In STS-48/STM-16 mode, only K1K2DMONM[A] is valid.	1
	8	F1DMONM[A—D]	**F1 Data Monitor Mask.** A 1 masks the corresponding occurrence of the alarm to the interrupt. In STS-48/STM-16 mode, only F1DMONM[A] is valid.	1
	7	TTOAC_PERRM[A—D]	**Transmit TOAC Parity Error Mask.** A 1 masks the corresponding occurrence of the alarm to the interrupt. All 4 bits are valid in every mode.	1

Register Descriptions (continued)

OHP Registers (continued)

Table 67. Registers 0x040 E, 0x0410, 0x0412, 0x0414: Mask Bits (R/W) (continued)

Reset default of registers = 0xFFFF.

Address (Hex)	Bit #	Name	Function	Reset Default
040E, 0410, 0412, 0414	6	S1BABBLEM[A—D]	**S1 Babbling Mask.** A 1 masks the corresponding occurrence of the alarm to the interrupt. In STS-48/STM-16 mode, only S1BABBLEM[A] is valid.	1
	5	SFM[A—D]	**Signal Fail Mask.** A 1 masks the corresponding occurrence of the alarm to the interrupt. In STS-48/STM-16 mode, only SFM[A] is valid.	1
	4	SDM[A—D]	**Signal Degrade Mask.** A 1 masks the corresponding occurrence of the alarm to the interrupt. In STS-48/STM-16 mode, only SDM[A] is valid.	1
	3	OOFM[A—D]	**Out-of-Frame Mask.** A 1 masks the corresponding occurrence of the alarm to the interrupt. In STS-48/STM-16 mode, only OOFM[A] is valid.	1
	2	LOFM[A—D]	**Loss-of-Frame Mask.** A 1 masks the corresponding occurrence of the alarm to the interrupt. In STS-48/STM-16 mode, only LOFM[A] is valid.	1
	1	LOSM[A—D]	**Loss-of-Signal Mask.** A 1 masks the corresponding occurrence of the alarm to the interrupt. In STS-48/STM-16 mode, only LOSM[A] is valid.	1
	0	LOCM[A—D]	**Loss-of-Clock Mask.** A 1 masks the corresponding occurrence of the alarm to the interrupt. In STS-48/STM-16 mode, only LOCM[A] is valid.	1

Table 68. Registers 0x040F, 0x0411, 0x0413, 0x0415: Mask Bits (R/W)

Reset default of registers = 0x8001.

040F, 0411, 0413, 0415	15	INTM[A—D]	**Interrupt Mask.** The corresponding occurrence of a 1 masks the alarm to the interrupt.	1
	14—1	—	**Reserved.** These bits must be written to their reset default value (00000000000000).	00 0000 0000 0000
	0	J0MISM[A—D]	**J0 Mismatch Mask.** The corresponding occurrence of a 1 masks the alarm to the interrupt.	1

Register Descriptions (continued)

OHP Registers (continued)

Table 69. Registers 0x0416—0x0419: Toggles (R/W)

Reset default of registers = 0x0000.

Note: These registers must be cleared by writing them to 0 following access.

Address (Hex)	Bit #	Name	Function	Reset Default
0416—0419	15—5	—	**Reserved.** These bits must be written to their reset default value (00000000000).	000 0000 0000
	4	TA1A2ERREN[A—D]	**Transmit A1/A2 Error Enable.** Enable signal to start the insertion of A2 errors in the outgoing frame. The number of consecutive errors is controlled by TA1A2ERRINS[4:0]. TA1A2ERREN[A] is valid in STS-48/STM-16 mode.	0
	3	SFCLEAR[A—D]	**Signal Fail Clear.** Allows the signal fail algorithm to be forced into the normal state.	0
	2	SFSET[A—D]	**Signal Fail Set.** Allows the signal fail algorithm to be forced into the failed state.	0
	1	SDCLEAR[A—D]	**Signal Degrade Clear.** Allows the signal degrade algorithm to be forced into the normal state.	0
	0	SDSET[A—D]	**Signal Degrade Set.** Allows the signal degrade algorithm to be forced into the degraded state.	0

Table 70. Registers 0x041A, 0x041C, 0x041E, 0x0420: Continuous N Times Detect (CNTD) Values (R/W)

Reset default of registers = 0x3333.

Address (Hex)	Bit #	Name	Function	Reset Default
041A, 041C, 041E, 0420	15—12	CNTDK2[A—D][3:0]	**Continuous N Times Detect for K2[2:0] Byte.** The valid range for these bits is 0x2—0xF. Invalid values will be mapped to a value of 0x1. In STS-48/STM-16 mode, CNTDK2[A] is valid.	0x3
	11—8	CNTDK1K2[A—D][3:0]	**Continuous N Times Detect for APS (K1, K2[7:3]) Byte.** The valid range for these bits is 0x2—0xF. Invalid values will be mapped to a value of 0x1. In STS-48/STM-16 mode, CNTDK1K2[A] is valid.	0x3
	7—4	CNTDF1[A—D][3:0]	**Continuous N Times Detect for F1 Byte.** The valid range for these bits is 0x2—0xF. Invalid values will be mapped to a value of 0x1. In STS-48/STM-16 mode, CNTDF1[A] is valid.	0x3
	3—0	CNTDJ0Z0[A—D][3:0]	**Continuous N Times Detect for J0Z0 Bytes.** The valid range for these bits is 0x2—0xF. Invalid values will be mapped to a value of 0x1. In STS-48/STM-16 mode, CNTDJ0Z0[A] is valid.	0x3

Register Descriptions (continued)

OHP Registers (continued)

Table 71. Registers 0x041B, 0x041D, 0x041F, 0x0421: Continuous N Times Detect (CNTD) Values (R/W)

Reset default of registers = 0x053C.

Address (Hex)	Bit #	Name	Function	Reset Default
041B, 041D, 041F, 0421	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—8	CNTDS1FRAME [A—D][3:0]	**Continuous N Times Detect for S1 Byte Babbling.** The valid range for these bits is 0x2—0xF. Invalid values will be mapped to a value of 0x1. In STS-48/STM-16 mode, CNTDS1FRAME[A] is valid.	0x5
	7—4	CNTDS1[A—D][3:0]	**Continuous N Times Detect for S1 Byte.** The valid range for these bits is 0x2—0xF. Invalid values will be mapped to a value of 0x1. In STS-48/STM-16 mode, CNTDS1[A] is valid.	0x3
	3—0	CNTDK1K2FRAME [A—D][3:0]	**Continuous N Times Detect for APS Frame.** The valid range for these bits is 0x2—0xF. Invalid values will be mapped to a value of 0x1. In STS-48/STM-16 mode, CNTDK1K2FRAME[A] is valid.	0xC

Register Descriptions (continued)

OHP Registers (continued)

Table 72. Registers 0x0422—0x042D: Receive Control (R/W)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0422, 0424, 0426, 0428	15—14	J0MONMODE[A—D][1:0]	**J0 Monitoring Mode.** There are four modes. 00 = The OHP will latch the value of the J0 byte every frame for a total of 16 bytes. The OHP will compare the incoming J0 byte with the next expected value (the expected value is obtained by cycling through the previously stored 16 received bytes in round robin fashion) and set the event bit if different. 01 = This is the SONET framing mode. The hardware looks for 0x0D followed by 0x0A to indicate that the next byte is the first byte of the path trace message. The J0 byte is continuously written into J0DMON with the first byte residing at the first address. If any received byte does not match the previously received byte for its location, then the event bit is set. 10 = This is the SDH framing mode. The hardware looks for the byte with the MSB set to 1, which indicates that the next byte is the second byte of the message. The rest of the operation is the same as the SONET framing mode. 11 = A new J0 byte J0DMON[0][7:0] will be detected after CNTDJ0Z0[3:0] consecutive consistent occurrences of a new pattern in the J0 overhead byte. Any changes to this byte are reported to J0MISE and J0MISM. These event bits will act as delta bits indicating a change of state for the J0DMON[0][7:0].	00
	13	M1B7IGNORE[A—D]	**Bit 7 of M1 Byte Ignore.** Bit 7 of M1 byte will be ignored if M1B7IGNORE is set to 1 for that channel. Only M1B7IGNORE[A] is valid for STS-48/STM-16.	0
	12	LAISINS[A—D]	**AIS Software Insertion.** Active-high for AIS insertion. In STS-48/STM-16 mode, only LAISINS[A] is valid.	0
	11	LOF_AISINH[A—D]	**Loss-of-Frame AIS Inhibit.** When set to logic 1, the AIS insertion will be inhibited in case of loss-of-frame.	0
	10	OOF_AISINH[A—D]	**Out-of-Frame AIS Inhibit.** When set to logic 1, the AIS insertion will be inhibited in case of out-of-frame.	0

Register Descriptions (continued)

OHP Registers (continued)

Table 72. Registers 0x0422—0x042D: Receive Control (R/W) (continued)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0422, 0424, 0426, 0428	9	LOS_AISINH[A—D]	**Loss-of-Signal AIS Inhibit.** When set to logic 1, the AIS insertion will be inhibited in case of loss-of-signal.	0
	8	SFB1B2SEL[A—D]	**Signal Fail B1/B2 Error Count Select.** When set to logic 0, the B1 errors will be used by the signal fail error rate algorithm; otherwise, B2 errors are used.	0
	7	SDB1B2SEL[A—D]	**Signal Degrade B1/B2 Error Count Select.** When set to logic 0, the B1 errors will be used by the signal degrade error rate algorithm; otherwise, B2 errors are used.	0
	6	CNTDB1SEL[A—D]	**Reset CNTD Counters on B1 Error.** Active-high control bits to reset continuous N time detect counters upon received B1 errors. Only CNTDB1SEL[0] is valid for STS-48/STM-16.	0
	5	S1MON8_OR_4CTL[A—D]	**S1 Byte or Nibble.** When set to logic 1, the S1 byte will be monitored as two nibbles. Otherwise, it is treated as a byte. Only S1MON8or4CTL[A] is valid for STS-48/STM-16.	0
	4	K1K2_2_OR_1[A—D]	**K1 and K2 Treated as 2 Registers or 1.** When a bit is set to 1, the K1 and K2 bytes will be treated as one 16-bit register. Otherwise, they will be treated as two registers of size 13 (K1[7:0] and K2[7:3]) and 3 (K2[2:0]). K1K2_2_OR_1[A] is valid for STS-48/STM-16.	0
	3	B2BITBLKCNT[A—D]	**B2 Error Count in Bit or Block.** When set to 0, B2 check logic will count bit errors; otherwise, it counts block errors. Only B2BITBLKCNT[A] is valid for STS-48/STM-16.	0
	2	DSCRINH[A—D]	**Descramble Inhibit Control.** When a bit is set to 1, the descrambler for that is disabled. In STS-48/STM-16 mode, all 4 bits need to be set to same value.	0
	1	B1BITBLKCNT[A—D]	**B1 Error Count in Bit or Block.** When set to 0, B1 check logic will count bit errors; otherwise, it counts block errors. Only B1BITBLKCNT[A] is valid for STS-48/STM-16.	0
	0	ROH_BYPASS[A—D]	**Receive Overhead Bypass.** Control bit, when set to 1, causes the received data to pass through the block retimed. In STS-48/STM-16 mode, all 4 bits need to be set to same value.	0

Register Descriptions (continued)

OHP Registers (continued)

Table 72. Registers 0x0422—0x042D: Receive Control (R/W) (continued)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0423, 0425, 0427, 0429	15	M1BITBLKCNT[A—D]	**M1 Error Count in Bit or Block.** When set to 0, M1 check logic will count bit errors. When set to 1, block errors are counted. Only M1BITBLKCNT[C] is valid for STS-48/STM-16.	0
	14—13	—	**Reserved.** These bits must be written to their reset default value (00).	00
	12—0	LOSDETCNT[A—D][12:0]	**Loss-of-Signal Detection Count.** Set the number of consecutive all-zeros/-ones pattern detected to declare receive LOS state for each channel. The time scale is in steps of 8 (for STS-3/STM-1 and STS-12/STM-4) or 32 (STS-48/STM-16) bits at a time. Only LOSDETCNT[A][12:0] is valid for STS-48/ STM-16.	0 0000 0000 0000
042A	15—14	RREFSEL[1:0]	**Receive Reference Sync Select.** Select reference output from channel A (00), B (01), C (10), and D (11).	00
	13	RREF_EN	**Receive Reference Sync Enable.** When set to 0, the receive 8 kHz (50% duty cycle) sync output, RxREF (pin AK3), is placed in the high-impedance state.	0
	12—4	—	**Reserved.** These bits must be written to their reset default value (000000000).	0000 00000
	3	RTOACSINH[A]	**Receive TOAC Frame (Sync) Inhibit Channel A.** When set to 1, the TOAC sync output, RxTOHF (pin AK4), is placed in the high-impedance state.	0
	2	RTOACCINH[A]	**Receive TOAC Clock Inhibit Channel A.** When set to 1, the TOAC clock output, RxTOHCK (pin AK5), is placed in the high-impedance state.	0
	1	RTOACDINH[A]	**Receive TOAC Data Inhibit Channel A.** When set to 1, the TOAC data output, RxTOHD (pin AL2), is placed in the high-impedance state.	0
	0	RTOAC_OEPINS[A]	**Receive TOAC Odd or Even Parity Insert Channel A.** When set to 1, the output TOAC parity bit is even. When set to 0, the parity is odd.	0

Register Descriptions (continued)

OHP Registers (continued)

Table 72. Registers 0x0422—0x042D: Receive Control (R/W) (continued)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
042B—042D	15—4	—	**Reserved.** These bits must be written to their reset default value (0x000).	0x000
	3	RTOACSINH[B—D]	**Receive TOAC Frame (Sync) Inhibit Channels B—D.** When set to 1, the TOAC sync output, RxTOHF (pins AL3, AN5, AP6), is placed in the high-impedance state.	0
	2	RTOACCINH[B—D]	**Receive TOAC Clock Inhibit Channels B—D.** When set to 1, the TOAC clock output, RxTOHCK (pins AL4, AL6, AL7), is placed in the high-impedance state.	0
	1	RTOACDINH[B—D]	**Receive TOAC Data Inhibit Channels B—D.** When set to 1, the TOAC data output, RxTOHD (pins AM5, AM6, AN7), is placed in the high-impedance state.	0
	0	RTOAC_OEPINS[B—D]	**Receive TOAC Odd or Even Parity Insert Channels B—D.** When set to 1, the output TOAC parity bit is even. When set to 0, the parity is odd.	0

Register Descriptions (continued)

OHP Registers (continued)

Table 73. Registers 0x042E, 0x0430, 0x0432, 0x0434: Transmit Control Registers (R/W)

Reset default of registers = 0x0003.

Address (Hex)	Bit #	Name	Function	Reset Default
042E	15	TTOACINH	**Transmit TOAC Clock and Sync Inhibit Channel A.** When set to 1, the transmit TOAC clock and sync are placed in the high-impedance state.	0
	14	TJ0INS[A]	**Transmit J0 Insert Control Channel A.** Control bit, when set to a logic 1, inserts the value in TJ0DINS[A—D][16:1][7:0] into the outgoing J0 bytes; otherwise, the insert value depends on TTOAC_J0[A—D] registers. TJ0INS[A] is valid in STS-48/STM-16 mode.	0
	13	TTOAC_J0[A]	**Transmit TOAC J0 Byte Control Channel A.** Control bit, when set to logic 0, causes the default value 00000000 for SONET or 11111111 for SDH to be inserted into the J0 byte in the transmit frame. Setting this bit to logic 1 causes the TTOAC value to be inserted into the J0 byte. TJ0INS (bit 14 above) has higher priority than TTOAC_J0 if both are set to 1. TTOAC_J0[A] is valid for STS-48/STM-16 mode.	0
	12	TTOAC_OEPMON[A]	**Transmit TOAC Odd or Even Parity Monitor Channel A.** When set to 1, even parity is checked for transmit TOAC channels; otherwise, odd parity is checked.	0
	11	TTOAC_INS[A]	**Transmit TOAC Byte Control Channel A.** Control bit, when set to logic 0, causes the default value 00000000 for SONET or 11111111 for SDH to be inserted into those overhead bytes within the transmit frame that do not have all specific insert control bits. Setting these bits to logic 1 causes the TTOAC value to be inserted into those overhead bytes not having specific insert control bits. TTOAC_INS[A] is valid for STS-48/STM-16 mode.	0
	10	TTOAC_E2[A]	**Transmit TOAC E2 Byte Control Channel A.** Control bit, when set to logic 0, causes the default value to be inserted into the E2 byte in the transmit frame. Setting these bits to logic 1 causes the TTOAC value to be inserted into the E2 byte. TTOAC_E2[A] is valid for STS-48/STM-16 mode.	0

Register Descriptions (continued)

OHP Registers (continued)

Table 73. Registers 0x042E, 0x0430, 0x0432, 0x0434: Transmit Control Registers (R/W) (continued)

Reset default of registers = 0x0003.

Address (Hex)	Bit #	Name	Function	Reset Default
042E	9	TTOAC_S1[A]	**Transmit TOAC S1 Byte Control Channel A.** Control bit, when set to logic 0, causes the default value to be inserted into the S1 byte in the transmit frame. Setting these bits to logic 1 causes the TTOAC value to be inserted into the S1 byte. TTOAC_S1[A] is valid for STS-48/ STM-16 mode.	0
	8	TTOAC_D4TO12[A]	**Transmit TOAC D4 to D12 Byte Control Channel A.** Control bit, when set to logic 0, causes the default value to be inserted into the D4 to D12 bytes in the transmit frame. Setting these bits to logic 1 causes the TTOAC value to be inserted into the D4 to D12 bytes. TTOAC_D4TO12[A] is valid for STS-48/STM-16 mode.	0
	7	TTOAC_D1TO3[A]	**Transmit TOAC D1 to D3 Byte Control Channel A.** Control bit, when set to logic 0, causes the default value to be inserted into the D1 to D3 bytes in the transmit frame. Setting these bits to logic 1 causes the TTOAC value to be inserted into the D1 to D3 bytes. TTOAC_D1TO3[A] is valid for STS-48/STM-16 mode.	0
	6	TTOAC_F1[A]	**Transmit TOAC F1 Byte Control Channel A.** Control bit, when set to logic 0, causes the default value to be inserted into the F1 byte in the transmit frame. Setting these bits to logic 1 causes the TTOAC value to be inserted into the F1 byte. TTOAC_F1[A] is valid for STS-48/ STM-16 mode.	0
	5	TTOAC_E1[A]	**Transmit TOAC E1 Byte Control Channel A.** Control bit, when set to logic 0, causes the default value to be inserted into the E1 byte in the transmit frame. Setting this bit to logic 1 causes the TTOAC value to be inserted into the E1 byte. TTOAC_E1[A] is valid for STS-48/ STM-16 mode.	0
	4	TAPSBABBLEINS[A]	**Transmit APS Babble Insert Channel A.** Control bit, when set to 1, causes an inconsistent APS byte (K1[7:0], K2[7:3]) to be inserted into the outgoing STS-M frame until this register is reset to 0.	0

Register Descriptions (continued)

OHP Registers (continued)

Table 73. Registers 0x042E, 0x0430, 0x0432, 0x0434: Transmit Control Registers (R/W) (continued)

Reset default of registers = 0x0003.

Address (Hex)	Bit #	Name	Function	Reset Default
042E	3	TM1_ERR_INS[A]	**Transmit M1 Error Insert Channel A.** Once this register is set to 1, an error will be inserted continuously into the outgoing M1 byte until this register is reset to 0. In STS-48/STM-16 mode, only TM1_ERR_INS[C] is valid.	0
	2	TM1_REIL_INH[A]	**Transmit M1 REI-L Inhibit Channel A.** Active-high to inhibit automatic insertion of REI-L (MS-REI). In STS-48/STM-16 mode, only TM1_REIL_INH[C] is valid.	0
	1	TF1INS[A]	**Transmit F1 Insert Control Channel A.** Control bit, when set to a logic 1, inserts the value in TF1DINS[7:0] into the outgoing F1 byte in the STS-M frame; otherwise, the insert value depends on TTOAC_F1 register. TF1INS[A] is valid in STS-48/STM-16 mode.	1
	0	TS1INS[A]	**Transmit S1 Insert Control Channel A.** Control bit, when set to a logic 1, inserts the value in TS1DINS[7:0] into the outgoing S1 byte in the STS-M frame; otherwise, the insert value depends on TTOAC_S1 register. TS1INS[A] is valid in STS-48/STM-16 mode.	1

Register Descriptions (continued)

OHP Registers (continued)

Table 74. Registers 0x042F, 0x0431, 0x0433, 0x0435: Transmit Control Registers (R/W)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
042F, 0431, 0433, 0435	15—11	TA1A2ERRINS[A—D][4:0]	**Number of Consecutive Frames with A2 Error Insertion.** These bits specify the number of consecutive frames to be inserted with a frame error of the first A2 byte.	0x00
	10	TOH_BYPASS[A—D]	**Transmit Overhead Bypass.** Control bit, when set to 1, causes the frame from PT pass through untouched. In STS-48/STM-16 mode, all 4 bits need to be set to same value.	0
	9	SCRINH[A—D]	**Scramble Inhibit.** When set to high, the scrambling is inhibited. In STS-48/STM-16 mode, all 4 bits need to be set to same value.	0
	8	TB1ERRINS[A—D]	**Transmit B1 Error Insertion.** When set to high, the B1 output will be inverted. For STS-48/STM-16, only TB1ERRINS[A] is valid.	0
	7	TB2ERRINS[A—D]	**Transmit B2 Error Insertion.** When set to high, all B2 bytes in that channel will be inverted. All 4 bits are valid in STS-48/STM-16 mode.	0
	6	TIMER_LRDIINH[A—D]	**Transmit 20-Frame Line RDI Inhibit.** Control bit, when set to logic high, inhibits the requirement of minimum 20 frame RDI insertion.	0
	5	TSF_LRDIINH[A—D]	**Transmit Signal Fail Line RDI Inhibit.** Active-high.	0
	4	TLAISMON_LRDIINH [A—D]	**Transmit Line-AIS-Monitored Line RDI Inhibit.** Active-high.	0
	3	TLOF_LRDIINH[A—D]	**Transmit Loss-of-Frame Line RDI Inhibit.** Active-high.	0
	2	TOOF_LRDIINH[A—D]	**Transmit Out-of-Frame Line RDI Inhibit.** Active-high.	0
	1	TLOS_LRDIINH[A—D]	**Transmit Loss-of-Signal Line RDI Inhibit.** Active-high.	0
	0	TLOC_LRDIINH[A—D]	**Transmit Loss-of-Clock Line RDI Inhibit.** Control bit, when set to a logic 1, causes the associated failure not to contribute to the automatic insertion of RDI-L; otherwise, the associated alarm contributes to the generation of RDI-L.	0

Register Descriptions (continued)

OHP Registers (continued)

Table 75. Registers 0x0430, 0x0432, 0x0434: Transmit Control Registers (R/W)

Reset default of registers = 0x0003.

Address (Hex)	Bit #	Name	Function	Reset Default
0430, 0432, 0434	15	—	**Reserved.** This bit must be written to its reset default value (0).	0
	14	TJ0INS[B—D]	**Transmit J0 Insert Control Channels [B—D].** Control bit, when set to a logic 1, insert the value in TJ0DINS[A—D][16:1][7:0] into the outgoing J0 bytes; otherwise, the insert value depends on TTOAC_J0[A—D] registers. TJ0INS[A] is valid in STS-48/STM-16 mode.	0
	13	TTOAC_J0[B—D]	**Transmit TOAC J0 Byte Control Channels [B—D].** Control bit, when set to logic 0, causes the default value 00000000 for SONET or 11111111 for SDH to be inserted into the J0 byte in the transmit frame. Setting this bit to logic 1 causes the TTOAC value to be inserted into the J0 byte. TJ0INS (bit 14 above) has higher priority than TTOAC_J0 if both are set to 1. TTOAC_J0[A] is valid for STS-48/STM-16 mode.	0
	12	TTOAC_OEPMON[B—D]	**Transmit TOAC Odd or Even Parity Monitor Channels [B—D].** When set to 1, even parity is checked for transmit TOAC channels; otherwise, odd parity is checked.	0
	11	TTOAC_INS[B—D]	**Transmit TOAC Byte Control Channels [B—D].** Control bit, when set to logic 0, causes the default value 00000000 for SONET or 11111111 for SDH to be inserted into those overhead bytes within the transmit frame that do not have all specific insert control bits. Setting this bit to logic 1 causes the TTOAC value to be inserted into those overhead bytes not having specific insert control bits. TTOAC_INS[A] is valid for STS-48/STM-16 mode.	0
	10	TTOAC_E2[B—D]	**Transmit TOAC E2 Byte Control Channels [B—D].** Control bit, when set to logic 0, causes the default value to be inserted into the E2 byte in the transmit frame. Setting this bit to logic 1 causes the TTOAC value to be inserted into the E2 byte. TTOAC_E2[A] is valid for STS-48/STM-16 mode.	0

Register Descriptions (continued)

OHP Registers (continued)

Table 75. Registers 0x0430, 0x0432, 0x0434: Transmit Control Registers (R/W) (continued)

Reset default of registers = 0x0003.

Address (Hex)	Bit #	Name	Function	Reset Default
0430, 0432, 0434	9	TTOAC_S1[B—D]	**Transmit TOAC S1 Byte Control Channels [B—D].** Control bit, when set to logic 0, causes the default value to be inserted into the S1 byte in the transmit frame. Setting this bit to logic 1 causes the TTOAC value to be inserted into the S1 byte. TTOAC_S1[A] is valid for STS-48/ STM-16 mode.	0
	8	TTOAC_D4TO12[B—D]	**Transmit TOAC D4 to D12 Byte Control Channels [B—D].** Control bit, when set to logic 0, causes the default value to be inserted into the D4 to D12 bytes in the transmit frame. Setting this bit to logic 1 causes the TTOAC value to be inserted into the D4 to D12 bytes. TTOAC_D4TO12[A] is valid for STS-48/STM-16 mode.	0
	7	TTOAC_D1TO3[B—D]	**Transmit TOAC D1 to D3 Byte Control Channels [B—D].** Control bit, when set to logic 0, causes the default value to be inserted into the D1 to D3 bytes in the transmit frame. Setting this bit to logic 1 causes the TTOAC value to be inserted into the D1 to D3 bytes. TTOAC_D1TO3[A] is valid for STS-48/STM-16 mode.	0
	6	TTOAC_F1[B—D]	**Transmit TOAC F1 Byte Control Channels [B—D].** Control bit, when set to logic 0, causes the default value to be inserted into the F1 byte in the transmit frame. Setting this bit to logic 1 causes the TTOAC value to be inserted into the F1 byte. TTOAC_F1[A] is valid for STS-48/ STM-16 mode.	0
	5	TTOAC_E1[B—D]	**Transmit TOAC E1 Byte Control Channels [B—D].** Control bit, when set to logic 0, causes the default value to be inserted into the E1 byte in the transmit frame. Setting this bit to logic 1 causes the TTOAC value to be inserted into the E1 byte. TTOAC_E1[A] is valid for STS-48/ STM-16 mode.	0

Register Descriptions (continued)

OHP Registers (continued)

Table 75. Registers 0x0430, 0x0432, 0x0434: Transmit Control Registers (R/W) (continued)

Reset default of registers = 0x0003.

Address (Hex)	Bit #	Name	Function	Reset Default
0430, 0432, 0434	4	TAPSBABBLEINS[B—D]	**Transmit APS Babble Insert Channels [B—D].** Control bit, when set to 1, causes an inconsistent APS byte (K1[7:0], K2[7:3]) to be inserted into the outgoing STS-M frame until this register is reset to 0.	0
	3	TM1_ERR_INS[B—D]	**Transmit M1 Error Insert [B—D].** Once this register is set to 1, an error will be inserted continuously into the outgoing M1 byte until this register is reset to 0. In STS-48/STM-16 mode, only TM1_ERR_INS[C] is valid.	0
	2	TM1_REIL_INH[B—D]	**Transmit M1 REI-L Inhibit Channel [B—D].** Active-high to inhibit automatic insertion of REI-L (MS-REI). In STS-48/STM-16 mode, only TM1_REIL_INH[C] is valid.	0
	1	TF1INS[B—D]	**Transmit F1 Insert Control [B—D].** Control bit, when set to a logic 1, inserts the value in TF1DINS[7:0] into the outgoing F1 byte in the STS-M frame; otherwise, the insert value depends on TTOAC_F1 register. TF1INS[A] is valid in STS-48/STM-16 mode.	1
	0	TS1INS[B—D]	**Transmit S1 Insert Control [B—D].** Control bit, when set to a logic 1, inserts the value in TS1DINS[7:0] into the outgoing S1 byte in the STS-M frame; otherwise, the insert value depends on TTOAC_S1 register. TS1INS[A] is valid in STS-48/STM-16 mode.	1

Register Descriptions (continued)

OHP Registers (continued)

Table 76. Registers 0x0436—0x0439: Transmit Control Registers (R/W)

Reset default of registers = 0xC000.

Address (Hex)	Bit #	Name	Function	Reset Default
0436—0439	15	TAPSINS[A—D]	**Transmit APS Software Insert.** When set to 1, the value in registers TK1DINS[7:0] and TK2DINS[7:3] will be inserted into K1[7:0] and K2[7:3] in the transmit frame. When set to 0, a value of all zeros will be inserted.	1
	14	TK2SINS[A—D]	**Transmit K2 Software Insert.** When set to logic 1, the value in registers TK2DINS[2:0] will be inserted into K2[2:0] in the transmit frame; otherwise, hardware insert is enabled for RDI-L (110) insertion.	1
	13—12	—	**Reserved.** These bits must be written to their reset default value (00).	00
	11—0	TAISLINS[A—D][11:0]	**Force Line AIS in the Selected Output Time Slot.** Active-high. For STS-3/STM-1, the index [0:2] corresponds to time slot 1-2-3; for STS-12/ STM-4, the index[0:11] corresponds to time slot 1-4-7-10-2-5-8-11-3-6-9-12; and for STS-48/ STM-16, the index [A][0:11] is for time slot 1-13-25-37-2-14-26-38-3-15-27-39, [B][0:11] for 4-16-28-40-5-17-29-41-6-18-30-42, [C][0:11] for 7-19-31-43-8-20-32-44-9-21-33-45, and [D][0:11] for 10-22-34-46-11-23-35-47-12-24-36-48.	0x000

Table 77. Registers 0x043A—0x0451: Signal Degrade BER Algorithm Parameters (R/W)

Reset default of registers = 0x0000.

Notes: SDNSSET[A—D][2:0] are located in registers 0x043B, 0x043D, 0x043F, and 0x0441, respectively.
SDNSCLEAR[A—D][2:0] are located in registers 0x0447, 0x0449, 0x044B, and 0x044D, respectively.

Address (Hex)	Bit #	Name	Function	Reset Default
043A, 043C, 043E, 0440	15—0	SDNSSET[A—D][18:3]	**Signal Degrade Ns Set [18:3].** Number of frames in a monitoring block for SD.	0x0000
043B, 043D, 043F, 0441	15	—	**Reserved.** This bit must be written to its reset default value (0).	0
	14—7	SDMSET[A—D][7:0]	**Signal Degrade M Set.** Threshold of the number of bad monitoring blocks in an observation interval. If the number of bad blocks is above this threshold, then signal degrade (SD) is set.	0000 0000
	6—3	SDLSET[A—D][3:0]	**Signal Degrade L Set.** Error threshold for determining if a monitoring block is bad.	0x0
	2—0	SDNSSET[A—D][2:0]	**Signal Degrade Ns Set [2:0].** Number of frames in a monitoring block for SD.	000

Register Descriptions (continued)

OHP Registers (continued)

Table 77. Registers 0x043A—0x0451: Signal Degrade BER Algorithm Parameters (R/W) (continued)

Reset default of registers = 0x0000.

Notes: SDNSSET[A—D][2:0] are located in registers 0x043B, 0x043D, 0x043F, and 0x0441, respectively.
SDNSCLEAR[A—D][2:0] are located in registers 0x0447, 0x0449, 0x044B, and 0x044D, respectively.

Address (Hex)	Bit #	Name	Function	Reset Default
0442—0445	15—0	SDBSET[A—D][15:0]	**Signal Degrade B Set.** Number of monitoring blocks.	0x0000
0446, 0448, 044A, 044C	15—0	SDNSCLEAR[A—D][18:3]	**Signal Degrade Ns Clear [18:3].** Number of frames in a monitoring block for SD.	0x0000
0447, 0449, 044B, 044D	15	—	**Reserved.** This bit must be written to its reset default value (0).	0
	14—7	SDMCLEAR[A—D][7:0]	**Signal Degrade M Clear.** Threshold of the number of bad monitoring blocks in an observation interval. If the number of bad blocks is below this threshold, then SD (signal degrade) is cleared.	0000 0000
	6—3	SDLCLEAR[A—D][3:0]	**Signal Degrade L Clear.** Error threshold for determining if a monitoring block is bad.	0x0
	2—0	SDNSCLEAR[A—D][2:0]	**Signal Degrade Ns Clear[2:0].** Number of frames in a monitoring block for SD.	000
044E—0451	15—0	SDBCLEAR[A—D][15:0]	**Signal Degrade B Clear.** Number of monitoring blocks.	0x0000

Table 78. Registers 0x0452—0x0469: Signal Fail BER Algorithm Parameters (R/W)

Reset default of registers = 0x0000.

Notes: SFNSSET[A—D][2:0] are located in registers 0x0453, 0x0455, 0x0457, and 0x0459, respectively.
SDNSCLEAR[A—D][2:0] are located in registers 0x045F, 0x0461, 0x0463, 0x0465, respectively.

Address (Hex)	Bit #	Name	Function	Reset Default
0452, 0454, 0456, 0458	15—0	SFNSSET[A—D][18:3]	**Signal Fail Ns Set [18:3].** Number of frames in a monitoring block for SF.	0x0000
0453, 0455, 0457, 0459	15	—	**Reserved.** This bit must be written to its reset default value (0).	0
	14—7	SFMSET[A—D][7:0]	**Signal Fail M Set.** Threshold of the number of bad monitoring blocks in an observation interval. If the number of bad blocks is above this threshold, then SF (signal fail) is set. (See Table 79, page 172, for register settings in terms of corresponding BER.)	0000 0000
	6—3	SFLSET[A—D][3:0]	**Signal Fail L Set.** Error threshold for determining if a monitoring block is bad. (See Table 79, page 172, for register settings in terms of corresponding BER.)	0x0
	2—0	SFNSSET[A—D][2:0]	**Signal Fail Ns Set [2:0].** Number of frames in a monitoring block for SF. (See Table 79, page 172, for register settings in terms of corresponding BER.)	000

Register Descriptions (continued)

OHP Registers (continued)

Table 78. Registers 0x0452—0x0469: Signal Fail BER Algorithm Parameters (R/W) (continued)

Reset default of registers = 0x0000.

Notes: SFNSSET[A—D][2:0] are located in registers 0x0453, 0x0455, 0x0457, and 0x0459, respectively.
SDNSCLEAR[A—D][2:0] are located in registers 0x045F, 0x0461, 0x0463, 0x0465, respectively.

Address (Hex)	Bit #	Name	Function	Reset Default
045A—045D	15—0	SFBSET[A—D][15:0]	**Signal Fail B Set.** Number of monitoring blocks. (See Table 79, page 172, for register settings in terms of corresponding BER.)	0x0000
045E, 0460, 0462, 0464	15—0	SFNSCLEAR[A—D][18:3]	**Signal Fail Ns Clear [18:3].** Number of frames in a monitoring block for SF.	0x0000
045F, 0461, 0463, 0465	15	—	**Reserved.** This bit must be written to its reset default value (0).	0
	14—7	SFMCLEAR[A—D][7:0]	**Signal Fail M Clear.** Threshold of the number of bad monitoring blocks in an observation interval. If the number of bad blocks is below this threshold, then SF (signal fail) is cleared.	0x00
	6—3	SFLCLEAR[A—D][3:0]	**Signal Fail L Clear.** Error threshold for determining if a monitoring block is bad.	0x0
	2—0	SFNSCLEAR[A—D][2:0]	**Signal Fail Ns Clear [2:0].** Number of frames in a monitoring block for SF.	000
0466—0469	15—0	SFBCLEAR[A—D][15:0]	**Signal Fail B Clear.** Number of monitoring blocks.	0x0000

Table 79. Values of SFNSSET[A—D][18:0], SFMSET[A—D][7:0], SFLSET[A—D][3:0], SFBSET[A—D][15:0] in Terms of Equivalent BER

Note: See the section BER Check, page 51, for details.

BER	SFNSSET [A—D][18:0]	SFMSET [A—D][7:0]	SFLSET [A—D][3:0]	SFBSET [A—D][15:0]
10^{-3}	0x00027	0x04	0xC	0x00EF
10^{-4}	0x00027	0xE5	0x1	0x012B
10^{-5}	0x00027	0x16	0x1	0x012B
10^{-6}	0x0018F	0x16	0x1	0x012B
10^{-7}	0x0018F	0x04	0x1	0x012B
10^{-8}	0x0018F	0x04	0x1	0x05DB
10^{-9}	0x61A7F	0x00	0x1	0x0001

Register Descriptions (continued)

OHP Registers (continued)

Table 80. Registers 0x046A—0x047D: B1, B2, M1 Error Count (RO)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
046A—046D	15—0	B1ECNT[A—D][15:0]	**B1 Error Count.** The value of the internal running counter is transferred into this holding register at the 0-to-1 transition of PMRST signal. The counter is then reset to 0.	0x0000
046E, 0470, 0472, 0474	15—6	—	**Reserved.** These bits must be written to their reset default value (0000000000).	00 0000 0000
	5—0	B2ECNT[A—D][21:16]	**B2 Error Count [21:16].** The value of the internal running counter is transferred into this holding register at the 0-to-1 transition of PMRST signal. The counter is then reset to 0.	000000
046F, 0471, 0473, 0475	15—0	B2ECNT[A—D][15:0]	**B2 Error Count [15:0].** Same description as above.	0x0000
0476, 0478, 047A, 047C	15—5	—	**Reserved.** These bits must be written to their reset default value (00000000000).	000 0000 0000
	4—0	M1ECNT[A—D][20:16]	**M1 Error Count [21:16].** The value of the internal running counter is transferred into this holding register at the 0-to-1 transition of PMRST signal. The counter is then reset to 0.	00000
0477, 0479, 047B, 047D	15—0	M1ECNT[A—D][15:0]	**M1 Error Count [15:0].** Same description as above.	0x0000

Table 81. Registers 0x047E—0x0485: Transmit F1, S1, K2, K1 OH Insert Value (R/W)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
047E, 0480, 0482, 0484	15—8	TF1DINS[A—D][7:0]	**Transmit F1 Byte Value.** Register value is inserted into the transmit F1 byte.	0x00
	7—0	TS1DINS[A—D][7:0]	**Transmit S1 Byte Value.** Register value is inserted into the transmit S1 byte.	0x00
047F, 0481, 0483, 0485	15—8	TK2DINS[A—D][7:0]	**Transmit K2 Byte Value.** Register value is inserted into the transmit K2 byte.	0x00
	7—0	TK1DINS[A—D][7:0]	**Transmit K1 Byte Value.** Register value is inserted into the transmit K1 byte.	0x00

Register Descriptions (continued)

OHP Registers (continued)

Table 82. Registers 0x0486—0x0491: Receive F1, S1, K2, K1 Monitor Value (RO)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0486, 0489, 048C, 048F	15—8	F1DMON1[A—D][7:0]	**Receive F1 Previous Monitor Value.**	0x00
	7—0	F1DMON0[A—D][7:0]	**Receive F1 Current Monitor Value.**	0x00
0487, 048A, 048D, 0490	15—8	K2DMON[A—D[7:0]	**Receive K2 Monitor Value.**	0x00
	7—0	K1DMON[A—D][7:0]	**Receive K1 Monitor Value.**	0x00
0488, 048B, 048E, 0491	15—8	—	**Reserved.** These bits must be written to their reset default value (0x00).	0x00
	7—0	S1DMON[A—D][7:0]	**Receive S1 Monitor Value.**	0x00

Table 83. Registers 0x0492—0x04F9: Receive J0 Monitor Value (RO)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0492—0499	15—0	RJ0DMON[A][1—16][7:0]	**Receive J0 Monitor Value.** Registers capture a 16-byte sequence from the J0 byte of each channel. In STS-48/STM-16 mode, J0DMON[A][1—16][7:0] is valid for J0 bytes while J0DMON[B—D][1][7:0] are used for Z0DMON[B—D][1][7:0].	0x0000
04B2—04B9	15—0	RJ0DMON[B][1—16][7:0]		
04D2—04D9	15—0	RJ0DMON[C][1—16][7:0		
04F2—04F9	15—0	RJ0DMON[D][1—16][7:0]		

Table 84. Registers 0x0512—0x0579: Transmit J0 Insert Value (R/W)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0512—0519	15—0	TJ0DINS[A][1—16][7:0]	**Transmit J0 Insert Value.** Registers allow a 16-byte sequence to be inserted into the J0 byte of each channel. In STS-48/STM-16 mode, TJ0DINS[A][1—16][7:0] is valid for J0 bytes while TJ0DINS[B—D][1][7:0] are used for TZ0DINS[B—D][1][7:0].	0x0000
0532—0539	15—0	TJ0DINS[B][1—16][7:0]		
0552—0559	15—0	TJ0DINS[C][1—16][7:0]		
0572—0579	15—0	TJ0DINS[D][1—16][7:0]		

Table 85. Registers 0x05AA—0x05C1: Transmit Z0 Insert Value (R/W)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
05AA—05AF	15—0	TZ0DINS[A][2—12][7:0]	**Transmit Z0 Insert Value.** Register values are inserted into the transmit Z0 bytes. In STS-3/ STM-1 mode, TZ0DINS[A—D][2—3] are valid; in STS-12/STM-4 mode, TZ0DINS[A—D][2—12] are valid; and in STS-48/STM-16 mode, all 44 TZ0DINS bytes plus TJ0DINS[B—D][1][7:0] are used for 47 Z0 byte values.	0x0000
05B0—05B5	15—0	TZ0DINS[B][2—12][7:0]		
05B6—05BB	15—0	TZ0DINS[C][2—12][7:0]		
05BC—05C1	15—0	TZ0DINS[D][2—12][7:0]		

Register Descriptions (continued)

OHP Registers (continued)

Table 86. Register 0x05C2: Scratch Register (R/W)

Reset default of register = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
05C2	15—0	OHP_SCRATCH[15:0]	**Scratch Register.** Allows the control system to verify read and write operations to the device without affecting device operation.	0x0000

Register Descriptions (continued)

PT Registers

This section gives a brief description of each register bit and its functionality. All algorithms are described in the main text of the document. The abbreviations after each register indicate if the register is read only (RO), read/write (R/W), write only (WO), or clear-on-read or clear-on-write (COR/W).

0x indicates a hexadecimal value in the Reset Default column. Otherwise, the entry is binary. This is true for every register table in the document.

Table 87. Register 0x0800: PT Macrocell Version Number (RO)

Reset default of register = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0800	15—8	—	**Reserved.** These bits must be written to their reset default value (0x00).	0x00
	7—0	PT_VERSION[7:0]	**Macrocell Version Number.** The version of the macrocell will increment each time a change occurs to the macrocell functionality.	0x00

Table 88. Register 0x0801: PT Interrupt (RO)

Reset default of register = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0801	15—4	—	**Reserved.** These bits must be written to their reset default value (0x000).	0x000
	3	PT_INT[D]	**Interrupt.** Active-high interrupt bit on a per-port basis. These bits are the ORing of all event and delta bits associated with a particular port. An event or delta bit contribution can be inhibited from contributing to the interrupt by setting the appropriate mask bit.	0x0
	2	PT_INT[C]		
	1	PT_INT[B]		
	0	PT_INT[A]		

Table 89. Registers 0x0802, 0x080F, 0x081C, 0x0829 and 0x0803, 0x0810, 0x081D, 0x082A: PT Delta/Event Registers (COR/W)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0802, 080F, 081C, 0829	15	RJ1DMONMIS[A—D]E	**Receive J1 Data Monitor Mismatch.** Event bit indicates a mismatch has occurred between the expected J1 value and the received value.	0
	14—12	—	**Reserved.** These bits must be written to their reset default value (000).	000
	11—0	RPIHD[A—D][1—12]	**Receive Pointer Interpretation Hardware Delta.** Delta bits indicate a change of the associated state bit.	0x000

Register Descriptions (continued)

PT Registers (continued)

Table 89. Registers 0x0802, 0x080F, 0x081C, 0x0829 and 0x0803, 0x0810, 0x081D, 0x082A: PT Delta/Event Registers (COR/W) (continued)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0803, 0810, 081D, 082A	15	TRDIPD[A—D]	**Transmit RDI-P Delta.** Delta bit indicates a change of the associated state byte.	0
	14—11	—	**Reserved.** These bits must be written to their reset default value (0000).	0000
	10	RZ5DMOND[A—D]	**Receive Z5 Data Monitor Delta.** Delta bit indicates a change of the associated state byte.	0
	9	RZ4DMOND[A—D]	**Receive Z4 Data Monitor Delta.** Delta bit indicates a change of the associated state byte.	0
0803, 0810, 081D, 082A	8	RZ3DMOND[A—D]	**Receive Z3 Data Monitor Delta.** Delta bit indicates a change of the associated state byte.	0
	7	RH4DMOND[A—D]	**Receive H4 Data Monitor Delta.** Delta bit indicates a change of the associated state byte.	0
	6	RF2DMOND[A—D]	**Receive F2 Data Monitor Delta.** Delta bit indicates a change of the associated state byte.	0
	5	RRDIPDMOND[A—D]	**Receive RDI-P Data Monitor Delta.** Delta bit indicates a change of the associated state bit.	0
	4	RC2DMOND[A—D]	**Receive C2 Data Monitor Delta.** Delta bit indicates a change of the associated state byte.	0
	3	RUC2D[A—D]	**Receive Unequipped C2 Values Delta.** Delta bit indicates a change of the associated state bit.	0
	2	RPPLMD[A—D]	**Receive Path Payload Label Mismatch Delta.** Delta bit indicates a change of the associated state bit.	0
	1	RSDD[A—D]	**Receive Signal Degrade Delta.** Delta bit indicates a change of the associated state bit.	0
	0	RSFD[A—D]	**Receive Signal Fail Delta.** Delta bit indicates a change of the associated state bit.	0

Register Descriptions (continued)

PT Registers (continued)

Table 90. Registers 0x0836—0x083B, 0x0868—0x0887, 0x0888—0x088D, 0x08BA—0x08D9, 0x08DA—0x08DF, 0x090C—0x092B, 0x092C—0x0931, 0x095E—0x097D: PT State Registers (RO)

Reset default of registers 0x0836, 0x0837, 0x0888, 0x0889, 0x08DA, 0x08DB, 0x092C, 0x092D = 0x0AAA.
Reset default of all other registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0836, 0888, 08DA, 092C	15—14	RSSDRP[A—D][1:0]	**Receive SS Drop Values.** SS bit values from the four selected ports.	00
	13—12	—	**Reserved.** These bits must be written to their reset default value (00).	00
	11—0	RPIH_STATE[A—D] [1—6][1:0]	**Receive Pointer Interpretation Hardware State[Bits 1—6].** Software access to the 48 STS-1 PI state values. 00 = Normal; 01 = Concat; 10 = LOP; 11 = AIS.	0xAAA
0837, 0889, 08DB, 092D	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—0	RPIH_STATE[A—D] [7—12][1:0]	**Receive Pointer Interpretation Hardware State[Bits 7—12].** Software access to the 48 STS-1 PI state values. 00 = Normal; 01 = Concat; 10 = LOP; 11 = AIS.	0xAAA
0838, 088A, 08DC, 092E	15—13	TRDIPINT[A—D][2:0]	**Transmit RDI-P State.** State bits indicating the value of the inserted RDI-P value.	000
	12—7	—	**Reserved.** These bits must be written to their reset default value (000000).	000000
0838, 088A, 08DC, 092E	6—4	RRDIPDMON[A—D][2:0]	**Receive RDI-P Data Monitor State.** State bits indicating the value of the G1[3:1] bits.	000
	3	RUC2VS[A—D]	**Receive Unequipped C2 Value State.** State bit indicating an unequipped value (0x00) has been detected in the C2 byte.	0
	2	RPPLMS[A—D]	**Receive Path Payload Label Mismatch State.** State bit indicating a mismatch occurred (logic 1).	0
	1	RSDS[A—D]	**Receive Signal Degrade State Bit.** State bit indicating the state of the BER algorithm. 0 = within BER programmed, 1 = exceed BER threshold programmed.	0
	0	RSF[A—D]	**Receive Signal Fail State Bit.** State bit indicating the state of the BER algorithm. 0 = within BER programmed, 1 = exceed BER threshold programmed.	0
0839, 088B, 08DD, 092F	15—8	RF2DMON[A—D][7:0]	**Receive F2 Byte Data Monitor.** State byte indicating the value of the validated F2 byte.	0x00
	7—0	RC2DMON[A—D][7:0]	**Receive C2 Data Monitor.** State byte holding the accepted value for the monitored C2 byte.	0x00

Register Descriptions (continued)

PT Registers (continued)

Table 90. Registers 0x0836—0x083B, 0x0868—0x0887, 0x0888—0x088D, 0x08BA—0x08D9, 0x08DA—0x08DF, 0x090C—0x092B, 0x092C—0x0931, 0x095E—0x097D: PT State Registers (RO) (continued)

Reset default of registers 0x0836, 0x0837, 0x0888, 0x0889, 0x08DA, 0x08DB, 0x092C, 0x092D = 0x0AAA.
Reset default of all other registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
083A, 088C, 08DE, 0930	15—8	RZ3DMON[A—D][7:0]	**Receive Z3 Byte Data Monitor.** State byte indicating the value of the validated Z3 byte.	0x00
	7—0	RH4DMON[A—D][7:0]	**Receive H4 Byte Data Monitor.** State byte indicating the value of the validated H4 byte.	0x00
083B, 088D, 08DF, 0931	15—8	RZ5DMON[A—D][7:0]	**Receive Z5 Byte Data Monitor.** State byte indicating the value of the validated Z5 byte.	0x00
	7—0	RZ4DMON[A—D][7:0]	**Receive Z4 Byte Data Monitor.** State byte indicating the value of the validated Z4 byte.	0x00
0868—0887	15—0	RJ1DMON[A][1—64][7:0]	**Receive J1 Data Monitor Values.** Status registers for J1 storage.	0x0000
08BA—08D9	15—0	RJ1DMON[B][1—64][7:0]		
090C—092B	15—0	RJ1DMON[C][1—64][7:0]		
095E—097D	15—0	RJ1DMON[D][1—64][7:0]		

Table 91. Register 0x097E: PT Interrupt Mask Control (R/W)

Reset default of register = 0x000F.

Address (Hex)	Bit #	Name	Function	Reset Default
097E	15—14	PT_FUNCMODE	**Path Terminator Functional Mode.** These bits set the functional mode of the path terminator. Only the values below are valid. Bit 15 Bit 14 PT Function 0 0 normal mode 1 0 pass-through mode (ATM/SDL over fiber)	00
	13—4	—	**Reserved.** These bits must be written to their reset default value (0000000000).	00 0000 0000
	3—0	PTINTM[D—A]	**Interrupt Masks.** Mask bits to inhibit the associated composite delta/event bits for each port from contributing to the interrupt signal from the PT macro. Setting these bits to 1 masks the interrupts.	0xF

Register Descriptions (continued)

PT Registers (continued)

Table 92. Registers 0x097F—0x0980, 0x098C—0x098D, 0x0999—0x099A, 0x09A6—0x09A7: PT Interrupt Mask Control (R/W)

Reset default of registers 0x097F, 0x098C, 0x0999, 0x09A6 = 0x8FFF.
Reset default of registers 0x0980, 0x098D, 0x099A, 0x09A7 = 0xFFFF.

Address (Hex)	Bit #	Name	Function (All Mask Bits Are Active-High)	Reset Default
097F, 098C, 0999, 09A6	15	RJ1DMONMISM[A—D]	**Receive J1 Data Monitor Mismatch Mask.** Mask bit to inhibit the associated event bit from contributing to the interrupt pin ($\overline{\text{INT}}$).	1
	14—12	—	**Reserved.** These bits must be written to their reset default value (000).	000
	11—0	RPIH_STATEM[A—D] [1—12]	**Receive Pointer Interpretation Hardware Mask.** Mask bits to inhibit the associated delta bits from contributing to the interrupt pin ($\overline{\text{INT}}$).	0xFFF

Register Descriptions (continued)

PT Registers (continued)

Table 92. Registers 0x097F—0x0980, 0x098C—0x098D, 0x0999—0x099A, 0x09A6—0x09A7: PT Interrupt Mask Control (R/W) (continued)

Reset default of registers 0x097F, 0x098C, 0x0999, 0x09A6 = 0x8FFF.
Reset default of registers 0x0980, 0x098D, 0x099A, 0x09A7 = 0xFFFF.

Address (Hex)	Bit #	Name	Function (All Mask Bits Are Active-High)	Reset Default
0980, 098D, 099A, 09A7	15	TRDIPINTM[A—D]	**Transmit RDI-P Mask.** Mask bit to inhibit the associated delta bit from contributing to the interrupt pin ($\overline{\text{INT}}$).	1
	14—11	—	**Reserved.** These bits must be written to their reset default value (1111).	1111
	10	RZ5DMONM[A—D]	**Receive Z5 Data Monitor Mask.** Mask bit to inhibit the associated delta bit from contributing to the interrupt pin ($\overline{\text{INT}}$).	1
	9	RZ4DMONM[A—D]	**Receive Z4 Data Monitor Mask.** Mask bit to inhibit the associated delta bit from contributing to the interrupt pin ($\overline{\text{INT}}$).	1
	8	RZ3DMONM[A—D]	**Receive Z3 Data Monitor Mask.** Mask bit to inhibit the associated delta bit from contributing to the interrupt pin ($\overline{\text{INT}}$).	1
	7	RH4DMONM[A—D]	**Receive H4 Data Monitor Mask.** Mask bit to inhibit the associated delta bit from contributing to the interrupt pin ($\overline{\text{INT}}$).	1
	6	RF2DMONM[A—D]	**Receive F2 Data Monitor Mask.** Mask bit to inhibit the associated delta bit from contributing to the interrupt pin ($\overline{\text{INT}}$).	1
	5	RRDIPDMONM[A—D]	**Receive RDI-P Data Monitor Mask.** Mask bit to inhibit the associated delta bit from contributing to the interrupt pin ($\overline{\text{INT}}$).	1
	4	RC2DMONM[A—D]	**Receive C2 Value Mask.** Mask bit to inhibit the associated delta bit from contributing to the interrupt pin ($\overline{\text{INT}}$).	1
	3	RUC2VM[A—D]	**Receive Unequipped C2 Values Mask.** Mask bit to inhibit the associated delta bit from contributing to the interrupt pin ($\overline{\text{INT}}$).	1
	2	RPPLMM[A—D]	**Receive Path Payload Label Mismatch Mask.** Mask bit to inhibit the associated delta bit from contributing to the interrupt pin ($\overline{\text{INT}}$).	1
	1	RSDM[A—D]	**Receive Signal Degrade Mask.** Mask bit to inhibit the associated delta bit from contributing to the interrupt pin ($\overline{\text{INT}}$).	1
	0	RSFM[A—D]	**Receive Signal Fail Mask.** Mask bit to inhibit the associated delta bit from contributing to the interrupt pin ($\overline{\text{INT}}$).	1

Register Descriptions (continued)

PT Registers (continued)

Table 93. Registers (0x09B3, 0x09BF, 0x09CB, 0x09D7, 0x09E3), (0x09EF, 0x09FB, 0x0A07, 0x0A14, 0x0A20), (0x0A2C, 0x0A38, 0x0A44, 0x0A50, 0x0A5C), (0x0A68, 0x0A74, 0x0A80, 0x0A8C, 0x0A98): Error Counters (RO)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
09B3, 09EF, 0A2C, 0A68	15—11	—	**Reserved.** These bits must be written to their reset default value (00000).	00000
	10—0	RPI_INC[A—D][10:0]	**Receive Pointer Interpreter Increment Counter.** Counter that counts the number of increments that occurred on the selected time slot.	000 0000 0000
09BF, 09FB, 0A38, 0A74	15—11	—	**Reserved.** These bits must be written to their reset default value (00000).	00000
	10—0	RPI_DEC[A—D][10:0]	**Receive Pointer Interpreter Decrements Counter.** Counter that counts the number of decrements that occurred on the selected time slot.	000 0000 0000
09CB, 0A07, 0A44, 0A80	15—13	—	**Reserved.** These bits must be written to their reset default value (000).	000
	12—0	RNDFCNT[A—D][12:0]	**Receive Pointer Interpreter NDF Counter.** Counter that counts the number of set NDF (1001) values received on the selected time slot.	0 0000 0000 0000
09D7, 0A14, 0A50, 0A8C	15—0	RB3ERRCNT[A—D][15:0]	**B3 Error Count.** Number of B3 errors detected on the monitored STS-1 time slots.	0x0000
09E3, 0A20, 0A5C, 0A98	15—0	RREIPERRCNT [A—D][15:0]	**Receive Remote Error Indication—Path Error Count.** Count of the number of B3 errors detected in the G1[7:4] nibble.	0x0000

Table 94. Register 0x0AA4: PT One-Shot Control Parameters (WO)

Address (Hex)	Bit #	Name	Function	Reset Default
0AA4	15—12	SDCLEAR[A—D]	**Signal Degrade Clear.** One-shot clear control.	—
	11—8	SDSET[A—D]	**Signal Degrade Set.** One-shot set control.	—
	7—4	SFCLEAR[A—D]	**Signal Fail Clear.** One-shot clear control.	—
	3—0	SFSET[A—D]	**Signal Fail Set.** One-shot set control.	—

Register Descriptions (continued)

PT Registers (continued)

Table 95. Registers 0x0AA6—0x0AAD, 0x0AAE, 0x0AB5, 0x0AB6—0x0ABD, 0x0ABE—0x0AC5: PT Control Parameters (R/W)

Reset default of registers 0x0AA6, 0x0AAE, 0x0AB6, 0x0ABE = 0xF200.
Reset default of registers 0x0AA7, 0x0AAF, 0x0AB7, 0x0ABF = 0x0000.
Reset default of registers 0x0AA8, 0x0AB0, 0x0AB8, 0x0AC0 = 0x0FFF.
Reset default of registers 0x0AA9, 0x0AB1, 0x0AB9, 0x0AC1 = 0x0000.
Reset default of registers 0x0AAA, 0x0AB2, 0x0ABA, 0x0AC2 = 0x0000.
Reset default of registers 0x0AAB, 0x0AB3, 0x0ABB, 0x0AC3 = 0x1AAA.
Reset default of registers 0x0AAC, 0x0AB4, 0x0ABC, 0x0AC4 = 0x3AAA.
Reset default of registers 0x0AAD, 0x0AB5, 0x0ABD, 0x0AC5 = 0x3333.

Address (Hex)	Bit #	Name	Function	Reset Default
0AA6, 0AAE, 0AB6, 0ABE	15—9	—	**Reserved.** These bits must be written to their reset default value (1111001).	1111001
	8—7	RJ1FRAMEA[A—D][1:0]	**Receive J1 Frame Algorithm.** Control bits, when set to 00 or 11 = no framing; 01 = SONET framing; 10 = SDH framing.	00
	6	RJ1DMPC[A—D]	**Receive J1 Dump Control.** Control bit, when set to a logic 1, causes the device to store the J1 byte of the selected STS-1 time slot.	0
	5	RSSPTRNORM[A—D]	**Receive SS Pointer Normal.** If set, uses the SS bits in the pointer interpretation algorithm. The expected values are stored in RSSEXP[A—D][1:0].	0
	4	RB3BITBLKCNT[A—D]	**Receive B3 Bit/Block Count.** Control bit, when set to a logic 0, causes the B3 error counter to count bit errors; otherwise, block errors are counted.	0
	3	RINCDEC_6OR8MAJ [A—D]	**Receive Increment/Decrement 6-or-8 Majority Voting.** If programmed to a logic 0, uses 6 of 10 majority voting to determine a valid increment or decrement; otherwise, uses 8 of 10 majority voting.	0
	2—1	—	**Reserved.** These bits must be written to their reset default value (00).	00
	0	RDIPMON_ENH_OR1B [A—D]	**Remote Defect Indication Enhanced or 1-Bit Monitoring.** Control bit, when set to a logic 1, causes the RDI-P to detect G1[3:1] bits for an enhanced failure code; otherwise, monitors G1[3] for a 1-bit code.	0
0AA7, 0AAF, 0AB7, 0ABF	15—12	RFORCE_LOP[A—D] [1—4]	**Receive FORCE_LOP.** Control bits, when set to a logic 1, force the associated time slot into the LOP state; otherwise, does nothing.	0x0
	11—0	CONCATI_EXPECTED [A—D][1—12]	**Concatenation Indication Expected.** Control bits, when set to 0 = do **not** expect associated time slot to be in CONC mode; otherwise, expect CONC mode.	0x000

Register Descriptions (continued)

PT Registers (continued)

Table 95. Registers 0x0AA6—0x0AAD, 0x0AAE, 0x0AB5, 0x0AB6—0x0ABD, 0x0ABE—0x0AC5: PT Control Parameters (R/W) (continued)

Reset default of registers 0x0AA6, 0x0AAE, 0x0AB6, 0x0ABE = 0xF200.
Reset default of registers 0x0AA7, 0x0AAF, 0x0AB7, 0x0ABF = 0x0000.
Reset default of registers 0x0AA8, 0x0AB0, 0x0AB8, 0x0AC0 = 0x0FFF.
Reset default of registers 0x0AA9, 0x0AB1, 0x0AB9, 0x0AC1 = 0x0000.
Reset default of registers 0x0AAA, 0x0AB2, 0x0ABA, 0x0AC2 = 0x0000.
Reset default of registers 0x0AAB, 0x0AB3, 0x0ABB, 0x0AC3 = 0x1AAA.
Reset default of registers 0x0AAC, 0x0AB4, 0x0ABC, 0x0AC4 = 0x3AAA.
Reset default of registers 0x0AAD, 0x0AB5, 0x0ABD, 0x0AC5 = 0x3333.

Address (Hex)	Bit #	Name	Function	Reset Default
0AA8, 0AB0, 0AB8, 0AC0	15—12	RFORCE_LOP[A—D] [5—8]	**Receive FORCE_LOP.** Control bits, when set to a logic 1, force the associated time slot into the LOP state; otherwise, does nothing.	0x0
	11—0	MASK_CONCAT[A—D] [1—12]	**MASK_CONCATENATION Expected Indication.** When set, mask bits inhibit the generation of AIS when the selected time slot transitions to a state other than CONCAT_EXPECTED[A—D].	0xFFF
0AA9, 0AB1, 0AB9, 0AC1	15—12	RFORCE_LOP[A—D] [9—12]	**Receive FORCE_LOP.** Control bits, when set to a logic 1, force the associated time slot into the LOP state; otherwise, does nothing.	0x0
	11—0	RFORCE_AIS[A—D] [1—12]	**Receive FORCE AIS.** If set, control bits insert AIS-P into the selected STS-1 time slot.	0x000
0AAA, 0AB2, 0ABA, 0AC2	15—12	Tx_REIP_VALUE [A—D][3:0]	**Transmit REI-P Error Value.** REI software error value. Error values are 1 to 8; all others are interpreted as no errors.	0x0
	11	TRDIPSINS[A—D]	**Transmit RDI-P Software Insert.** Control bit, when set, forces the value in TRDIPDINS[A—D][2:0] into the outgoing G1[3:1] bits.	0
	10	—	**Reserved.** This bit must be written to its reset default value (0).	0
	9	TRDIP_PLMPINH[A—D]	**Transmit RDI-P PLM-P Inhibit.** Control bit, when set, causes the PLM-P failure to not contribute to RDI-P generation.	0
	8	TRDIP_UNEQUIPINH [A—D]	**Transmit RDI-P UNEQUIP Inhibit.** Control bit, when set, causes the UNEQUIP failure to not contribute to RDI-P generation.	0

Register Descriptions (continued)

PT Registers (continued)

Table 95. Registers 0x0AA6—0x0AAD, 0x0AAE, 0x0AB5, 0x0AB6—0x0ABD, 0x0ABE—0x0AC5: PT Control Parameters (R/W) (continued)

Reset default of registers 0x0AA6, 0x0AAE, 0x0AB6, 0x0ABE = 0xF200.
Reset default of registers 0x0AA7, 0x0AAF, 0x0AB7, 0x0ABF = 0x0000.
Reset default of registers 0x0AA8, 0x0AB0, 0x0AB8, 0x0AC0 = 0x0FFF.
Reset default of registers 0x0AA9, 0x0AB1, 0x0AB9, 0x0AC1 = 0x0000.
Reset default of registers 0x0AAA, 0x0AB2, 0x0ABA, 0x0AC2 = 0x0000.
Reset default of registers 0x0AAB, 0x0AB3, 0x0ABB, 0x0AC3 = 0x1AAA.
Reset default of registers 0x0AAC, 0x0AB4, 0x0ABC, 0x0AC4 = 0x3AAA.
Reset default of registers 0x0AAD, 0x0AB5, 0x0ABD, 0x0AC5 = 0x3333.

Address (Hex)	Bit #	Name	Function	Reset Default
0AAA, 0AB2, 0ABA, 0AC2	7	TRDIP_LCDINH[A—D]	**Transmit RDI-P LCD Inhibit.** Control bit, when set, causes the LCD failure to not contribute to RDI-P generation.	0
	6	TRDIP_LOPPINH[A—D]	**Transmit RDI-P LOP-P Inhibit.** Control bit, when set, causes the LOP-P failure to not contribute to RDI-P generation.	0
	5	TRDIP_AISINH[A—D]	**Transmit RDI-P AIS-P Inhibit.** Control bit, when set, causes the AIS-P failure to not contribute to RDI-P generation.	0
	4	TRDIP_ENH_OR1B[A—D]	**Transmit RDI-P Enhanced or 1-Bit Monitoring.** Control bit, when set, causes enhanced failure code insert to occur on the G1[3:1] bits; otherwise, inserts a single bit failure code into G1[3].	0
	3	TREIPERRINS[A—D]	**Transmit REI-P Error Insert.** Control bit, when set, causes an error to be continuously injected into the G1[7:4] bits.	0
	2	TB3ERRINS[A—D]	**Transmit B3 Error Insert.** Control bit, when set, causes the B3 value to be inverted.	0
	1	TJ1SINS[A—D]	**Transmit J1 Software Insert.** Control bit, when set, causes the J1 byte stored in the TJ1DINS[A—D][1—64][7:0] register to be injected into the outgoing J1 byte; otherwise, inserts 0x00 into the J1 byte.	0
	0	—	**Reserved.** This bit must be written to its reset default value (0).	0
0AAB, 0AB3, 0ABB, 0AC3	15—12	TPOHINSSEL[A—D][3:0]	**Transmit POH Insert Select.** Control bits, when set, select the STS-1 time slot into which POH data is injected.	0x1
	11—0	THx_STATE[A—D] [1—6][1:0]	**Transmit H Bytes Software State.** Control bits, when set to a logic 00 = normal state, 01 = CONC, 10 = unequipped, 11 = AIS.	0xAAA

Register Descriptions (continued)

PT Registers (continued)

Table 95. Registers 0x0AA6—0x0AAD, 0x0AAE, 0x0AB5, 0x0AB6—0x0ABD, 0x0ABE—0x0AC5: PT Control Parameters (R/W) (continued)

Reset default of registers 0x0AA6, 0x0AAE, 0x0AB6, 0x0ABE = 0xF200.
Reset default of registers 0x0AA7, 0x0AAF, 0x0AB7, 0x0ABF = 0x0000.
Reset default of registers 0x0AA8, 0x0AB0, 0x0AB8, 0x0AC0 = 0x0FFF.
Reset default of registers 0x0AA9, 0x0AB1, 0x0AB9, 0x0AC1 = 0x0000.
Reset default of registers 0x0AAA, 0x0AB2, 0x0ABA, 0x0AC2 = 0x0000.
Reset default of registers 0x0AAB, 0x0AB3, 0x0ABB, 0x0AC3 = 0x1AAA.
Reset default of registers 0x0AAC, 0x0AB4, 0x0ABC, 0x0AC4 = 0x3AAA.
Reset default of registers 0x0AAD, 0x0AB5, 0x0ABD, 0x0AC5 = 0x3333.

Address (Hex)	Bit #	Name	Function	Reset Default
0AAC, 0AB4, 0ABC, 0AC4	15—12	CNTDH4Z3Z4[A—D][3:0]	**Continuous N Times Detect H4/Z3/Z4 Bytes.** Control signal for detecting changes in state of the H4, Z3, and Z4 bytes. Valid values are 0 to 15. A value of 0 or 1 causes the data monitor byte to be updated every frame. A value of n, where 2 ≤ n ≤ 15, of these four bits means that the same value of the H4, Z3, or Z4 byte must be detected n times consecutively to declare a new value in the H4, Z3, or Z4 byte register.	0x3
	11—0	THx_STATE[A—D] [7—12][1:0]	**Transmit H Bytes Software State.** Control bits, when set to a logic 00 = normal state, 01 = CONC, 10 = unequipped, 11 = AIS.	0xAAA

Register Descriptions (continued)

PT Registers (continued)

Table 95. Registers 0x0AA6—0x0AAD, 0x0AAE, 0x0AB5, 0x0AB6—0x0ABD, 0x0ABE—0x0AC5: PT Control Parameters (R/W) (continued)

Reset default of registers 0x0AA6, 0x0AAE, 0x0AB6, 0x0ABE = 0xF200.
Reset default of registers 0x0AA7, 0x0AAF, 0x0AB7, 0x0ABF = 0x0000.
Reset default of registers 0x0AA8, 0x0AB0, 0x0AB8, 0x0AC0 = 0x0FFF.
Reset default of registers 0x0AA9, 0x0AB1, 0x0AB9, 0x0AC1 = 0x0000.
Reset default of registers 0x0AAA, 0x0AB2, 0x0ABA, 0x0AC2 = 0x0000.
Reset default of registers 0x0AAB, 0x0AB3, 0x0ABB, 0x0AC3 = 0x1AAA.
Reset default of registers 0x0AAC, 0x0AB4, 0x0ABC, 0x0AC4 = 0x3AAA.
Reset default of registers 0x0AAD, 0x0AB5, 0x0ABD, 0x0AC5 = 0x3333.

Address (Hex)	Bit #	Name	Function	Reset Default
0AAD, 0AB5, 0ABD, 0AC5	15—12	CNTDZ5[A—D][3:0]	**Continuous N Times Detect Z5 Byte.** Control signal for detecting changes in state of the Z5 byte. Valid values are 0 to 15. A value of 0 or 1 causes the data monitor byte to be updated every frame. A value of n, where 2 ≤ n ≤ 15, of these four bits means that the same value of the Z5 byte must be detected n times consecutively to declare a new value in the Z5 byte register.	0x3
	11—8	CNTDF2[A—D][3:0]	**Continuous N Times Detect F2 Byte.** Control signal for detecting changes in state of the F2 byte. Valid values are 0 to 15. A value of 0 or 1 causes the data monitor byte to be updated every frame. A value of n, where 2 ≤ n ≤ 15, of these four bits means that the same value of the F2 byte must be detected n times consecutively to declare a new value in the F2 byte register.	0x3
	7—4	CNTDRDIP[A—D][3:0]	**Continuous N Times Detect RDI-P.** Control signal for detecting changes in state of the G1[3:1] bits. Valid values are 0 to 15. A value of 0 or 1 causes the data monitor byte to be updated every frame. A value of n, where 2 ≤ n ≤ 15, of these four bits means that the same value of the RDI-P byte must be detected n times consecutively to declare a new value in the RDI-P byte register.	0x3
	3—0	CNTDC2[A—D][3:0]	**Continuous N Times Detect C2 Byte.** Control signal for detecting changes in state of the C2 byte. Valid values are 0 to 15. A value of 0 or 1 causes the data monitor byte to be updated every frame. A value of n, where 2 ≤ n ≤ 15, of these four bits means that the same value of the C2 byte must be detected n times consecutively to declare a new value in the C2 byte register.	0x3

Register Descriptions (continued)

PT Registers (continued)

Table 96. Registers 0x0AC6—0x0AF7: PT Provisioning Registers (R/W)

Reset default of register 0x0AC6 = 0x0001.
Reset default of registers 0x0AC7—0x0AFC = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0AC6	15—6	—	**Reserved.** These bits must be written to their reset default value (0000000000).	00 0000 0000
	5—4	PG_PROV_PNUM[1:0]	**Page Provisioning Port Number.** Control bit that selects the port being provisioned. 00 = port A, 01 = port B, 10 = port C, and 11 = port D.	00
	3—0	PG_PROV_TNUM[3:0]	**Page Provisioning Time-Slot Number.** Control bit that selects the time slot being provisioned. Legal values are 1 to 12, all illegal values default to time slot 1.	0x1
0AC7	15—13	TRDIPDINS[2:0]	**Transmit RDI-P Data Insert.** Software insert value.	000
	12—11	TSS[1:0]	**Transmit SS Value.** Control values inserted into the SS bits in the H1 byte.	00
	10—2	—	**Reserved.** These bits must be written to their reset default value (000000000).	0 0000 0000
	1—0	RSSEXP[1:0]	**Receive Expected SS Value.** Expected SS bit values for the selected STS-1 input streams.	00
0AC8	15—8	—	**Reserved.** These bits must be written to their reset default value (0x00).	0x00
	7—0	RC2EXPVAL[7:0]	**Receive C2 Expected Value.** Expected value for the C2 byte.	0x00
0AC9	15—8	TF2DINS[7:0]	**Transmit F2 Data Insert.** Programmable F2 byte insert value.	0x00
	7—0	TC2DINS[7:0]	**Transmit C2 Data Insert.** Insert byte for the outgoing C2 bytes. **Note:** A value of zero causes an unequipped signal to be generated.	0x00
0ACA	15—8	TZ3DINS[7:0]	**Transmit Z3 Data Insert.** Programmable Z3 byte insert value.	0x00
	7—0	TH4DINS[7:0]	**Transmit H4 Data Insert.** Programmable H4 byte insert value.	0x00
0ACB	15—8	TZ5DINS[7:0]	**Transmit Z5 Data Insert.** Programmable Z5 byte insert value.	0x00
	7—0	TZ4DINS[7:0]	**Transmit Z4 Data Insert.** Programmable Z4 byte insert value.	0x00

Register Descriptions (continued)

PT Registers (continued)

Table 96. Registers 0x0AC6—0x0AF7: PT Provisioning Registers (R/W) (continued)

Reset default of register 0x0AC6 = 0x0001.
Reset default of registers 0x0AC7—0x0AFC = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0ACC	15—8	SFM_SET[7:0]	**Signal Fail M Set.** Threshold of the number of bad monitoring blocks in an observation interval. If the number of bad blocks is below this threshold, then RHSSD is cleared.	0x00
	7—4	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	3—0	SFL_SET[3:0]	**Signal Fail L Set.** Error threshold for determining if a monitoring block is bad.	0x0
0ACD	15—13	SFNSSET[18:16]	**Signal Fail Ns Set.** Number of frames in a monitoring block for RHSSD.	000
	12	—	**Reserved.** This bit must be written to its reset default value (0).	0
	11—0	SFBSET[11:0]	**Signal Fail B Set.** Number of monitoring blocks.	0x000
0ACE	15—0	SFNSSET[15:0]	**Signal Fail Ns Set.** Number of frames in a monitoring block for RHSSD.	0x0000
0ACF	15—8	SFMCLEAR[7:0]	**Signal Fail M Clear.** Threshold of the number of bad monitoring blocks in an observation interval. If the number of bad blocks is below this threshold, then RHSSD is cleared.	0x00
	7—4	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	3—0	SFLCLEAR[3:0]	**Signal Fail L Clear.** Error threshold for determining if a monitoring block is bad.	0x0
0AD0	15—13	SFNSCLEAR[18:16]	**Signal Fail Ns Clear.** Number of frames in a monitoring block for RHSSD.	000
	12	—	**Reserved.** This bit must be written to its reset default value (0).	0
	11—0	SFBCLEAR[11:0]	**Signal Fail B Clear.** Number of monitoring blocks.	0x000
0AD1	15—0	SFNSCLEAR[15:0]	**Signal Fail Ns Clear.** Number of frames in a monitoring block for RHSSD.	0x0000
0AD2	15—8	SDMSET[7:0]	**Signal Degrade M Set.** Threshold of the number of bad monitoring blocks in an observation interval. If the number of bad blocks is below this threshold, then RHSSD is cleared.	0x00
	7—4	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	3—0	SDLSET[3:0]	**Signal Degrade L Set.** Error threshold for determining if a monitoring block is bad.	0x0

Register Descriptions (continued)

PT Registers (continued)

Table 96. Registers 0x0AC6—0x0AF7: PT Provisioning Registers (R/W) (continued)

Reset default of register 0x0AC6 = 0x0001.
Reset default of registers 0x0AC7—0x0AFC = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0AD3	15—13	SDNSSET[18:16]	**Signal Degrade Ns Set.** Number of frames in a monitoring block for RHSSD.	000
	12	—	**Reserved.** This bit must be written to its reset default value (0).	0
	11—0	SDBSET[11:0]	**Signal Degrade B Set.** Number of monitoring blocks.	0x000
0AD4	15—0	SDNSSET[15:0]	**Signal Degrade Ns Set.** Number of frames in a monitoring block for RHSSD.	0x0000
0AD5	15—8	SDMCLEAR[7:0]	**Signal Degrade M Clear.** Threshold of the number of bad monitoring blocks in an observation interval. If the number of bad blocks is below this threshold, then RHSSD is cleared.	0x00
	7—4	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	3—0	SDLCLEAR[3:0]	**Signal Degrade L Clear.** Error threshold for determining if a monitoring block is bad.	0x0
0AD6	15—13	SDNSCLEAR[18:16]	**Signal Degrade Ns Clear.** Number of frames in a monitoring block for RHSSD.	000
	12	—	**Reserved.** This bit must be written to its reset default value (0).	0
	11—0	SDBCLEAR[11:0]	**Signal Degrade B Clear.** Number of monitoring blocks.	0x000
0AD7	15—0	SDNSCLEAR[15:0]	**Signal Degrade Ns Clear.** Number of frames in a monitoring block for RHSSD.	0x0000
0AD8—0AF7	15—0	TJ1DINS[1—64][7:0]	**Transmit J1 Data Insert.** Insert values for the selected J1 bytes.	0x0000

Table 97. Register 0x0AF8: Scratch Register (R/W)

Reset default of register = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
0AF8	15—0	PT_SCRATCH[15:0]	**Scratch Register.** Diagnostic register used by the microprocessor. Has no effect on the macro operation.	0x0000

Register Descriptions (continued)

DE Registers

This section gives a brief description of each register bit and its functionality. All algorithms are described in the main text of the document. The abbreviations after each register indicate if the register is read only (RO), read/write (R/W), write only (WO), or clear-on-read or clear-on-write (COR/W).

0x indicates a hexadecimal value in the Reset Default column. Otherwise, the entry is binary. This is true for every register table in the document.

Table 98. Register 0x1000: DE Macrocell Number (RO)

Reset default of register = 0x0001.

Address (Hex)	Bit #	Name	Function	Reset Default
1000	15—0	DE_VERSION	**Macrocell Version Number.** The version of the macrocell will increment each time a change occurs to the macrocell functionality.	0x0001

Register Descriptions (continued)

DE Registers (continued)

Table 99. Registers 0x1001 and 0x1002: DE Interrupts (RO)

Reset default of registers = 0x0000.

Note: The registers are cleared by accessing the source register of the interrupt. The source register must be read and cleared to clear these registers.

Address (Hex)	Bit #	Name	Function	Reset Default
1001	15—5	—	**Reserved.** These bits must be written to their reset default value (00000000000).	000 0000 0000
	4	DEINT_SDLMS	**SDL Message Sent Interrupt.** **Note:** This bit indicates that the SDL frame inserter is experiencing an interrupt. This bit will **not** clear on a read or a write of this register, but will clear when the SDL SDLMSI register (0x1606, bit 0) is read. These interrupts will generate a DE interrupt.	0
	3—0	DEINTCH[3:0]	**Channel Interrupt.** Active-high interrupt bit on a per-channel basis. These bits are the ORing of all interrupt bits associated with the error counters described in registers 0x1100—0x111F (pages 219—page 130). The error counter can be inhibited from contributing to the interrupt by setting the appropriate mask bit in register DEDINTM[0—3] (addresses 0x1180, 0x1182, 0x1184, 0x1186 on page 224). The following interrupts will generate a DE interrupt: Bit 0 corresponds to channel 0 interrupt. Bit 1 corresponds to channel 1 interrupt. Bit 2 corresponds to channel 2 interrupt. Bit 3 corresponds to channel 3 interrupt. **Note:** This bit indicates that the channel is experiencing an interrupt. This bit will **not** clear on a read or a write of this register, but will clear when the counter interrupt register DEDINTM[0—3] (addresses 0x1181, 0x1183, 0x1185, 0x1187 on page 225) is read or written.	0x0

Register Descriptions (continued)

DE Registers (continued)

Table 99. Registers 0x1001 and 0x1002: DE Interrupts (RO) (continued)

Reset default of registers = 0x0000.

Note: The registers are cleared by accessing the source register of the interrupt. The source register must be read and cleared to clear these registers.

Address (Hex)	Bit #	Name	Function	Reset Default
1002	15—12	DEINT_SDLRxFS	**SDL Rx Frame State Interrupt.** This interrupt is generated when the SDL frame state is transitioned from sync to hunt. This bit may clear when read or written. The following interrupts will generate a DE interrupt: Bit 12 corresponds to channel 0 interrupt. Bit 13 corresponds to channel 1 interrupt. Bit 14 corresponds to channel 2 interrupt. Bit 15 corresponds to channel 3 interrupt.	0x0
	11—8	DEINT_ATMRxAC	**ATM Rx All-Cool Interrupt.** This interrupt is generated when the payload of received null/ idle cells is correctly incrementing. This bit may clear when read or written. This interrupt is used in conjunction with the optional incrementing payload sequence mode for debug purposes and is used in conjunction with DE register 0x12F0. Bit 8 corresponds to channel 0 interrupt. Bit 9 corresponds to channel 1 interrupt. Bit 10 corresponds to channel 2 interrupt. Bit 11 corresponds to channel 3 interrupt. **Note:** This signal does not generate a DE interrupt under any circumstances.	0x0
	7—4	DEINT_ATMRxS	**ATM Rx X^{31}Scrambler State Interrupt.** This interrupt is generated when the ATM scrambler state is transitioned from synchronization to verification. This bit may clear when read or written. The following interrupts will generate a DE interrupt: Bit 4 corresponds to channel 0 interrupt. Bit 5 corresponds to channel 1 interrupt. Bit 6 corresponds to channel 2 interrupt. Bit 7 corresponds to channel 3 interrupt.	0x0

Register Descriptions (continued)

DE Registers (continued)

Table 99. Registers 0x1001 and 0x1002: DE Interrupts (RO) (continued)

Reset default of registers = 0x0000.

Note: The registers are cleared by accessing the source register of the interrupt. The source register must be read and cleared to clear these registers.

Address (Hex)	Bit #	Name	Function	Reset Default
1002	3—0	DEINT_ATMRxF	**ATM Rx Frame State Interrupt.** This interrupt is generated when the ATM frame state is transitioned from sync to hunt. This bit may clear when read or written. The following interrupts will generate a DE interrupt: Bit 0 corresponds to channel 0 interrupt. Bit 1 corresponds to channel 1 interrupt. Bit 2 corresponds to channel 2 interrupt. Bit 3 corresponds to channel 3 interrupt.	0x0

Table 100. Register 0x1004: Dry Escape Marker (R/W)

Reset default of register = 0x0020.

Address (Hex)	Bit #	Name	Function	Reset Default
1004	15—8	—	**Reserved.** These bits must be written to their reset default value (0x00).	0x00
	7—0	DRYESCAPE[7:0]	**Dry Escape Value.** This 8-bit value, attached with 0x7d, sets the dry marker value. The default dry marker value would then be 0x7d20.	0x20

Register Descriptions (continued)

DE Registers (continued)

Table 101. Registers 0x1010—0x1015: Sequencer Provisioning Registers (R/W)

Reset default of register 0x1010 = 0x0002.
Reset default of register 0x1011 = 0x2210.
Reset default of registers 0x1012, 0x1014 = 0x0435.
Reset default of registers 0x1013, 0x1015 = 0x0025.

Note: The settings of these registers must be consistent with core mode register (address 0x0010).

Address (Hex)	Bit #	Name	Function	Reset Default
1010	—	SEQ_CTRL	**Sequencer Control.** Selects STS-3/STM-1, STS-12/STM-4, or STS-48/STM-16 mode for the data engine. Allowed values are as follows: STS-3/STM-1 = 0x0001 STS-12/STM-4 = 0x0003 STS-48/STM-16 = 0x0002	0x0002
	15—2	—	**Reserved.** These bits must be written to their reset default value (00000000000000).	00 0000 0000 0000
	1	SEQ_RATE	**Sequencer Rate.** Configures internal clock derived from TxCKP/TxCKN. 0 = STS-3/STM-1 (internal clock = 19.440 MHz) 1 = STS-12/STM-4 or STS-48/STM-16 (internal clock = 77.760 MHz)	1
	0	SEQ_MODE	**Sequencer Mode.** Used with bit 1 above to select the mode. 0 = STS-48/STM-16 1 = STS-3/STM-1 or STS-12/STM-4	0
1011	15—0	INIT_CNTS	**Initial Counts.** This register must be set to the default value (0x2210).	0x2210
1012	15—0	OH_MARKER_LO	**OHP Marker Low.** This register must be programmed as follows. STS-48/STM-16 = 0x0435 STS-12/STM-4 = 0x0435 STS-3/STM-1 = 0x010B	0x0435
1013	15—0	OH_MARKER_HI	**OHP Marker High.** This register must be programmed as follows. STS-48/STM-16 = 0x0025 STS-12/STM-4 = 0x0025 STS-3/STM-1 = 0x0007	0x0025
1014	15—0	SOH_MARKER_LO	**Sequence Provisioning for OHP Marker Low.** This register must be programmed as follows. STS-48/STM-16 = 0x0435 STS-12/STM-4 = 0x0435 STS-3/STM-1 = 0x010B	0x0435
1015	15—0	SOH_MARKER_HI	**Sequence Provisioning for OHP Marker High.** This register must be programmed as follows. STS-48/STM-16 = 0x0025 STS-12/STM-4 = 0x0025 STS-3/STM-1 = 0x0007	0x0025

Register Descriptions (continued)

DE Registers (continued)

Table 102. Registers 0x1016—0x1021: Egress Configuration Registers (R/W)

Reset default of registers 0x1016, 0x101A, 0x101E = 0x4444.
Reset default of registers 0x1017, 0x101B, 0x101F = 0x5555.
Reset default of registers 0x1018, 0x101C, 0x1020 = 0x6666.
Reset default of registers 0x1019, 0x101D, 0x1021 = 0x7777.

Note: See Figures 13—16, pages 70—73. The notation X/Y means the following: X = OC-48 byte, Y = OC-12/OC-3 byte.

Address (Hex)	Bit #	Name	Function	Reset Default
1016—1021	15—0	Tx_TS[0—11]	**Egress Time Slot [0—11].** These 12 registers define the egress time slots. The default is set to quad channel STS-48/STM-16. The payload bits may be set low to account for any unused slots. Possible configurations are as follows: ■ Multichannel STS-48/STM-16. Each time slot will use only one channel, but the channel will vary for each time slot. ■ Single-channel STS-48/STM-16. Each time slot will use only one channel for every time slot. ■ STS-3/STM-1 or STS-12/STM-4. Each of four channels will be defined once for each time slot.	See below.

Register Descriptions (continued)

DE Registers (continued)

Table 102. Registers 0x1016—0x1021: Egress Configuration Registers (R/W) (continued)

Reset default of registers 0x1016, 0x101A, 0x101E = 0x4444.
Reset default of registers 0x1017, 0x101B, 0x101F = 0x5555.
Reset default of registers 0x1018, 0x101C, 0x1020 = 0x6666.
Reset default of registers 0x1019, 0x101D, 0x1021 = 0x7777.

Note: See Figures 13—16, pages 70—73. The notation X/Y means the following: X = OC-48 byte, Y = OC-12/OC-3 byte.

Address (Hex)	Bit #	Name	Function	Reset Default
1016	—	Tx_TS0	**Egress Time Slot 0.**	0x444
	—	—	**Tx_TS0[15:12]:** Byte 1/1A : Byte 1 transmit sequence map and channel.	0x4
	15	—	**Reserved.** This bit must be written to its reset default value (0).	0
	14	Tx_PLD1	**PLD.** Defines the validity of the payload in the time slot. 1 = valid 0 = invalid	1
	13—12	Tx_CH1	**CH.** Defines one of four channels (00, 01, 10, 11).	00
	—	—	**Tx_TS0[11:8]:** Byte 4/1B: Byte 4 transmit sequence map and channel.	0x4
	11	—	**Reserved.** This bit must be written to its reset default value (0).	0
	10	Tx_PLD4	**PLD.** Defines the validity of the payload in the time slot. 1 = valid 0 = invalid	1
	9—8	Tx_CH4	**CH.** Defines one of four channels (00, 01, 10, 11).	00
	—	—	**Tx_TS0[7:4]:** Byte 7/1C: Byte 7 transmit sequence map and channel.	0x4
	7	—	**Reserved.** This bit must be written to its reset default value (0).	0
	6	Tx_PLD7	**PLD.** Defines the validity of the payload in the time slot. 1 = valid 0 = invalid	1
	5—4	Tx_CH7	**CH.** Defines one of four channels (00, 01, 10, 11).	00
	—	—	**Tx_TS0[3:0]:** Byte 10/1D: Byte 10 transmit sequence map and channel.	0x4
	3	—	**Reserved.** These bits must be written to their reset default value (0x4).	
	2	Tx_PLD10	**PLD.** Defines the validity of the payload in the time slot. 1 = valid 0 = invalid	
	1—0	Tx_CH10	**CH.** Defines one of four channels (00, 01, 10, 11).	

Register Descriptions (continued)

DE Registers (continued)

Table 102. Registers 0x1016—0x1021: Egress Configuration Registers (R/W) (continued)

Reset default of registers 0x1016, 0x101A, 0x101E = 0x4444.
Reset default of registers 0x1017, 0x101B, 0x101F = 0x5555.
Reset default of registers 0x1018, 0x101C, 0x1020 = 0x6666.
Reset default of registers 0x1019, 0x101D, 0x1021 = 0x7777.

Note: See Figures 13—16, pages 70—73. The notation X/Y means the following: X = OC-48 byte, Y = OC-12/OC-3 byte.

Address (Hex)	Bit #	Name	Function	Reset Default
1017		Tx_TS1	**Egress Time Slot 1.** Refer to egress time slot 0.	0x5555
	15—12	—	Byte 13/4A definition.	
	11—8	—	Byte 16/4B definition.	
	7—4	—	Byte 19/4C definition.	
	3—0	—	Byte 22/4D definition.	
1018	—	Tx_TS2	**Egress Time Slot 2.** Refer to egress time slot 0.	0x6666
	15—12	—	Byte 25/7A definition.	
	11—8	—	Byte 28/7B definition.	
	7—4	—	Byte 31/7C definition.	
	3—0	—	Byte 34/7D definition.	
1019	—	Tx_TS3	**Egress Time Slot 3.** Refer to egress time slot 0.	0x7777
	15—12	—	Byte 37/10A definition.	
	11—8	—	Byte 40/10B definition.	
	7—4	—	Byte 43/10C definition.	
	3—0	—	Byte 46/10D definition.	
101A	—	Tx_TS4	**Egress Time Slot 4.** Refer to egress time slot 0.	0x4444
	15—12	—	Byte 2/2A definition.	
	11—8	—	Byte 5/2B definition.	
	7—4	—	Byte 8/2C definition.	
	3—0	—	Byte 11/2D definition.	
101B	—	Tx_TS5	**Egress Time Slot 5.** Refer to egress time slot 0.	0x5555
	15—12	—	Byte 14/5A definition.	
	11—8	—	Byte 17/5B definition.	
	7—4	—	Byte 20/5C definition.	
	3—0	—	Byte 23/5D definition.	
101C	—	Tx_TS6	**Egress Time Slot 6.** Refer to egress time slot 0.	0x6666
	15—12	—	Byte 26/8A definition.	
	11—8	—	Byte 29/8B definition.	
	7—4	—	Byte 32/8C definition.	
	3—0	—	Byte 35/8D definition.	

Register Descriptions (continued)

DE Registers (continued)

Table 102. Registers 0x1016—0x1021: Egress Configuration Registers (R/W) (continued)

Reset default of registers 0x1016, 0x101A, 0x101E = 0x4444.
Reset default of registers 0x1017, 0x101B, 0x101F = 0x5555.
Reset default of registers 0x1018, 0x101C, 0x1020 = 0x6666.
Reset default of registers 0x1019, 0x101D, 0x1021 = 0x7777.

Note: See Figures 13—16, pages 70—73. The notation X/Y means the following: X = OC-48 byte, Y = OC-12/OC-3 byte.

Address (Hex)	Bit #	Name	Function	Reset Default
101D	—	Tx_TS7	**Egress Time Slot 7.** Refer to egress time slot 0.	0x7777
	15—12	—	Byte 38/11A definition.	
	11—8	—	Byte 41/11B definition.	
	7—4	—	Byte 44/11C definition.	
	3—0	—	Byte 47/11D definition.	
101E	—	Tx_TS8	**Egress Time Slot 8.** Refer to egress time slot 0.	0x4444
	15—12	—	Byte 3/3A definition.	
	11—8	—	Byte 6/3B definition.	
	7—4	—	Byte 9/3C definition.	
	3—0	—	Byte 12/3D definition.	
101F	—	Tx_TS9	**Egress Time Slot 9.** Refer to egress time slot 0.	0x5555
	15—12	—	Byte 15/6A definition.	
	11—8	—	Byte 18/6B definition.	
	7—4	—	Byte 21/6C definition.	
	3—0	—	Byte 24/6D definition.	
1020	—	Tx_TS10	**Egress Time Slot 10.** Refer to egress time slot 0.	0x6666
	15—12	—	Byte 27/9A definition.	
	11—8	—	Byte 30/9B definition.	
	7—4	—	Byte 33/9C definition.	
	3—0	—	Byte 36/9D definition.	
1021	—	Tx_TS11	**Egress Time Slot 11.** Refer to egress time slot 0.	0x7777
	15—12	—	Byte 39/12A definition.	
	11—8	—	Byte 42/12B definition.	
	7—4	—	Byte 45/12C definition.	
	3—0	—	Byte 48/12D definition.	

Register Descriptions (continued)

DE Registers (continued)

Table 103. Registers 0x1022—0x102D: Ingress Configuration Registers (R/W)

Reset default of registers 0x1022, 0x1026, 0x102A = 0x4444.
Reset default of registers 0x1023, 0x1027B, 0x102B = 0x5555.
Reset default of registers 0x1024, 0x1028, 0x102C = 0x6666.
Reset default of registers 0x1025, 0x1029, 0x102D = 0x7777.

Note: See Figures 13—16, pages 70—73. The notation X/Y means the following: X = OC-48 byte, Y = OC-12/OC-3 byte.

Address (Hex)	Bit #	Name	Function	Reset Default
1022—102D	15—0	Rx_TS[0—11]	**Ingress Time Slot [0—11].** These 12 registers define the ingress time slots. The default is set to quad channel STS-48/STM-16. The payload bits may be turned low to account for any unused slots. Possible configurations are as follows: ■ Multichannel STS-48/STM-16. Each time slot will use only one channel, but the channel will vary for each time slot. ■ Single-channel STS-48/STM-16. Each time slot will use only one channel for every time slot. ■ STS-3/STM-1 or STS-12/STM-4. Each of four channels will be defined once for each time slot.	See below.

Register Descriptions (continued)

DE Registers (continued)

Table 103. Registers 0x1022—0x102D: Ingress Configuration Registers (R/W) (continued)

Reset default of registers 0x1022, 0x1026, 0x102A = 0x4444.
Reset default of registers 0x1023, 0x1027B, 0x102B = 0x5555.
Reset default of registers 0x1024, 0x1028, 0x102C = 0x6666.
Reset default of registers 0x1025, 0x1029, 0x102D = 0x7777.

Note: See Figures 13—16, pages 70—73. The notation X/Y means the following: X = OC-48 byte, Y = OC-12/OC-3 byte.

Address (Hex)	Bit #	Name	Function	Reset Default
1022	—	Rx_TS0	**Ingress Time Slot 0.**	0x4444
	—	—	**Rx_TS0[15:12].** Byte 1/Byte 1A: Byte 1 receive sequence map and channel.	0x4
	15	—	**Reserved.** This bit must be written to its reset default value (0).	0
	14	Rx_PLD1	**PLD.** Defines the validity of the payload in the time slot. 1 = valid 0 = invalid	1
	13—12	Rx_CH1	**CH.** Defines one of four channels (00, 01, 10, 11).	00
	—	—	**Rx_TS0[11:8].** Byte 4/Byte 1B: Byte 4 receive sequence map and channel.	0x4
	11	—	**Reserved.** This bit must be written to its reset default value (0).	0
	10	Rx_PLD4	**PLD.** Defines the validity of the payload in the time slot. 1 = valid 0 = invalid	1
	9—8	Rx_CH4	**CH.** Defines one of four channels (00, 01, 10, 11).	00
	—	—	**Rx_TS0[7:4].** Byte 7/Byte 1C: Byte 7 receive sequence map and channel.	0x4
	7	—	**Reserved.** This bit must be written to its reset default value (0).	0
	6	Rx_PLD7	**PLD.** Defines the validity of the payload in the time slot. 1 = valid 0 = invalid	1
	5—4	Rx_CH7	**CH.** Defines one of four channels (00, 01, 10, 11).	00
	—	—	**Rx_TS0[3:0].** Byte 10/Byte 1D: Byte 10 receive sequence map and channel.	0x4
	3	—	**Reserved.** This bit must be written to its reset default value (0).	0
	2	Rx_PLD10	**PLD.** Defines the validity of the payload in the time slot. 1 = valid 0 = invalid	1
	1—0	Rx_CH10	**CH.** Defines one of four channels(00, 01, 10, 11).	00

Register Descriptions (continued)

DE Registers (continued)

Table 103. Registers 0x1022—0x102D: Ingress Configuration Registers (R/W) (continued)

Reset default of registers 0x1022, 0x1026, 0x102A = 0x4444.
Reset default of registers 0x1023, 0x1027B, 0x102B = 0x5555.
Reset default of registers 0x1024, 0x1028, 0x102C = 0x6666.
Reset default of registers 0x1025, 0x1029, 0x102D = 0x7777.

Note: See Figures 13—16, pages 70—73. The notation X/Y means the following: X = OC-48 byte, Y = OC-12/OC-3 byte.

Address (Hex)	Bit #	Name	Function	Reset Default
1023	—	Rx_TS1	**Ingress Time Slot 1.** Refer to ingress time slot 0.	0x5555
	15—12	—	Byte 13/4A definition.	
	11—8	—	Byte 16/4B definition.	
	7—4	—	Byte 19/4C definition.	
	3—0	—	Byte 22/4D definition.	
1024	—	Rx_TS2	**Ingress Time Slot 2.** Refer to ingress time slot 0.	0x6666
	15—12	—	Byte 25/7A definition.	
	11—8	—	Byte 28/7B definition.	
	7—4	—	Byte 31/7C definition.	
	3—0	—	Byte 34/7D definition.	
1025	—	Rx_TS3	**Ingress Time Slot 3.** Refer to ingress time slot 0.	0x7777
	15—12	—	Byte 37/10A definition.	
	11—8	—	Byte 40/10B definition.	
	7—4	—	Byte 43/10C definition.	
	3—0	—	Byte 46/10D definition.	
1026	—	Rx_TS4	**Ingress Time Slot 4.** Refer to ingress time slot 0.	0x4444
	15—12	—	Byte 2/2A definition.	
	11—8	—	Byte 5/2B definition.	
	7—4	—	Byte 8/2C definition.	
	3—0	—	Byte 11/2D definition.	
1027	—	Rx_TS5	**Ingress Time Slot 5.** Refer to ingress time slot 0.	0x5555
	15—12	—	Byte 14/5A definition.	
	11—8	—	Byte 17/5B definition.	
	7—4	—	Byte 20/5C definition.	
	3—0	—	Byte 23/5D definition.	
1028	—	Rx_TS6	**Ingress Time Slot 6.** Refer to ingress time slot 0.	0x6666
	15—12	—	Byte 26/8A definition.	
	11—8	—	Byte 29/8B definition.	
	7—4	—	Byte 32/8C definition.	
	3—0	—	Byte 35/8D definition.	

Register Descriptions (continued)

DE Registers (continued)

Table 103. Registers 0x1022—0x102D: Ingress Configuration Registers (R/W) (continued)

Reset default of registers 0x1022, 0x1026, 0x102A = 0x4444.
Reset default of registers 0x1023, 0x1027B, 0x102B = 0x5555.
Reset default of registers 0x1024, 0x1028, 0x102C = 0x6666.
Reset default of registers 0x1025, 0x1029, 0x102D = 0x7777.

Note: See Figures 13—16, pages 70—73. The notation X/Y means the following: X = OC-48 byte, Y = OC-12/OC-3 byte.

Address (Hex)	Bit #	Name	Function	Reset Default
1029	—	Rx_TS7	**Ingress Time Slot 7.** Refer to ingress time slot 0.	0x7777
	15—12	—	Byte 38/11A definition.	
	11—8	—	Byte 41/11B definition.	
	7—4	—	Byte 44/11C definition.	
	3—0	—	Byte 47/11D definition.	
102A	—	Rx_TS8	**Ingress Time Slot 8.** Refer to ingress time slot 0.	0x4444
	15—12	—	Byte 3/3A definition.	
	11—8	—	Byte 6/3B definition.	
	7—4	—	Byte 9/3C definition.	
	3—0	—	Byte 12/3D definition.	
102B	—	Rx_TS9	**Ingress Time Slot 9.** Refer to ingress time slot 0.	0x5555
	15—12	—	Byte 15/6A definition.	
	11—8	—	Byte 18/6B definition.	
	7—4	—	Byte 21/6C definition.	
	3—0	—	Byte 24/6D definition.	
102C	—	Rx_TS10	**Ingress Time Slot 10.** Refer to ingress time slot 0.	0x6666
	15—12	—	Byte 27/9A definition.	
	11—8	—	Byte 30/9B definition.	
	7—4	—	Byte 33/9C definition.	
	3—0	—	Byte 36/9D definition.	
102D	—	Rx_TS11	**Ingress Time Slot 11.** Refer to ingress time slot 0.	0x7777
	15—12	—	Byte 39/12A definition.	
	11—8	—	Byte 42/12B definition.	
	7—4	—	Byte 45/12C definition.	
	3—0	—	Byte 48/12D definition.	

Register Descriptions (continued)

DE Registers (continued)

Table 104. Registers 0x102E—0x1031: Over-Fiber Mode (Packet-Over-Fiber or POF) Control (R/W)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
102E	—	Rx_OF_CTRL	**Ingress Over-Fiber Mode Register.** This register will define the channels, if any, that are carrying over-fiber payload in the ingress direction. 0 = SONET 1 = over-fiber mode (For specific bits, see register Rx_TS[0—11], page 200.)	0x0000
	15	—	**Reserved.** These bits must be written to their reset default value (0).	
	14	—	Physical channel (line) A mode.	
	13—12	—	**Reserved.** These bits must be written to their reset default value (00).	
	10	—	Physical channel (line) B mode.	
	9—7	—	**Reserved.** These bits must be written to their reset default value (000).	
	6	—	Physical channel (line) C mode.	
	5—3	—	**Reserved.** These bits must be written to their reset default value (000).	
	2	—	Physical channel (line) D mode.	
	1—0	—	**Reserved.** These bits must be written to their reset default value (00).	
102F	—	Tx_OF_CTRL	**Egress Over-Fiber Mode Register.** This register will define the channels, if any, that are carrying over-fiber payload in the egress direction. 0 = SONET 1 = over-fiber mode (For specific bits, see register Tx_TS[0—11], page 196.)	0x0000
	15	—	**Reserved.** These bits must be written to their reset default value (0).	
	14	—	Physical channel (line) A mode.	
	13—12	—	**Reserved.** These bits must be written to their reset default value (00).	
	10	—	Physical channel (line) B mode.	
	9—7	—	**Reserved.** These bits must be written to their reset default value (000).	
	6	—	Physical channel (line) C mode.	
	5—3	—	**Reserved.** These bits must be written to their reset default value (000).	
	2	—	Physical channel (line) D mode.	
	1—0	—	**Reserved.** These bits must be written to their reset default value (00).	

Register Descriptions (continued)

DE Registers (continued)

Table 104. Registers 0x102E—0x1031: Over-Fiber Mode (Packet-Over-Fiber or POF) Control (R/W) (continued)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
1030	—	Rx_CHCD_FM[15:0]	**Receive Channel C/D Framer Mode.** This register is used in over-fiber mode to give the Rx sequencer prior knowledge of the time slot and byte location within a time slot of the valid byte of a transparent packet for a given frame.	0x0000
	15—14	—	**Reserved.** These bits must be written to their reset default value (00).	
	13—10	—	Time slot having the last payload for channel C.	
	9—8	—	Last byte location out of 4-byte output for channel C.	
	7—6	—	**Reserved.** These bits must be written to their reset default value (00).	
	5—2	—	Time slot having the last payload for channel D.	
	1—0	—	Last byte location out of 4-byte output for channel D.	
1031	—	Rx_CHAB_FM[15:0]	**Receive Channel A/B Framer Mode.** This register is used in over-fiber mode to give the Rx sequencer prior knowledge of the time slot and byte location within a time slot of the valid byte of a transparent packet for a given frame.	0x0000
	15—14	—	**Reserved.** These bits must be written to their reset default value (00).	
	13—10	—	Time slot having the last payload for channel A.	
	9—8	—	Last byte location out of 4-byte output for channel A.	
	7—6	—	**Reserved.** These bits must be written to their reset default value (00).	
	5—2	—	Time slot having the last payload for channel B.	
	1—0	—	Last byte location out of 4-byte output for channel B.	

Register Descriptions (continued)

DE Registers (continued)

Table 105. Registers 0x1032—0x1036: Sequencer Cell State Registers (R/W)

Reset default of registers 0x1032—0x1035 = 0x0000.
Reset default of register 0x1036 = 0x000F.

Address (Hex)	Bit #	Name	Function	Reset Default
1032—1035	—	Rx_CELL[A—D]_FM	**Rx Channel [A—D] Cell Register.** This register is used in over-fiber mode to give the Rx sequencer prior knowledge of the cell in which the last byte of a transparent packet for a given frame is located.	0x0000
	15—10	—	**Reserved.** These bits must be written to their reset default value (000000).	00 0000
	9—0	RxLBCF	**Rx Last Byte of Current Frame.** Defines which of the 810 SONET cells has the last byte of the current frame in channel [A—D].	00 0000 0000
1036	—	Tx_SEQ_DISABLE	**Tx Sequencer Disable.** This register is used to enable or disable channels. The default is all four channels are disabled. In other words, the disables on the channels must be cleared or the sequencer will not operate. 1 = the channel is disabled; 0 = the channel is enabled.	0x000F
	15—4	—	**Reserved.** These bits must be written to their reset default value (0x000).	0x000
	3	—	**Channel A Disable.**	1
	2	—	**Channel B Disable.**	1
	1	—	**Channel C Disable.**	1
	0	—	**Channel D Disable.**	1

Table 106. Registers 0x1040—0x1043: Ingress Payload Type and Mode Control (R/W)

Reset default of registers = 0x0700.

Address (Hex)	Bit #	Name	Function	Reset Default
1040—1043	—	Rx_PCTL_[0—3]	**Channel [0—3] Payload Type and Control.** See Table 107 for receive type and mode control summary.	0x0700
	15—11	—	**Reserved.** These bits must be written to their reset default value (00000).	00000
	10—8	—	**Payload Type.** Defines the payload type being received.	111
	7—0	—	**Payload Control.** Allows for different options when receiving data, such as pre- or post-unscrambling, PPP header discard, etc.	0x00

Register Descriptions (continued)

DE Registers (continued)

Table 107. Receive Type and Mode Control Summary Table (Registers 0x1040—0x1043)

Payload Type, Bits [10:8]	Payload Control, Bits [7:0]							
	7	**6**	**5**	**4**	**3**	**2**	**1**	**0**
000 PPP	0 = discard 1 = no discard	0 = header stripped 1 = header on	0 = CRC-16 1 = CRC-32	0 = CRC stripped 1 = CRC on	0 = CRC reversed 1 = CRC normal	0 = no dry mode 1 = dry mode	00 = no unscrambling 01 = post-unscrambling 10 = pre-unscrambling 11 = undefined	
001 HDLC with CRC	0	0	0 = CRC-16 1 = CRC-32	0 = CRC stripped 1 = CRC on	0 = CRC reversed 1 = CRC normal	0 = no dry mode 1 = dry mode	00 = no unscrambling 01 = post-unscrambling 10 = pre-unscrambling 11 = undefined	
010 HDLC without CRC	0	0	0	0	0	0 = no dry mode 1 = dry mode	00 = no unscrambling 01 = post-unscrambling 10 = pre-unscrambling 11 = undefined	
011 ATM	0 = byte sync 1 = bit sync	0	00 = X^{43} unscrambling 01 = no unscrambling 10 = X^{31} unscrambling 11 = no unscrambling		0 = unassigned cell discard 1 = unassigned cell passthrough	0 = idle cell discard 1 = idle cell passthrough	00 = no discard 01 = discard 10 = smart discard 11 = discard, no correction	
100 SDL without CRC	0 = byte sync 1 = bit sync	0 = length stripped 1 = length on	0	0	Length offset (0x0 to 0xF)			
101 SDL with CRC	0 = byte sync 1 = bit sync	0 = length stripped 1 = length on	0 = CRC-16 1 = CRC-32	0 = CRC stripped 1 = CRC on	Length offset (0x0 to 0xF)			
110 Transparent payload	0	0	0	0	0	0	0	0
111 Not defined (reset mode)	0	0	0	0	0	0	0	0

Register Descriptions (continued)

DE Registers (continued)

Table 108. Registers 0x1080—0x1087: ATM Framer Idle Cell Match Mask (R/W)

Reset default of registers = 0xFFFF.

Address (Hex)	Bit #	Name	Function	Reset Default
1080—1087	—	ATM_IDM_[0—3][31:0]	**ATM Idle Cell Match Mask Channel [0—3].** This 32-bit register defines which of the 32 bits will be used for comparison between the idle cell register and the header data in the ATM framer. A value of 1 enables the comparison with the corresponding bit in the ATM idle cell register.	0xFFFF
1080	15—0	ATM_IDM_0[31:16]	[31:24] is the MSByte of ATM_IDM_0.	0xFFFF
1081	15—0	ATM_IDM_0[15:0]	[7:0] is the LSByte of ATM_IDM_0.	0xFFFF
1082	15—0	ATM_IDM_1[31:16]	[31:24] is the MSByte of ATM_IDM_1.	0xFFFF
1083	15—0	ATM_IDM_1[15:0]	[7:0] is the LSByte of ATM_IDM_1.	0xFFFF
1084	15—0	ATM_IDM_2[31:16]	[31:24] is the MSByte of ATM_IDM_2.	0xFFFF
1085	15—0	ATM_IDM_2[15:0]	[7:0] is the LSByte of ATM_IDM_2.	0xFFFF
1086	15—0	ATM_IDM_3[31:16]	[31:24] is the MSByte of ATM_IDM_3.	0xFFFF
1087	15—0	ATM_IDM_3[15:0]	[7:0] is the LSByte of ATM_IDM_3.	0xFFFF

Table 109. Registers 0x1088—0x108F: ATM Idle Cell Registers (R/W)

Reset default of registers 0x1088, 0x108A, 0x108C, 0x108E = 0x0000.
Reset default of registers 0x1089, 0x108B, 0x108D, 0x108F = 0x0001.

Address (Hex)	Bit #	Name	Function	Reset Default
1088—108F	—	ATM_IDC_[0—3][31:0]	**ATM Idle Cell Register Channel [0—3].** This 32-bit register will store the expected header value for idle cells. If the ATM framer sees a header for an ATM packet which matches this register at the bit positions designated by the ATM idle cell match mask, the packet will be treated as an idle cell.	See below.
1088	15—0	ATM_IDC_0[31:16]	[31:24] is the MSByte of ATM_IDC_0.	0x0000
1089	15—0	ATM_IDC_0[15:0]	[7:0] is the LSByte of ATM_IDC_0.	0x0001
108A	15—0	ATM_IDC_1[31:16]	[31:24] is the MSByte of ATM_IDC_1.	0x0000
108B	15—0	ATM_IDC_1[15:0]	[7:0] is the LSByte of ATM_IDC_1.	0x0001
108C	15—0	ATM_IDC_2[31:16]	[31:24] is the MSByte of ATM_IDC_2.	0x0000
108D	15—0	ATM_IDC_2[15:0]	[7:0] is the LSByte of ATM_IDC_2.	0x0001
108E	15—0	ATM_IDC_3[31:16]	[31:24] is the MSByte of ATM_IDC_3.	0x0000
108F	15—0	ATM_IDC_3[15:0]	[7:0] is the LSByte of ATM_IDC_3.	0x0001

Register Descriptions (continued)

DE Registers (continued)

Table 110. Registers 0x1090—0x1097: ATM Unassigned Cell Match Mask (R/W)

Reset default of registers = 0xFFFF.

Address (Hex)	Bit #	Name	Function	Reset Default
1090—1097	—	ATM_USM_[0—3][31:0]	**ATM Unassigned Cell Match Mask Channel [0—3].** This 32-bit register defines which of the 32 bits will be used for comparison between the unassigned cell register and the header data in the ATM framer. A value of 1 enables the comparison with the corresponding bit in the ATM unassigned cell register.	0xFFFF
1090	15—0	ATM_USM_0[31:16]	[31:24] is the MSByte of ATM_USM_0.	0xFFFF
1091	15—0	ATM_USM_0[15:0]	[7:0] is the LSByte of ATM_USM_0.	0xFFFF
1092	15—0	ATM_USM_1[31:16]	[31:24] is the MSByte of ATM_USM_1.	0xFFFF
1093	15—0	ATM_USM_1[15:0]	[7:0] is the LSByte of ATM_USM_1.	0xFFFF
1094	15—0	ATM_USM_2[31:16]	[31:24] is the MSByte of ATM_USM_2.	0xFFFF
1095	15—0	ATM_USM_2[15:0]	[7:0] is the LSByte of ATM_USM_2.	0xFFFF
1096	15—0	ATM_USM_3[31:16]	[31:24] is the MSByte of ATM_USM_3.	0xFFFF
1097	15—0	ATM_USM_3[15:0]	[7:0] is the LSByte of ATM_USM_3.	0xFFFF

Table 111. Registers 0x1098—0x109F: ATM Unassigned Cell Registers (R/W)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
1098—109F	—	ATM_USG_[0—3][31:0]	**ATM Unassigned Cell Register Channel 0.** This 32-bit register will store the expected header value for unassigned cells. If the ATM framer sees a header for an ATM packet which matches this register at the bit positions designated by the ATM unassigned cell match mask, the packet will be treated as an unassigned cell.	0x0000
1098	15—0	ATM_USG_0[31:16]	[31:24] is the MSByte of ATM_USG_0.	0x0000
1099	15—0	ATM_USG_0[15:0]	[7:0] is the LSByte of ATM_USG_0.	0x0000
109A	15—0	ATM_USG_1[31:16]	[31:24] is the MSByte of ATM_USG_1.	0x0000
109B	15—0	ATM_USG_1[15:0]	[7:0] is the LSByte of ATM_USG_1.	0x0000
109C	15—0	ATM_USG_2[31:16]	[31:24] is the MSByte of ATM_USG_2.	0x0000
109D	15—0	ATM_USG_2[15:0]	[7:0] is the LSByte of ATM_USG_2.	0x0000
109E	15—0	ATM_USG_3[31:16]	[31:24] is the MSByte of ATM_USG_3.	0x0000
109F	15—0	ATM_USG_3[15:0]	[7:0] is the LSByte of ATM_USG_3.	0x0000

Register Descriptions (continued)

DE Registers (continued)

Table 112. Registers 0x10A0—0x10A3: ATM Framer State Registers (RO)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
10A0—10A3	—	ATM_ST_[0—3]	**Channel [0—3] ATM Scrambler Framer State.**	0x0000
	15—4	—	**Reserved.** These bits must be written to their reset default value (0x000).	0x000
	3—2	—	**ATM Framer Sync State.** These bits indicate the X31 sync state of each channel. ATM_ST_[0—3][3:2] = 00 Acquisition ATM_ST_[0—3][3:2] = 01 Verification ATM_ST_[0—3][3:2] = 10 Synchronized ATM_ST_[0—3][3:2] = 11 Undefined	00
	1—0	—	**ATM Frame State.** These bits indicate the frame state of each channel. ATM_ST_[0—3][1:0] = 00 Hunt ATM_ST_[0—3][1:0] = 01 Presync ATM_ST_[0—3][1:0] = 10 Sync ATM_ST_[0—3][1:0] = 11 Undefined	00

Table 113. Register 0x10A4: ATM X43 Frame Control (R/W)

Reset default of register = 0x01C6.

Address (Hex)	Bit #	Name	Function	Reset Default
10A4	—	ATM_X43[11:0]	**ATM X43 Frame Control.**	0x01C6
	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—6	—	**X43-Alpha.** This register will define the alpha value for the X43 alpha-delta framer which is the number of consecutive incorrect ATM cells that must be received in order to transition from the sync state to the hunt state.	000111
	5—0	—	**X43-Delta.** This register will define the delta value for the X43 alpha-delta framer which is the number of consecutive correct ATM cells that must be received in order to transition from the presync state to the sync state.	000110

Register Descriptions (continued)

DE Registers (continued)

Table 114. Register 0x10A5: ATM X31 Frame Control (R/W)

Reset default of register = 0x01C8.

Address (Hex)	Bit #	Name	Function	Reset Default
10A5	—	ATM_X31[11:0]	**ATM X31 Framer Control.**	0x01C8
	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—6	—	**X31-Alpha.** This register will define the alpha value for the X31 alpha-delta framer which is the number of consecutive incorrect ATM cells that must be received in order to transition from the sync state to the hunt state.	000111
	5—0	—	**X31-Delta.** This register will define the delta value for the X31 alpha-delta framer which is the number of consecutive correct ATM cells that must be received in order to transition from the presync state to the sync state.	001000

Table 115. Register 0x10A6: ATM X31 V/W Values (R/W)

Reset default of register = 0x0210.

Address (Hex)	Bit #	Name	Function	Reset Default
10A6	—	ATM_X31VW[11:0]	**X31 V and W Values.**	0x0210
	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—6	—	**X31 V Value.** This register specifies the value the confidence counter in the X^{31} scrambler synchronization process must drop below in order to transition to the acquisition state from the verification state. The confidence counter is incremented every time the local scrambler samples match the received samples, and decremented when they do not (see standard I.432).	001000
	5—0	—	**X31 W Value.** This register specifies the value the confidence counter in the X^{31} scrambler synchronization process must drop below in order to declare loss of synchronization and transition to the acquisition state. The confidence counter is incremented every time the local scrambler samples match the received samples, and decremented when they do not (see standard I.432).	010000

Register Descriptions (continued)

DE Registers (continued)

Table 116. Register 0x10A7: ATM X31 X/Y Values (R/W)

Reset default of register = 0x0418.

Address (Hex)	Bit #	Name	Function	Reset Default
10A7	—	ATM_X31XY[11:0]	**X31 X and Y Values.**	0x0418
	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—6	—	**X31 X Value.** This register specifies the minimum value the confidence counter in the X^{31} scrambler synchronization process must reach in order to transition to the verification state from the acquisition state. The confidence counter is incremented every time the local scrambler samples match the received samples, and decremented when they do not (see standard I.432).	010000
	5—0	—	**X31 Y Value.** This register specifies the minimum value the confidence counter in the X^{31} scrambler synchronization process must reach in order to transition to the synchronized state from the verification state. The confidence counter is incremented every time the local scrambler samples match the received samples, and decremented when they do not (see standard I.432).	011000

Table 117. Register 0x10A8: ATM X31 Z Value (R/W)

Reset default of register = 0x0018.

Address (Hex)	Bit #	Name	Function	Reset Default
10A8	—	ATM_X31Z[5:0]	**X31 Z Value.**	0x0018
	15—6	—	**Reserved.** These bits must be written to their reset default value (0000000000).	00 0000 0000
	5—0	—	**X31 Z Value.** This register specifies the maximum value the confidence counter in the X^{31} scrambler synchronization process can achieve. The confidence counter is incremented every time the local scrambler samples match the received samples, and decremented when they do not (see standard I.432).	011000

Register Descriptions (continued)

DE Registers (continued)

Table 118. Register 0x10A9: Frame State Interrupt Mask (R/W)

Reset default of register = 0x000F.

Address (Hex)	Bit #	Name	Function	Reset Default
10A9	—	FS_INT_MASK[3:0]	**Frame State Interrupt Mask.** When active (logic 1), the associated event/delta is inhibited from contributing to the interrupt on a per-channel basis. Otherwise, an interrupt is generated when the ATM frame state transitions from sync to hunt state.	0x000F
	15—4	—	**Reserved.** These bits must be written to their reset default value (0x000).	0x000
	3	—	**Channel 3 Mask Value.**	1
	2	—	**Channel 2 Mask Value.**	1
	1	—	**Channel 1 Mask Value.**	1
	0	—	**Channel 0 Mask Value.**	1

Table 119. Register 0x10AA: Scrambler State Interrupt Mask (R/W)

Reset default of register = 0x000F.

Address (Hex)	Bit #	Name	Function	Reset Default
10AA	—	SS_INT_MASK[3:0]	**Scrambler State Interrupt Mask.** When active (logic 1), the associated event/delta is inhibited from contributing to the interrupt on a per-channel basis. Otherwise, an interrupt is generated when the ATM frame state transitions from synchronization to verification state.	0x000F
	15—4	—	**Reserved.** These bits must be written to their reset default value (0x000).	0x000
	3	—	**Channel 3 Mask Value.**	1
	2	—	**Channel 2 Mask Value.**	1
	1	—	**Channel 1 Mask Value.**	1
	0	—	**Channel 0 Mask Value.**	1

Register Descriptions (continued)

DE Registers (continued)

Table 120. Register 0x10AB: ATM Receive Debug Register (R/W)

Reset default of register = 0x003C.

Address (Hex)	Bit #	Name	Function	Reset Default
10AB	—	ATM_Rx_DEBUG_REG[5:0]	**ATM Receive Debug Register.**	0x003C
	15—6	—	**Reserved.** These bits must be written to their reset default value (0000000000).	00 0000 0000
	5	—	**Channel 3 All Cool-Interrupt Mask Value.** When active (logic 1), the associated event/ delta is inhibited from contributing to the interrupt on a per-channel basis.	1
	4	—	**Channel 2 All-Cool Interrupt Mask Value.** When active (logic 1), the associated event/ delta is inhibited from contributing to the interrupt on a per-channel basis.	1
	3	—	**Channel 1 All-Cool Interrupt Mask Value.** When active (logic 1), the associated event/ delta is inhibited from contributing to the interrupt on a per-channel basis.	1
	2	—	**Channel 0 All-Cool Interrupt Mask Value.** When active (logic 1), the associated event/ delta is inhibited from contributing to the interrupt on a per-channel basis.	1
	1	—	**Incrementing NULL Cell Payload Sequence.** This bit governs whether 0x6A is used for the payload of NULL cells, or whether an incrementing 8-bit count is used (0x00 → 0xFF). A value of 1 selects the incrementing sequence. This can be used with the All_Cool interrupt.	0
	0	—	**X31_Sync_Compare.** In X^{31} mode, when this value is 0, the ATM framer does 6-bit comparisons of the HEC, which does not allow for error correction. When this value is 1, all 8 bits of the HEC are used, which does allow for error correction.	0

Register Descriptions (continued)

DE Registers (continued)

Table 121. Registers 0x10B0—0x10B3: PPP Attach (R/W)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
10B0—10B3	15—0	PPP_Tx_CHAN[0—3]	**Channel [0—3] PPP Header.** This register defines the 2 bytes that will be generated as the PPP header in compressed header PPP mode. In uncompressed header PPP mode, they will serve as the third and fourth bytes of the 4-byte header, with 0xFF03 being the first and second bytes.	0x0000

Table 122. Registers 0x10E0—0x10E3: Egress Payload Type and Mode Control (R/W)

Reset default of registers = 0x0700.

Address (Hex)	Bit #	Name	Function	Reset Default
10E0—10E3	—	Tx_PCTL_[0—3][10:0]	**Channel [0—3] Payload Type and Control.** See Table 123 for transmit type and mode control summary.	0x0700
	15—11	—	**Reserved.** These bits must be written to their reset default value (00000).	00000
	10—8	—	**Payload Type.** Defines the payload type being received.	111
	7—0	—	**Payload Control.** Allows for different options when transmitting data, such as pre- or postscrambling, dry mode, PPP header discard, etc.	0x00

Register Descriptions (continued)

DE Registers (continued)

Table 123. Transmit Type and Mode Control Summary Table (Registers 0x10E0—0x10E3)

Note: In the table below, X indicates the bit may either be 0 or 1.

Payload Type, Bits [10:8]	Payload Control, Bits [7:0]							
	7	6	5	4	3	2	1	0
000 PPP	0 = compression 1 = no compression	0	0 = CRC-16 1 = CRC-32	0	0 = CRC reversed 1 = CRC normal	0 = no dry mode 1 = dry mode	00 = no scrambling 01 = postscrambling 10 = pre-scrambling 11 = undefined	
001 HDLC with CRC	0	0	0 = CRC-16 1 = CRC-32	0	0 = CRC reversed 1 = CRC normal	0 = no dry mode 1 = dry mode	00 = no scrambling 01 = postscrambling 10 = prescrambling 11 = undefined	
010 HDLC without CRC	0	0	0	0	0	0 = no dry mode 1 = dry mode	00 = no scrambling 01 = postscrambling 10 = prescrambling 11 = undefined	
011 ATM	0	0	00 = X^{43} scrambling 01 = no scrambling 10 = X^{31} scrambling 11 = no scrambling		0	0	0	0
100 SDL without CRC	X	X	X	X	X	X	X	X
101 SDL with CRC	0	0	0 = CRC-16 1 = CRC-32	0	0	0	0	0
110 Transparent payload	0	0	0	0	0	0	0	0
111 Not defined (reset mode)	0	0	0	0	0	0	0	0

Table 124. Registers 0x10F0—10FB: PPP Header Value Detach (R/W)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
10F0—10FB	15—0	PPP_Rx_HDR0 [0—11][15:0]	**Register [0—11] PPP Header.** This register defines the 2 bytes that can be used by all four channels to validate a PPP packet. By programming registers 0x0FC—0x0FF, any of the channels can compare any received headers to this value. If there is a mismatch, then the bad header counters will increment.	0x0000

Register Descriptions (continued)

DE Registers (continued)

Table 125. Registers 0x10FC—0x10FF: PPP Header Detach Search (R/W)

Reset default of register 10FC = 0xC001.
Reset default of register 10FD = 0xC002.
Reset default of register 10FE = 0xC004.
Reset default of register 10FF = 0xC008.

Address (Hex)	Bit #	Name	Function	Reset Default
10FC—10FF	—	PPP_Rx_CHK_CH [0—3][15:0]	**Channel [0—3] PPP Header Search.** This register will control the headers that channel 0 PPP detach block looks for. If there is a mismatch, a bad header will be noted in a separate counter.	See below.
	15—14	—	Controls the way the PPP headers are searched for and passed through. 00 = Pass any 32-bit header where the first 16 bits are 0xFF03. 01 = Pass only specified uncompressed patterns (first 16 bits are 0xFF03; last 16 bits are defined by fixed patterns and/or register values). See below. 10 = Pass only specified compressed pattern (all 16 bits are defined by fixed patterns and/or register values). See below. 11 = Pass any pattern defined by fixed patterns and/or registers values. See below.	11
	13	—	A value of 1 in this bit will enable a search for the 16-bit fixed value 0x8021.	0
	12	—	A value of 1 in this bit will enable a search for the 16-bit fixed value 0x0021.	0
	11	—	A value of 1 in this bit will enable a search of the 16-bit value in register address 0x10FB.	0
	10	—	A value of 1 in this bit will enable a search of the 16-bit value in register address 0x10FA.	0
	9	—	A value of 1 in this bit will enable a search of the 16-bit value in register address 0x10F9.	0
	8	—	A value of 1 in this bit will enable a search of the 16-bit value in register address 0x10F8.	0
	7	—	A value of 1 in this bit will enable a search of the 16-bit value in register address 0x10F7.	0
	6	—	A value of 1 in this bit will enable a search of the 16-bit value in register address 0x10F6.	0
	5	—	A value of 1 in this bit will enable a search of the 16-bit value in register address 0x10F5.	0
	4	—	A value of 1 in this bit will enable a search of the 16-bit value in register address 0x10F4.	0

Register Descriptions (continued)

DE Registers (continued)

Table 125. Registers 0x10FC—0x10FF: PPP Header Detach Search (R/W) (continued)

Reset default of register 10FC = 0xC001.
Reset default of register 10FD = 0xC002.
Reset default of register 10FE = 0xC004.
Reset default of register 10FF = 0xC008.

Address (Hex)	Bit #	Name	Function	Reset Default
10FC	3	—	A value of 1 in this bit will enable a search of the 16-bit value in register address 0x10F3.	0
10FD		—		0
10FE		—		0
10FF		—		1
10FC	2	—	A value of 1 in this bit will enable a search of the 16-bit value in register address 0x10F2.	0
10FD		—		0
10FE		—		1
10FF		—		0
10FC	1	—	A value of 1 in this bit will enable a search of the 16-bit value in register address 0x10F1.	0
10FD		—		1
10FE		—		0
10FF		—		0
10FC	0	—	A value of 1 in this bit will enable a search of the 16-bit value in register address 0x10F0.	1
10FD		—		0
10FE		—		0
10FF		—		0

Register Descriptions (continued)

DE Registers (continued)

Table 126. Registers 0x1100—0x1107: ATM/HDLC/SDL Framer—Condition Counter 1 (PMRST Update) (RO)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
1100—1107	—	PM_FC1_[0—3][27:0]	**ATM/HDLC/SDL Counter 1 Channel [0—3].** Keeps a count of conditions detected by the data framer in the particular channel. This register can represent only one of the following based upon the channel's payload type: ■ HDLC invalid sequences (as defined in IETF RFC 1622 below) ■ ATM corrected cells ■ SDL corrected header This value is updated upon assertion of PMRST and the real-time counter value is reset to zero. From IETF RFC 1622, invalid sequences are: 1. Frames which are too short (less than 4 data bytes). See register PM_FC2_0 (addresses 0x1108—0x110F). 2. Frames which end with a control escape octet followed immediately by a coding flag sequence (0x7D7E). 3. Frames in which octet framing is violated by transmitting a 0 stop bit where a 1 bit is expected.	0x0000
1100	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—0	PM_FC1_0[27:16]	[11:4] is the MSByte of PM_FC1_0.	0x000
1101	15—0	PM_FC1_0[15:0]	[7:0] is the LSByte of PM_FC1_0.	0x0000
1102	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—0	PM_FC1_1[27:16]	[11:4] is the MSByte PM_FC1_1.	0x000
1103	15—0	PM_FC1_1[15:0]	[7:0] is the LSByte of PM_FC1_1.	0x0000
1104	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—0	PM_FC1_2[27:16]	[11:4] is the MSByte of PM_FC1_2.	0x000
1105	15—0	PM_FC1_2[15:0]	[7:0] is the LSByte of PM_FC1_2.	0x0000
1106	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—0	PM_FC1_3[27:16]	[11:4] is the MSByte of PM_FC1_3.	0x000
1107	15—0	PM_FC1_3[15:0]	[7:0] is the LSByte of PM_FC1_3.	0x0000

Register Descriptions (continued)

DE Registers (continued)

**Table 127. Registers 0x1108—0x110F:
ATM/HDLC/SDL Framer—Condition Counter 2 (PMRST Update) (RO)**

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
1108—110F	—	PM_FC2_[0—3][27:0]	**ATM/HDLC/SDL Counter 2 Channel [0—3].** Keeps a count of conditions detected by the data framer in the particular channel. This register can represent only one of the following based upon the channel's payload type: ■ HDLC short packets (packet < 4 data bytes) ■ ATM discarded cells ■ SDL errored header This value is updated upon PMRST and the real-time counter value is reset to zero.	0x0000
1108	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—0	PM_FC2_0[27:16]	[11:4] is the MSByte of PM_FC2_0.	0x000
1109	15—0	PM_FC2_0[15:0]	[7:0] is the LSByte of PM_FC2_0.	0x0000
110A	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—0	PM_FC2_1[27:16]	[11:4] is the MSByte of PM_FC2_1.	0x000
110B	15—0	PM_FC2_1[15:0]	[7:0] is the LSByte of PM_FC2_1.	0x0000
110C	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—0	PM_FC2_2[27:16]	[11:4] is the MSByte of PM_FC2_2.	0x000
110D	15—0	PM_FC2_2[15:0]	[7:0] is the LSByte of PM_FC2_2.	0x0000
110E	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—0	PM_FC2_3[27:16]	[11:4] is the MSByte of PM_FC2_3.	0x000
110F	15—0	PM_FC2_3[15:0]	[7:0] is the LSByte of PM_FC2_3.	0x0000

Register Descriptions (continued)

DE Registers (continued)

Table 128. Registers 0x1110—0x1117: CRC Checker—Bad Packet Counter (PMRST Update) (RO)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
1110—1117	—	PM_BPC_[0—3][27:0]	**CRC Bad Packet Counter Channel [0—3].** Keeps a count of bad packets detected by the CRC checker. This value is updated upon PMRST and the real-time counter value is reset to zero.	0x0000
1110	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—0	PM_BPC_0[27:16]	[11:4] is the MSByte of PM_BPC_0.	0x000
1111	15—0	PM_BPC_0[15:0]	[7:0] is the LSByte of PM_BPC_0.	0x0000
1112	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—0	PM_BPC_1[27:16]	[11:4] is the MSByte of PM_BPC_1.	0x000
1113	15—0	PM_BPC_1[15:0]	[7:0] is the LSByte of PM_BPC_1.	0x0000
1114	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—0	PM_BPC_2[27:16]	[11:4] is the MSByte of PM_BPC_2.	0x000
1115	15—0	PM_BPC_2[15:0]	[7:0] is the LSByte of PM_BPC_2.	0x0000
1116	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—0	PM_BPC_3[27:16]	[11:4] is the MSByte of PM_BPC_3	0x000
1117	15—0	PM_BPC_3[15:0]	[7:0] is the LSByte of PM_BPC_3	0x0000

Register Descriptions (continued)

DE Registers (continued)

Table 129. Registers 0x1118—0x111F: PPP Detach—Mismatched Header Counter (PMRST Update) (RO)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
1118—111F	—	PM_BHC_[0—3][27:0]	**PPP Mismatched Header Counter Channel [0—3].** Keeps a count of packets with a mismatched header detected by the PPP detach block. This value is updated upon PMRST and the real-time counter value is reset to zero.	0x0000
1118	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—0	PM_BHC_0[27:16]	[11:4] is the MSByte of PM_BHC_0.	0x000
1119	15—0	PM_BHC_0[15:0]	[7:0] is the LSByte of PM_BHC_0.	0x0000
111A	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—0	PM_BHC_1[27:16]	[11:4] is the MSByte of PM_BHC_1.	0x000
111B	15—0	PM_BHC_1[15:0]	[7:0] is the LSByte of PM_BHC_1.	0x0000
111C	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—0	PM_BHC_2[27:16]	[11:4] is the MSByte of PM_BHC_2.	0x000
111D	15—0	PM_BHC_2[15:0]	[7:0] is the LSByte of PM_BHC_2.	0x0000
111E	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—0	PM_BHC_3[27:16]	[11:4] is the MSByte of PM_BHC_3.	0x000
111F	15—0	PM_BHC_3[15:0]	[7:0] is the LSByte of PM_BHC_3.	0x0000

Register Descriptions (continued)

DE Registers (continued)

Table 130. Registers 0x1120—0x1127: Receive Good Packet/Cell Counter (PMRST Update) (RO)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
1120—1127	—	PM_GPC_RX_[0—3] [27:0]	**Good Packet/Cell Counter Channel [0—3].** Keeps a count of good packets detected by the receive data engine. This value is updated upon PMRST and the real-time counter value is reset to zero. In ATM mode, this counter counts the number of good ATM cells received.	0x0000
1120	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—0	PM_GPC_RX_0[27:16]	[11:4] is the MSByte of PM_GPC_RX_0.	0x000
1121	15—0	PM_GPC_RX_0[15:0]	[7:0] is the LSByte of PM_GPC_RX_0.	0x0000
1122	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—0	PM_GPC_RX_1[27:16]	[11:4] is the MSByte of PM_GPC_RX_1.	0x000
1123	15—0	PM_GPC_RX_1[15:0]	[7:0] is the LSByte of PM_GPC_RX_1.	0x0000
1124	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—0	PM_GPC_RX_2[27:16]	[11:4] is the MSByte of PM_GPC_RX_2.	0x000
1125	15—0	PM_GPC_RX_2[15:0]	[7:0] is the LSByte of PM_GPC_RX_2.	0x0000
1126	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—0	PM_GPC_RX_3[27:16]	[11:4] is the MSByte of PM_GPC_RX_3.	0x000
1127	15—0	PM_GPC_RX_3[15:0]	[7:0] is the LSByte of PM_GPC_RX_3.	0x0000

Register Descriptions (continued)

DE Registers (continued)

Table 131. Registers 0x1128—0x112F: Transmit Good Packet/Cell Counter (PMRST Update) (RO)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
1128—112F	—	PM_GPC_TX_[0—3] [27:0]	**Good Packet/Cell Counter Channel [0—3].** Keeps a count of good packets detected by the transmit data engine. This value is updated upon PMRST and the real-time counter value is reset to zero. In ATM mode, this counter counts the number of good ATM cells transmitted.	0x0000
1128	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—0	PM_GPC_TX_0[27:16]	[11:4] is the MSByte of PM_GPC_TX_0.	0x000
1129	15—0	PM_GPC_TX_0[15:0]	[7:0] is the LSByte of PM_GPC_TX_0.	0x0000
112A	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—0	PM_GPC_TX_1[27:16]	[11:4] is the MSByte of PM_GPC_TX_1.	0x000
112B	15—0	PM_GPC_TX_1[15:0]	[7:0] is the LSByte of PM_GPC_TX_1.	0x0000
112C	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—0	PM_GPC_TX_2[27:16]	[11:4] is the MSByte of PM_GPC_TX_2.	0x000
112D	15—0	PM_GPC_TX_2[15:0]	[7:0] is the LSByte of PM_GPC_TX_2.	0x0000
112E	15—12	—	**Reserved.** These bits must be written to their reset default value (0x0).	0x0
	11—0	PM_GPC_TX_3[27:16]	[11:4] is the MSByte of PM_GPC_TX_3.	0x000
112F	15—0	PM_GPC_TX_3[15:0]	[7:0] is the LSByte of PM_GPC_TX_3.	0x0000

Table 132. Registers 0x1180—0x1186: Interrupt Masks for Packet Counters (R/W)

Reset default of registers = 0x001F.

Address (Hex)	Bit #	Name	Function	Reset Default
1180, 1182, 1184, 1186	—	DEDINTM[0—3]	**Data Interrupt Mask Channel [0—3].** When active (logic 1), the associated event/delta is inhibited from contributing to the interrupt on a per-channel basis.	0x001F
	15—5	—	**Reserved.** These bits must be written to their reset default value (00000000000).	000 0000 0000
	4	—	**Rx-Side Good Packet.**	1
	3	—	**PPP Bad Header.**	1
	2	—	**CRC Bad Packet.**	1
	1	—	**ATM/HDLC/SDL Counter 2.**	1
	0	—	**ATM/HDLC/SDL Counter 1.**	1

Register Descriptions (continued)

DE Registers (continued)

Table 133. Registers 0x1181—0x1187: Interrupts for Packet Counters (COR/W)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
1181, 1183, 1185, 1187	—	DEDINT[0—3]	**Data Interrupt Channel [0—3].** Stores bits that describe which conditions of corrupted data exist in channel [0—3].	0x0000
	15—5	—	**Reserved.** These bits must be written to their reset default value (00000000000).	000 0000 0000
	4	—	**Rx-Side Good Packet.**	0
	3	—	**PPP Bad Header.**	0
	2	—	**CRC Bad Packet.**	0
	1	—	**ATM/HDLC/SDL Counter 2.**	0
	0	—	**ATM/HDLC/SDL Counter 1.**	0

Table 134. Registers 0x1200—0x1213, 0x12F0: ATM Transmit Registers (R/W)

Reset default of registers 0x1200—0x1203, 0x12F0 = 0x0000.
Reset default of registers 0x1210—0x1213 = 0x0001.

Address (Hex)	Bit #	Name	Function	Reset Default
1200, 1201, 1202, 1203	15—0	NULLCELL1[0—3]	**ATM Null (Idle) Cell MSB Channel [0—3].** This defines the first 2 bytes of a NULL ATM cell (i.e., 15:0 = h0h1).	0x0000
1210, 1211, 1212, 1213	15—0	NULLCELL2[0—3]	**ATM Null (Idle) Cell LSB Channel [0—3].** This defines the second 2 bytes of a NULL ATM cell (i.e., 15:0 = h2h3).	0x0001

Register Descriptions (continued)

DE Registers (continued)

Table 134. Registers 0x1200—0x1213, 0x12F0: ATM Transmit Registers (R/W) (continued)

Reset default of registers 0x1200—0x1203, 0x12F0 = 0x0000.
Reset default of registers 0x1210—0x1213 = 0x0001.

Address (Hex)	Bit #	Name	Function	Reset Default
12F0	—	ATM_HEADER_ERROR	**ATM Tx Debug Control.** Used for debug purposes to inject errors, and to increment the payload sequence for NULL cells.	0x0000
	15—8	—	**Reserved.** These bits must be written to their reset default value (0x00).	0x00
	7	—	**Incrementing Null (Idle) Cell Payload Sequence.** This bit governs whether 0x6A is used for the payload of NULL cells, or whether an incrementing 8-bit count is used (0x00 → 0xFF). A value of 1 selects the incrementing sequence. This is used with DE register 0x1002 bits [11:8].	0
	6	—	**Error Strobe.** Writing a value of 1 to this register initiates the injection of a single or double shot error injection, assuming one of these two modes is selected.	0
	5—4	—	**Error Injection Mode.** These bits control the mode of operation of the error injection. 00 = continuous injection 01 = single shot (isolated cell) 10, 11 = double shot (i.e., two back-to-back cells)	00
	3—2	—	**Error Type.** These bits control the injection of a walking error pattern into the headers of all outgoing cells. 00 = no errors 01 = single bit errors 10, 11 = double bit errors	00
	1—0	—	**Error Channel ID.** The logical channel in which to inject the header errors.	00

Register Descriptions (continued)

DE Registers (continued)

Table 135. Registers 0x1400—0x1403: SDL State Registers (RO)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
1400, 1401, 1402, 1403	—	SDL_ST[0—3]	**SDL State Channel [0—3].** These registers describe the SDL framer and scrambler states.	0x0000
	15—4	—	**Reserved.** These bits must be written to their reset default value (0x000).	0x000
	3—2	—	**SDL Frame State.** Indicates the frame state of each channel. SDL_ST[0—3][3:2] = 00. **Out-of-Frame.** The SDL framer is in search of a successful SDL framing. SDL_ST[0—3][3:2] = 01. **Presync.** The SDL framer has transitioned from the out of frame to the presync state. The SDL framer has successfully framed one SDL header. SDL_ST[0—3][3:2] = 10. **Sync.** The SDL framer has transitioned from the presync to the sync state. The framer has successfully detected the second consecutive SDL packet. The SDL framer is correctly framed on the SDL signal. The SDL framer remains in the sync state until a bad packet frame is detected. Detection of a bad packet frame places the SDL framer in the out-of-frame state. SDL_ST[0—3][3:2] = 11. **Undefined.**	00
	1—0	—	**SDL Scram State.** Indicates the X48 sync state of each channel. SDL_ST[0—3][1:0] = 00. **Hunt.** The SDL scrambler has yet to detect a valid scrambler state. SDL_ST[0—3][1:0] = 01. **Sync.** The SDL scrambler is in sync. SDL_ST[0—3][1:0] = 10. **Postsync.** The SDL scrambler was in sync, but detected an SDL state that did not match the expected state. If two consecutive non-matching states are detected, then (1) the SDL framer is reset with the scrambler state received in the bit stream, and (2) a sync slip interrupt is generated. SDL_ST[0—3][1:0] = 11. **Undefined.**	00

Register Descriptions (continued)

DE Registers (continued)

Table 136. Registers 0x1470—0x1473: A Message Mailbox Registers (RO)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
1470, 1471, 1472, 1473	15—0	SDL_AMM1[0—3]	**A Message Mailbox 1: Channel [0—3].** These registers will store the first 16 bits of a valid A message header. A maskable interrupt will be generated if the SDL framer receives an A message.	0x0000

Table 137. Registers 0x1480—0x1483: A Message Mailbox Registers (RO)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
1480, 1481, 1482, 1483	15—0	SDL_AMM2[0—3]	**A Message Mailbox 2: Channel [0—3].** These registers will store the middle 16 bits of a valid A message header. A maskable interrupt will be generated if the SDL framer receives an A message.	0x0000

Table 138. Registers 0x1490—0x1493: A Message Mailbox Registers (RO)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
1490, 1491, 1492, 1493	15—0	SDL_AMM3[0—3]	**A Message Mailbox 3: Channel [0—3].** These registers will store the last 16 bits of a valid A message header. A maskable interrupt will be generated if the SDL framer receives an A message.	0x0000

Table 139. Registers 0x14A0—0x14A3: B Message Mailbox Registers (RO)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
14A0, 14A1, 14A2, 14A3	15—0	SDL_BMM1[0—3]	**B Message Mailbox 1: Channel [0—3].** These registers will store the first 16 bits of a valid B message header. A maskable interrupt will be generated if the SDL framer receives a B message.	0x0000

Register Descriptions (continued)

DE Registers (continued)

Table 140. Registers 0x14B0—0x14B3: B Message Mailbox Registers (RO)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
14B0, 14B1, 14B2, 14B3	15—0	SDL_BMM2[0—3]	**B Message Mailbox 2: Channel [0—3].** These registers will store the middle 16 bits of a valid B message header. A maskable interrupt will be generated if the SDL framer receives a B message.	0x0000

Table 141. Registers 0x14C0— 0x14C3: B Message Mailbox Registers (RO)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
14C0, 14C1, 14C2, 14C3	15—0	SDL_BMM3[0—3]	**B Message Mailbox 3: Channel [0—3].** These registers will store the last 16 bits of a valid B message header. A maskable interrupt will be generated if the SDL framer receives a B message.	0x0000

Table 142. Registers 0x14D0—0x14D3: SDL Interrupt Masks (R/W)

Reset default of registers = 0x00FF.

Address (Hex)	Bit #	Name	Function	Reset Default
14D0, 14D1, 14D2, 14D3	—	SDLINTM[0—3]	**SDL Interrupt Mask Channel [0—3].** When active (logic 1), the associated event/delta is inhibited from contributing to the interrupt on a per-channel basis.	0x00FF
	15—8	—	**Reserved.** These bits must be written to their reset default value (0x00).	0x00
	7	—	**B_Message Reception.**	1
	6	—	**A_Message Reception.**	1
	5	—	**Uncorrectable Special Payload Error.**	1
	4	—	**Uncorrectable Bit Error.**	1
	3	—	**Reserved.** This bit must be written to its reset default value (1).	1
	2	—	**Single Bit Error.**	1
	1	—	**Scrambler Out of Sync.**	1
	0	—	**Framer Out of Sync.**	1

Register Descriptions (continued)

DE Registers (continued)

Table 143. Registers 0x14E0—0x14E3: SDL Interrupts (COR/W)

Reset default of registers = 0x0000.

Address (Hex)	Bit #	Name	Function	Reset Default
14E0, 14E1, 14E2, 14E3	—	SDLINT[0—3]	**SDL Interrupt Channel [0—3].** Used to record various occurrences within the SDL framer. The bits will generate an interrupt if defined by the interrupt mask, but the register values here are independent of the interrupt mask values.	0x0000
	15—8	—	**Reserved.** These bits must be written to their reset default value (0x00).	0x00
	7	—	**B_Message Reception.**	0
	6	—	**A_Message Reception.**	0
	5	—	**Uncorrectable Special Payload Error.** Indicates occurrence of two or more special payload errors.	0
	4	—	**Uncorrectable Header Bit Error.** Indicates occurrence of two or more header errors.	0
	3	—	**Reserved.** This bit must be written to its reset default value (0).	0
	2	—	**Single Bit Header Error.**	0
	1	—	**Scrambler Out of Sync.** Indicates a scrambler sync slip.	0
	0	—	**Framer Out of Sync.**	0

Table 144. Register 0x14F0: SDL Receive Configuration Registers (R/W)

Reset default of registers = 0x0001.

Address (Hex)	Bit #	Name	Function	Reset Default
14F0	—	SDL_DELTA	**SDL Receive Frame Configuration Register.**	0x0001
	15—7	—	**Reserved.** These bits must be written to their reset default value (000000000).	0000 00000
	6	—	**Disable Scrambling.** When this value is 1, the SDL framer will not unscramble the data prior to framing.	0
	5	—	**Reserved.** These bits must be written to their reset default value (0).	0
	4	—	**Sync Mode.** When bit 4 has a value of 1, then only one framer is used at all times to frame SDL data. Normally, this bit is 0, and four coordinated framers are active simultaneously to synchronize the scrambler process.	0
	3—0	—	**Framer Delta.** This register will define the delta value for the CRC-16 framer.	0x1

Register Descriptions (continued)

DE Registers (continued)

Table 145. Registers 0x1600—0x1607: SDL Transmit Registers (R/W)

Reset default of registers 0x1600, 0x1601, 0x1602, 0x1603, 0x1606 = 0x000.
Reset default of register 0x1604 = 0x0008.
Reset default of register 0x1605 = 0x8000.

Note: These registers must be written in the following order: 0x1603, then 0x1600, 0x1601, 0x1602.

Address (Hex)	Bit #	Name	Function	Reset Default
1600	15—0	SDLFI_MSG1	**SDL Message.** These registers will store the first 16 bits of a header of an outgoing A or B message.	0x0000
1601	15—0	SDLFI_MSG2	**SDL Message.** These registers will store the middle 16 bits of a header of an outgoing A or B message.	0x0000
1602	15—0	SDLFI_MSG3	**SDL Message.** These registers will store the last 16 bits of a header of an outgoing A or B message. Writing to this register causes the message to be sent.	0x0000
1603	—	SDLFI_MSG_TYPE	**SDL Message Type.**	0x0000
	15	SDLMTB	**Message Type Bit.** 0 = A Message 1 = B Message	0
	14—2	—	**Reserved.** These bits must be written to their reset default value (0000000000000).	0 0000 0000 0000
	1—0	SDLCHID[1:0]	**Channel ID.** Defines on which channel the special message will be transmitted.	00
1604	15—0	SDLFI_INT	**SDL State Transmit Interval.** Defines the number of packets (or dWords) separating scrambler state transmissions. Use register 1605 to determine if units are packets or dwords.	0x0008
1605	—	SDLFI_MODE	**SDL State Transmit Mode.**	0x8000
	15	SDLSMIE	**Special Message Interrupt Enable.** The SDL line transmitter generates an interrupt when transmission of a special message is complete. In this case, used to signal the sending of a special message (A or B message).	1
	14—2	—	**Reserved.** These bits must be written to their reset default value (0000000000000).	0 0000 0000 0000
	1	SDLSC	**Scrambler Control.** 1 = disables data scrambling 0 = enables data scrambling	0
	0	SDLSSTMS	**Scrambler State Transmit Mode Select.** 0 = packets 1 = dWord (32 bits)	0

Table 145. Registers 0x1600—0x1607: SDL Transmit Registers (R/W) (continued)

Reset default of registers 0x1600, 0x1601, 0x1602, 0x1603, 0x1606 = 0x000.
Reset default of register 0x1604 = 0x0008.
Reset default of register 0x1605 = 0x8000.

Note: These registers must be written in the following order: 0x1603, then 0x1600, 0x1601, 0x1602.

Address (Hex)	Bit #	Name	Function	Reset Default
1606	—	SDLFI_INTR	**Status Register.**	0x0000
	15—2	—	**Reserved.** These bits must be written to their reset default value (00000000000000).	00 0000 0000 0000
	1	SDLFDO	**SDLFIFO Depth Out.** When this bit has a value of 1, it indicates that the FIFO in the SDL Tx data buffer is over half full.	0
	0	SDLMSI	**Message Sent Interrupt.** When this bit has a value of 1, it indicates that an SDL A/B message has been sent. This value may be cleared when read or written.	0
1607	—	SDLFI_DEBUG	**SDL Debug Register.**	0x0000
	15—6	—	**Reserved.** These bits must be written to their reset default value (0000000000).	00 0000 0000
	5—4	SDLHE[1:0]	**Header Error.** This value indicates the number of errors to insert into the SDL header on a given channel for debug purposes. The error injection is done using a walking ones pattern to cover all possibilities. 0x0 = no errors 0x1 = single error 0x2 = double error 0x3 = double error	00
	3—2	SDLPE[1:0]	**Payload Error.** This value indicates the number of errors to insert into the payload of special packets on a given channel for debug purposes. The error injection is done using a walking ones pattern to cover all possibilities. 00 = no errors 01 = single error 10 = double error 11 = double error	00
	1—0	SDLECID[1:0]	**Error Channel ID.** This value specifies the channel on which the errors are to be sent.	00

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent or latent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of this device specification. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Min	Max	Unit
Power Supply Voltage	–0.5	4.2	V
Storage Temperature	–65	125	°C
Pin Voltage (3.3 V)	GND – 0.5	V_{DD} + 0.5	V
Pin Voltage (5 V tolerant)	GND – 0.5	5.5	V

Note: $V_{DD} = V_{DDA} = V_{DDD}$.

Handling Precautions

Although protection circuitry has been designed into this device, proper precautions should be taken to avoid exposure to electrostatic discharge (ESD) during handling and mounting. Lucent employs a human-body model (HBM) and charged-device model (CDM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in the defined model. No industry-wide standard has been adopted for the CDM. However, a standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes:

Device	Voltage
TDAT042G5	TBD

Operating Conditions

Table 146. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply (dc voltage)	V_{DD}	3.135	3.3	3.465	V
Ground	—	—	—	—	V
Input Voltage:		—			
Low	V_{IL}		GND	1.0	V
High	V_{IH}		V_{DD} – 1.0	V_{DD}	V
Ambient Temperature	—	–40	—	85	°C
Power Dissipation	P_D	—	—	7.8	W

Note: $V_{DD} = V_{DDA} = V_{DDD}$.

Electrical Characteristics

The following characteristics are guaranteed over the recommended operating conditions, unless otherwise specified in the test conditions.

Table 147. 3.3 V Logic Interface Characteristics

These logic levels are TTL 5 V compliant.

Parameter	Symbol	Test Conditions	Min	Max	Unit
Input Leakage	I_L	—	—	1.0	µA
Output Voltage:					
Low	V_{OL}	–5.0 mA	GND	0.5	V
High	V_{OH}	5.0 mA	V_{DD} – 1.0	V_{DD}	V
Input Capacitance	C_I	—	—	—	pF
Load Capacitance	C_L	—	—	—	pF

Note: $V_{DD} = V_{DDA} = V_{DDD}$.

Table 148. LVPECL Interface Characteristics

The range for V_{DD} in this table is as follows: 3.0 V < V_{DD} < 3.63 V, and V_{DD} nominal = 3.30 V.

Parameter	Symbol	Test Conditions	Min	Nominal	Max	Unit
Output Voltage:						
Low	V_{OL}	—	V_{DD} – 1.810		V_{DD} – 1.620	V
High	V_{OH}	—	V_{DD} – 1.025	—	V_{DD} – 0.880	V
Input Voltage:						
Low	V_{IL}	—	V_{DD} – 1.810	—	V_{DD} – 1.475	V
High	V_{IH}	—	V_{DD} – 1.165	—	V_{DD} – 0.880	V
Input Capacitance	C_I	—	—	—	2.5	pF
Load Capacitance	C_L	—	—	—	0.4	pF
Input Buffer Gain	V_G	—	—	125	—	dB

Note: $V_{DD} = V_{DDA} = V_{DDD}$.

Interface Timing Specifications

This section specifies the interface timing requirements for the microprocessor interface, line interface, UTOPIA interface, and SONET transport overhead (TOAC) interface.

Microprocessor Interface Timing

Synchronous Mode

The synchronous microprocessor interface mode is selected when MPMODE (pin D8) = 1. Interface timing for the synchronous mode write cycle is given in Figure 33 and in Table 149 (pages 235—236), and for the read cycle in Figure 34 and in Table 150 (pages 237—238).

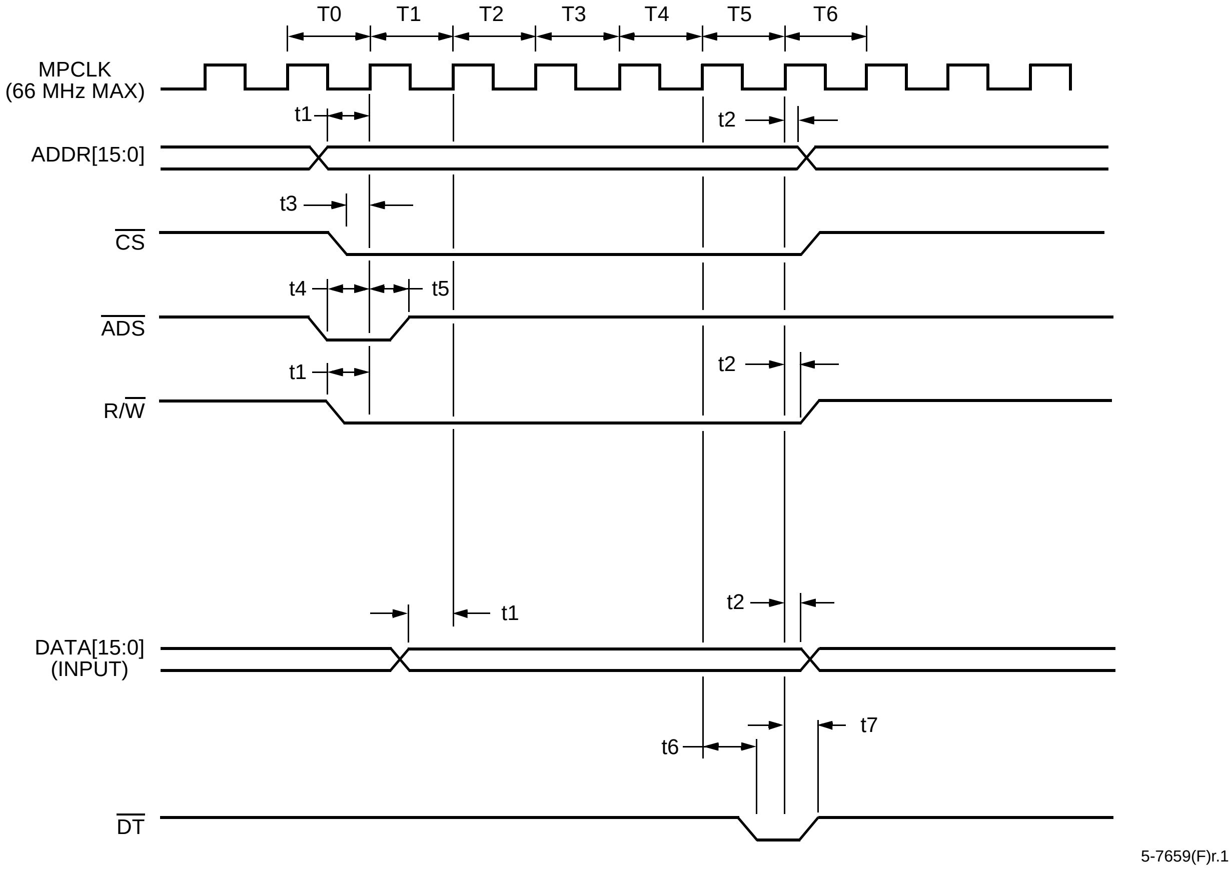


Figure 33. Microprocessor Interface Synchronous Write Cycle (MPMODE (Pin D8) = 1)

ADDR [15:0]	The address will be available throughout the entire cycle.
DATA[15:0]	Data will be available during cycle T1.
R/$\overline{W}$ (Input)	The read (H) write (L) signal is always high except during a write cycle.
$\overline{CS}$ (Input)	Chip select is an active-low signal.
$\overline{DT}$ (Output)	Data transfer acknowledge is active-low on the host bus interface is initiated in timing cycle T5. This signal is active for one clock and then driven high before entering a high-impedance state. (This is done with an I/O pad using the input as feedback to qualify the 3-state term.) $\overline{DT}$ will become 3-stated when $\overline{CS}$ is high.
$\overline{ADS}$ (Input)	Address strobe is active-low. When used with the Power PC (*Motorola** MC68360), this is $\overline{TS}$ (transfer start).

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* Motorola is a registered trademark of Motorola, Inc.

Interface Timing Specifications (continued)

Microprocessor Interface Timing (continued)

Synchronous Mode (continued)

Table 149. Microprocessor Interface Synchronous Write Cycle Specifications

(See Figure 33 on page 235 for the timing diagram.)

Symbol	Parameter	Setup (ns) (Min)	Hold (ns) (Min)	Delay (ns) (Max)
t1	ADDR, R/$\overline{W}$, DATA (write) Valid to MPCLK	3	—	—
t2	MPCLK to ADDR, R/$\overline{W}$, DATA (write) Invalid	—	5	—
t3	$\overline{CS}$ Valid to MPCLK	3.5	—	—
t4	$\overline{ADS}$ Valid to MPCLK	5.5	—	—
t5	MPCLK to $\overline{ADS}$ Invalid	—	5	—
t6	MPCLK to $\overline{DT}$ Valid	—	—	8
t7	MPCLK to $\overline{DT}$ Invalid	—	1	—

Interface Timing Specifications (continued)

Microprocessor Interface Timing (continued)

Synchronous Mode (continued)

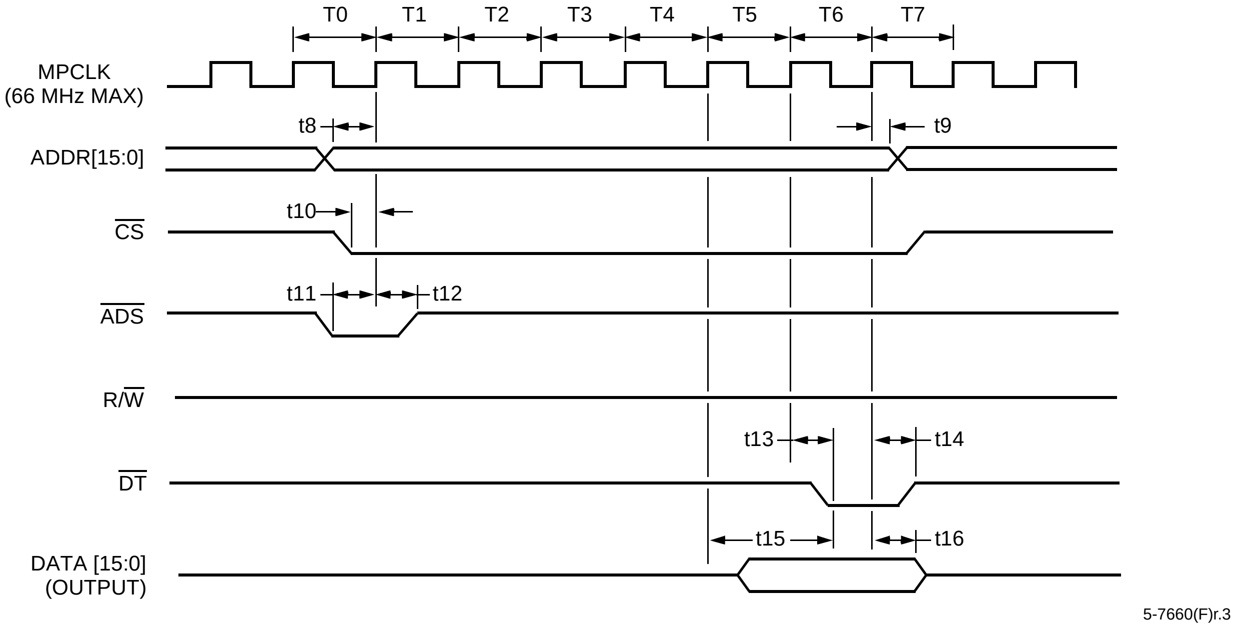

Figure 34. Microprocessor Interface Synchronous Read Cycle (MPMODE (Pin D8) = 1)

ADDR [15:0]	The host bus address is always asynchronously passed from the host bus to the internal bus. The address will be available throughout the entire cycle.
DATA [15:0]	Read data is available in T6.
R/$\overline{W}$ (Input)	The read (H) write (L) signal is always high during the read cycle.
$\overline{CS}$ (Input)	Chip select is an active-low signal.
$\overline{DT}$ (Output)	Data transfer acknowledge on the host bus interface is initiated on T6. This signal is active for one clock and then driven high before entering a high-impedance state. (This is done with an I/O pad using the input as feedback to qualify the 3-state term.) $\overline{DT}$ will become 3-stated when $\overline{CS}$ is high.
$\overline{ADS}$ (Input)	Address strobe is active-low. When used with the Power PC (*Motorola* MC68360), this is $\overline{TS}$ (transfer start).

Interface Timing Specifications (continued)

Microprocessor Interface Timing (continued)

Synchronous Mode (continued)

Table 150. Microprocessor Interface Synchronous Read Cycle Specifications

(See Figure 34 on page 237 for the timing diagram.)

Symbol	Parameter	Setup (ns) (Min)	Hold (ns) (Min)	Delay (ns) (Max)
t8	ADDR Valid to MPCLK	3	—	—
t9	MPCLK to ADDR Invalid	—	5	—
t10	$\overline{\text{CS}}$ Valid to MPCLK	3.5	—	—
t11	$\overline{\text{ADS}}$ Valid to MPCLK	5.5	—	—
t12	MPCLK to $\overline{\text{ADS}}$ Invalid	—	5	—
t13	MPCLK to $\overline{\text{DT}}$ Valid	—	—	8
t14	MPCLK to $\overline{\text{DT}}$ Invalid	—	1	—
t15	MPCLK to DATA Valid	—	—	24
t16	MPCLK to DATA 3-state	—	1	—

Interface Timing Specifications (continued)

Microprocessor Interface Timing (continued)

Asynchronous Mode

The asynchronous microprocessor interface mode is selected when MPMODE (pin D8) = 0. Interface timing for the asynchronous mode write cycle is given in Figure 35 and in Table 151 (see pages 239—240), and for the read cycle in Figure 36 and in Table 152 (see pages 241—242).

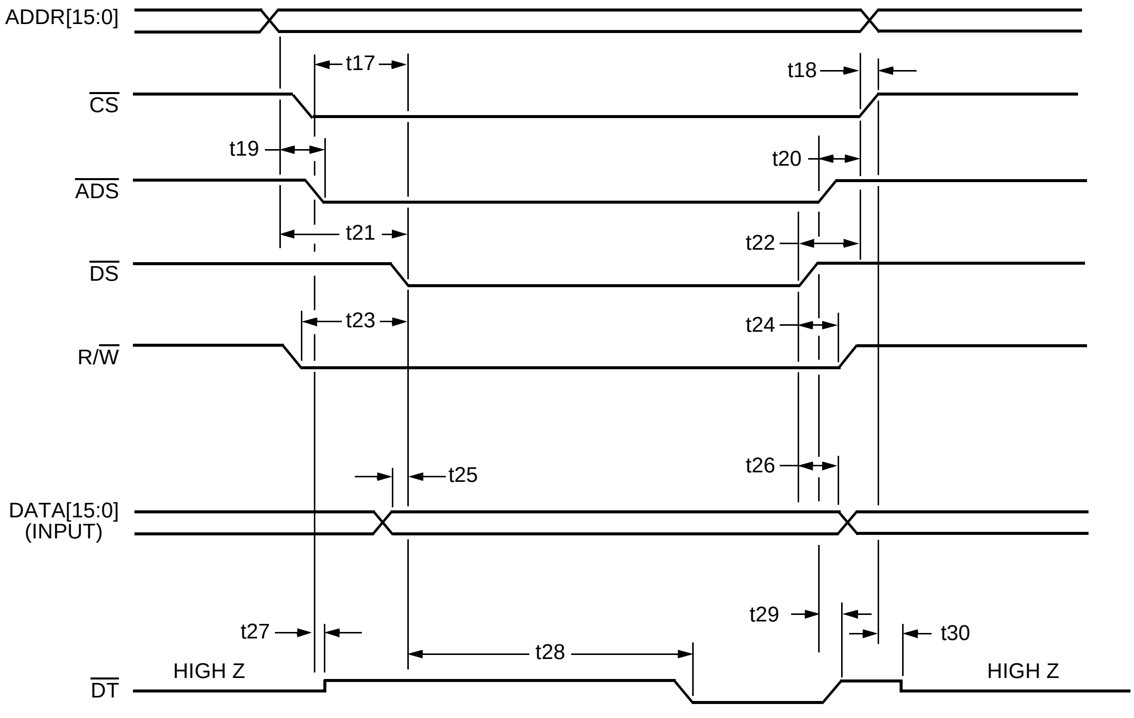

Figure 35. Microprocessor Interface Asynchronous Write Cycle Description (MPMODE (Pin D8) = 0)

ADDR [15:0]	Address is asynchronously passed from the host bus to the internal bus. The address will be available throughout the entire cycle.
DATA [15:0]	Write data is asynchronously passed from the host bus to the internal bus. Data will be available throughout the entire cycle.
R/$\overline{\text{W}}$ (Input)	The read (H) write (L) signal is always high except during a write cycle.
$\overline{\text{CS}}$ (Input)	Chip select is an active-low signal.
$\overline{\text{DT}}$ (Output)	Data transfer acknowledge (active-low). $\overline{\text{DT}}$ is driven asynchronously based on the arrival of $\overline{\text{CS}}$. $\overline{\text{DT}}$ is driven high until the internal transaction is done. $\overline{\text{DT}}$ is driven high again when $\overline{\text{ADS}}$ is deasserted. $\overline{\text{DT}}$ will become 3-stated when $\overline{\text{CS}}$ is high.
$\overline{\text{ADS}}$ (Input)	Address strobe is active-low.
$\overline{\text{DS}}$ (Input)	Data strobe is active-low.

Interface Timing Specifications (continued)

Microprocessor Interface Timing (continued)

Asynchronous Mode (continued)

Table 151. Microprocessor Interface Asynchronous Write Cycle Specifications

(See Figure 35 on page 239 for the timing diagram.)

Symbol	Parameter	Min Interval (ns)	Max Interval (ns)
t17	$\overline{\text{CS}}$ Fall to $\overline{\text{DS}}$ Fall	0	—
t18	ADDR Invalid to $\overline{\text{CS}}$ Rise	0	—
t19	ADDR Valid to $\overline{\text{ADS}}$ Fall	0	—
t20	$\overline{\text{ADS}}$ Rise to ADDR Invalid	5	—
t21	ADDR Valid to $\overline{\text{DS}}$ Fall	0	—
t22	$\overline{\text{DS}}$ Rise to ADDR Invalid	0	—
t23	R/$\overline{\text{W}}$ Fall to $\overline{\text{DS}}$ Fall	0	—
t24	$\overline{\text{DS}}$ Rise to R/$\overline{\text{W}}$ Rise	0	—
t25	DATA Valid to $\overline{\text{DS}}$ Fall	0	—
t26	$\overline{\text{DS}}$ Rise to DATA Invalid	0	—
t27	$\overline{\text{CS}}$ Fall to $\overline{\text{DT}}$ High	0	—
t28	$\overline{\text{DS}}$ Fall to $\overline{\text{DT}}$ Fall	0	72
t29	$\overline{\text{ADS}}$ Rise to $\overline{\text{DT}}$ Rise	0	37.5
t30	$\overline{\text{CS}}$ Rise to $\overline{\text{DT}}$ 3-state	0	—

Interface Timing Specifications (continued)

Microprocessor Interface Timing (continued)

Asynchronous Mode (continued)

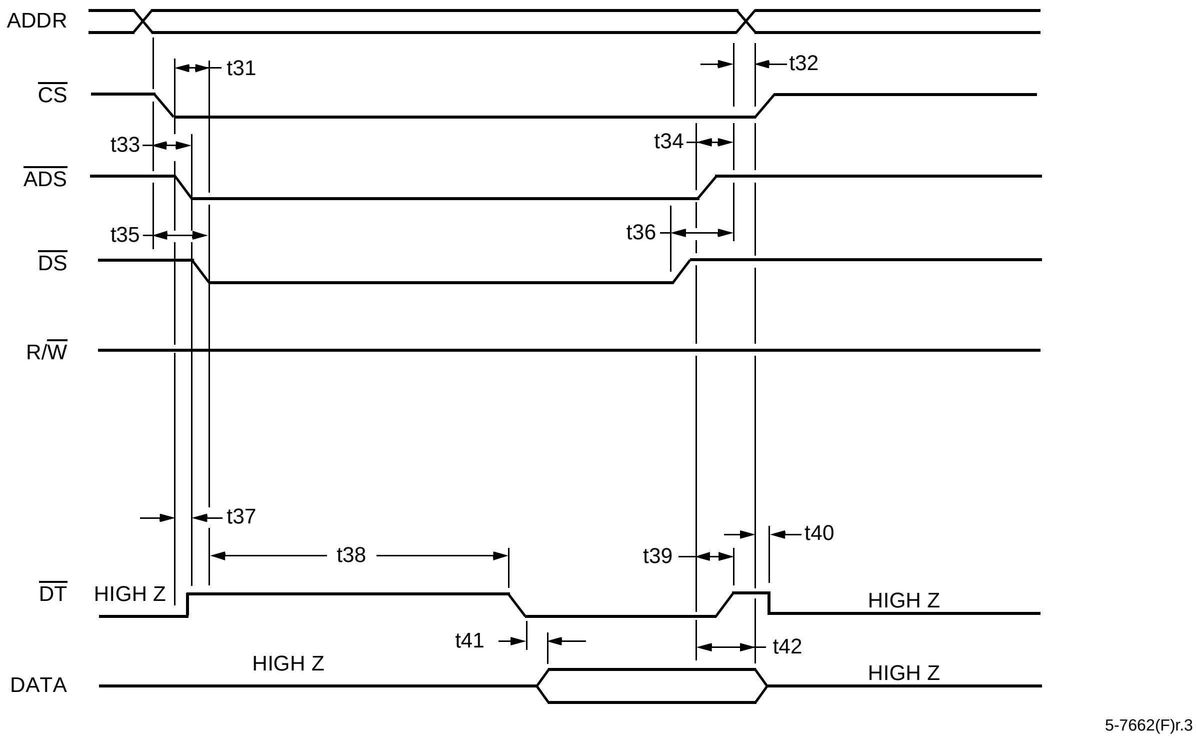

Figure 36. Microprocessor Interface Asynchronous Read Cycle (MPMODE (Pin D8) = 0)

ADDR [15:0]	Address is asynchronously passed from the host bus to the internal bus. The address will be available throughout the entire cycle.
DATA [15:0]	Read data on the internal bus is only valid for one clock cycle, therefore, a latch is necessary to meet the correct timing on the host bus.
R/$\overline{W}$ (Input)	The read (H) write (L) signal is always high during a read cycle.
$\overline{CS}$ (Input)	Chip select is an active-low signal.
$\overline{DT}$ (Output)	Data transfer acknowledge (active-low). $\overline{DT}$ is driven asynchronously based on the arrival of $\overline{CS}$, $\overline{DS}$, and $\overline{ADS}$. $\overline{DT}$ is driven high while the internal bus transaction is in progress. There is no need to provide synchronization to outgoing signals in this mode. $\overline{DT}$ is driven high and then placed in a high-impedance state when either $\overline{ADS}$ or $\overline{DS}$ is deasserted. $\overline{DT}$ will become 3-stated when $\overline{CS}$ is high.
$\overline{ADS}$ (Input)	Address strobe is active-low.
$\overline{DS}$ (Input)	Data strobe is active-low.

Interface Timing Specifications (continued)

Microprocessor Interface Timing (continued)

Asynchronous Mode (continued)

Table 152. Microprocessor Interface Asynchronous Read Cycle Specifications

(See Figure 36 on page 241 for the timing diagram.)

Symbol	Parameter	Min Interval (ns)	Max Interval (ns)
t31	$\overline{\text{CS}}$ Fall to $\overline{\text{DS}}$ Fall	0	—
t32	ADDR Invalid to $\overline{\text{CS}}$ Rise	0	—
t33	ADDR Valid to $\overline{\text{ADS}}$ Fall	0	—
t34	$\overline{\text{ADS}}$ Rise to ADDR Invalid	5	—
t35	ADDR Valid to $\overline{\text{DS}}$ Fall	0	—
t36	$\overline{\text{DS}}$ Rise to ADDR Invalid	0	—
t37	$\overline{\text{CS}}$ Fall to $\overline{\text{DT}}$ High	0	—
t38	$\overline{\text{DS}}$ Fall to $\overline{\text{DT}}$ Fall	0	84
t39	$\overline{\text{ADS}}$ Rise to $\overline{\text{DT}}$ Rise	—	37.5
t40	$\overline{\text{CS}}$ Rise to $\overline{\text{DT}}$ 3-state	0	—
t41	$\overline{\text{DT}}$ Valid to DATA Valid	—	12
t42	$\overline{\text{ADS}}$ Rise to DATA 3-state	0	—

Reset

Software Reset

Writing the binary value 101 to SWRST (core register 0x000E, bits 2—0) causes a 0 to 1 transition on the internal PMRST signal. This pulse will be high for 100 clock cycles and then low for 100 clock cycles of the 77.76 MHz internal clock. Writing a logic 1 to these bits during this 200 clock-cycle interval (2.57 µs) has no effect.

Interrupt

Occurrence of an interrupt is event driven. The interrupt pin, $\overline{\text{INT}}$ (B7), will be deasserted after a minimum of either one MPU clock cycle in the synchronous microprocessor mode or 13 ns in the asynchronous microprocessor mode after clearing the interrupt register.

Interface Timing Specifications (continued)

Line Interface I/O Timing

Figure 37 and Figure 38, and Table 153 through Table 155 give the timing specifications for the STS-3/STM-1, STS-12/STM-4, and STS-48/STM-16 interfaces.

Note: VDD = VDDA = VDDD in this section.

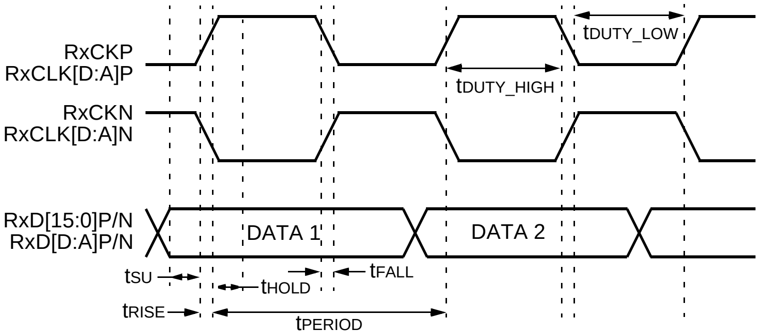

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Figure 37. Receive Line-Side Timing Waveform

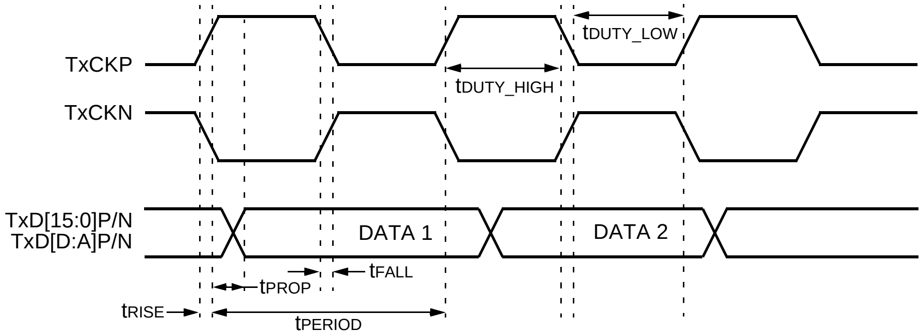

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Figure 38. Transmit Line-Side Timing Waveform

Interface Timing Specifications (continued)

Line Interface I/O Timing (continued)

Table 153. Clock Input Specifications

For the following table,
V_{IL} (max) = (V_{DD} –1.475) volts, nominal of 1.825 volts;
V_{IH} (min) = (V_{DD} –1.165), nominal of 2.135 volts;
V_{OH} (min) = (V_{DD} –1.025), nominal of 2.275 volts; and
V_{OL} (max) = (V_{DD} –1.620) volts, nominal of 1.680 volts.

Clock Name	Mode	t_{period} (Min) (ns)	t_{rise} (Max) (ns)	t_{fall} (Max) (ns)	Duty Cycle	
					t_{duty_high} (Min) (ns)	t_{duty_low} (Min) (ns)
Quad STS-3/STM-1, Quad STS-12/STM-4 Application Input Clock Specifications						
RxD[14]P/**RxCLK[A]P,** RxD[14]N/**RxCLK[A]N**	STS-3/STM-1	6.428	1.5	1.5	2.5	2.5
	STS-12/STM-4	1.608	0.5	0.5	0.7	0.7
RxD[13]P/**RxCLK[B]P,** RxD[13]N/**RxCLK[B]N**	STS-3/STM-1	6.428	1.5	1.5	2.5	2.5
	STS-12/STM-4	1.608	0.5	0.5	0.7	0.7
RxD[11]P/**RxCLK[C]P,** RxD[11]N/**RxCLK[C]N**	STS-3/STM-1	6.428	1.5	1.5	2.5	2.5
	STS-12/STM-4	1.608	0.5	0.5	0.7	0.7
RxD[9]P/**RxCLK[D]P,** RxD[9]N/**RxCLK[D]N**	STS-3/STM-1	6.428	1.5	1.5	2.5	2.5
	STS-12/STM-4	1.608	0.5	0.5	0.7	0.7
TxCKP, **TxCKN**	STS-3/STM-1	6.428	1.5	1.5	2.5	2.5
	STS-12/STM-4	1.608	0.5	0.5	0.7	0.7
STS-48/STM-16 Application Input Clock Specification						
RxCKP/RxD[A]P, **RxCKN**/RxD[A]N	STS-48/STM-16	6.428	1.5	1.5	2.5	2.5
TxCKP, **TxCKN**	STS-48/STM-16	6.428	1.5	1.5	2.5	2.5
TxCKQP, **TxCKQN**	STS-48/STM-16	6.428	1.5	1.5	2.5	2.5

Note: The bold portion of the signal name is the function that is active in the given mode. For example, in STS-48/STM-16 mode, RxCKP is bold in **RxCKP**/RxDAP since it is the active function.

Interface Timing Specifications (continued)

Line Interface I/O Timing (continued)

Table 154. Line Input Specifications

For the following table,
V_{IL} (max) = (V_{DD} –1.475) volts, nominal of 1.825 volts;
V_{IH} (min) = (V_{DD} –1.165), nominal of 2.135 volts;
V_{OH} (min) = (V_{DD} –1.025), nominal of 2.275 volts; and
V_{OL} (max) = (V_{DD} –1.620) volts, nominal of 1.680 volts.

Input Name	Mode	trise (Max) (ns)	tfall (Max) (ns)	Ref Clock	Edge (+/–)	tsetup (Min) (ns)	thold (Min) (ns)	Internal Pull-up (Ω)*
Quad STS-3/STM-1, Quad STS-12/STM-4 Application Input Specifications								
RxCKP/**RxD[A]P,** RxCKN/**RxD[A]N**	STS-3/STM-1	2.2	2.2	RxD[14]P/**RxCLK[A]P,** RxD[14]N/**RxCLK[A]N**	+	0.6	0.6	NA
	STS-12/STM-4	0.5	0.5		–	0.4	0.4	
RxD[15]P/**RxD[B]P,** RxD[15]N/**RxD[B]N**	STS-3/STM-1	2.2	2.2	RxD[13]P/**RxCLK[B]P,** RxD[13]N/**RxCLK[B]N**	+	0.6	0.6	NA
	STS-12/STM-4	0.5	0.5		–	0.4	0.4	
RxD[12]P/**RxD[C]P,** RxD[12]N/**RxD[C]N**	STS-3/STM-1	2.2	2.2	RxD[11]P/**RxCLK[C]P,** RxD[11]N/**RxCLK[C]N**	+	0.6	0.6	NA
	STS-12/STM-4	0.5	0.5		–	0.4	0.4	
RxD[10]P/**RxD[D]P,** RxD[10]N/**RxD[D]N**	STS-3/STM-1	2.2	2.2	RxD[9]P/**RxCLK[D]P,** RxD[9]N/**RxCLK[D]N**	+	0.6	0.6	NA
	STS-12/STM-4	0.5	0.5		–	0.4	0.4	
TxFSYNCP, **TxFSYNCN**	STS-3/STM-1	2.2	2.2	**TxCKP,** **TxCKN**	+	0.6	0.6	200k PD, 200k PU
	STS-12/STM-4	0.5	0.5		–	0.4	0.4	
STS-48/STM-16 Application Input Specification								
RxD[15]P/RxD[B]P, **RxD[15]N/**RxD[B]N	STS-48/STM-16	1.5	1.5	**RxCKP**/RxD[A]P, **RxCKN**/RxD[A]N	+ –	0.5	1.0	NA
RxD[14]P/RxCLK[A]P, **RxD[14]N**/RxCLK[A]N	STS-48/STM-16	1.5	1.5	**RxCKP**/RxD[A]P, **RxCKN**/RxD[A]N	+ –	0.5	1.0	NA
RxD[13]P/RxCLK[B]P, **RxD[13]N**/RxCLK[B]N	STS-48/STM-16	1.5	1.5	**RxCKP**/RxD[A]P, **RxCKN**/RxD[A]N	+ –	0.5	1.0	NA
RxD[12]P/RxD[C]P, **RxD[12]N**/RxD[C]N	STS-48/STM-16	1.5	1.5	**RxCKP**/RxD[A]]P, **RxCKN**/RxD[AN	+ –	0.5	1.0	NA
RxD[1]1P/RxCLK[C]P, **RxD[11]N**/RxCLK[C]N	STS-48/STM-16	1.5	1.5	**RxCKP**/RxD[A]P, **RxCKN**/RxD[A]N	+ –	0.5	1.0	NA
RxD[10]P/RxD[D]P, **RxD[10]N**/RxD[D]N	STS-48/STM-16	1.5	1.5	**RxCKP**/RxD[A]P, **RxCKN**/RxD[A]N	+ –	0.5	1.0	NA
RxD[9]P/RxCLK[D]P, **RxD[9]N**/RxCLK[D]N	STS-48/STM-16	1.5	1.5	**RxCKP**/RxD[A]P, **RxCKN**/RxD[A]N	+ –	0.5	1.0	NA
RxD[8:0]P, **RxD[8:0]N**	STS-48/STM-16	1.5	1.5	**RxCKP**/RxD[A]P, **RxCKN**/RxD[A]N	+ –	0.5	1.0	NA
TxFSYNCP, **TxFSYNCN**	STS-48/STM-16	1.5	1.5	**TxCKP** no PLL, **TxCKN** no PLL	+ –	0	2.0	50k PD, 50k PU
				TxCKP with PLL, **TxCKN** with PLL	+ –	2	0	

* PU refers to pull-up and PD refers to pull-down.

Note: The bold portion of the signal name is the function that is active in the given mode. For example, in STS-48/STM-16 mode, RxCKP is bold in **RxCKP**/RxD[A]P since it is the active function.

Interface Timing Specifications (continued)

Line Interface I/O Timing (continued)

Table 155. Line Output Specifications

For the following table, test conditions are the outputs sinking a source I_L of a standard LVPECL load.*, †

Output Name	**tprop**		**Ref Clock**	**Edge (+/–)**	**Cap Load (Max) (pF)**†	**3-Stated**
	(Min) (ns)	**(Max) (ns)**				
Quad STS-3/STM-1 or Quad STS-12/STM-4 Application Input Specification						
TxD[3]P/**TxD[A]P** TxD[3]N/**TxD[A]N**	2	5	**TxCKP** **TxCKN**	+ –	8	NA
			RxD[14]P/**RxCLK[A]P** RxD[14]N/**RxCLK[A]N**	+ –	8	
TxD[2]P/**TxD[B]P** TxD[2]N/**TxD[B]N**	2	5	**TxCKP** **TxCKN**	+ –	8	NA
			RxD[13]P/**RxCLK[B]P** RxD[13]N/**RxCLK[B]N**	+ –	8	
TxD[1]P/**TxD[C]P** TxD[1]N/**TxD[C]N**	2	5	**TxCKP** **TxCKN**	+ –	8	NA
			RxD[11]P/**RxCLK[C]P** RxD[11]N/**RxCLK[C]N**	+ –	8	
TxD[0]P/**TxD[D]P** TxD[0]N/**TxD[D]N**	2	5	**TxCKP** **TxCKN**	+ –	8	NA
			RxD[9]P/**RxCLK[D]P** RxD[9]N/**RxCLK[D]N**	+ –	8	
Quad STS-48/STM-16 Application Input Specification						
TxD[15:4]P **TxD[15:4]N**	1	3	**TxCKP** with PLL‡ **TxCKN** with PLL‡	+ –	12	NA
TxD[3]P/TxD[A]P **TxD[3]N**/TxD[A]N	1	3	**TxCKP** with PLL‡ **TxCKN** with PLL‡	+ –	8	NA
TxD[2]P/TxD[B]P **TxD[2]N**/TxD[B]N	1	3	**TxCKP** with PLL‡ **TxCKN** with PLL‡	+ –	8	NA
TxD[1]P/TxD[C]P **TxD[1]N**/TxD[C]N	1	3	**TxCKP** with PLL‡ **TxCKN** with PLL‡	+ –	8	NA
TxD[0]P/TxD[D]P **TxD[0]N**/TxD[D]N	1	3	**TxCKP** with PLL‡ **TxCKN** with PLL‡	+ –	8	NA
TxD[15:4]P **TxD[15:4]N**	1	3	**TxCKP** no PLL‡ **TxCKN** no PLL‡	+ –	12	NA

* The following are characteristics of the LVPECL outputs; more details can be found in Table 148, page 234.
V_{OH}(min) = (V_{DD} – 1.025) volts,
V_{OL}(max) = (V_{DD} – 1.620) volts,
V_{IH}(min) = (V_{DD} – 1.165) volts,
V_{IL}(max) = (V_{DD} – 1.475) volts.

† The recommended termination for LVPECL outputs is as follows: 50 Ω to a termination voltage equal to V_{DD} – 2 V.

‡ The PLL can be invoked in STS-48/STM-16 mode only.

Note: The bold portion of the signal name is the function that is active in the given mode. For example, in STS-48/STM-16 mode, RxCKP is bold in **RxCKP**/RxD[A]P since it is the active function.

Interface Timing Specifications (continued)

Line Interface I/O Timing (continued)

Table 155. Line Output Specifications (continued)

For the following table, test conditions are the outputs sinking a source IL of a standard LVPECL load.*, †

Input Name	tprop		Ref Clock	Edge (+/–)	Cap Load (Max) (pF)†	3-stated
	(Min) (ns)	(Max) (ns)				
STS-48/STM-16 Application Input Specification (continued)						
TxD3P/**TxDAP** TxD3N/**TxDAN**	1	5	**TxCKP** no PLL‡ **TxCKN** no PLL‡	+ –	12	NA
TxD2P/**TxDBP** TxD2N/**TxDBN**	2	5	**TxCKP** no PLL‡ **TxCKN** no PLL‡	+ –	12	NA
TxD1P/**TxDCP** TxD1N/**TxDCN**	2	5	**TxCKP** no PLL‡ **TxCKN** no PLL‡	+ –	12	NA
TxD0P/**TxDDP** TxD0N/**TxDDN**	2	5	**TxCKP** no PLL‡ **TxCKN** no PLL‡	+ –	12	NA
TxCKQP **TxCKQN**	1.5	4.5	**TxCKP** no PLL‡ **TxCKN** no PLL‡	+ –	12	NA
TxD[15:4]P TxD[15:4]N	0.5	1.5	TxCKQP TxCKQN	+ –	12	NA
TxD[3:0]P TxD[3:0]N	0.5	1.5	TxCKQP TxCKQN	+ –	12	NA

* The following are characteristics of the LVPECL outputs; more details can be found in Table 148, page 234.
VOH(min) = (VDD – 1.025) volts,
VOL(max) = (VDD – 1.620) volts,
VIH(min) = (VDD – 1.165) volts,
VIL(max) = (VDD – 1.475) volts.

† The recommended termination for LVPECL outputs is as follows: 50 Ω to a termination voltage equal to VDD – 2 V.

‡ The PLL can be invoked in STS-48/STM-16 mode only.

Note: The bold portion of the signal name is the function that is active in the given mode. For example, in STS-48/STM-16 mode, RxCKP is bold in **RxCKP**/RxD[A]P since it is the active function.

Interface Timing Specifications (continued)

UTOPIA Interface Timing

UTOPIA interface timing specifications are given for the transmit direction in Figure 39 and in Table 156, and for the receive direction in Figure 40 and in Table 157 (see page 249). Specifications for the UTOPIA clock interface are given in Table 158 (see page 250).

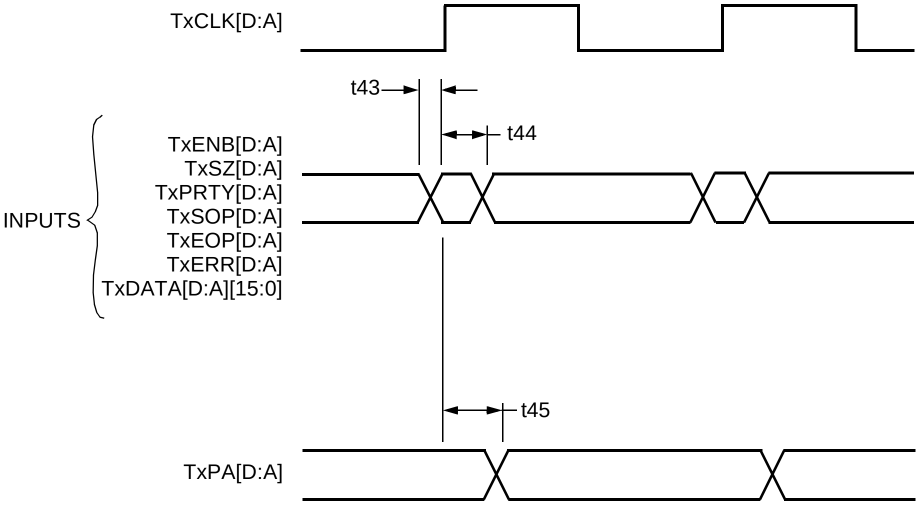

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Figure 39. Transmit UTOPIA Interface Timing

Table 156. Transmit UTOPIA Interface Timing Specifications

Symbol	Test Conditions	Setup (Min)	Hold (Min)	Valid (Min)	Valid (Max)	Unit
t43	C_L = 25 pF	2.5	—	—	—	ns
	C_L = 50 pF	4.0	—	—	—	ns
t44	C_L = 25 pF	—	0.0	—	—	ns
	C_L = 50 pF	—	1.0	—	—	ns
t45	C_L = 25 pF	—	—	2.0	5.0	ns
	C_L = 50 pF	2.0	—	2.0	13.0	ns

Interface Timing Specifications (continued)

UTOPIA Interface Timing (continued)

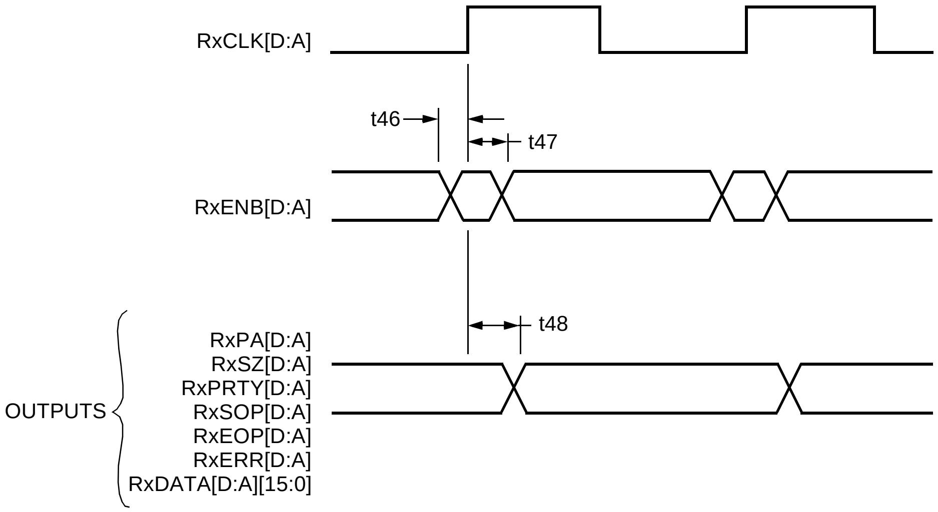

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Figure 40. Receive UTOPIA Interface Timing

Table 157. Receive UTOPIA Interface Timing Specifications

Symbol	Test Conditions		Setup (Min)	Hold (Min)	Valid (Min)	Valid (Max)	Unit
	RxCLK[D:A] Output	RxCLK[D:A] Input					
t46	CL = 25 pF	—	2.5	—	—	—	ns
	—	CL = 50 pF	4.0	—	—	—	ns
t47	CL = 25 pF	—	—	0.0	—	—	ns
	—	CL = 50 pF	—	1.0	—	—	ns
t48	CL = 25 pF	—	—	—	2.0	—	ns
	—	CL = 50 pF	6.5	—	4.0	13.0	ns

Interface Timing Specifications (continued)

UTOPIA Interface Timing (continued)

Table 158. UTOPIA Interface Clock Specifications

Mode	Signal Name	Parameter	Test Conditions	Min	Max	Unit
Transmit						
U3+	TxCLK[D:A]	TxCLK Frequency	104 MHz, Multi-PHY Signal	0	104	MHz
		TxCLK Duty Cycle		40	60	%
		TxCLK Peak-to-Peak Jitter		—	2	%
		TxCLK Rise/Fall Time		—	2	ns
		TxCLK Skew		—	1	ns
Receive						
U3+	RxCLK[D:A]	RxCLK Frequency	104 MHz, Multi-PHY Signal	0	104	MHz
		RxCLK Duty Cycle		40	60	%
		RxCLK Peak-to-Peak Jitter		—	2	%
		RxCLK Rise/Fall Time		—	2	ns
		RxCLK Skew		—	1	ns
Transmit						
U2+	TxCLK[D:A]	TxCLK Frequency	52 MHz, Multi-PHY Signal	0	50	MHz
		TxCLK Duty Cycle		40	60	%
		TxCLK Peak-to-Peak Jitter		—	5	%
		TxCLK Rise/Fall Time		—	2	ns
		TxCLK Skew		—	1	ns
Receive						
U2+	RxCLK[D:A]	RxCLK Frequency	52 MHz, Multi-PHY Signal	0	50	MHz
		RxCLK Duty Cycle		40	60	%
		RxCLK Peak-to-Peak Jitter		—	5	%
		RxCLK Rise/Fall Time		—	2	ns
		RxCLK Skew		—	1	ns

Interface Timing Specifications (continued)

Transport Overhead (TOAC) Interface Timing

Transport overhead (TOAC) interface timing specifications are given for the transmit direction in Figure 41 and in Table 159, and for the receive direction in Figure 42 and in Table 160.

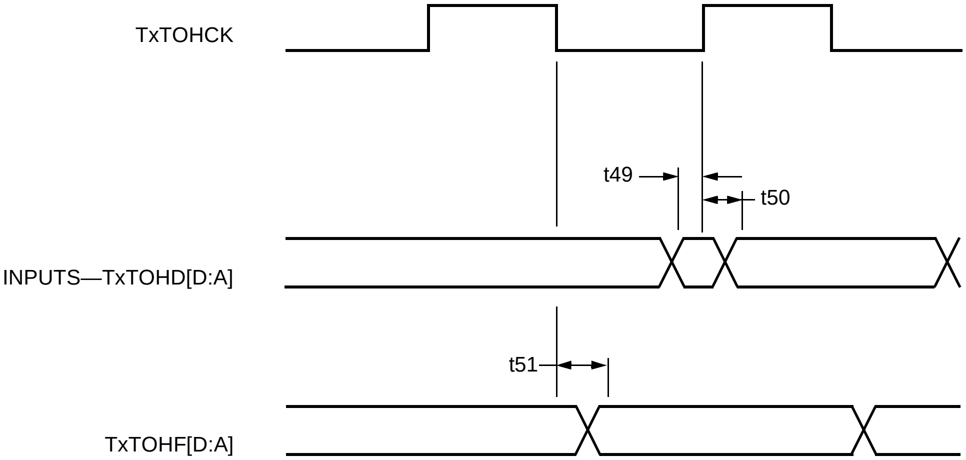

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Figure 41. Transmit TOAC Interface Timing

Table 159. Transmit TOAC Interface Timing Specifications

Symbol	Test Conditions	Setup (Min)	Hold (Min)	Valid		Unit
				(Min)	(Max)	
t49	—	10	—	—	—	ns
t50	—	—	10	—	—	ns
t51	C_L = 50 pF	—	—	0	10	ns

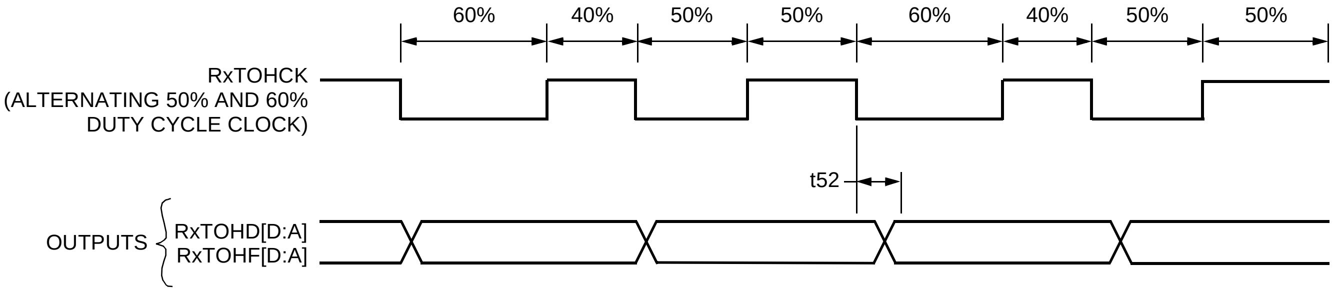

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Figure 42. Receive TOAC Interface Timing

Table 160. Receive TOAC Interface Timing Specifications

Symbol	Test Conditions	Valid		Unit
		(Min)	(Max)	
t52	C_L = 50 pF	0	10	ns

Reference of SONET/SDH Terms and Comparisons

Definitions of SONET/SDH Bytes

- A1: Framing byte 0xF6
- A2: Framing byte 0x28
- B1: BIP-8 parity for section (regenerator section)
- B2: BIP-8xN parity for STS-N signal for line (multiplexer section)
- B3: BIP-8 parity for path
- C1: Redefined to J0/Z0
- D1—D3: Section (regenerator section) data communication channels
- D4—D12: Line (multiplexer section) data communication channels
- E1: Section (regenerator section) orderwire
- E2: Line (multiplexer section) orderwire
- F1: Section user channel
- F2, F3: Path user channels
- G1: Path status byte
- H1, H2: Higher-order (AU) pointer
- H3: Pointer action byte
- H4: Multiframe indicator
- J0: Section (regenerator section) trace
- J1: Path trace
- J2: Lower-order path trace
- K1, K2: Automatic protection switching (APS) channel and line (multiplexer section) RDI
- K3: Path APS
- K4: Lower-order path APS
- M1: Line (multiplexer section) REI
- N1: Higher-order tandem connection
- N2: Lower-order tandem connection
- S1: Synchronization status
- V1, V2: Lower-order (TU) pointer
- V3: Lower-order pointer action byte
- V4: Reserved
- V5: Lower-order BIP-2, SLM, and status
- Z0, Z1, Z2: Growth bytes

Reference of SONET/SDH Terms and Comparisons (continued)

SONET/SDH Comparisons

Table 161. SONET/SDH Comparisons

SONET	SDH
SPE	VC
SPE and Pointer	AU
STS-3xN	STM-N
VT1.5	TU-11
VT2	TU-12
VT6	TU-2
VTG	TUG-2
Transport Overhead	Section overhead
Section Overhead	Regenerator Section Overhead
Line Overhead	Multiplexer Section Overhead

SONET/SDH New Terminology

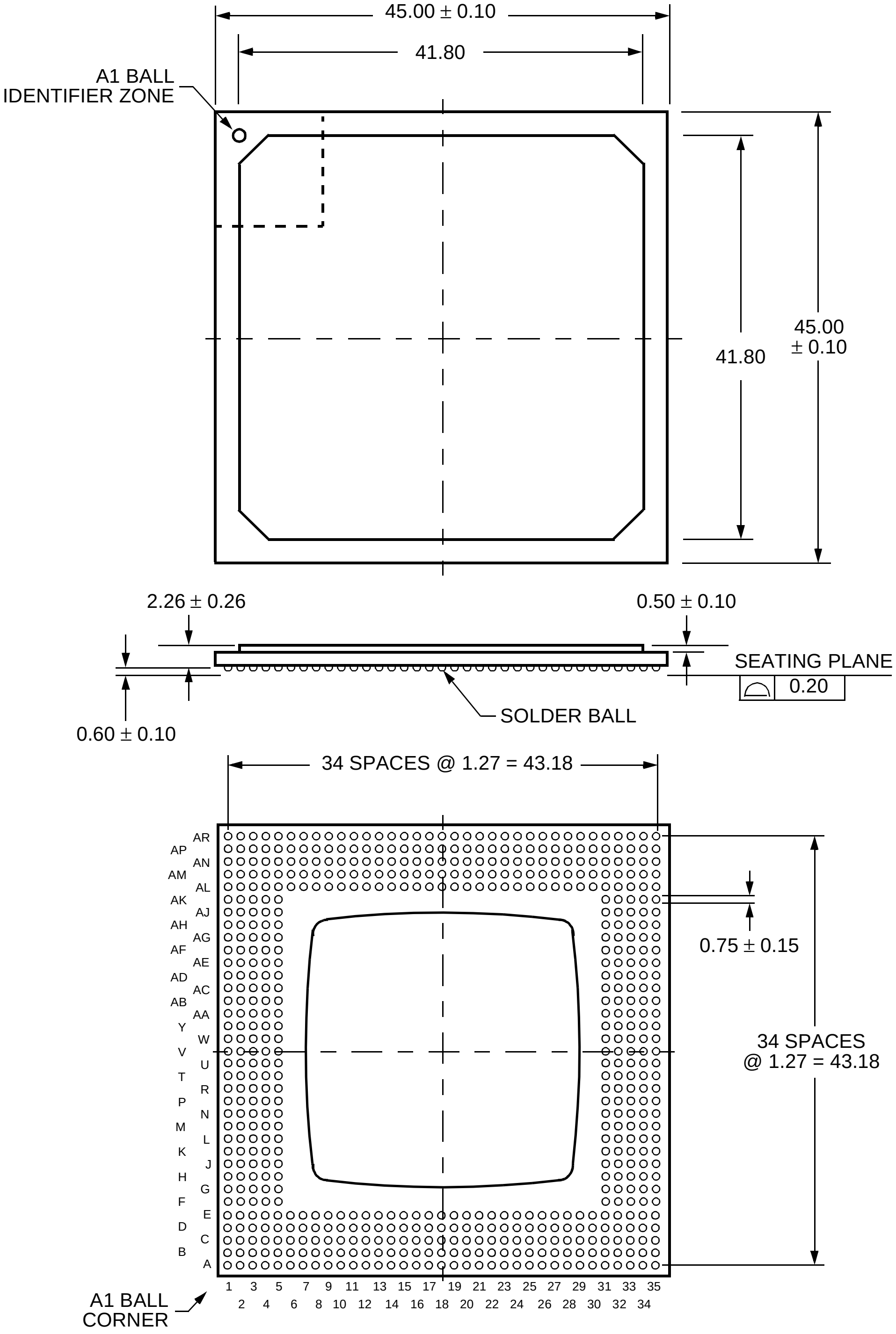
Table 162. SONET/SDH New Terminology

Was	Is
FERF: Far-End Receive Failure	RDI: Remote Defect Indicator
FEBE: Far-End Block Error	REI: Remote Error Indicator (SDH only)
Path Yellow Alarm	RAI: Remote Alarm Indicator
C1: STS-1 Identifier	J0: Section Trace /Z0: Growth
First Z1: Growth	S1: Synchronization
Third Z1: Growth	M1: Line REI
Z3: Growth	F3: User Channel (SDH only)
Z4: Growth	K3: APS (SDH only)
Z5: Growth	N1: Tandem Connection (SDH only)
Z6: Growth	N2: Tandem Connection (SDH only)
Z7: Growth	K4: LO APS (SDH only)

Outline Diagram

600-Pin LBGA

Dimensions are in millimeters.



5-7174(F)

Ordering Information

Device Code	Package	Temperature	Comcode (Ordering Number)
TDAT042G5-3BLL1	600-pin LBGA	–40 °C to +85 °C	108269457

DS98-193SONT-3 Replaces DS98-193TIC-02 to Incorporate the Following Updates

Due to extensive alterations in the data sheet (pin listings, timing diagrams, register maps, etc.), specific changes have not been identified.

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