

MM58539 Multiplexed LCD Driver

General Description

The MM58539 is a monolithic integrated circuit utilizing CMOS metal-gate, low threshold P- and N-channel devices, which can drive up to 34 columns of a dot matrix LCD array directly under the control of an external processor. The MM58539 should be used with an MM58538 or MM58548 to drive a display that has up to 8 or 16 rows and an arbitrary number of columns. Data is input serially from the microprocessor which will service the drivers in response to an interrupt signal.

The circuit is available in a 40-pin molded dual-in-line package or dice.

Features

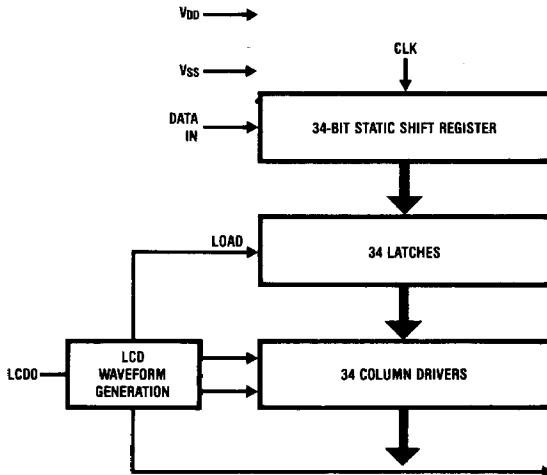
- Drives up to 34 columns
- Used with the MM58538 or MM58548 for expanding to larger displays

- Flexible organization allows any display pattern
- Simple 3 line interface to microprocessor
- Interrupt output
- Low power
- Wide supply voltage range
- On chip oscillator
- Compatible with HLCD 0539

Applications

- Toys and games
- Word processor text displays
- Automotive dashboards

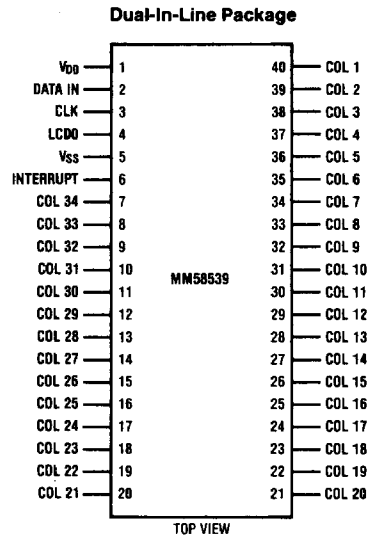
Block Diagram



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FIGURE 1

Connection Diagrams



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FIGURE 2

**Order Number MM58539N
See NS Package N40A**

Absolute Maximum Ratings

Voltage at any input pin	$V_{DD} - 20V$ to $V_{DD} + 0.3V$	Power Dissipation	250 mW
Voltage at any display pin	$V_{SS} - 0.3V$ to $V_{DD} + 0.3V$	Lead Temperature (Soldering, 10 seconds)	300°C
Storage Temperature	-65°C to 150°C	Operating Temperature	-40°C to 70°C

Electrical Characteristics $T = 25^\circ\text{C}$ and $V_{DD} = 5V$ unless otherwise noted.

Parameter	Conditions	Min	Typ	Max	Units
V_{DD} Supply Voltage		3		15	V
I_{DD} Supply Current				400	μA
V_{IH} Input High Level	All V_{DD}	$.75V_{DD}$		V_{DD}	V
V_{IL} Input Low Level	All V_{DD}	$V_{DD} - 15$		$.25V_{DD}$	V
I_L Input Leakage				5	μA
C_I Input Cap.				5	pF
V_{OH} Column O/P High	All V_{DD}		$.68V_{DD}$		V
V_{OL} Column O/P Low	All V_{DD}		$.32V_{DD}$		V
V_{OFF} Average DC Offset, any display element				100	mV
R_{ON} Interrupt Output Impedance	$I_L = 100 \mu\text{A}$			1	$\text{k}\Omega$
f Clock Frequency		DC		1.5	MHz
t_{ds} Data-in Setup Time	Data change to clock fall	300			ns
T_{DH} Data in Hold Time	Clock fall to data change	100			ns
t_d LCD0 to Int. Out Delay		300			ns
$t_{r/f}$ Clock Rise/Fall Time				200	ns
V_{IH} LCD0 High Level	All V_{DD}	$.9V_{DD}$		V_{DD}	V
V_{IL} LCD0 Low Level	All V_{DD}	0		$.1V_{DD}$	V
R_{IN} LCD0 Input Impedance		1		3	$\text{M}\Omega$

Functional Description

A block diagram of the MM58539 LCD driver is shown in Figure 1. Connection diagrams are shown in Figure 2.

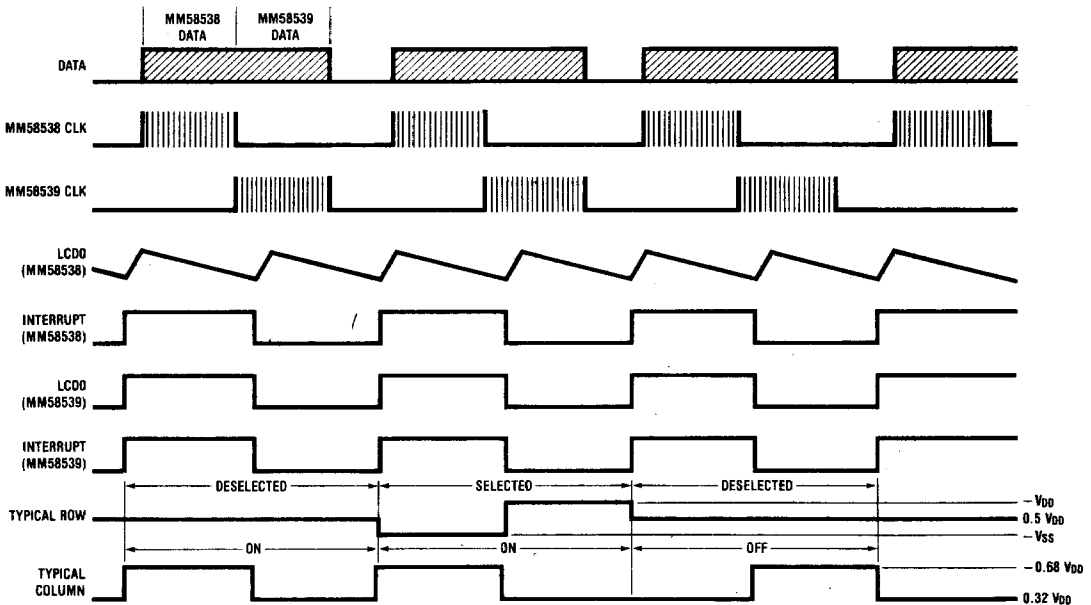
MICROPROCESSOR INTERFACE

Figure 3 shows some typical waveforms for the microprocessor interface when the MM58539 is used with the MM58538 to provide row and column information. All character or pattern generation is done externally by the processor. Data is loaded into the shift register on the falling edge of the clock. A data logic "1" on a coincident row/column causes a segment to be visible. On the next rising edge of the interrupt signal, a parallel transfer from the shift register to the latches occurs and the row and column outputs change accordingly. This Interrupt signal also acts as a refresh request and new data must be loaded before the next Interrupt signal. The output locations correspond to a clock-wise advancing shift register. Pin 40 is the last bit of data loaded and pin 7 is the first bit loaded.

ROW AND COLUMN OUTPUTS

Waveforms for both selected and deselected row and column outputs are shown for an MM58539 together with an MM58538 in Figure 3.

Rows generated from the MM58538 are out of phase with Interrupt if selected and at midpoint voltage otherwise; levels are V_{DD} , V_{SS} and $V_{DD}/2$. Columns generated from both the MM58538 and the MM58539 are in phase with Interrupt if selected and out of phase if not selected; levels are $0.32V_{DD}$ and $0.68V_{DD}$. Backplanes, ie rows, should be addressed sequentially and individually. If the supply voltage has to be altered to optimise LCD contrast or for temperature compensation it is recommended that all positive supply terminals be connected together and the negative supply varied.



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FIGURE 3

LCD0 INPUT

This input can be used in two modes:

1. Oscillating Mode

When this pin is connected with an external resistor and capacitor in parallel to V_{SS} , this input operates as an RC oscillator. This frequency is divided by two to provide a 50% duty cycle and will then appear at the Interrupt output as a frequency of approximately $1/RC$, where R should exceed $1\text{ M}\Omega$.

The Interrupt output frequency should be the minimum no-flicker frequency (approximately 30Hz) multiplied by the number of backplanes used.

2. Driven Mode

In this mode, the Interrupt output will follow the waveform input on the LCD0 pin.

LCD0 of a driven mode device should preferably be connected to the Interrupt output of the previous oscillating device. If driven from an external source, it must be a 50% $\pm 1\%$ duty cycle waveform to maintain low DC offset on the display.

MODE DETECTION

The mode of operation is achieved automatically in the following manner. When the circuit is first powered on, an internal power-on-reset signal is generated which primes the mode detect logic. This signal sets all the Row outputs to

the Deselected state, all the Column outputs to the Off state and the Interrupt output high. If the circuit is in the Oscillating mode, the LCD0 pin is held low by the external oscillator resistor. If the circuit is in the driven mode, the LCD0 pin is held high by the low impedance Interrupt output of the previous device. When the first clock pulse goes to a logic "1", the level on the LCD0 pin is internally latched, which indicates to the rest of the logic whether the circuit is driven or oscillating.

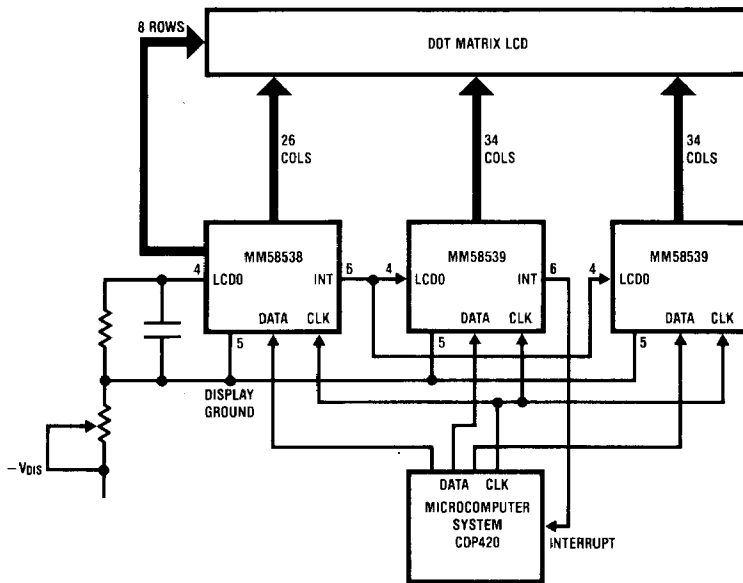
The oscillator on the oscillating device starts as soon as the clock pin goes high.

In the Driven mode, the Interrupt frequency is in phase with the input frequency on LCD0.

CASCADING

Figure 4 shows an application where two or more LCD drivers are cascaded. Only a single resistor and capacitor are needed to provide frequency control for all circuits. The Interrupt output from the "master" oscillating circuit is connected to the LCD0 input of the other "slave" circuits, with the "slave" Interrupt going to the microprocessor. It would also be possible to connect all LCD0 inputs to a common drive signal.

The interface to the microprocessor can be done by having a common clock and separate data bus lines or vice versa.



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FIGURE 4. Typical Application Diagram