

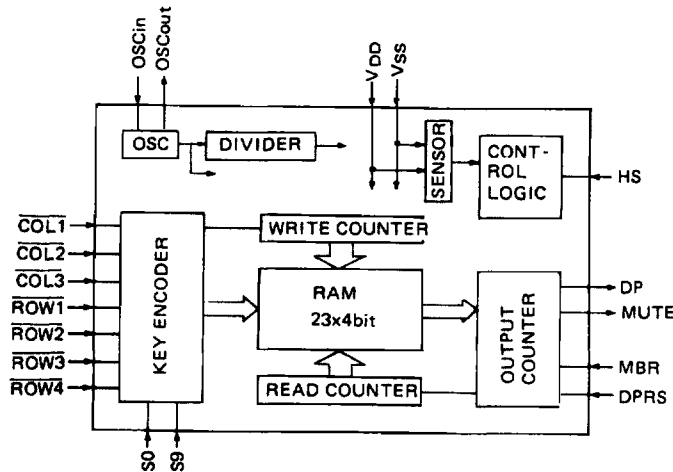
HD61825A/B Series

Pulse Dialer with Redial

■ FEATURES

- Direct telephone-line operation.
- Low power and low voltage operation by CMOS process.
- Uses either a standard 2-of-7 keyboard or the inexpensive matrix keyboard
- Stable operation by using ceramic resonator.
- Make/Break ratio pin-selectable
- 10 pps/20 pps pin-selectable
- Redial function (# key)
- Pause input (# key)
- Selectable of mute output
 - Mute (continuous) HD61825A
 - Mute (each digit) HD61825B
- 0 dialing in inhibition pin
- 9 dialing in inhibition pin
- 23-digit dial memory
- Dial memory overflow protection (inhibit redial)
- On chip power supply voltage sense circuit
 - Reset voltage
 - Memory clear voltage

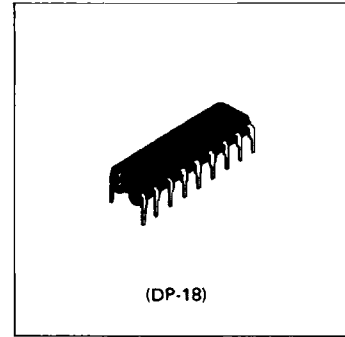
■ BLOCK DIAGRAM



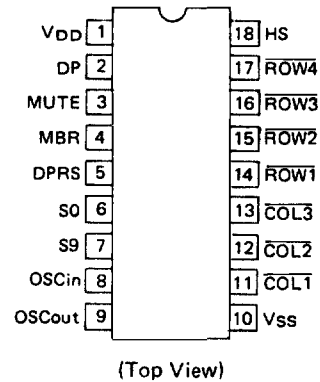
■ ABSOLUTE MAXIMUM RATINGS (V_{SS} = 0V)

Item	Symbol	Value	Unit
Power supply voltage	V _{DD}	5.5	V
Terminal voltage	V _T	V _{SS} - 0.3 to V _{DD} + 0.3	V
Operating temperature	T _{opr}	-20 to +75	°C
Storage temperature	T _{stg}	-55 to +125	°C

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is not guaranteed. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.



■ PIN ASSIGNMENT



▪ ELECTRICAL CHARACTERISTICS

• DC Characteristics ($V_{SS} = 0V$, $V_{DD} = 2.0$ to $5.0V$, $T_a = -20$ to $+75^\circ C$)

Item	Symbol	Test condition	min.	typ.*1	max.	Unit
Operating voltage	V_{DD}		1.7	—	5.0	V
Reset voltage	V_{DR}		—	1.5	—	V
Memory clear voltage	V_{DC}		—	1.15	—	V
Operating current	I_{DD}		—	170	—	μA
Memory hold (reset) current	I_{DR}		—	0.5	—	μA
Input High voltage	V_{IH}	except HS pin	$80\%V_{DD}$	—	—	V
Input High voltage	V_{IH}	HS pin $V_{DD} = 3.0$ to $5.0V$	$90\%V_{DD}$	—	—	V
Input High voltage	V_{IH}	HS pin $V_{DD} = 2.0$ to $3.0V$	$V_{DD}-0.1$	—	—	V
Input Low voltage	V_{IL}	HS pin $V_{DD} = 2.0$ to $5.0V$	—	—	$20\%V_{DD}$	V
Input Low voltage	V_{IL}		—	—	$20\%V_{DD}$	V
Input leak current	$ I_{IN} $	Pull up MOS off, $V_{IN}=0$ to V_{DD}	—	—	1	μA
Input Pull up MOS current	$-I_P$	$V_{IN} = 0$, (MBR, DP, RS, S0, S9, ROW, COW, HS)	—	10	—	μA
Output High voltage	V_{OH}	$-I_{OH} = 0.1$ mA (DP, MUTE)	$V_{DD}-0.5$	—	—	V
Output Low voltage	V_{OL}	$I_{OL} = 0.1$ mA (ROW, COL)	—	—	0.3	V
Open drain output leak current	I_{OL}	$V_{IN} = V_{DD}$ (DP, MUTE)	—	—	1	μA

• AC Characteristics ($V_{SS} = 0V$, $V_{DD} = 2.0$ to $5.0V$, $T_a = -20$ to $+75^\circ C$)

Item	Symbol	Test condition	min.	typ.*1	max.	Unit
Oscillation frequency	f_{osc}		396	400	404	kHz
Oscillation start up time	t_{str}		—	5	—	ms

*1 Typ. value is the design value (the standard value at $V_{DD} = 2.5V$ and $T_a = 25^\circ C$)

• DESCRIPTION

HD61825 is a CMOS IC for button telephone and converts keyboard inputs into the dial pulse signal. Using low-voltage and low-power consumption CMOS process, it can operate directly from the telephone line and interfaces with the telephone line by loop-disconnect signal (DP output). Besides, it has MUTE output to mute the receiver during the sending pulses. In the HD61825, ON HOOK/OFF HOOK is detected by the HS pin.

Further, while the supply voltage is less than reset voltage, even if the HS is OFF HOOK, the HD61825 will be ON HOOK state of inhibition key input. When the power supply voltage is less than memory clear voltage, the internal memory data is cleared.

While the telephone is OFF-HOOK and the supply voltage is more than the reset voltage, the oscillator starts up with a key input and this key input is implemented with the key debounce circuit. In this case, if the first key after the reset (note 1) is other than # and * (note 2), the internal memory data is cleared, and then this input key is encoded and stored into the memory. Then the following keys are stored ordinal into the memory, and also at the same time these keys are converted into the output pulse.

The key input speed is same as that of DTMF telephone because the input data is stored in the memory. The internal memory capacity is 23 digits. When key input are more than 23 digits, the completed key code are cleared (FIFO type memory) and then the new keys are stored into the memory. However, considering the capacity, in the moment while the stored data reach 23 digits, the key input is temporarily neglected.

After dialing, once the HD61825 is reset (note 1) and then is redial mode with the first # key. However, if the 24 or more keys has been dialled previously or the memory has already cleared, it cannot be redial mode. During the redial, any key input is not accepted but after that it can be used as a usual dialer.

The pulse output (DP output) stops with the pause during the redial and the redial starts again with # key. # key is used to insert the pause data in the memory. In the normal dial mode, # key does not influence the output of pulse but is stored in the memory as one digit.

NOTES

1. In the HD61825, the reset means the clearing all logic (counter, etc.) except RAM. HD61825 is reset when the



telephone is ON-HOOK or the supply voltage is less than the reset voltage.

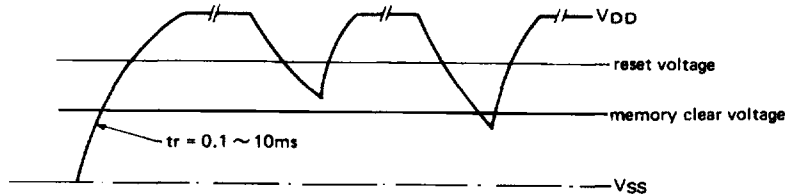
2. * key is not used and always neglected in HD61825.

■ PIN FUNCTIONS

● VDD (Pin 1)

This is a positive voltage supply pin which applies voltage on a basis of the VSS pin. HD61825 provides the internal sense circuit for the supply voltage. To

make this circuit operate stable, the following rising time is necessary.



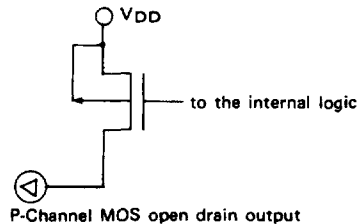
● DP (Pin 2) Dial Pulse

This is a pulse signal output pin for Loop Disconnect. Output circuit is P-Channel MOS open drain.

Break High level

Make Low level

While reset, the output voltage is held to the low level.



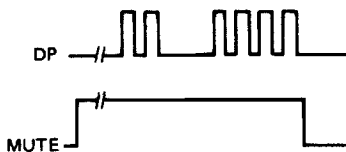
● MUTE (Pin 3)

This is a pin which mute the receiver. Output circuit is P-Channel MOS open drain.

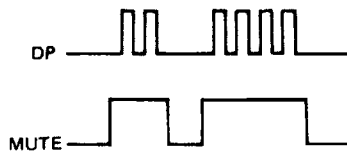
While reset, the output voltage is held to the low level. In the HD61825, the following two kinds of MUTE — continuous MUTE and each digit MUTE are selectable. (IC's are different.)

Mute High level

● Continuous MUTE (HD61825A)



● Each digit MUTE (HD61825B)

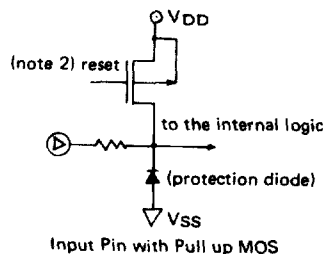


● MBR (Pin 4) Make/Break Ratio

This is an input pin with the pull up MOS to change the Make/Break ratio of DP output. To realize the

low power dissipation on reset, the pull up MOS is turned off at the reset. (note 1)

MBR terminal	DP output	
	Make	Break
High (to V _{DD}) or open	33%	67%
Low (to V _{SS})	40%	60%



NOTES:

- The input pins with the pull up MOS which is turned OFF at the reset, can be applied to MBR, DPRS, S0, S9 and HS.
- The logic is positive. P MOS is ON with the low voltage and OFF with the high voltage.

• **DPRS (Pin 5) Dial Pulse Rate Selection**

This is a input pin to decide the pulse output speed (dial rate). It has a pull up MOS which is turned OFF at the reset.

DPRS terminal	Dial rate
High (to V _{DD}) or open	10 pps
Low (to V _{SS})	20 pps

• **S0, S9 (Pin 6, 7) Selection**

These are input pins to select functions and has pull up MOS which is turned OFF at the reset. The function of this terminal is to prevent the 0 dialing in and the 9 dialing in. When 0 or 9 is pushed after the reset.

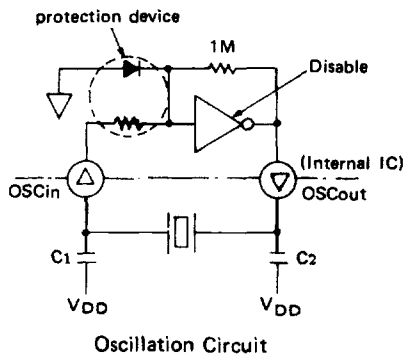
all the key inputs including the 0 or 9 key become invalid after then. In other words, the signals are not output to DP and MUTE. The telephone is initialized by the reset.

S0 terminal	S9 terminal	Function
High (to V _{DD}) or open	High (to V _{DD}) or open	Normal dialing mode
High (to V _{DD}) or open	Low (to V _{SS})	9 dialing in prevention mode
Low (to V _{SS})	High (to V _{DD}) or open	0 dialing in prevention mode
Low (to V _{SS})	Low (to V _{SS})	Test mode (for testing IC, Do not use.)

• **OSCin, OSCout (Pin 8, 9) Oscillation Input, Output**

These are input pins for the oscillator and constructs the inverter (with disable function to stop the oscillation). Using the ceramic resonator, the frequency is stable in the circuit. Moreover, the oscillator section needs two output capacitors externally. The ceramic oscillator should be 400 kHz and High Q.

Recommended ceramic oscillator
 Kyoto Ceramic Co., Ltd. KBR-400H
 Murata Co., Ltd. CSB-400
 ex. ceramic oscillator KBR-400H
 C₁ = 100 pF
 C₂ = 470 pF



• **VSS (Pin 10)**

Negative power supply pin

• **COL1 to COL3 (Pin 11 to 13) Column Input**
ROW1 to ROW4 (Pin 14 to 17) Row Input

These are input/output pins for a key board which consists of PMOS pull up and NMOS driver. (As a matter of form, they are CMOS.)

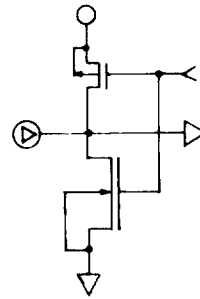
As the signals scan in Row side and Column side alternately, HD61825 can be connected both to the matrix-type keyboard and the 2-of-7 keyboard. While waiting the key input, Row is High level and Column is Low level. And in the reset condition, both Row and Column are Low level.

The hold time of the key should be more than 10 ms. (When the oscillation stops, the period for starting oscillation should be added.) (note 1)

The key debounce time is 20 ms.

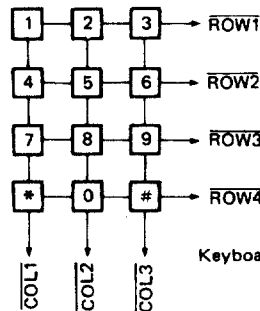
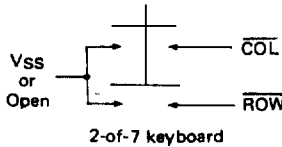
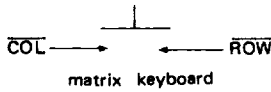
NOTE:

1. The oscillation stops in HD61825;
 1. After the reset
 2. After the completion of DP output.
 3. On Pause



I/O Circuit for Keyboard Input/Output Pins

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Keyboard Configuration

When two keys are pushed at the same time, the key of smaller number of ROW and COL is given priority and is input.

Ex. When typing [2] and [5] at the same time, [2] is input.

• **HS (PIN 18) HOOK SWITCH**

This is an input pin for detecting ON-HOOK/OFF-HOOK switch. It has a pull up MOS which is turned OFF at the reset.

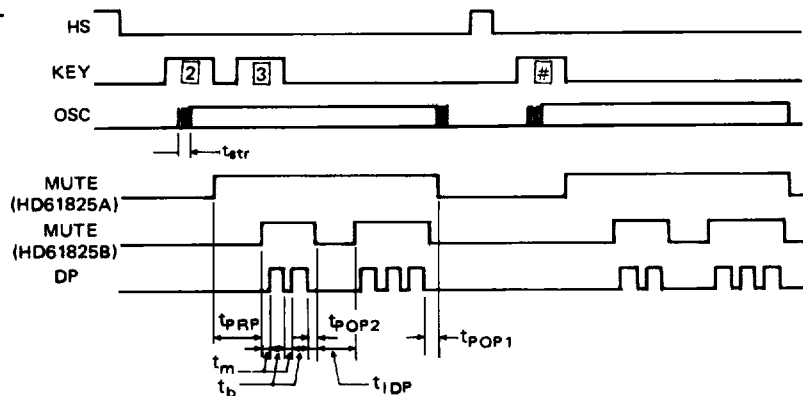
ON HOOK High (to V_{DD}) or open
 OFF HOOK Low (to V_{SS})

reset voltage. So, in this case, the HS pin is not used and the HD61825 controls the operation mode by the monitor of the supply voltage. However, as the pull up MOS is turned OFF with the reset signal, the current does not increase on reset.

An external capacitor must be provided between the HS pin and V_{SS} to prevent the noise from the switch.

HD61825 is reset by making the HS terminal High level. If HS terminal is fixed to Low level, HD61825 is reset when the supply voltage falls less than the

• **TIMING CHART**



Item	Symbol	MBR	DPRS	min	typ	max	Unit
Pre-Digital pause	tPRP	-	-	-	800	-	ms
Make time	tm	33%	10PPS	-	33.3	-	ms
		40%	10PPS	-	39.7	-	ms
		33%	20PPS	-	16.6	-	ms
		40%	20PPS	-	20.5	-	ms
Breka time	tb	33%	10PPS	-	66.7	-	ms
		40%	10PPS	-	60.2	-	ms
		33%	20PPS	-	33.3	-	ms
		40%	20PPS	-	29.4	-	ms
Inter-Digit Pause	tIDP	-	10PPS	-	767	-	ms
		-	20PPS	-	500	-	ms
Post-Digital Pause	tPOP1	-	-	-	36	-	ms
	tPOP2	-	-	-	33	-	ms

■ AN EXAMPLE OF KEY OPERATION

	HOOK	KEY	DP
Normal Dial	ON		
Dial after Pause	OFF	0 1 2 3 4	0-1-2-3-4
		5 6	5-6
Redial	ON		
Dial after Redial	OFF	#	0-1-2-3-4-5-6
		7 8	7-8
Redial	ON		
	OFF	#	0-1-2-3-4-5-6-7-8
Normal Dial	ON		
(Pause Entry)	OFF	9 # 1 2	9-1-2
	ON		
Redial	OFF	#	9
(Including Pause)		#	1-2
Dial of 24 digits	ON		
or more	OFF	1 1 1	1-1 -1
		24 times	24 times
Prevention of Over Flow	ON		
	OFF	#	
		0 1	0-1

	HOOK	KEY	DP
(0 dialing in prevention mode with S0 = Low and S9 = High.)			
ON			
OFF	1	2	3
OFF	0	4	5
ON		6	7
OFF	#		
			1-2-3-0
			1-2-3-0

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NOTE:
After the output of pulse which corresponds to the each key operation are finished, Mute (also in HD61825A) is Low.

• APPLICATION CIRCUIT

