ASSP CMOS

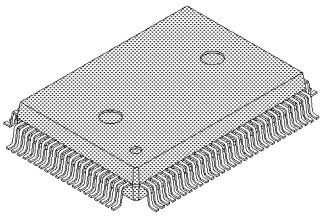
Dolby Digital AC-3 Decoder LSI

MB86342

Description

Dolby Digital AC-3 is a perceptual digital audio coding technique of great efficiency, quality and versatility.

The MB86342 is Fujitsu's Dolby Digital 5.1-channel decoder. It is fully certified as a "Dolby Digital AC-3 Decoder LSI" by Dolby Laboratories Licensing Corporation.



100-pin, Plastic QFP

Features

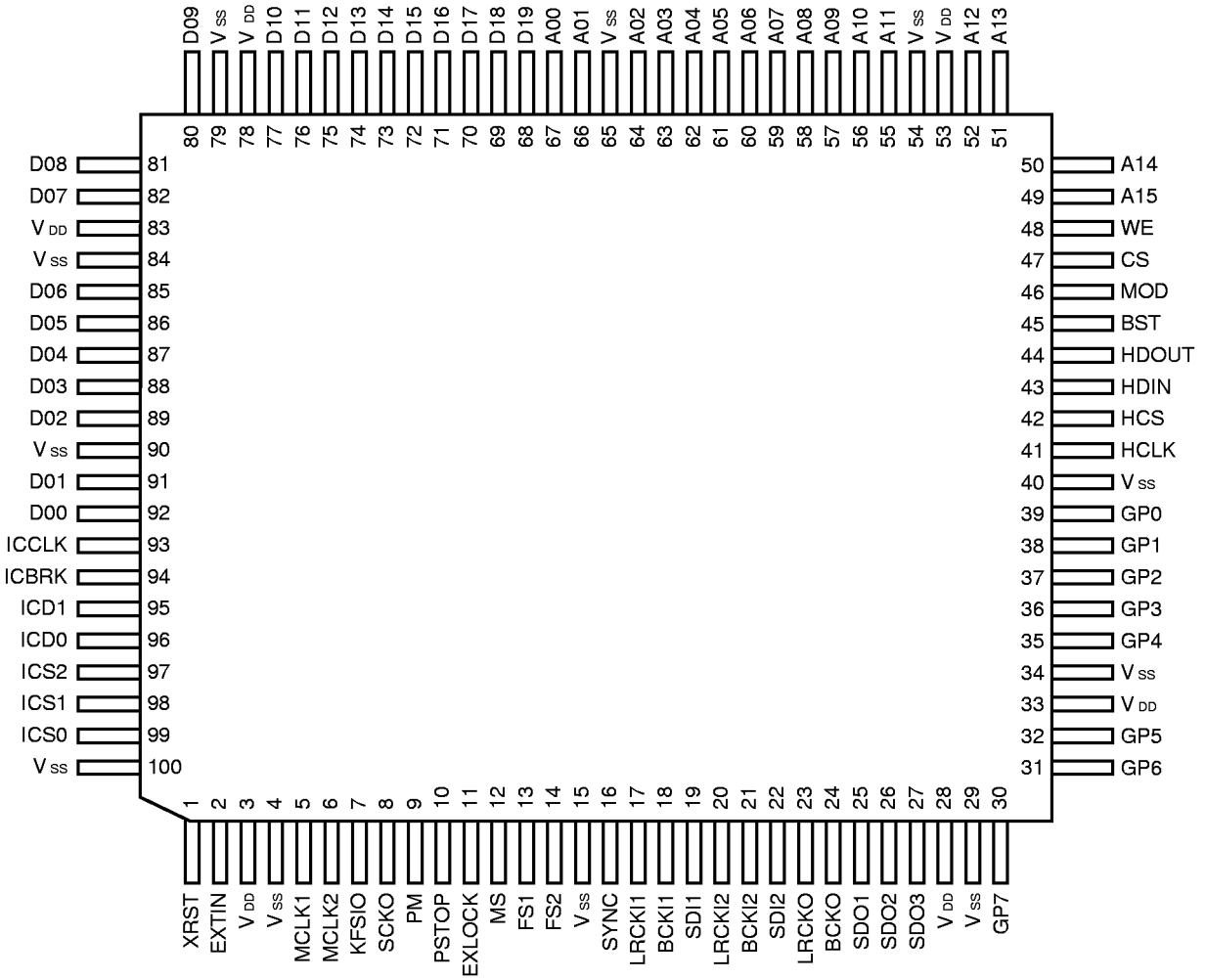
- Dolby Digital AC-3 5.1-Channel Full Decode
  - All bit rate and all sampling frequencies
  - Downmix capability
  - Dynamic-range compression and Dialog normalization
  - Noise sequencer (test tone)
  - Delay for each channel can be independently set
- Dolby Pro Logic Decode
- Dolby Digital AC-3 + Dolby Pro Logic Decode
- 16-, 18-, or 20-bit Audio Data Input/Output
- Operates with one audio system clock (384fs) via a built-in PLL
- Compatible with ADC, DAC, DIR and DIT with 3-line-type audio I/F
- Control by Host I/F
- 3V to 3.6V operation
- 100-pin QFP package

Table of Contents

Doby Digital AC-3 Decoder IST

Pin Assignment

(Top View)



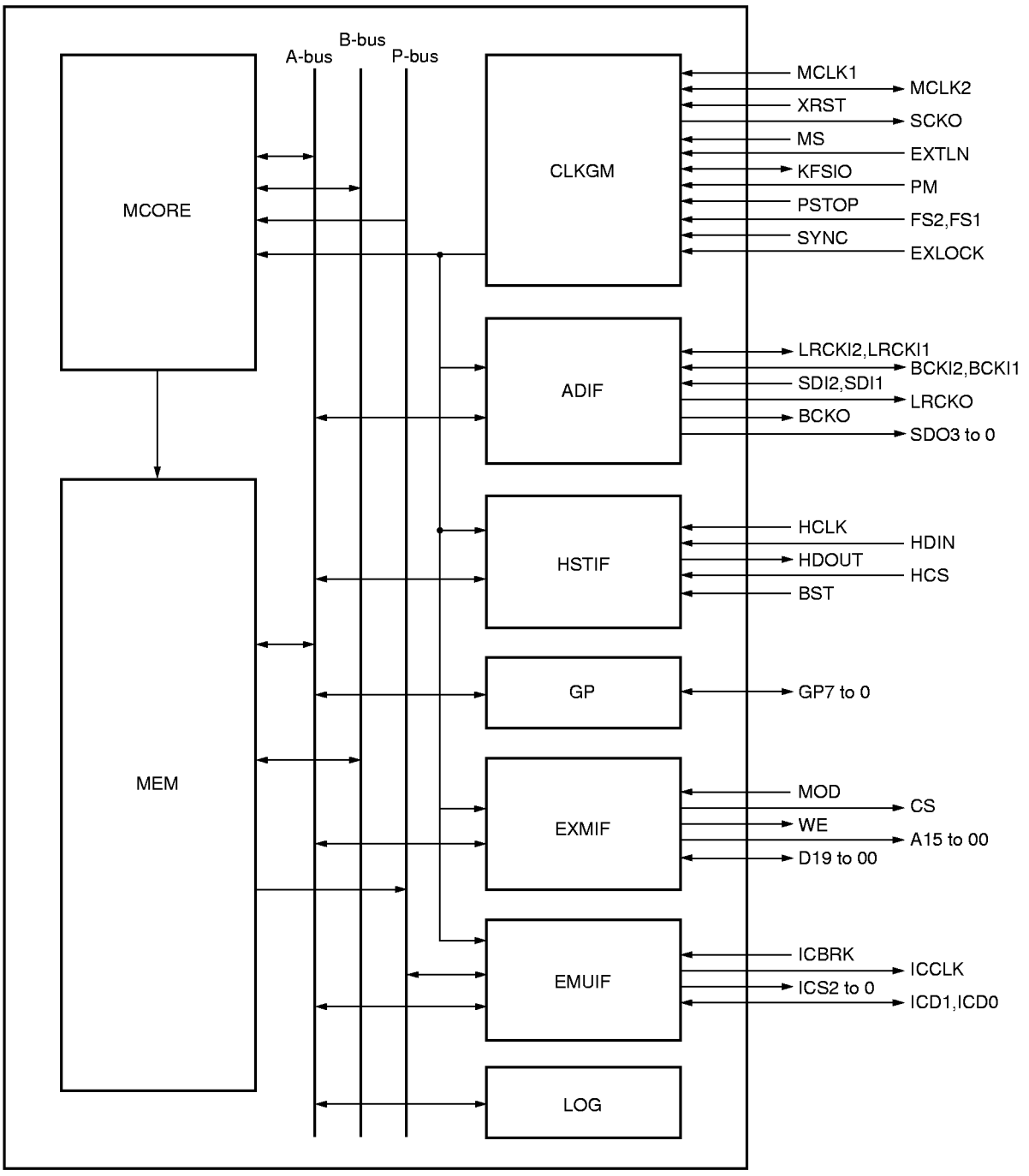
(FPT-100P- M06)

Pin Descriptions

Pin No.	Name	I/O	Description
Clock and Control Signals			
5, 6	MCLK1, MCLK2	I	Crystal oscillator inputs. This connects the external crystal oscillator.
1	XRST	I	Active-Low hardware reset signal
8	SCKO	O	System clock output
12	MS	I	Master/Slave control input. This pin controls the clock operation mode of the device. When Low, the crystal oscillator is used to generate the master clock; when High, the crystal oscillator is not used and the external clock input on pin EXTIN is used.
16	SYNC	I	This pin selects synchronous/asychronous modes. When Low, the synchronous mode is selected. The audio clocks (KFSIO, BCK1/2 and LRCK1/2) are generated from the internal system clock. When High, the asychronous mode is selected. In this mode, the audio clocks are supplied from an external source.
2	EXTIN	I	External master clock input at 384fs. This pin supplies the system clock when the MS pin is high.
13,14	FS1, FS2	I	Sample frequency select. The combination of these 2 inputs selects the audio sampling frequency as follows: FS1 FS2 Sampling Frequency (MHz) L L 44.1 L H 48.0 H L Undefined H H 32.0 The combination FS1=High and FS2=Low is illegal and should NOT be used
7	KFSIO	I/O	Audio input/output clock (384fs)
9	PM	I	Test pin. This pin should be connected to GND for normal operation.
10	PSTOP	I	This pin controls the crystal oscillator and the internal clock generation PLL. When Low, the crystal oscillator and the internal clock generation PLL is enabled. When High, the crystal oscillator and internal PLL is disabled.
11	EXLOCK	I	External clock "Lock" indication. This signal can be used to indicate whether the external clock is stable (locked) or not. A Low input indicates to the device that the external clock is stable. A High input indicates that it is unstable (unlocked).
Host Interface Signals			
41	HCLK	I	Clock input for serial data of host interface
43	HDIN	I	Host interface serial data input. Writes data from host to the device.
44	HDOUT	O	Serial data output for the host interface. Reads data from the device to the host.
42	HCS	I	Host interface chip select signal. Low indicates that the host interface is active.
45	BST	I	This pin should be connected to GND for normal operation.
Audio and General Purpose Interfaces			
30 to 32, 35 to 39	GP0 - GP7	I/O	General purpose I/O port
17	LRCKI1	I/O	Sample clock input/output for the digital audio interface. Identifies L or R for a 2-channel multiplexed data stream.
18	BCKI	I/O	Bit clock input/output for the digital audio interface
19	SD1	I	Digital audio interface data input for channel 1
20	LRCKI2	I/O	Sample clock input/output for the second digital audio input interface
21	BCKI1	I/O	Bit clock input/output for the second digital audio interface
22	SD2	I	Serial audio interface data input for the second channel

Pin No.	Name	I/O	Description
23	LRCKO	O	Sample clock output for digital audio output interface
24	BCKO	O	Bit clock for output audio interface
25 to 27	SDO1 to SDO3	O	3-channel digital audio output data. For Dolby 5.1-channels, this would contain the L, R, C, Ls, Rs, and LFE channels.
External Memory Interface Signals			
46	MOD	I	Bus mode control signal. This pin controls the word width of the external RAM. When Low, the external RAM is byte wide and the system performs 3 accesses for a single word (20 bits). When High, the external RAM is word wide (20 bits), and the MB86342 reads and writes one word each time from external RAM.
47	CS	O	Chip select signal for the external RAM
48	WE	O	Read/write control for the external RAM
49 to 52, 55 to 64, 66, 67	A00 to A15	O	Address bus for the external RAM
68 to 77, 80 to 82, 85 to 89, 91, 92	D00 to D19	I/O	Bidirectional, 20-bit data bus for external RAM. For byte-wide mode, only D00 to D07 are used.
Emulator Control Signals			
			Note: These pins are used for system debug. They are NOT used for normal operation.
93	ICCLK	O	Emulator clock output
94	ICBRK	I	External break control signal
95, 96	ICD0, ICD1	I/O	I/O for data/address of emulator
97 to 99	ICS0 to ICS2	O	Status output for emulator
Power and Ground Pins			
3, 28, 33, 53, 78, 83	V_{DD}	P	Positive supply
4, 15, 29, 34, 40, 54, 65, 79, 84, 90, 100	V_{SS}	G	System Ground

Block Diagram



Block Description

MCORE: **MUCAP Core**
MUCAP Core is a 20-bit fixed point DSP core. This core performs all the control and decoding operations.

CLKGM: **Clock Generation Module**
This module generates internal and external clocks. Two types of clocks are generated from a single source. This source can be either an external crystal oscillator or a clock input signal.

ADIF: **Audio Interface Module**
This module is an interface of input/output serial audio data to an external device. The interface consists of the following:

- 2-channels of input port and 3-channels of output port
- 2-audio data input registers and 6-output registers (20-bit)

HSTIF: **Host Interface Module**
This module transfers asynchronous serial data to the host CPU, which has an input data register and an output data register (20-bit).

GP: **General Port Module**
This module has an 8-bit direction register and an 8-bit data register. Each port is independent as a 1 pin input/output general port (total 8 pins).

EXMIF: **External Memory Interface Module**
This module reads and writes data to external memory (SRAM), which has a 3-byte data read/write mode and a 1 word (20-bit) data read/write mode.

This module uses an in-service register to read and write 3-byte data.

EMUIF: **Emulator Interface Module**
This module is used for in-circuit emulation and is not used for normal operation.

LOG: **LOG Module**
This module has registers to refer to table data for the operation of logarithmic functions.

MEM: **Memory Module**
This module stores all the programs and intermediate data for the entire decoding process.

Operation Flow

The Dolby Digital decoder program has the configuration shown in the figure below. This program consists of five blocks whose operation is explained as follows:

Default Value Setting Routine

The default value setting routine is executed only when the MB86342 is in the reset state. The default value of each parameter is written to the host command area of RAM inside the MB86342. The values in the host command area are kept as the default values specified in this routine unless the user sets them via the host interface after a reset. For the defaults, see the section on "Setting Parameter Values."

Initialize Routine

This routine provides initialization, such as clearing memory for Dolby Digital decoding and other processes. The initialize routine also provides the setting for decomposing and decoding parameters specified in the host command area to make the parameters valid for programs actually executed. During this routine, Dolby Digital decoding and other processes are activated.

Parameters specified by the user via the host interface are written once to the host command area of RAM inside the MB86342. However, these parameters are not valid for the Dolby Digital decoding process until this routine is executed.

To specify parameters, proceed as follows:

1. Write all parameters one-by-one to the host command area via the host interface.
2. Issue an initialize request. When the MB86342 receives the request, it mutes the output and returns to the initialize routine.
3. Perform initialization according to the data written in the host command area and execute Dolby Digital decoding and other processes to resume the output.

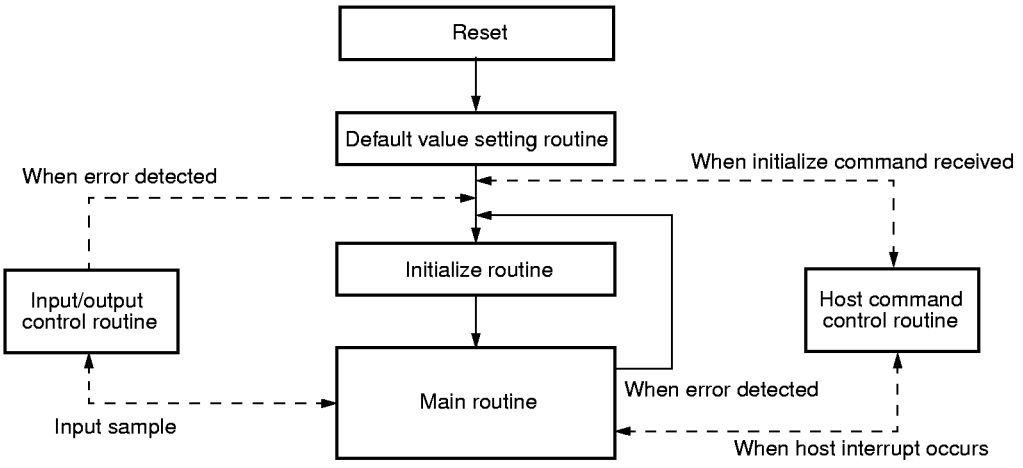
Refer to the "Host Control" section for information on how to issue an initialization request.

Output is muted in the initialize routine. The initialize routine has an execution cycle of about 170,000 steps.

Main Routine

The functioning of the main routine varies according to the parameter settings made by the user. In the Dolby Digital mode, this routine provides Dolby Digital decoding; in other modes, it provides an infinite loop routine.

When an error is detected in a bit stream during Dolby Digital decoding, the MB86342 mutes the output in order to return to the initialize routine and start over.



I/O Control Routine

The input/output control routine is the process executed for an input LR lock interrupt each time one sample audio signal is input. This routine provides input/output control in Dolby Digital and other modes and audio signal processes for Pro Logic decoding, delay setting and also user application program execution.

When an error is detected in an input signal, when an input bit stream is intermittent or when the EXLOCK pin goes High during Dolby Digital decoding, the MB86342 mutes the output, returns to the initialize routine and goes back to Dolby Digital decoding. Even in the PCM mode, the MB86342 returns to the initialize routine when the EXLOCK pin goes High.

Host Command Control Routine

The host command control routine decodes and executes commands (referred to as the host command) input by the user via the host interface. This routine executes the process each time a host interface interrupt occurs. The host command can execute a Dolby Digital decoding, a parameter setting, a mute ON/OFF control, a write to and read from the user area of internal RAM, and an initialize request (a request for jump to initialize the routine). When an initialize request is received, the MB86342 mutes the output and returns to the initialize routine.

The next section describes how to control the MB86342 from the host.

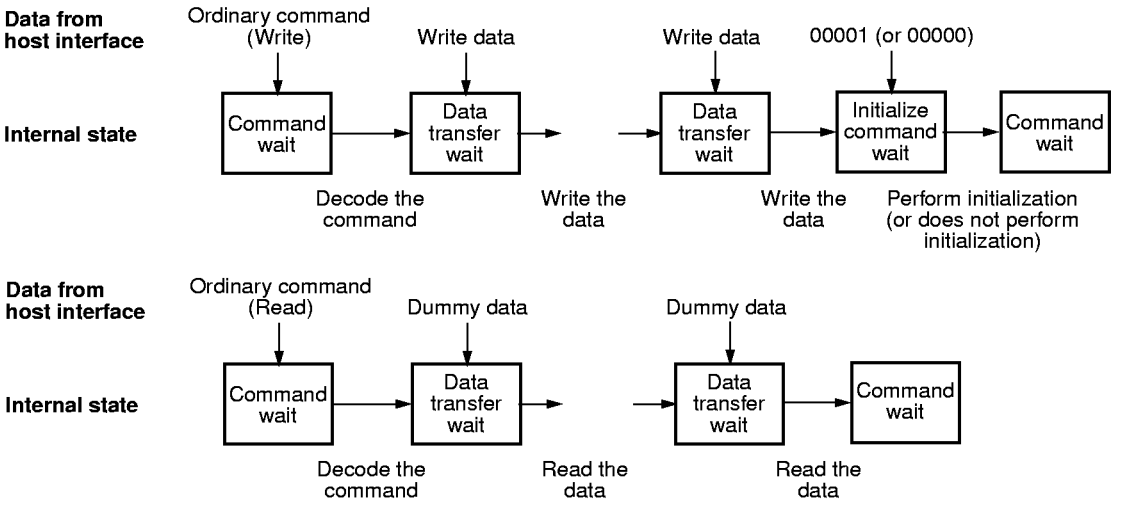
Host Control

Data Send/Receive Format

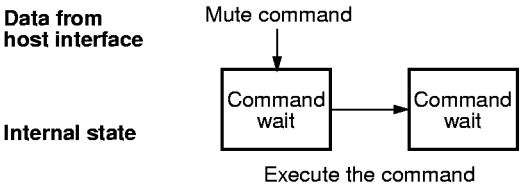
The internal program is controlled via the host interface. This section explains the format of commands and data transferred from the host interface.

After reset, the internal program starts running according to the default settings (A/D mode). The host interface enters the command wait state. For external communication, a command transfer must be performed during this command wait state. The host command includes the ordinary command for writing to and reading data from internal memory and the mute command for issuing a mute ON/OFF request.

When a command is transferred from the host interface with the MB86342 in the command wait state, the MB86342 decodes and executes the command. If the transferred command is an ordinary command, the MB86342 waits until the word count specified by the command is transferred. After the data transfer is completed, in the case of the read command, the MB86342 enters the command wait state again; in the case of the write command, the MB86342 enters the initialize command wait state. An input of "1" in the initialize command wait state causes initialization, and an input of "0" does not cause initialization. Most commands do not become valid for the internal program unless initialization is performed, so initialization should be performed after transferring all parameters. At initialization, the output is muted once and then unmuted after resetting all modes again according to the input data. When the initialization command is input, the MB86342 enters the command wait state again.



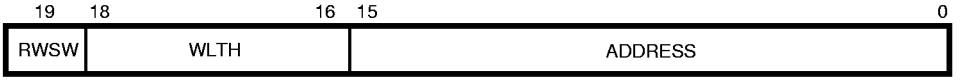
If the command is the mute command, the MB86342 executes the command as soon as it is input and enters the command wait state again. Initialization is performed at the input of the mute command.



There are two commands transferred from the host: ordinary command and mute command. The ordinary command provides the transfer (read or write) of 1 to 8 words of data from the MB86342 to the host or from the host to the MB86342. The mute command provides mute ON/OFF control. These two commands are accepted when the MB86342 is in the command wait state. After the chip reset, the MB86342 executes the mute command or the ordinary command, accesses by the specified word count (reads data by the word count specified by the read command, writes data by the word count specified by the write command, and transfers the initialize command), and then enters the command wait state.

Ordinary command

The ordinary command has the following format:



RWSW: Read/write instruction identification flag
0: Data transfer (read) from MB86342 to host
1: Data transfer (write) from host to MB86342

WLTH: Read/write word count 0 to 7: 1 to 8 words

ADDRESS: Read/write starting address

WLTH has a value of the actual read/write word count minus 1. For example, WLTH = 3 indicates that the actual access word count is 4 words. The write instruction is transferred and then followed by the initialize command. There are two types of data written to memory by the write instruction: one that is used for MB86342 signal processing immediately after it is written, and another that is not used unless initialization is performed. The latter allows multiple settings at once by initialization after all necessary bits are set. Initialization takes 32 ms of mute until it is completed.

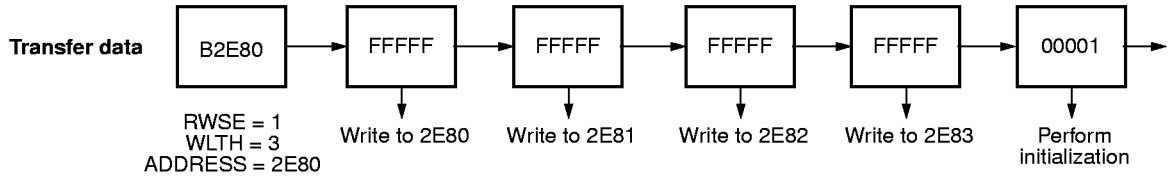
The initialize command has the following settings:

0: Initialization not performed
1: Initialization performed

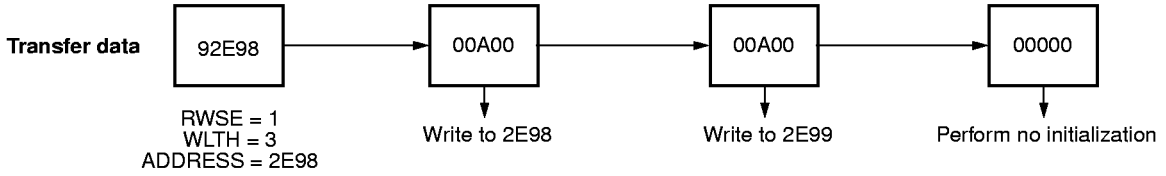
Note: The initialization command "0" must be transferred after a data write even if the initialization is not performed.

Example of Data Write from Host to MB86342

When transferring 4 words of $FFFFF from host to address $2E80 (and subsequent) and performing the initialization:

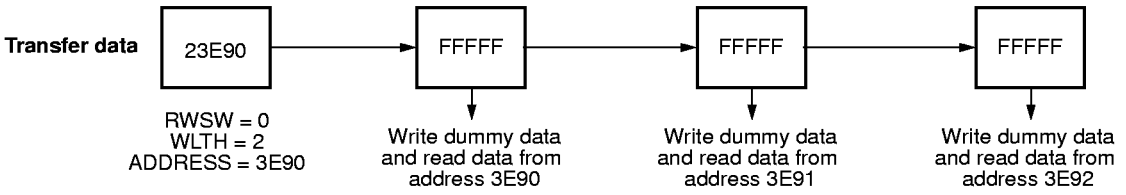


When transferring 2 words of $00A00 from host to address $2E98 (and subsequent) and performing no initialization:



Example of Data Read from MB86342 to Host

When transferring 3 words of data from address $3E90 (and subsequent) from MB86342 to host:



Mute command

The mute command has the following settings:

0: Mute OFF
1: Mute ON

This command is accepted when the MB86342 is in the command wait state.

Setting Parameter Values

The following parameters are set through the host command to program the MB86342 to the appropriate operation states.

Parameters are specified by transferring the values to the host command area from addresses $2F60_H$ to $2F7F_H$ of the internal RAM in the MB86342. The parameters corresponding to the RAM addresses of the MB86342 are shown below.

When data is rewritten to addresses other than those shown below, a malfunction may occur. Therefore, do not write data to any other addresses of the host command area.

Each value should be set within limits. For example, MOD of PSMOD are two bits and may theoretically be set with the values 0 to 3, where no mode is actually assigned to 3. Thus, MOD can be set with the values 0 to 2 but should not be set with the value 3. Unless otherwise specified, always set the parameter's unassigned bits in one word to 0.

KABC
Address: 2F60
Initial Value: 00000

19 18	17 12	11 6	5 0
KMOD	c	b	a

KDEF
Address: 2F61
Initial Value: 00000

19 18	17 12	11 6	5 0
KCDS	f	e	d

KGHI
Address: 2F62
Initial Value: 00000

19 18	17 12	11 6	5 0
0	i	h	g

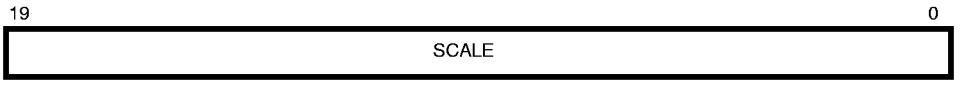
a to i: Downmix factors in Karaoke and capable mode ($00F_H$ to $3F_H$ (0.0 to 0.984375))

KMOD: Karaoke mode
0: Aware
1: Capable and default
2: Capable and a to i valid

KCDS: Setting at capable and default
0: No vocal
1: V1 only
2: V2 only
3: V1 + V2

Notes:
1) The KABC, KDEF and KGHI Karaoke modes are valid only when a Dolby Digital Karaoke bit stream is input. These parameters become valid immediately after they are specified, without initialization.
2) a to i are valid only when KMOD is set to 2.
3) Bits 18 and 19 of the KGHI register should be set to 0.

GSET1
Address: 2F63
Initial Value: 40000

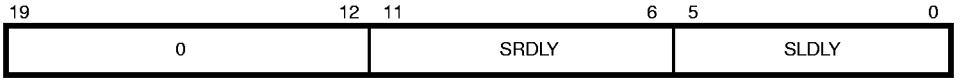


SCALE: Output scale factor 00000_H to 40000_H(0.0 to 1.0)

Notes:
1) This factor is used for scaling the output value of a previous channel. The values of the GSET1 register become valid for the program immediately after they are specified, even without initialization.
2) After a reset, always write 0 to addresses 2F66 and 2F67.

TDF
Address: 2F6D
Initial Value: 00000

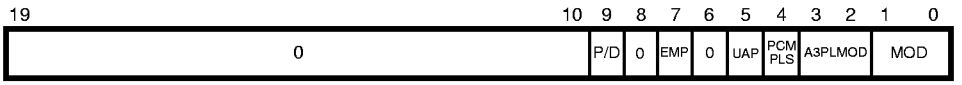
TDR
Address: 2F6E
Initial Value: 00000



LDLY: L-channel delay (0 to 10 (ms))
RDLY: R-channel delay (0 to 10 (ms))
CDLY: C-channel delay (0 to 10 (ms))
LFEDLY: LFE-channel delay (0 to 10 (ms))
SLDLY: SL-channel delay (0 to 30 (ms))
SRDLY: SR-channel delay (0 to 30 (ms))

Notes:
1) Bits 16 to 19 of the TDF register should be set to 0.
2) Bits 12 to 19 of the TDR register should be set to 0.
3) Each channel delay can be adjusted in 1 ms steps.

PSMOD
Address: 2F70
Initial Value: 00201



MOD: Input data mode
0: Test tone
1: A/D input
2: DIR input

A3PLMOD: Pro Logic mode in Dolby Digital decoding
0: Pro Logic OFF
1: Pro Logic ON
2: Auto select

PCMPLS: Pro Logic mode in PCM
0: Pro Logic OFF
1: Pro Logic ON

UAP: User application switch
0: OFF
1: ON

EMP: De-emphasis filter switch
0: De-emphasis filter OFF
1: De-emphasis filter ON

P/D: PCM/Dolby Digital mode selector switch with MOD = 2
0: Dolby digital mode
1: PCM mode

Notes:
1) User applications are valid even with MOD = 0.
2) The A3PLMOD switch is valid only for Dolby Digital 2-ch input.
3) PCMPLS is valid only in A/D input or PCM mode.
4) The UAP switch should be set to ON after booting the user application program properly.
5) The EMP switch is valid only with MOD = 2 and P/D = 1
6) The P/D switch is valid only with MOD = 2.
7) Bits 6, 8, and 10 to 19 of the PSMOD register should be set to 0.

A3MOD
Address: 2F71
Initial Value: 0FEB8

19 16	15	14 13	12 10	9 8	7 6	5	4	3	2 0
0	LFE	DM	DMX	CMPMOD2	CMPMOD1	1	1	1	BSN

BSN: Detect bit stream numbers 0 to 7

CMPMOD1: Compression mode 1
0: Custom and analog dial norm
1: Custom and digital dial norm
2: Lineout mode
3: RF mode

CMPMOD2: Compression mode 2
0: Custom and analog dial norm
1: Custom and digital dial norm
2: Lineout mode
3: RF mode

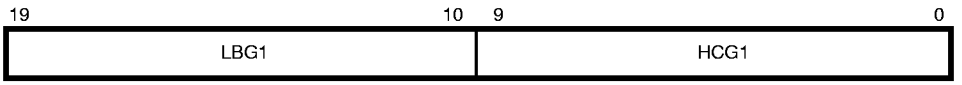
DMX: Downmix types 0 to 7
0: Dolby Surround Compatible
Others: acmod (audio coding mode) compatible

DM: Dual monophonic output mode
0: Monophonic
1: Channel 1 only
2: Channel 2 only
3: Stereo

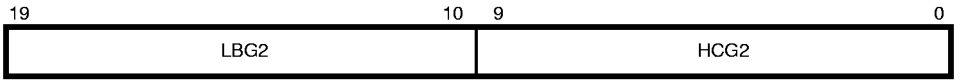
LFE: LFE output enable flag
0: OFF
1: ON

Notes:
1) The A3MOD's parameters above are valid only in the Dolby Digital mode.
2) CMPMOD1 is a compression mode of L-ch with acmod=0 (1+1 mode) and acmod<> 0 (other than 1+1 mode).
3) CMPMOD2 is a compression mode valid only for R-ch with acmod=0 (1+1 mode).
4) DMX should be set according to the speaker count.
5) DM is valid only with acmod=0 (1+1 mode).
6) Bits 3, 4, and 5 of the A3MOD register should be set to 1.
7) Bits 16 to 19 of the A3MOD should be set to 0.

CMPGAIN1
Address: 2F72
Initial Value: 00000



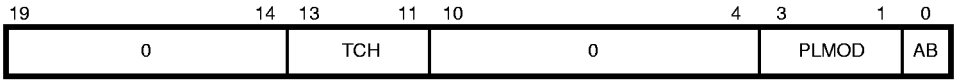
CMPGAIN2
Address: 2F73
Initial Value: 00000



HCG1 and HCG2: High-level signal cut gain (000 to 3FE (0.0 to 0.99805), 3FF (1.0))
LBG1 and LBG2: Low-level signal boost gain (000 to 3FE (0.0 to 0.99805), 3FF (1.0))

Notes:
1) The CMPGAIN1 and CMPGAIN2 parameters are valid only in the Dolby Digital mode.
2) The HCG1 and LBG1 parameters are valid for L-ch with acmod=0 and acmod<>0. They are valid when CMPMOD1 of the A3MOD register is set to 0, 1 or 2.
3) The HCG2 and LBG2 parameters are valid only for R-ch with acmod=0. They are valid when CMPMOD2 of the A3MOD register is set to 0, 1 or 2.
4) HCG1 and HCG2 are scaling factors operating on dynamic range values which decrease the level of a high-level signal.
5) LBG1 and LBG2 are scaling factors operating on dynamic range values which increase the level of a low-level signal.

PLSET
Address: 2F75
Initial Value: 00009



AB: Pro Logic auto input balance switch
0: OFF
1: ON

PLMOD: Pro Logic output channel setting
0: LCRS output
1: LRS output
2: LCR output
4: LCRS (S = -3 dB) output
5: LRS (S = -3) output

TCH: Test tone channel
0: L
1: R
3: SR
4: C

Notes:
1) PLMOD should be set identical to the rear speaker count. The rear speaker count specified by PLMOD is valid both in the Pro Logic mode and in other modes (Dolby Digital and PCM). When not using rear speakers, PLMOD should be set to 2.
2) Bits 4 to 10 and 14 to 19 of the PLSET register should be set to 0.

AMR
Address: 2F78
Initial Value: 00A9A

19 ... 12	11	10	9	8	7 ... 6	5	4	3	2 ... 1	0
0	ICK	IDS	IFS	IDF	IDL	ILRF	OFS	ODF	ODL	OLRF

OLRF: L-ch output logic
0: Output at LRCKO-H
1: Output at LRCKO-L

ODL: Output data word length
0: 20-bit
1: 18-bit
2: 16-bit

ODF: Output valid data
0: Back-filled
1: Front-filled

OFS: BCKO output
0: 32 fs
1: 64 fs

ILRF: L-ch input logic
0: Input at LRCKI-H
1: Input at LRCKI-L

IDL: Input data word length
0: 20-bit
1: 18-bit
2: 16-bit

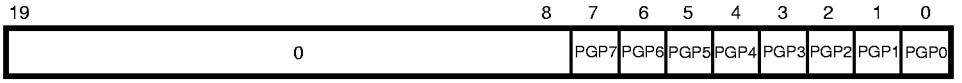
IDF: Input valid data
0: Back-filled
1: Front-filled

IFS: BCKI input
0: 32 fs
1: 64 fs

IDS: Valid channel
0: Ch 1
1: Ch 2

ICK: BCKI1 and LRCKI1 setting
0: Input
1: Output

DRR
Address: 2F79
Initial Value: 000FF



RGP0: gp0 direction register
0: Input
1: Output

RGP1: gp1 direction register
0: Input
1: Output

RGP2: gp2 direction register
0: Input
1: Output

RGP3: gp3 direction register
0: Input
1: Output

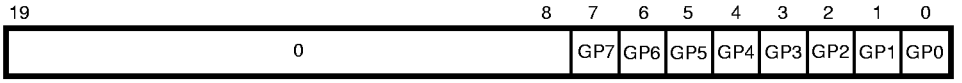
RGP4: gp4 direction register
0: Input
1: Output

RGP5: gp5 direction register
0: Input
1: Output

RGP6: gp6 direction register
0: Input
1: Output

RGP7: gp7 direction register
0: Input
1: Output

DAR
Address: 2F7A
Initial Value: 00000



GP0: gp0 register (0, 1)

GP1: gp1 register (0, 1)

GP2: gp2 register (0, 1)

GP3: gp3 register (0, 1)

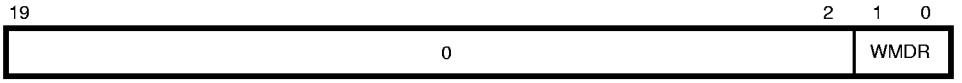
GP4: gp4 register (0, 1)

GP5: gp5 register (0, 1)

GP6: gp6 register (0, 1)

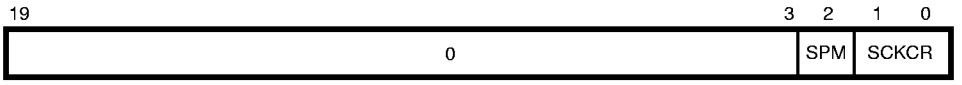
GP7: gp7 register (0, 1)

WMDR
Address: 2F7B
Initial Value: 00003



WMDR: External memory wait value (0 to 3; values exceeding 3 must not be set)

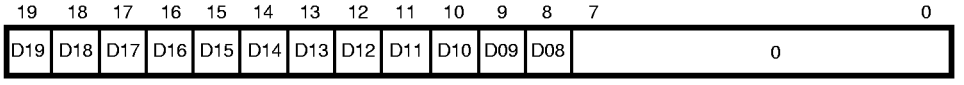
SCKCR
Address: 2F7C
Initial Value: 00004



SCKCR: Clock control
0: ADC clock output
1 or 2: Output clock stop
3: Internal clock output

SPM: Clock speed control
0: Low-speed mode
1: High-speed mode

DAR
Address: 2F7A
Initial Value: 00000



D08: D08 setting (0, 1)

D09: D09 setting (0, 1)

D10: D10 setting (0, 1)

D11: D11 setting (0, 1)

D12: D12 setting (0, 1)

D13: D13 setting (0, 1)

D14: D14 setting (0, 1)

D15: D15 setting (0, 1)

D16: D16 setting (0, 1)

D17: D17 setting (0, 1)

D18: D18 setting (0, 1)

D19: D19 setting (0, 1)

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Vss = 0V	V_{SS}–0.5 to +4.0	V
Input voltage	V_{IN}	—	V_{SS}–0.5 to V_{DD}+0.5	V
Output voltage	V_{OUT}	—	V_{SS}–0.5 to V_{DD}+0.5	V
Output current	I_{OUT}	I_{OL} = 4.0mA	±14	mA
		I_{OL} = 8.0mA	±14	mA
Storage temperature	T_{stg}	—	–40 to +125	°C
Overshoot	—	50ns (Max.)	V_{DD}+1.0	V
Undershoot	—	50ns (Max.)	V_{DD}+1.0	V

Note: Permanent device damage may occur if the above Absolute Maximum Ratings are exceeded. Functional operation should be restricted to the conditions detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Value			Unit
		Min.	Typ.	Max.	
Power supply voltage	V_{DD}	3.00	3.30	3.60	V
"H"-level input voltage	V_{IH}	$V_{DD} \times 0.7$	—	V_{DD}	V
"L"-level input voltage	V_{IL}	V_{SS}	—	$V_{DD} \times 0.2$	V
Operating temperature	T_a	0	—	70	°C

Electrical Characteristics

Input/Output Pin Capacitance

T_a = 25°C, frequency = 1 MHz

Parameter	Symbol	Requirements	Unit
Input pin	C_{IN}	Max.16	pF
Output pin: I_{OL} = 4mA 8mA	C_{OUT}	Max.16	pF
I/O pin: I_{OL} = 4mA 8mA	$C_{I/O}$	Max.16	pF

DC Characteristics

V_{DD} = 3.0 to 3.6V, V_{SS} = 0V, T_a = 0 to 70°C

Parameter	Symbol	Condition	Value			Unit
			Min.	Typ.	Max.	
Power supply current	I_{DDS}	Standby mode *1	—	—	100	µA
	I_{DD}	Operating mode	—	160	240	mA
"H"-level input voltage	V_{IH}	—	$V_{DD} \times 0.7$	—	V_{DD}	V
"L"-level input voltage	V_{IL}	—	V_{SS}	—	$V_{SS} \times 0.2$	V
"H"-level output voltage	V_{OH}	I_{OH} = −4mA	V_{DD}−0.5	—	V_{DD}	V
		I_{OH} = −8mA	V_{DD}−0.5	—	V_{DD}	V
"L"-level output voltage	V_{OL}	I_{OL} = 4mA	V_{SS}	—	0.4	V
		I_{OL} = 4mA	V_{SS}	—	0.4	V
Input leakage current *2 (Tri-state pin input)	I_{LI}	V_I = 0–V_{DD}	−10	—	10	µA
	I_{LZ}	V_I = 0–V_{DD}	−10	—	10	µA
Pull-up/-down resistance	RP	—	10	25	50	kΩ
Output short-circuit current	I_O*3	Type/condition	$V_O = V_{DD}$		V_O = 0V	mA
		Normal/I_{OL} = 4mA	+40		−40	mA
		Normal/I_{OL} = 8mA	+80		−80	mA

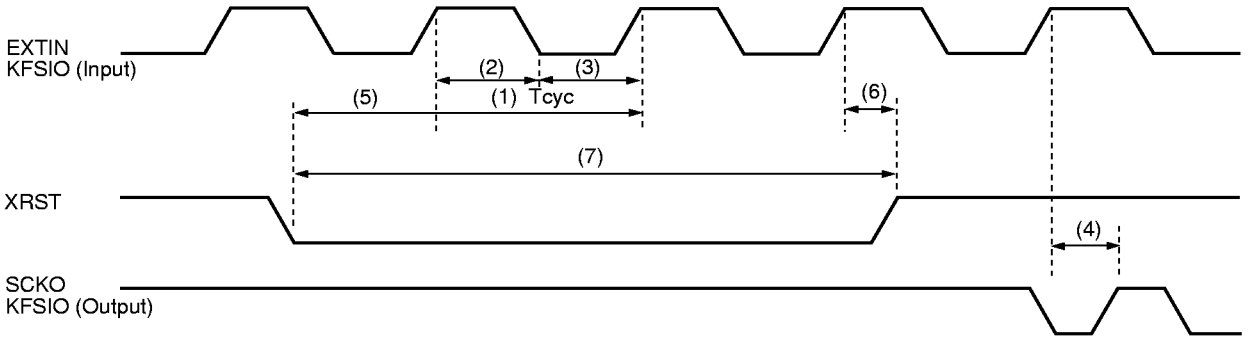
Notes: *1) $V_{IH} = V_{DD}$, $V_{IL} = V_{SS}$. The memory is in the standby mode.

*2) If an input buffer with a pull-up/-down resistor is used, the input leakage current may exceed the above value.

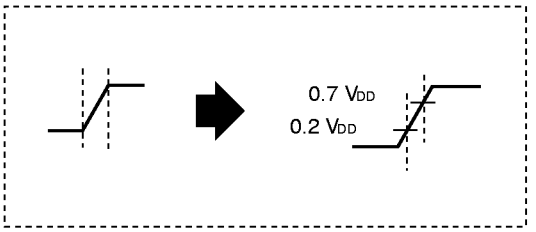
*3) Maximum supply current at the short circuit of output V_{DD} or V_{SS}. The short can only last one second per LSI pin when connected to output V_{DD} or V_{SS}.

AC Characteristics

EXTIN, SCKO, XRST



Note: Dotted line represents:



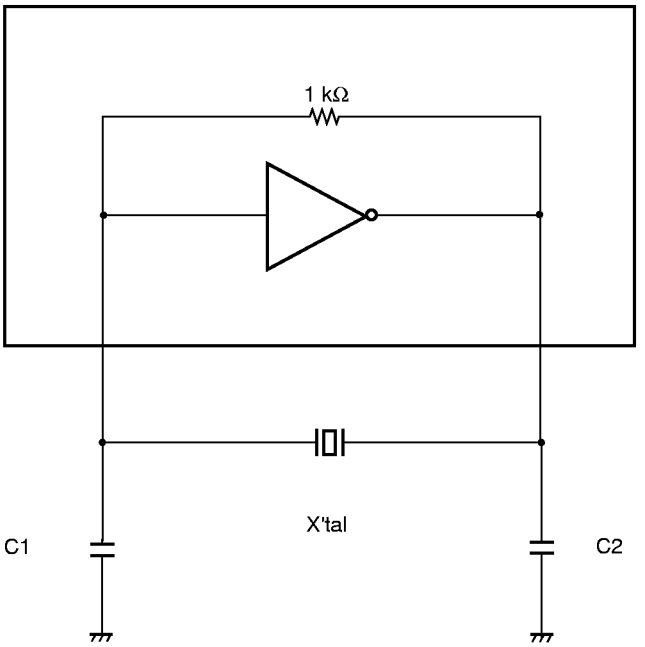
V_{DD} = 3.0 to 3.6V, V_{SS} = 0V, T_a = 0 to 70°C

No.	Characteristics	Min.	Typ.	Max.	Unit
(1)	EXTIN cycle	—	Tcyc	—	ns
(2)	EXTIN "H" pulse width	0.4×Tcyc	—	—	ns
(3)	EXTIN "L" pulse width	0.4×Tcyc	—	—	ns
(4)	SCKO delay time	—	—	11	ns
(5)	XRST setup time	6	—	—	ns
(6)	XRST hold time	3	—	—	ns
(7)	XRST "L" pulse width	(see table below)	—	—	ns
(8)	PLL lock-up time	100	—	—	µs

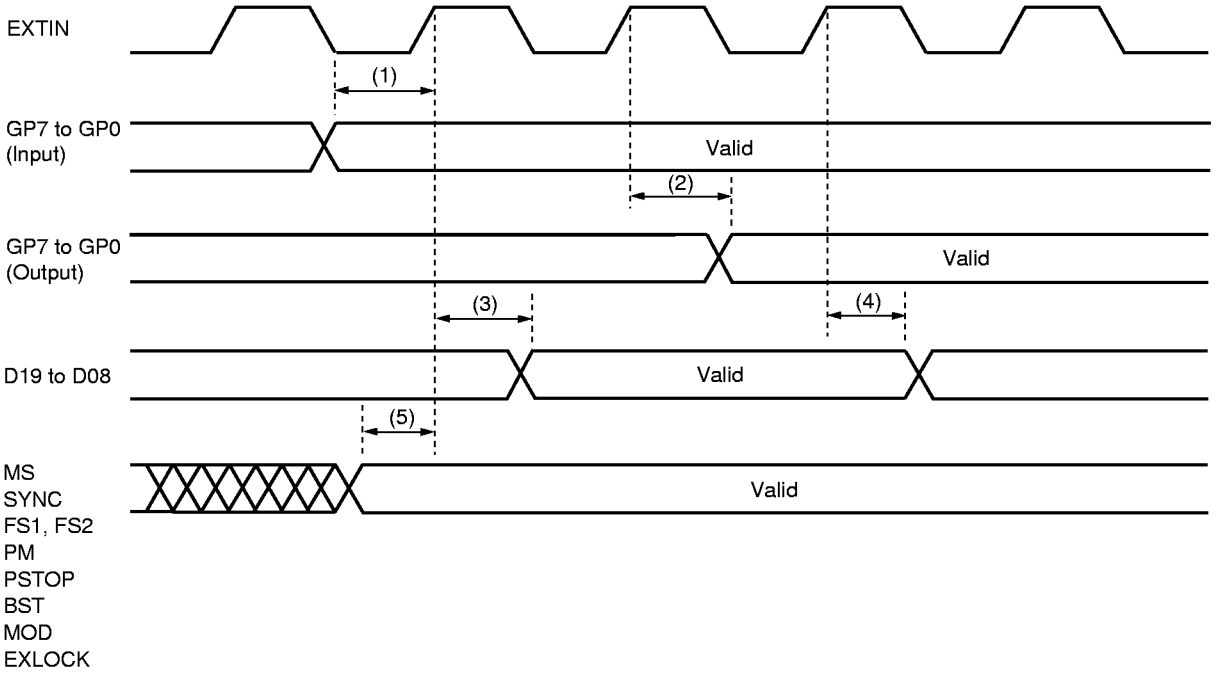
EXTIN frequency

EXTIN Frequency (MHz)	Tcyc(ns)	Clock Mode	Sampling Frequency	PLL Select	CORE Master Clock (MHz)	XRST "L" Pulse Width(ns)
18.432	54.253	Fast mode	48	16/3	98.304	9/8Tcyc=61.035
		Slow mode	48	6	110.592	1Tcyc=54.253
16.9344	59.0514	—	44.1	6	101.6064	1Tcyc=59.0514
12.288	81.380	—	32	8	98.304	3/4Tcyc=61.035

Crystal Oscillator



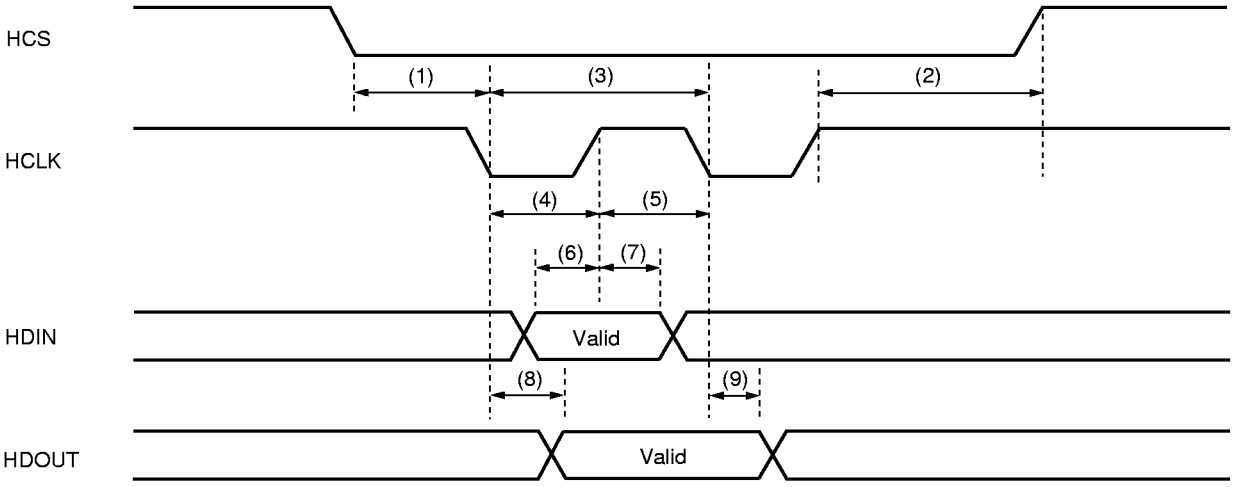
GP0 to 7, D08 to 19, MS, SYSNC, FS1, FS2, PM, PSTOP



V_{DD} = 3.0 to 3.6V, V_{SS} = 0V, T_a = 0 to 70°C

No.	Characteristics	Min.	Typ.	Max.	Unit
(1)	GP0 to 7 setup time	6	—	—	ns
(2)	GP0 to 7 delay time	—	—	17	ns
(3)	D08 to 19 delay time	—	—	17	ns
(4)	D08 to 19 hold time	2	—	—	ns
(5)	Setup time	4	—	—	ns

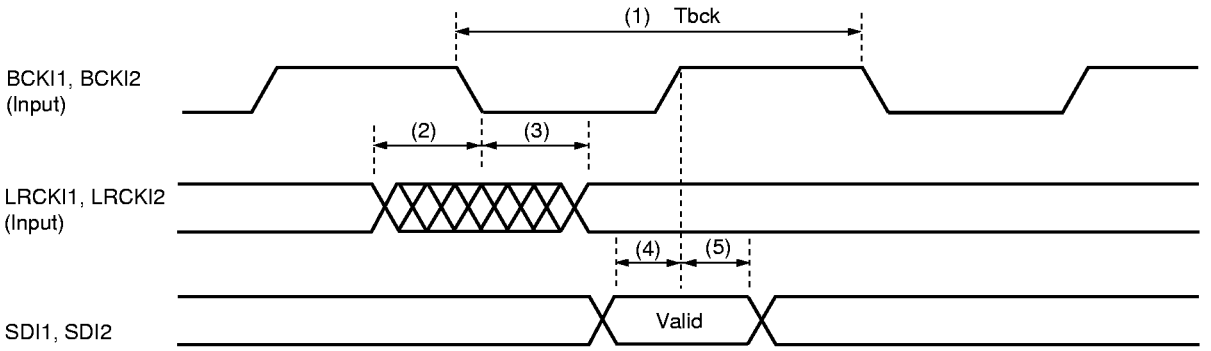
HCS, HCLK, HDIN, HDOUT



V_{DD} = 3.0 to 3.6V, V_{SS} = 0V, T_a = 0 to 70°C

No.	Characteristics	Min.	Typ.	Max.	Unit
(1)	HCS clock active setup time	16	—	—	ns
(2)	HCS clock active hold time	16	—	—	ns
(3)	HCLK pulse cycle	36	—	—	ns
(4)	HCLK "H" pulse width	16	—	—	ns
(5)	HCLK "L" pulse width	16	—	—	ns
(6)	HDIN setup time	4	—	—	ns
(7)	HDIN hold time	6	—	—	ns
(8)	HDOUT delay time	—	—	10	ns
(9)	HDOUT hold time	1	—	—	ns

LRCKI1, LRCKI2, BCKI2, SDI1, SDI2 (Input Mode)



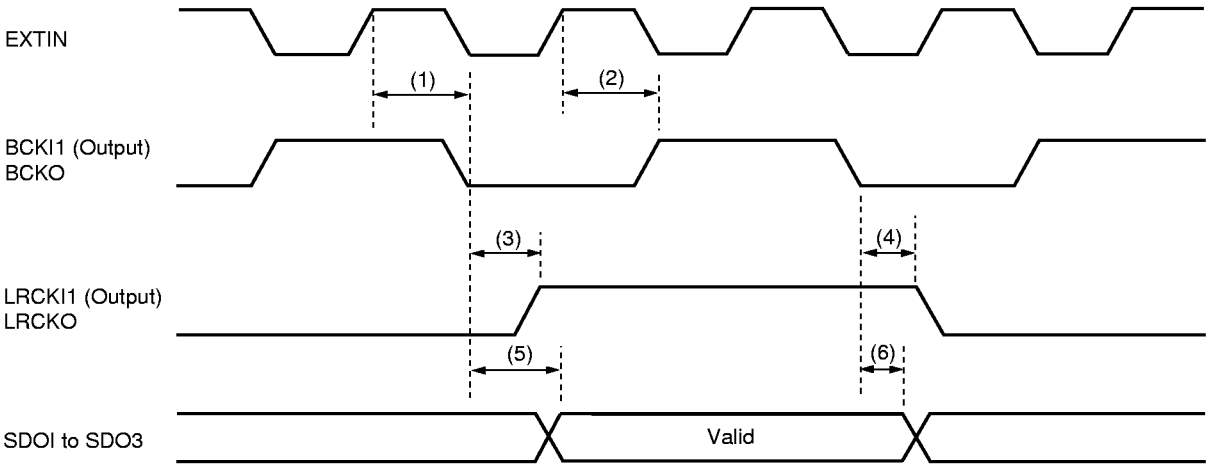
V_{DD} = 3.0 to 3.6V, V_{SS} = 0V, T_a = 0 to 70°C

No.	Characteristics	Min.	Typ.	Max.	Unit
(1)	BCKI1, BCKI2 cycle (Tbck)	—	(see table below)	—	ns
(2)	LRCKI1, LRCKI2 setup time	—	—	1/4 Tbck	ns
(3)	LRCKI1, LRCKI2 hold time	—	—	1/4 Tbck	ns
(4)	SDI1, SDI2 setup time	3	—	—	ns
(5)	SDI1, SDI2 hold time	6	—	—	ns

BCKI1, BCKI2 frequency

BCKI1, BCKI2 Tbck (ns)	Audio Mode Setting	EXTIN (MHz)
651.036	32fs	18.432
325.518	64fs	18.432
708.6168	32fs	16.9344
354.3084	64fs	16.9344
976.560	32fs	12.288
488.280	64fs	12.288

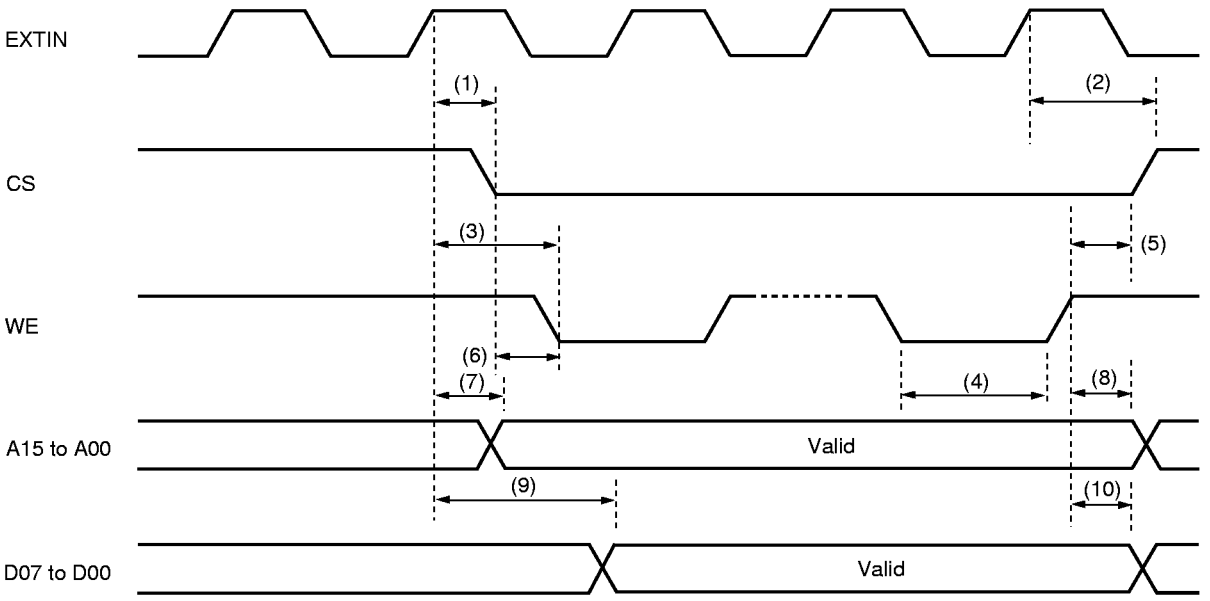
LRCKI1, BCKI1, LRCKO, BCKO, SDO1 to 3 (Output Mode)



V_{DD} = 3.0 to 3.6V, V_{SS} = 0V, T_a = 0 to 70°C

No.	Characteristics	Min.	Typ.	Max.	Unit
(1)	BCKI1, BCKO fall delay time	—	—	11	ns
(2)	BCKI1, BCKO rise delay time	—	—	11	ns
(3)	LRCKI1, LRCKO fall delay time	—	—	5	ns
(4)	LRCKI1, LRCKO rise delay time	—	—	5	ns
(5)	SDO1 to 3 delay time	—	—	7	ns
(6)	SDO1 to 3 hold time	0.5	—	—	ns

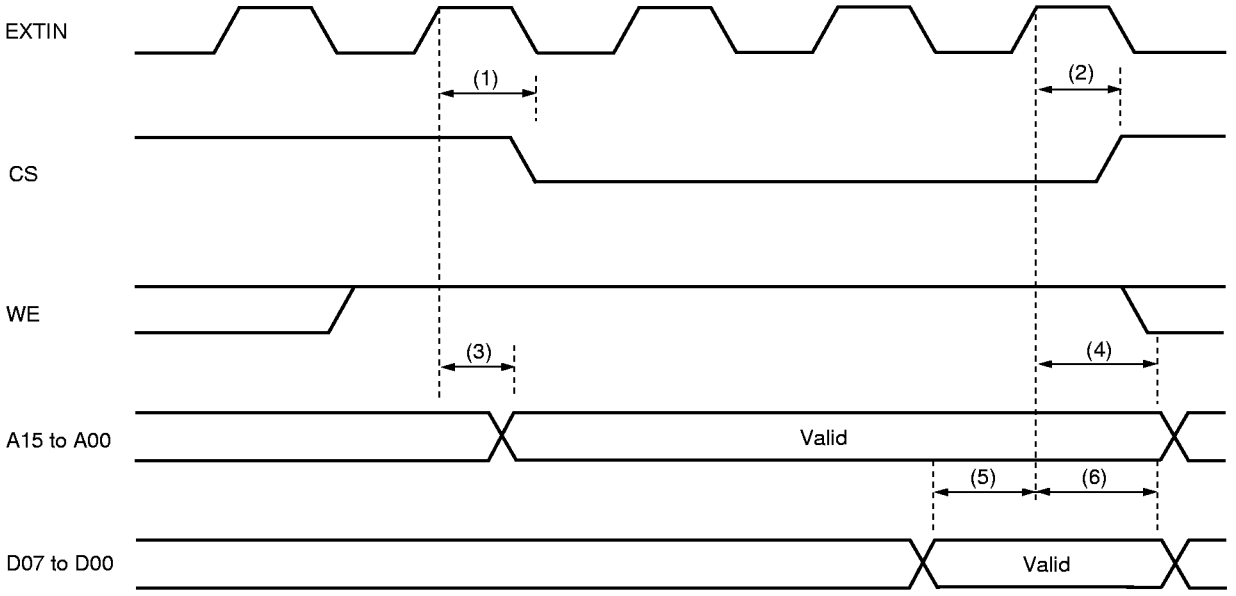
CS, WE, A00 to 15, D00 to 07 (Data Write)



V_{DD} = 3.0 to 3.6V, V_{SS} = 0V, T_a = 0 to 70°C

No.	Characteristics	Min.	Typ.	Max.	Unit
(1)	CS delay time	—	—	20	ns
(2)	CS hold time	2	—	—	ns
(3)	WE delay time	—	—	22	ns
(4)	WE "H" pulse width	8	—	—	ns
(5)	WE hold time	2	—	—	ns
(6)	WE setup time	0.7	—	—	ns
(7)	A00 to 15 delay time	—	—	20	ns
(8)	A00 to 15 hold time	2	—	—	ns
(9)	D00 to 07 delay time	—	—	22	ns
(10)	D00 to 07 hold time	2	—	5	ns

CS, WE, A00 to 15, D00 to 07 (Data Read)

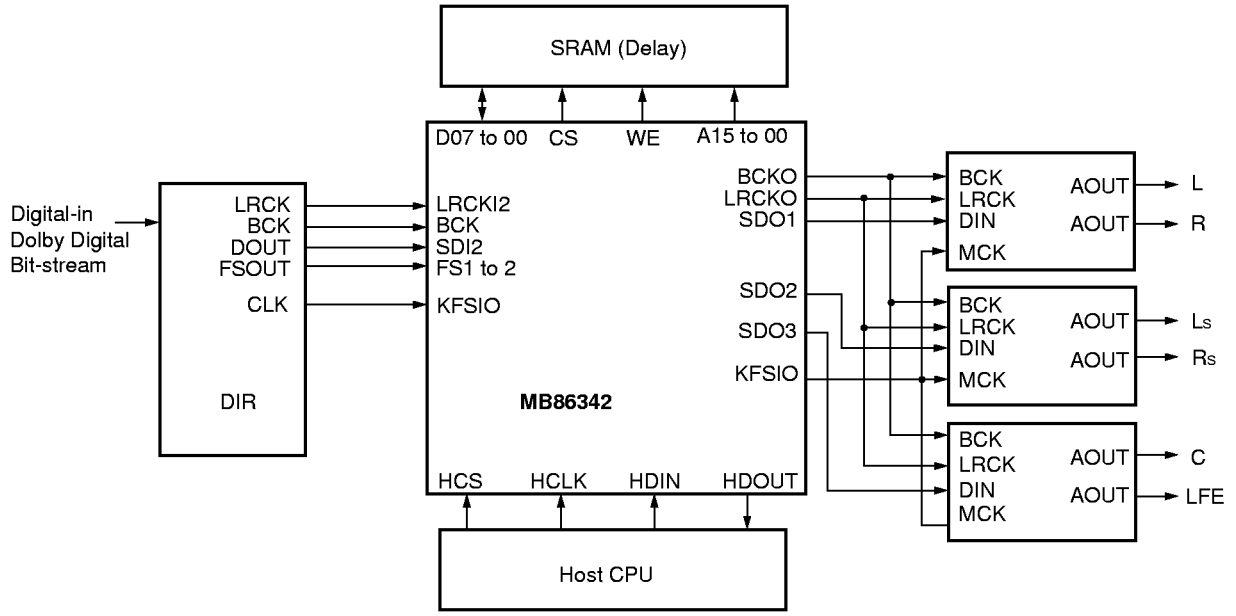


V_{DD} = 3.0 to 3.6V, V_{SS} = 0V, T_a = 0 to 70°C

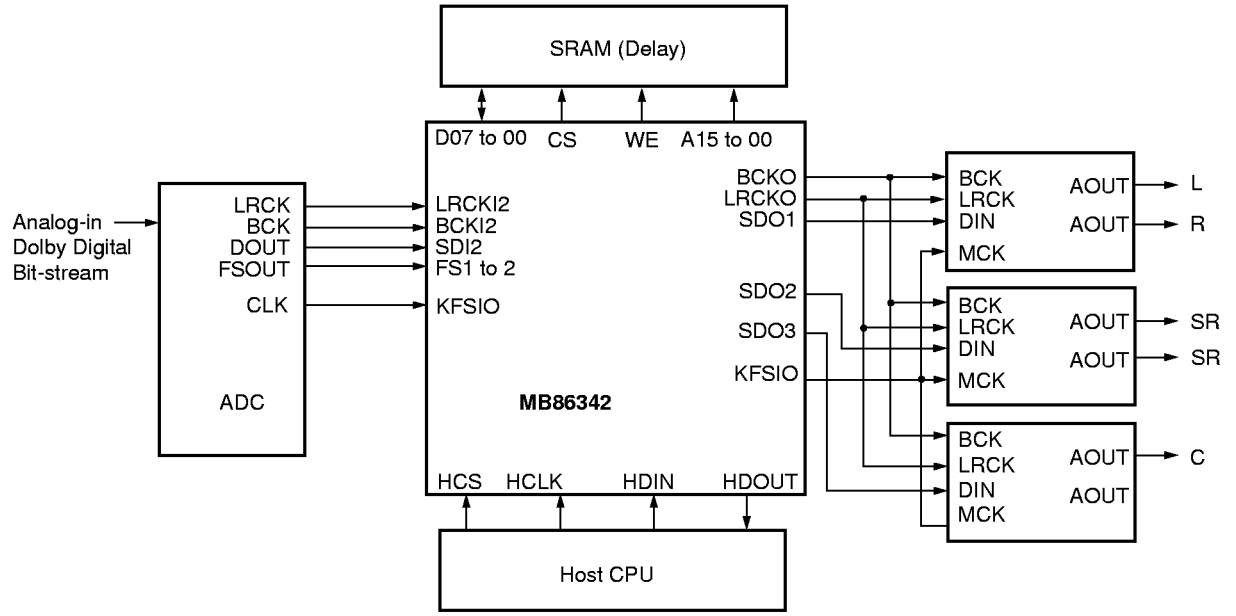
No.	Characteristics	Min.	Typ.	Max.	Unit
(1)	CS delay time	—	—	20	ns
(2)	CS hold time	2	—	—	ns
(3)	A00 to 15 delay time	—	—	22	ns
(4)	A00 to 15 hold time	3	—	—	ns
(5)	D00 to 07 setup time	3	—	—	ns
(6)	D00 to 07 hold time	7	—	—	ns

System Configuration

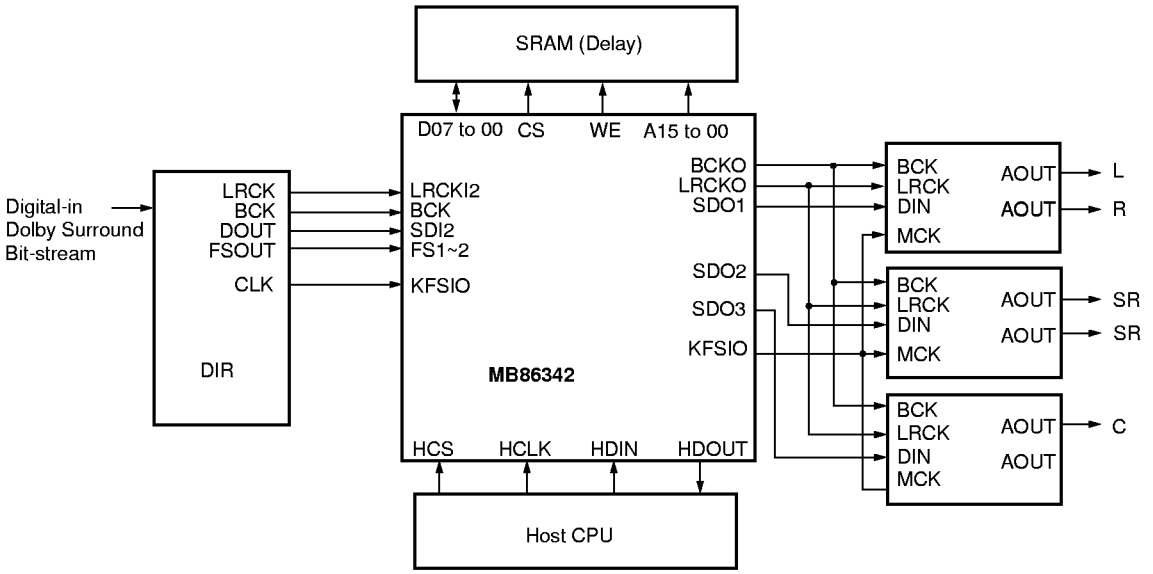
Dolby Digital Decoder (5.1-channel)



Dolby Pro Logic Decoder (4-channel)

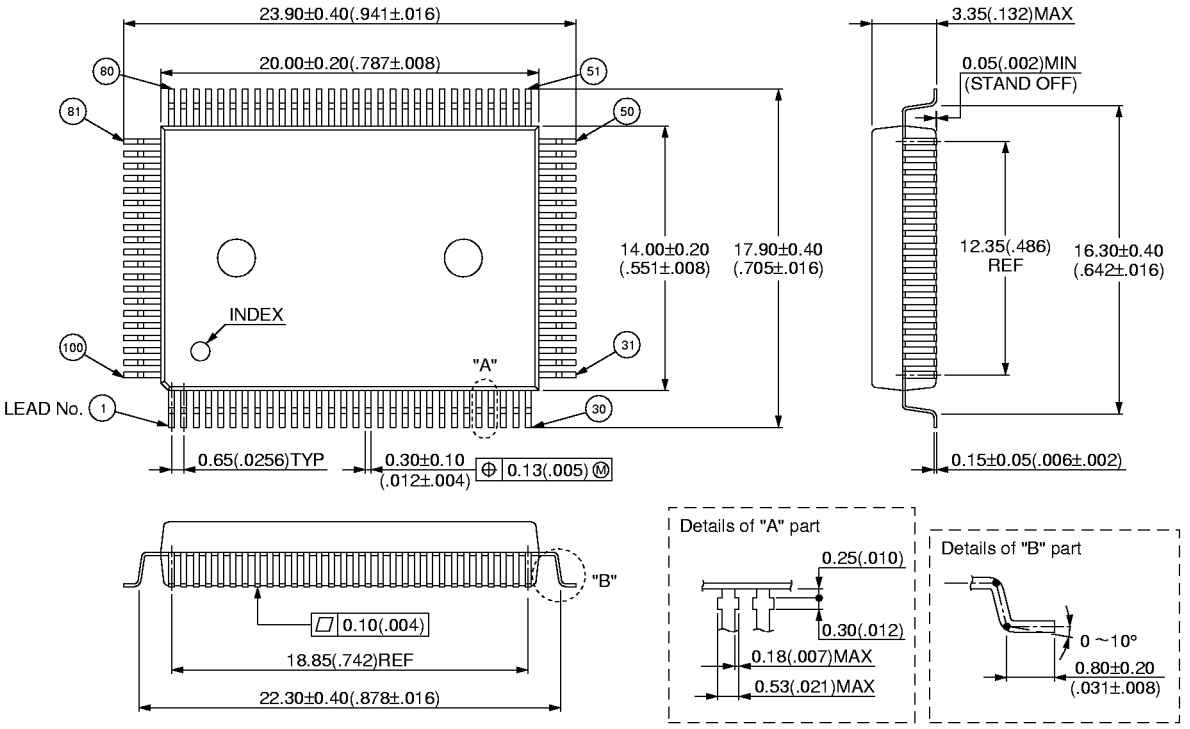


Dolby Digital + Dolby Pro Logic Decoder



Package Dimensions

100-pin, Plastic QFP
(FPT-100P-M06)



Dimensions in mm (inch)