

Drivers with Differentially Driven Normally Open and Normally Closed FET Switches designed for . . .



- Switching High Frequencies
- Switching in Satellite Applications
- Portable, Battery Operated Circuits
- Low Signal Distortion Switching Circuits such as Audio Switching

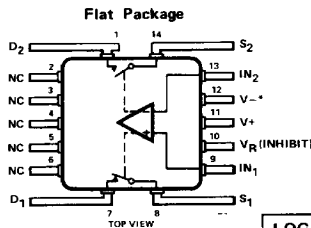
BENEFITS

- Higher Signal Bandwidth Switching Capabilities
 - OFF Isolation > 60 dB @ 1 MHz
- Better Radiation Resistance than PMOS Drivers
 - Bipolar Drivers
- Minimizes Standby Power Requirements
 - < 1 mW Standby Power
- Less Signal Distortion than CMOS or PMOS Switches
 - Constant ON Resistance

DESCRIPTION

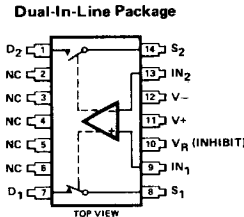
The DG164 contains four junction-type field-effect transistors designed to function as electronic switches. Level-shifting drivers enable low-level inputs (2 to 3 V) to control the ON-OFF state of the switches. The driver inputs are connected differentially so that with input IN_2 connected to a 2.5 voltage reference, a positive logic "0" at input IN_1 will turn switches 1 and 3 OFF and switches 2 and 4 ON. A positive logic "1" at IN_1 will turn switches 1 and 3 ON and switches 2 and 4 OFF. The normally-grounded V_R terminal may be used as an "Inhibit" terminal, in which case all switches may be held OFF with a positive voltage applied to V_R . In the ON state, each switch conducts equally well in either direction, has a series resistance of < 50 ohms, and a shunt leakage of < 2 nA. In the OFF state the switches will hold off voltages up to 15 V peak-to-peak. Switches have make-before-break action. The DG162 is similar to the DG164, except that it contains two FET switches instead of four. It is recommended that the DG187 (or DG188) and DG190 (or DG191) be used for new designs.

PIN CONFIGURATIONS

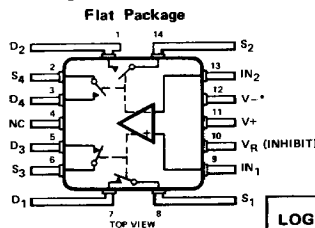


ORDER NUMBER:
DG162AL
SEE PACKAGE 5

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

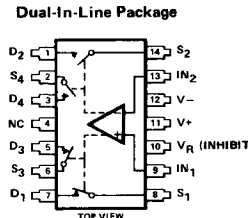


ORDER NUMBERS:
DG162AP OR DG162BP
SEE PACKAGE 11



ORDER NUMBER:
DG164AL
SEE PACKAGE 5

LOGIC	SW 1 SW 3	SW 2 SW 4
0	OFF	ON
1	ON	OFF

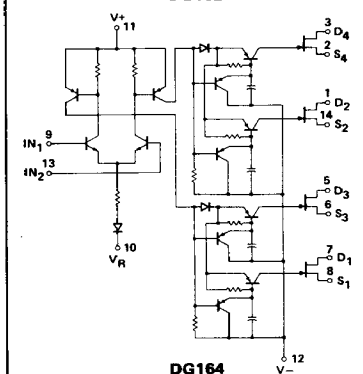
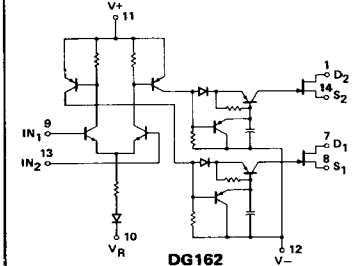


ORDER NUMBERS:
DG164AP OR DG164BP
SEE PACKAGE 11

*Common to Substrate and Base of Package

SWITCH STATES ARE FOR V_{IN1} = LOGIC "1" INPUT AND
 V_{IN2} = 2.5 V BIAS (POSITIVE LOGIC)

SCHEMATIC DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

V+ to V-	36 V	Current (Any Terminal)	30 mA
V+ to V _D or V _S	36 V	Storage Temperature	-65 to 150°C
V _D or V _S to V-	36 V	Operating Temperature (A Suffix)	-55 to 125°C
V _D to V _S	±22 V	(B Suffix)	-20 to 85°C
V+ to V _R	25 V	Power Dissipation*	
V+ to V _{IN1} or V _{IN2}	25 V	Flat Package**	750 mW
V _R to V-	25 V	14 Pin DIP***	825 mW
V _{IN1} to V _{IN2}	±6 V	*All leads welded or soldered to PC board.	
V _{IN1} or V _{IN2} to V _R	±6 V	**Derate 10 mW/°C above 75°C.	
V _{IN1} or V _{IN2} to V-	30 V	***Derate 11 mW/°C above 75°C.	

ELECTRICAL CHARACTERISTICS All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters and high and low temperature limits to assure conformance with specifications.

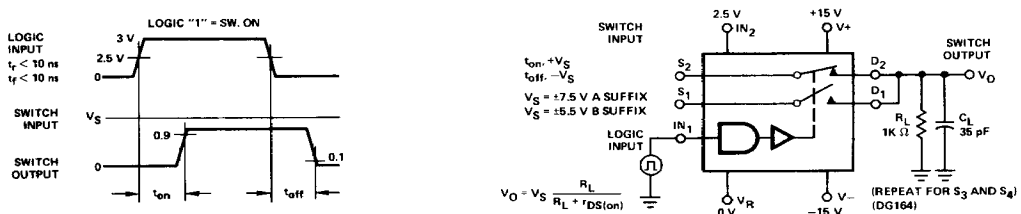
CHARACTERISTIC	MAX LIMITS						UNIT	TEST CONDITIONS, UNLESS NOTED: V+ = 15 V, V- = -15 V, V _R = 0, V _{IN2} = 2.5 V*	
	A SUFFIX			B SUFFIX					
	-55°C	25°C	125°C	-20°C	25°C	85°C			
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24	DS(on) ON Resistance	Ω	50	50	100			V _D = 7.5 V V _D = 5.5 V	I _S = -10 mA V _{IN1} = 3 V* (SW _{1,3} ON), V _{IN1} = 2 V* (SW _{2,4} ON)
2					100	100	150		
3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24	S(off) Leakage Current	nA		2	100			V _S = 7.5 V, V _D = -7.5 V V _S = 5.5 V, V _D = -5.5 V V _D = 7.5 V, V _S = -7.5 V V _D = 5.5 V, V _S = -5.5 V	V _{IN1} = 2 V* (SW _{1,3} OFF), V _{IN1} = 3 V* (SW _{2,4} OFF)
4						5	100		
5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24	D(off) Leakage Current	nA		2	100			V _D = V _S = -7.5 V V _D = V _S = -5.5 V	V _{IN1} = 3 V* (SW _{1,3} ON), V _{IN1} = 2 V* (SW _{2,4} ON)
6						5	100		
7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24	D(on) + S(on) Leakage Current	nA		-2	100				
8						-5	100		
9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24	IN1L Input 1 Current, Input 1 Voltage Low	μA	0.1	0.1	2	4	4	V _{IN1} = 2 V*	
10									
10 11 12 13 14 15 16 17 18 19 20 21 22 23 24	IN2L Input 2 Current, Input 2 Voltage Low	μA	0.1	0.1	2	4	4	V _{IN2} = 2 V*, V _{IN1} = 2.5 V*	
11									
11 12 13 14 15 16 17 18 19 20 21 22 23 24	IN1H Input 1 Current, Input 1 Voltage High	μA	120	60	60	150	100	V _{IN1} = 3 V*	
12									
12 13 14 15 16 17 18 19 20 21 22 23 24	IN2H Input 2 Current, Input 2 Voltage High	μA	120	60	60	150	100	V _{IN2} = 3 V*, V _{IN1} = 2.5 V*	
13									
13 14 15 16 17 18 19 20 21 22 23 24	t _{on} Turn-ON Time	μs		0.8		1	See Switching Time Test Circuit		
14	t _{off} Turn-OFF Time			1.6		2			
15 16 17 18 19 20 21 22 23 24	C _{S(off)} Source OFF Capacitance	pF		2.4 Typ		2.4 Typ	V _S = 0, I _D = 0 V _D = 0, I _S = 0 V _D = V _S = 0	f = 1 MHz	
16	C _{D(off)} Drain OFF Capacitance			2.4 Typ		2.4 Typ			
17	C _{D(on) + C_{S(on)}} Channel ON Capacitance			2.8 Typ		2.8 Typ			
18	Off Isolation		Typ > 60 dB at 1 MHz**					R _L = 75 Ω	
19 20 21 22 23 24	I+ Positive Supply Current	mA		4			4.4	V _{IN1} = 2 V* or V _{IN1} = 3 V*, One Channel ON	
20	I- Negative Supply Current			-2			-2.2		
21 22 23 24	I _R Reference Supply Current	μA		-2			-2.2	V _{IN1} = V _{IN2} = 0.8 V*, All Channels OFF	
22	I+ Positive Supply Current			25			25		
23	I- Negative Supply Current			-25			-25		
24	I _R Reference Supply Current			-25			-25		

*V_{IN} must be a step function with a minimum rise and fall rate of 1 V/μs.
**Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.

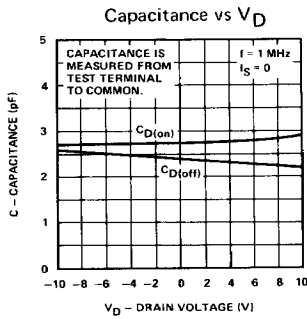
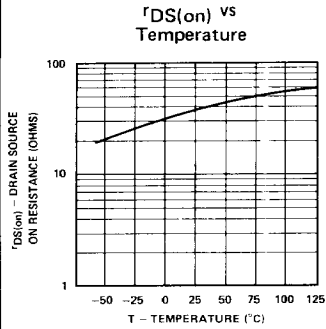
LOADF + NC

SWITCHING TIME TEST CIRCUIT

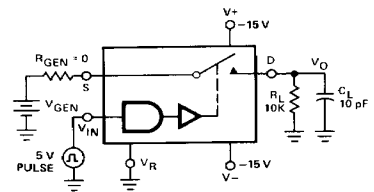
Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or - as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.



TYPICAL CHARACTERISTICS

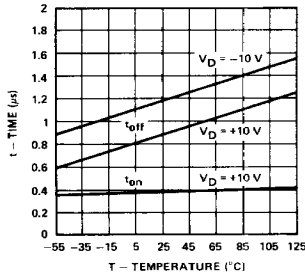


Typical delay, rise, fall, settling times, and switching transients in this circuit.

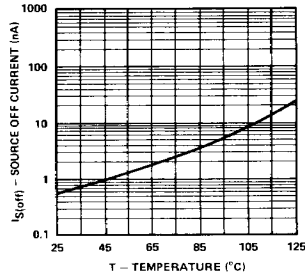


If R_{GEN} , R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times.

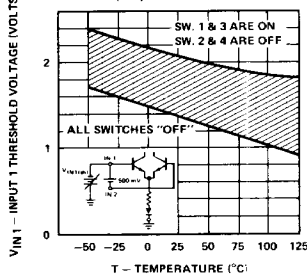
Switching Time vs V_D and Temperature



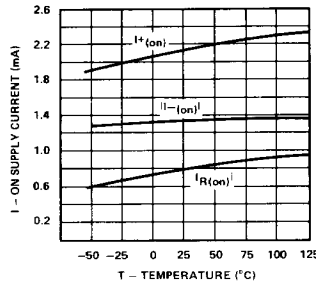
$I_{S(off)}$ vs Temperature



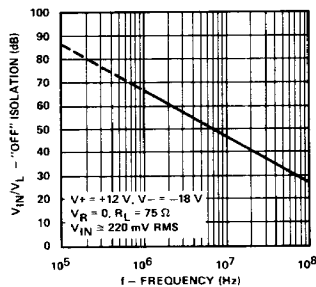
$V_{IN(th)}$ vs Temperature



Supply Current vs Temperature



"OFF" Isolation vs R_L and Frequency



Equivalent "OFF" Circuit

