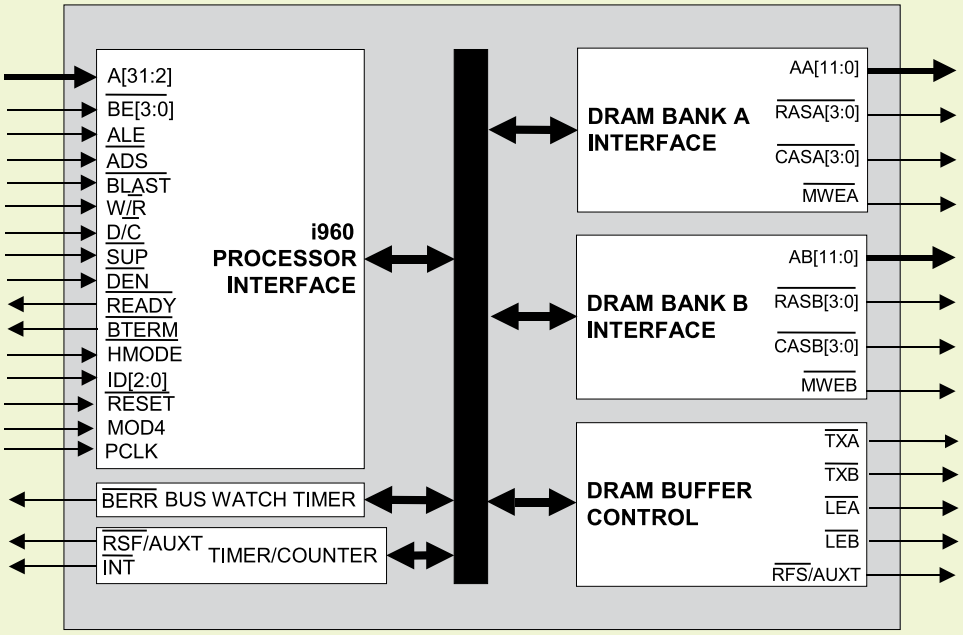
# V96BMC Rev D

## HIGH PERFORMANCE BURST DRAM CONTROLLER

### FOR i960®Cx/Hx/Jx and PowerPC™401Gx PROCESSORS




BLOCK DIAGRAM

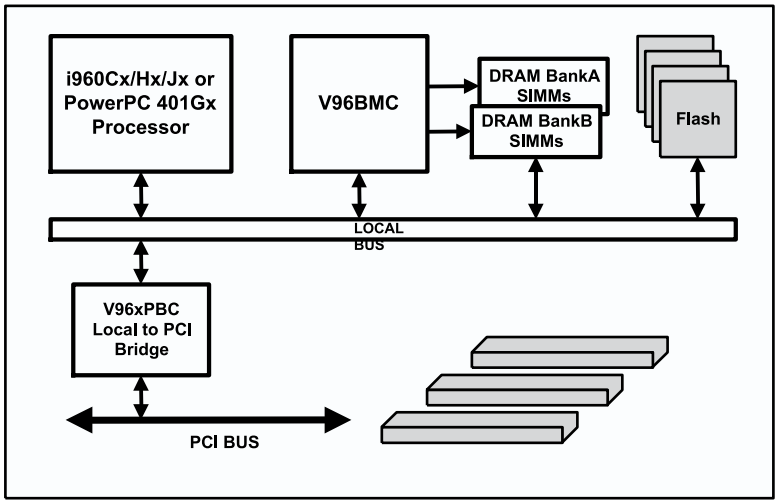
- Direct interface to i960Cx/Hx/Jx processors
- SRAM performance achieved with DRAM
- Supports up to 512Mbytes of DRAM
- 3.3V DRAM interface support
- Interleaved or non-interleaved operation
- Supports symmetric and non-symmetric arrays
- Software-configured operational parameters
- Integrated Page Cache Management
- 2Kbyte burst transaction support
- Designed to work with V961PBC and V962PBC PCI bridges
- On chip memory address multiplexer/drivers
- Two 24-bit counters/timers
- 8-bit bus watch timer
- Auto refresh
- Up to 40MHz operation
- Low cost 132-pin PQFP package

V3 SEMICONDUCTOR
THE EMBEDDED CHIPSET COMPANY

# COST EFFECTIVE SOLUTIONS THAT SIMPLIFY EMBEDDED SYSTEM DESIGN!

## TYPICAL APPLICATIONS

### EMBEDDED PCI MOTHERBOARD




The V96BMC Burst DRAM Controller provides all aspects of DRAM control for high performance systems.

The V96BMC provides the DRAM access protocols, buffer signals, data multiplexer signals, and bus timing resources required to work with the latest technology of DRAMs. By using the V96BMC, system designers can replace expensive FPGAs, and valuable board space with a single, high-performance, easily configured device. The V96BMC provides dedicated Power and Ground rails for the DRAM interface to provide compatibility with 3.3V DRAM modules.

The processor interface of the V96BMC implements the bus protocol of the i960Cx/Hx/Jx. The pin naming convention has been duplicated on the V96BMC. Simply connect like-named pins to create the interface.

The V96BMC supports a total DRAM memory subsystem size of 512Mbytes. The array may be organized as 1 or 2 leaves of 32 bits each. Standard memory sizes of 256Kbit to 64Mbit are supported and 8, 16, and 32-bit accesses are allowed. The V96BMC takes advantage of Fast Page Mode or EDO DRAMs and row comparison logic to achieve static RAM performance using dynamic RAMs.

The V96BMC supplies the control signals needed for external data path buffer components. The use of multi-mode control signals gives the designer flexibility to select buffer components which are optimized for the desired cost and performance. Most standard buffers can be used without additional external logic.

The V96BMC provides an 8-bit bus watch timer to detect and recover from accesses to unpopulated memory regions.

Two 24-bit counters/timers can supply an external interrupt signal at a constant frequency relative to the system clock.

The V96BMC is packaged in a low-cost 132-pin PQFP package and is available in 33 and 40MHz versions.

## ABOUT V3 SEMICONDUCTOR

V3 Semiconductor has been providing embedded systems designers with innovative products since 1987. V3 products are supported throughout North America, Europe, the Middle East and the Far East by a network of distributors and manufacturers' representatives.

*For more information on the V96BMC, or our other i960® and PowerPC™ processors support components, please contact:*

SEMICONDUCTOR
THE EMBEDDED CHIPSET COMPANY

**V3 Semiconductor**
2348G Walsh Ave.
Santa Clara, CA 95051
Phone: (408)988-1050 Fax: (408)988-2601
Toll Free: (800)488-8410 (Canada and US)
www.vcubed.com / or
www.v3semiconductor.com