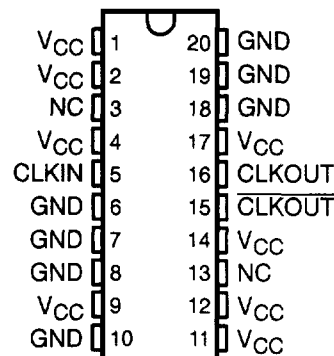


TNETA1530 155.52-MHz CLOCK-GENERATION DEVICE

SDNS016E – FEBRUARY 1994 – REVISED APRIL 1996

- Generates a 155.52-MHz Clock From a 19.44-MHz TTL Clock
- Provides Differential Pseudo-ECL (PECL) Outputs
- Operates From a Single 5-V Power Supply
- Packaged in 20-Pin Plastic Small-Outline (DW) Package

DW PACKAGE
(TOP VIEW)

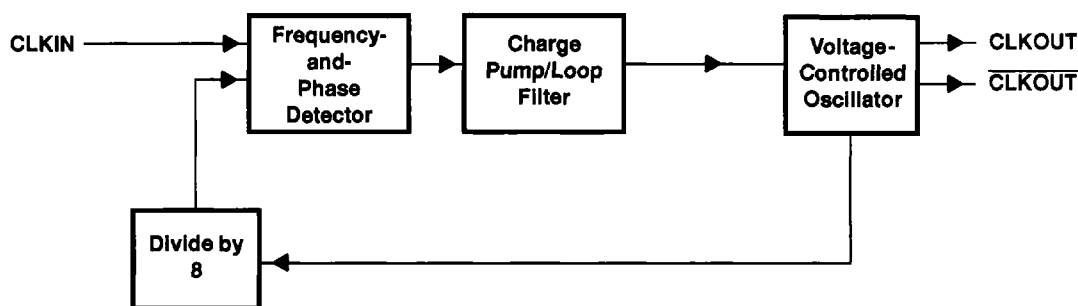


NC – No internal connection

description

The TNETA1530 is a 155.52-MHz clock-generation device that utilizes a TTL-clock input at 19.44 MHz. The 155.52-MHz clock is provided on differential pseudo-ECL (PECL) outputs. The device operates from a single 5-V power supply. An internal second-order low-pass filter is used to reduce jitter.

functional block diagram



Terminal Functions

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLKIN	5	I	19.44-MHz TTL-input clock
CLKOUT	16	O	155.52-MHz PECL-output clock true
$\overline{\text{CLKOUT}}$	15	O	155.52-MHz PECL-output clock complement
GND	6, 7, 8, 10, 18, 19, 20		Ground (0-V reference)
NC	3, 13		No internal connection. Leave floating.
VCC	1, 2, 4, 9, 11, 12, 14, 17		Supply voltage



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS
INSTRUMENTS**

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TNETA1530

155.52-MHz CLOCK-GENERATION DEVICE

SDNS016E – FEBRUARY 1994 – REVISED APRIL 1996

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} (see Note 1)	–0.5 V to 7 V
Input voltage range, V_I	–1.2 V to 7 V
Operating free-air temperature range, T_A	–40°C to 85°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: All voltage values are with respect to the GND terminals.

recommended operating conditions

	MIN	NOM	MAX	UNIT
V_{CC} Supply voltage	4.75	5	5.25	V
V_{IH} High-level input voltage	TTL (see Note 2)			V
V_{IL} Low-level input voltage	TTL (see Note 2)			V
I_{IK} Input clamp current	TTL			–18 mA
T_A Operating free-air temperature	–40		85	°C

NOTE 2: The algebraic convention, in which the least positive (most negative) value is designated minimum, is used in this data sheet for logic-level voltages only.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH} High-level output voltage	$V_{CC} = 5$ V,	See Note 3	$V_{CC} - 0.925$			V
V_{OL} Low-level output voltage	$V_{CC} = 5$ V,	See Note 3	$V_{CC} - 1.650$			V
$V_{O(PP)}$ Output voltage swing, PECL	$V_{CC} = 4.75$ V to 5.25 V,	See Note 3	525			mV
V_{IK} Input clamp voltage	$V_{CC} = 4.75$ V,	$I_L = -18$ mA			–1.2	V
I_I Input current, TTL	$V_{CC} = 5.25$ V,	$V_I = V_{CC}$ or GND			±1	μA
I_{CC} Supply current	$V_{CC} = 5.25$ V, Outputs open	$f = 155.52$ MHz,			50	mA
	$V_{CC} = 5.25$ V, See Note 3	$f = 155.52$ MHz,			75	

NOTE 3: These outputs are terminated with a 50-Ω resistor to $V_{CC} - 2$ V.

operating characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Duty cycle, generated clock	See Note 3	45%	50%	55%	
RMS jitter, generated clock			13	32	ps
Peak-to-peak jitter, generated clock			90	320	ps

NOTE 3: These outputs are terminated with a 50-Ω resistor to $V_{CC} - 2$ V.



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