Features

April 2006

- Time slot interchange function between eight pairs of ST-BUS/GCI/MVIP™ streams (512 channels) and parallel data port
- Programmable data rates on the parallel port (19.44, 16.384, or 6.480 Mbyte/s)
- Programmable data rates on the serial port (2.048 Mbps, 4.096 Mbps or 8.192 Mbps)
- Supports star and point-to-point connections, and unidirectional or bidirectional ring topologies for distributed systems
- Input-to-output bypass function on the parallel data port for use in add/drop applications
- Provides elastic buffer at parallel input port in the receive direction
- Provides byte switching for up to 2430 channels
- Per-channel direction control on the serial port side
- Per-channel message mode and high-impedance control on both parallel and serial port sides
- 8-bit multiplexed microprocessor port compatible with Intel and Motorola microcontrollers
- Guarantees frame integrity when switching nX64 wideband channels such as ISDN H0 channel

Ordering Information

MT90840AL	100 Pin MQFP	Trays
MT90840AP	84 Pin PLCC	Tubes
MT90840AL1	100 Pin MQFP*	Trays
MT90840AP1	84 Pin PLCC*	Tubes
MT90840APR1	84 Pin PLCC*	Tape & Reel

*Pb Free Matte Tin

-40°C to +85°C

- Provides external control lines allowing fast parallel interface to be shared with other devices

Applications

- Bridging ST-BUS/MVIP buses to high speed Time Division Multiplexed backplanes at SONET rates (STS-1, STS-3)
- High speed isochronous backbones for distributed PBX and LAN systems
- Switch platforms of up to 2430 channels with guaranteed frame integrity for wideband channels
- Serial bus control and monitoring
- Data multiplexing
- High speed communications interface

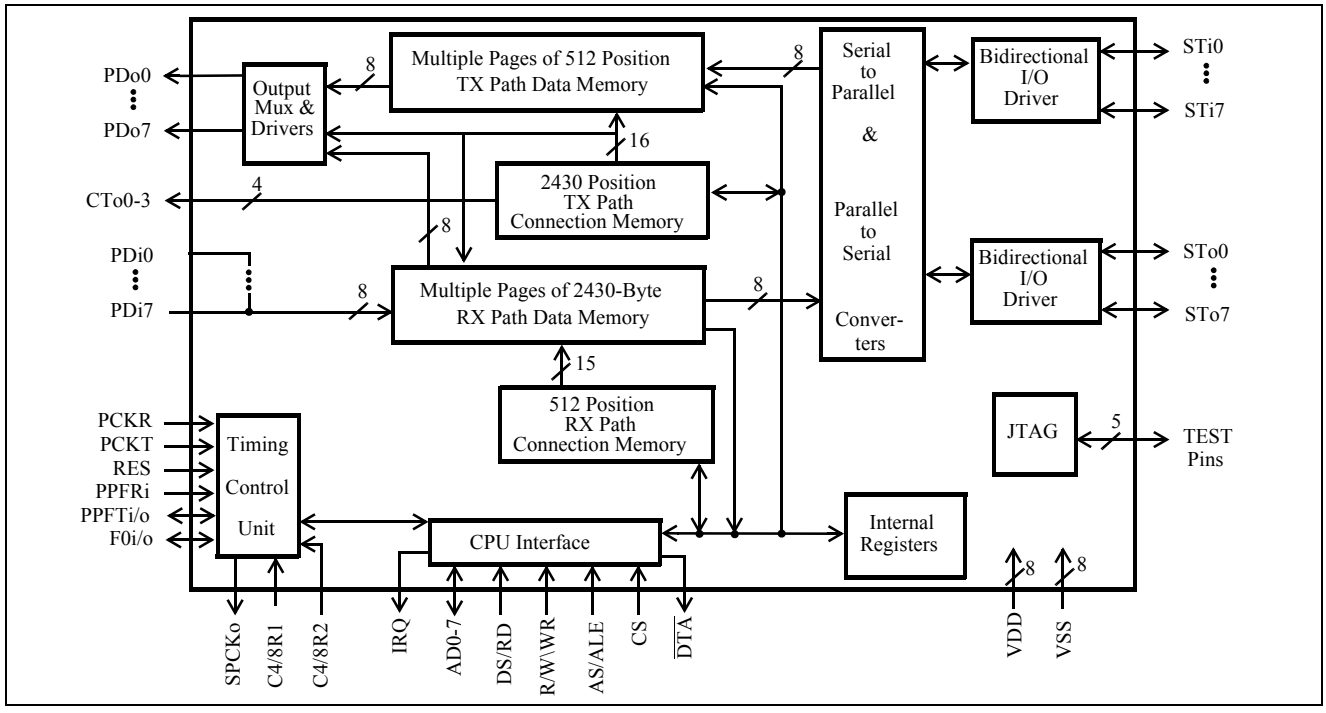


Figure 1 - Functional Block Diagram

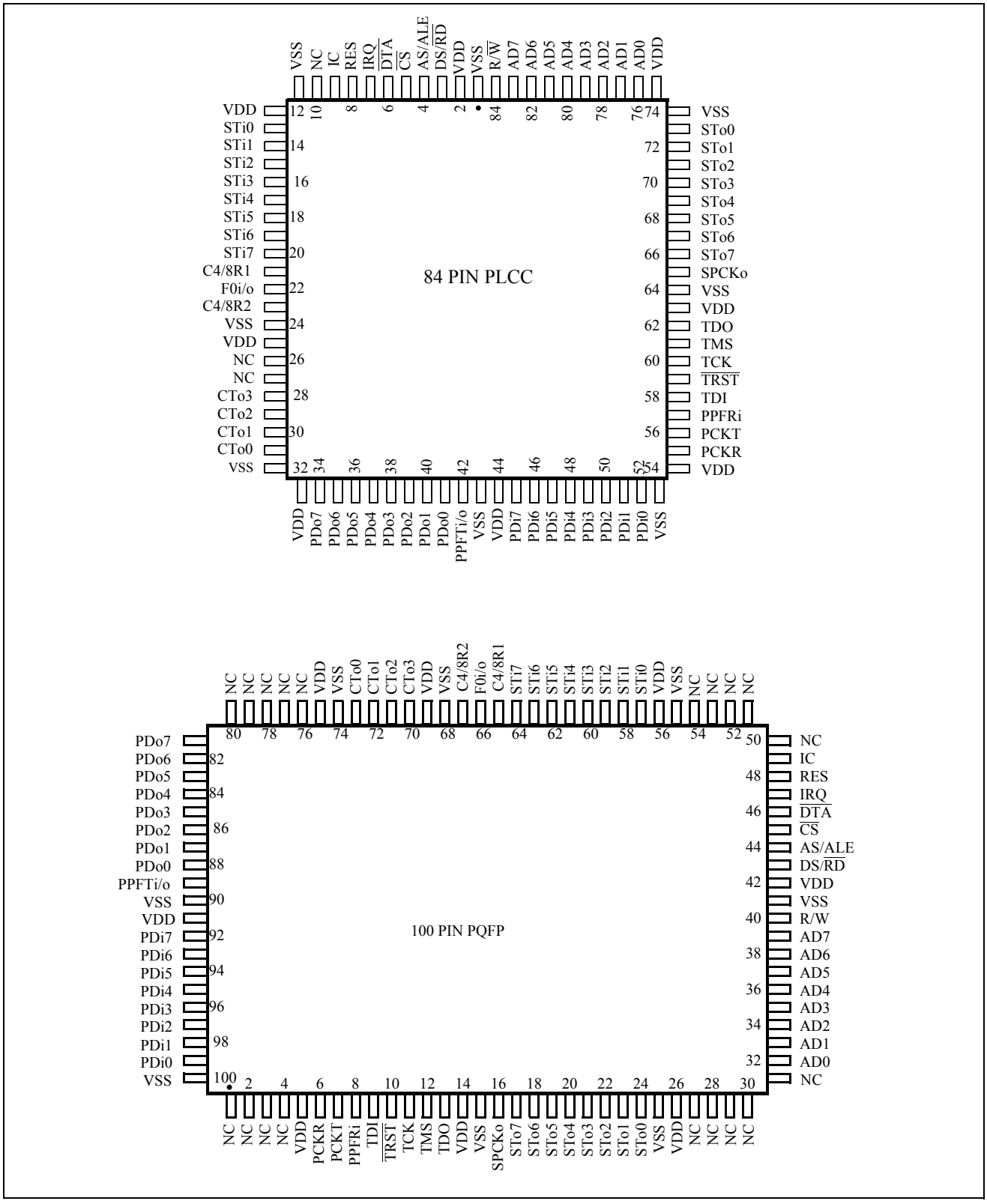


Figure 2 - Pin Connections

Pin Description

Pin #		Name	Description
84	100		
3	43	$\overline{DS}/\overline{RD}$	**Data Strobe/Read (Input**). In Motorola multiplexed-bus mode this pin is DS, an active high input which works with $\overline{CS}$ to enable read and write operation. In Intel/National multiplexed-bus mode this pin is $\overline{RD}$, an active low input which enables a read-cycle and configures the data bus lines (AD0-AD7) as outputs.
4	44	AS/ALE	**Address Strobe / Address Latch Enable (Input**). Falling edge is used to sample address into the Address Latch circuit.
5	45	$\overline{CS}$	**Chip Select (Input)**. Active low input enabling a microprocessor read or write of control or status registers.
6	46	$\overline{DTA}$	**Data Acknowledgment (Active Low Output)**. Indicates that a data bus transfer is complete. When the bus cycle ends, this pin drives HIGH and then tri-states, allowing for faster bus cycles with a weaker pull-up resistor. A pull-up resistor is required to hold a HIGH level when the pin is tri-stated. Note that CPU read/writes from/to the Data and Connection memories occur on the serial or parallel port clock edges, and $\overline{DTA}$ will not change state if the clock is halted.
7	47	IRQ	**Interrupt Request (Active High Output)**. Output indicates that the MT90840 has detected an alarm condition. The indication of the specific condition can be read in the ALS (Alarm Status) Register. The CPU should read ALS, identify the source for the interrupt and then rewrite the mask bits to re-enable the IRQ signal.
8	48	RES	**RESET (Schmitt Input).** Asynchronous device reset. A logic-high signal should be applied during power-up to bring the MT90840 internal circuitry to a defined state. Serial and parallel TDM outputs (STo0-7, STi0-7, and PDo0-7) are held in high-impedance state after reset until programmed otherwise. This input must be held low during normal operation.
9	49	IC	Internal Connection. The user must connect this pin to V_{SS}. This pin must remain low for the MT90840 to function normally, and to comply with IEEE 1149 (JTAG) boundary scan requirements. This pin is pulled low internally when not driven.
10, 26, 27	1-4, 27-31 50-54 76-80	NC	No Connection.
13-20	57-64	STi0-STi7	**Serial Inputs 0 to 7 (Bidirectional)**. Serial TDM data-streams at 2.048, 4.096 or 8.192 Mbps, with 32, 64 or 128 channels respectively per stream. For 2.048 and 4.096 Mbps applications, streams STi0-STi7 can be used, while for 8.192 Mbps, only streams STi0-STi3 are used (512 channel limit). These eight bidirectional lines can be programmed as inputs (default) or outputs on a per-channel basis.

Pin Description (continued)

Pin #		Name	Description
84	100		
21	65	C4/8R1	**Serial Clock Reference Input 1.** When enabled by the C4/8R bit (high) in the TIM Register, this input receives the 4.096 or 8.192 MHz serial port clock reference. If the C4/8R bit is set low, or if the INTCLK bit is set high, this input is ignored by the MT90840. In Timing Mode 1 (TM1), or at 8.192 MHz, the C4/8 input is used directly to shift data in and out of the serial port. In Timing Mode 2 (TM2) at 4.096 MHz, the C4 input from an external clock source (e.g. a PLL locked to an 8 kHz reference) is phase-corrected by the MT90840, and used to generate the serial port SPCKo and F0 outputs. In Timing Modes 3 and 4 (TM3 and TM4) this input is not used. For more details on the use of this signal, see the description of Timing Mode 1 and Timing Mode 2.
22	66	F0i/o	Serial Port Frame Synchronization (Bidirectional). This 8 kHz frame pulse signal indicates the TDM 125 μsec frame boundary on the serial data port. This pin is compatible with both ST-BUS/MVIP and GCI formatted framing signals. In TM1 this pin is an input, and the MT90840 senses the polarity of this frame pulse and automatically adapts the serial data port timing to the applicable format (ST-BUS or GCI). In TM2 with SFDI =1 this signal is an input, and its expected format is determined by the SPFP bit in the GPM Register. In TM2 (with SFDI =0), and in TM3, this signal is an output, generated from the internal timing and synchronized to the SPCKo output clock. The polarity of the F0 pulse is determined by the SPFP bit in the GPM Register. In TM4 this pin is not used.
23	67	C4/8R2	**C4/8R2 Serial Clock Reference Input 2.** When enabled by the C4/8R bit (low) in the TIM Register, this input receives the 4.096 or 8.192 MHz serial port clock reference. If the C4/8R bit is set high, or if the INTCLK bit is set high, this input is ignored by the MT90840. (See pin description for C4/8R1.)
28-31	70-73	CTo3-CTo0	**External Control Lines 3 to 0 (Output).** Output signals generated from the MT90840 Transmit Path Connection Memory (TPCM). The four serial CTo output lines represent the contents of the four CT bits in the TPCM, and are clocked at the parallel port rate (up to 19.44 MHz). See Per-Channel Functions section.
34-41	81-88	PDo7-PDo0	**Parallel Data Output Port 7 to 0 (Output)**. These eight outputs carry the parallel port data bytes in the transmit direction and operate at data rates up to 19.44 Mbyte/s.

Pin Description (continued)

Pin #		Name	Description
84	**100**		
42	89	PPFTi/o	**Parallel Port Framing, Transmit (Bidirectional).** This signal delineates the start of a new data frame at the PDo0-7 lines on the transmit parallel port. Normally an output, when the PFDI bit in the TIM Register is set high PPFT becomes an input, and is used to receive the frame reference from another MT90840. Used in all timing modes except TM3.
45-52	92-99	PDi7-0	**Parallel Data Input Port 7 to 0 (Input)**. These eight inputs carry the parallel port data bytes in the receive direction and operate at data rates up to 19.44 Mbyte/s.
55	6	PCKR	**Parallel Port Clock, Receive (Input).** This is a 19.44, 16.384, or 6.48 MHz clock input. It might typically be provided by a high speed framer. PCKR clocks in data on the receive parallel port (PDi7-0 and PPFRi). In Timing Modes 2, 3, and 4, PCKR clocks both the transmit and receive parallel ports.
56	7	PCKT	**Parallel Port Clock, Transmit (Input**). This is a 19.44, 16.384, or 6.48 MHz clock input. It might typically be provided by a high speed framer. In TM1 PCKT clocks out the data on the transmit parallel port (PDo0-7, CTo0-3, and PPFTo). In TM2, TM3, & TM4, this input is ignored.
57	8	PPFRi	**Parallel Port Framing, Receive (Input)**. This 8 kHz frame pulse input determines the start of a new frame at the PDi0-7 lines of the receive parallel port. It might typically be connected to the frame pulse output of a high speed framer. In TM3, PPFRi is the frame sync reference for both the transmit and receive parallel ports.
58	9	TDI	**Test Data** (**Input**). JTAG serial test instructions and data are shifted in on this pin on rising TCK. This pin is pulled high internally when not driven.
59	10	TRST	**Test Reset** (**Input**). Asynchronously initializes the JTAG TAP controller, placing it in the *Test-Logic-Reset* state. This pin is pulled high internally when not driven. This pin should be pulsed low on power-up, or held low continuously, to ensure that the MT90840 is in the normal functional state, and not the test state.
60	11	TCK	**Test Clock** (**Input**). Provides the clock to the JTAG test logic. This pin is pulled high by an internal pull-up when not driven.
61	12	TMS	**Test Mode Select** (**Input**). JTAG signal that controls the state transitions of the TAP controller, sampled on rising TCK. This pin is pulled high by an internal pull-up when not driven.
62	13	TDO	**Test Data** (**Output**). JTAG serial data is output on this pin on the falling edge of TCK. This pin is held in a high impedance state when JTAG scan is not enabled.
65	16	SPCKo	**Serial Port Clock (Output)** In TM2 and TM3, this is a 4.096 MHz clock output derived from the system 4.096 MHz reference. (As controlled by the C4/8R bit and the INTCLK bit in the TIM Register.) This output is used to shift data in and out of the serial port. In TM1 and TM4, this output is automatically placed in high impedance. For applications with the serial port running at 8.192 Mbps this output is not used, and an 8.192 MHz clock source must be supplied at C4/8R1 or C4/8R2.

Pin Description (continued)

Pin #		Name	Description
84	100		
66-73	17-24	STo7-STo0	**Serial Output Streams 7 to 0 (Bidirectional)**. Serial TDM data-streams at 2.048, 4.096 or 8.192 Mbps, with 32, 64 or 128 channels respectively per stream. For 2.048 and 4.096 Mbps applications, streams STo0-STo7 can be used, while for 8.192 Mbps, only streams STo0-STo3 are used (512 channel limit). These eight bidirectional lines can be programmed as inputs or outputs (default) on a per-channel basis.
76-83	32-39	AD0-AD7	**Multiplexed Address/Data Bus (Bidirectional**). These I/O lines provide an 8-bit interface to a microprocessor for control and monitoring of the MT90840. These pins function as eight input address lines to the Address Latch circuit as well as eight data I/O lines.
84	40	R/$\overline{W}$ \ $\overline{WR}$	**Read/$\overline{\text{Write}}$ \ $\overline{\text{Write}}$ (Input)**. In Motorola multiplexed-bus mode this input is R/$\overline{W}$, which controls the direction of the data bus lines (AD0-AD7) during a microprocessor access. In Intel/National multiplexed-bus mode this input is $\overline{WR}$, an active low signal which configures the data bus lines (AD0-AD7) as inputs during a microprocessor write access.
1,11 24,32, 43,53, 64,74	15,25, 41,55, 68,74, 90,100	V_{SS}	**Ground**.
2, 12, 25,33 44,54, 63,75	5, 14, 26,42 56,69, 75,91	V_{DD}	+5 Volt Power Supply.

Functional Description

The MT90840 Distributed Hyperchannel Switch is a large switching, multiplexing, and rate-adapting device. The MT90840 bridges serial-bus telecom components, using the Zarlink ST-BUS or other industry-standard serial buses, onto a higher speed “backbone”. Mixed data, voice and video signals can be time-interchanged or multiplexed from serial Time Division Multiplexed (TDM) streams onto a high speed parallel bus. The parallel bus can be used for interconnect, or an external framer can be connected to the parallel bus to access serial isochronous backbones operating at up to 155 Mbps SONET rates (STS-3).

The MT90840 Distributed Hyperchannel Switch supports real-time multimedia applications through constant delay switching. Multimedia data at N x 64 kbps rates uses N bytes (“time slots”, or “channels”) per 125 μsec frame. This is also referred to as hyperchannel data. To ensure the integrity of data at N x 64 kbps rates, the network must ensure that the N bytes in a given input frame remain together as a frame, and arrive at the destination as a frame. The MT90840 supports this requirement by providing constant delay (frame integrity) which ensures that the multiple time slots of associated data remain in the intended order.

Total TDM channel capacity of the MT90840 at maximum data rates is:

- 512 serial input time slots,
- 512 serial output time slots,
- 2430 parallel input time slots, and

- • 2430 parallel output time slots.

The number of time slots available is dependent upon the selected data rates, and is reduced at lower data rates.

Figure 1 shows the MT90840 functional block diagram. The figure shows the TDM data paths and the device interfaces.

The MT90840 has three main TDM data paths:

- Transmit Path: serial port input (STi) to parallel port output (PDo),
- Receive Path: parallel port input (PDi) to serial port output (STo),
- Bypass and Parallel-Switching: PDi to PDo.

In addition, Zarlink Message Mode capabilities allow the user to force data on TDM output time slots and to monitor TDM input time slots through the microprocessor port.

The MT90840 has four main interfaces:

- the serial TDM bus interface (STi, STo and timing),
- the parallel TDM bus interface (PDi, PDo and timing) with programmable control outputs (CTo),
- the microprocessor (CPU) interface,
- the test interface (JTAG).

The MT90840 supports four major timing/switching modes:

- TM1/Ring Master: PDo timing slaved to STi/o timing, PDi timing elastic;
- TM2/Ring Slave: PDo and STi/o timing slaved to PDi;
- TM3/Bus Slave: PDo and PDi timing tied together, STi/o timing slaved to parallel bus;
- TM4/Parallel Switching: parallel channel switching from PDi to PDo.

Other features of the MT90840 are programmable for individual TDM channels on the serial and parallel ports (per-channel features):

- Zarlink Message Mode,
- Per-channel output enable,
- Per-channel bypass (parallel bus),
- Programmable CTo control outputs (parallel bus),
- Per-channel direction control (serial bus).

Device Operation

Time Slot Interchange Operation (Switching)

The MT90840 provides access and time slot interchange (switching) functions between the serial and parallel TDM data ports. Switching is provided on three paths: transmit (serial input to parallel output), receive (parallel input to serial output) and bypass/parallel-switching (parallel input to parallel output). Switching functions between serial data streams are not provided.

The MT90840 guarantees wideband or hyper-channel data integrity through the switch by using constant delay switching. This is done by storing a full frame (125 μsec) of data at the input rate and then, under control of the Connection Memory for that path, reading the frame at the output data rate (frame integrity). Therefore the Transmit Path and the Receive Path each have separate Data and Connection Memories.

Switching in a given data path is controlled by programming the Connection Memory for that path. Each output time slot has a control-address in the path's Connection Memory. Each input time slot has an address-value in the path's Data Memory. A given output time slot is controlled by programming the Connection Memory control-address with the address-value of the source input time slot. At the same control-address the output time slot is enabled or tri-stated and other per-channel functions set up. Thus each output time slot is individually controlled, and any given input time slot might be copied to one, several, or none of the output time slots.

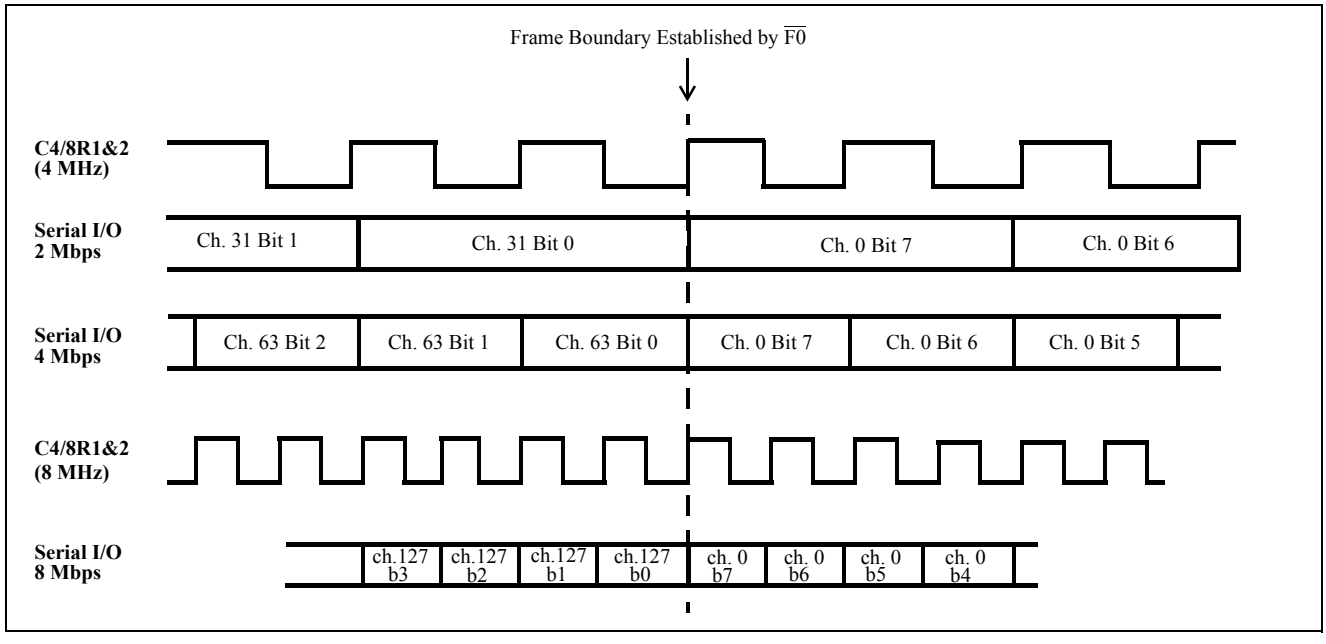


Figure 3 - Serial Port Interface Functional Timing

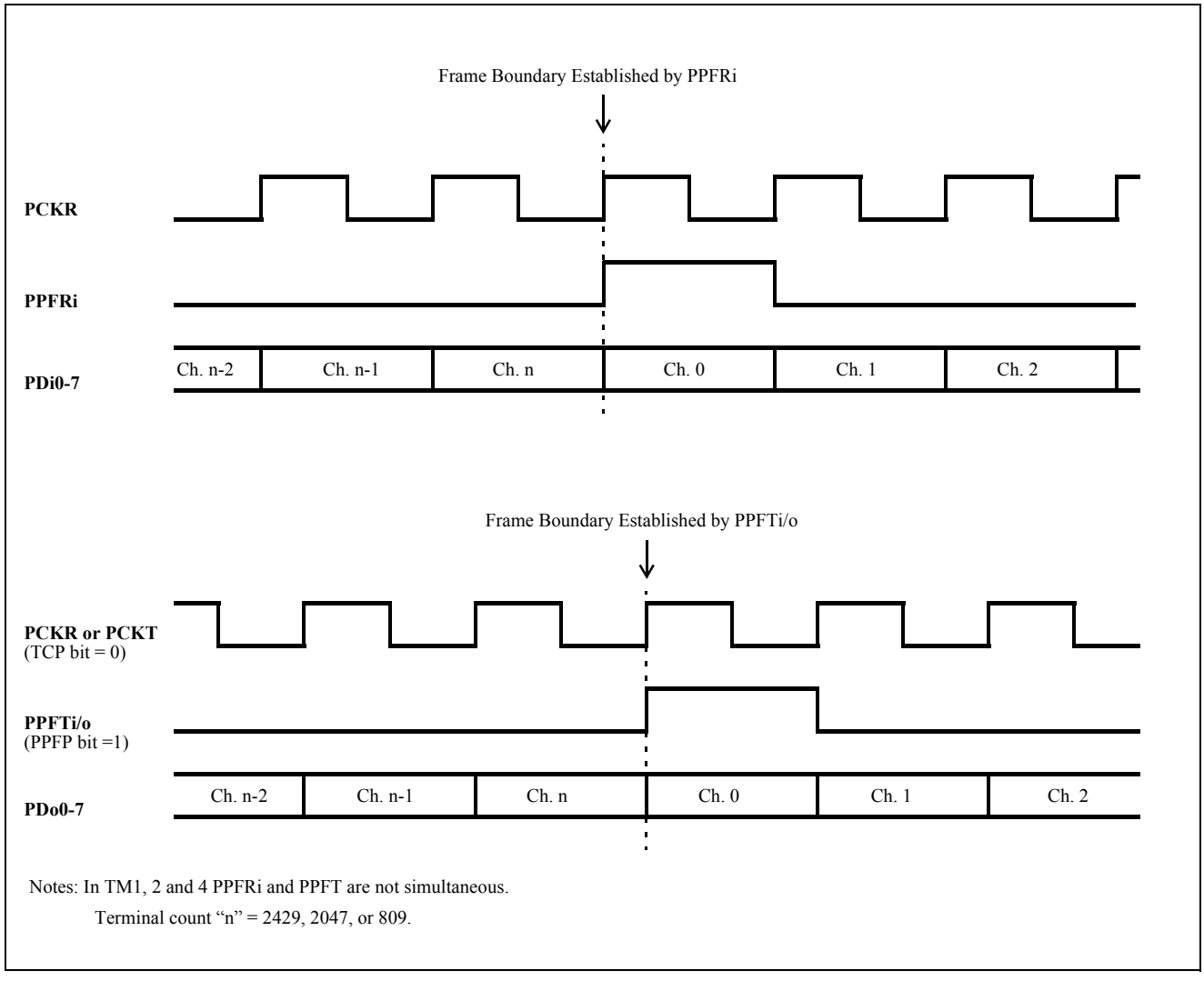


Figure 4 - Parallel Data Port Functional Timing

Transmit Path

The Transmit Path is from the serial inputs, through the Transmit (Tx) Path Data Memory, to the parallel outputs (PDo0-7). This path is controlled by the contents of the Tx Connection Memory. The Tx Connection Memory is programmed, for each output time slot, with the address-value of the source channel to be read out of the Tx Data Memory. Up to 512 channels of serial input can be switched to up to 2430 channels of parallel output.

Transmit Path Connection Memory

The Tx Path Connection Memory is structured as 2430 words of 16 bits. This supports up to 2430 DS0 channels for parallel rates up to 19.44 Mbyte/s (155 Mbps). The Tx Path Connection Memory is accessed as two-sub memories: High and Low. The Connection Memory Low (2430 X 8) is the low byte of the word, and is programmed with the address-value of the serial-input source channel. The Connection Memory High (2430 x 8) is the high byte of the word. Connection Memory High holds the high-order bit(s) of the source address-value, and is also programmed to control per-channel functions such as output driver-enable and programmable control outputs.

Transmit Path Data Memory

The Tx Path Data Memory is structured as 512 words of 8 bits. Serial input time slots are converted to parallel bytes and copied to the Tx Path Data Memory sequentially, serial-stream by serial-stream. The lowest address of the Tx Path Data Memory is STi0-channel0, the next is STi0-channel1, and so on. At 2 Mbps, with 32 channels per STi pin, STi1-channel0 would be 32 addresses higher than STi0-channel0. The Tx Path Data Memory is read out to the parallel outputs by the Tx Connection Memory.

Receive Path

The Receive Path is from the parallel inputs (PDi0-7), through the Receive (Rx) Path Data Memory, to the serial outputs. This path is controlled by the contents of the Rx Path Connection Memory. The Rx Path Connection Memory is programmed, for each output time slot, with the address-value of the source channel to be read out of the Rx Path Data Memory. Up to 2430 channels of parallel input can be switched to up to 512 channels of serial output. Each output byte, whether switched data or message mode data, is read from memory and passed to the parallel-to-serial converters, and then driven out the serial port.

Receive Path Connection Memory

The Rx Path Connection Memory is structured as 512 words of 16 bits. This supports up to 512 DS0 channels. The Rx Path Connection Memory is accessed as two sub-memories: High and Low. The Connection Memory Low (512 x 8) is the low byte of the word, and is programmed with the address-value of the parallel-input source channel. The Connection Memory High (512 x 8) is the high byte of the word. Connection Memory High holds the high-order bits of the source address-value, and is also programmed to control per-channel functions such as output driver-enable and direction-control.

Receive Path Data Memory

The Rx Path Data Memory is structured as 2430 words of 8 bits (1 byte). Parallel input time slots are copied to the Rx Path Data Memory sequentially. The Rx Path Data Memory is read out to the serial port by the Rx Path Connection Memory.

Bypass/Parallel-Switching Path

The Bypass/Parallel Switching path is from parallel input to parallel output. Data received at the parallel inputs (PDi0-7) is copied to the Rx Path Receive Memory, and may be passed to the parallel outputs (PDo0-7) under control of the Tx Path Connection Memory.

Bypass

In ring timing modes (TM1 and TM2) this is a bypass path. When the Bypass bit (PPBY) for a given parallel output channel is set in the Tx Path Connection Memory, the same-address parallel input channel is copied (bypassed) to that parallel output channel. This allows data channels not destined for the local node to be bypassed to the output port and down the ring. “Broadcast” channels destined for every node can also be bypassed, since PPBY is an output control, and it does not affect the availability of the Receive Parallel data for switching to the serial port or monitoring through the CPU interface.

Parallel Switching

In Parallel Switching Mode (TM4) this is a switching path, and the Tx Path Connection Memory is programmed to switch parallel inputs to parallel outputs. For each parallel output channel control-address, the Tx Path Connection Memory is programmed with the 12-bit address-value of the desired parallel input channel.

Serial Data Port

The serial port consists of 16 bidirectional serial data lines (STo0-7, STi0-7), two reference input clock pins (C4/8R1, C4/8R2), one serial clock output (SPCKo) and a bidirectional frame synchronization signal (F0i/o). The STi pins are the default inputs, but the user can program the direction of the pins on a per-channel basis in the Rx Path Connection Memory.

The serial port modes are controlled by the DR bits and the FDC bit in the IMS register, and are:

- 2.048 Mbps Balanced: 8 inputs and 8 outputs per serial time slot (FDC = 0),
- 2.048 Mbps Add/Drop: 16 serial I/O individually programmed per time slot (FDC = 1),
- 4.096 Mbps: 8 inputs and 8 outputs per time slot,
- 8.192 Mbps: 4 inputs and 4 outputs per time slot.

Figure 3 shows the different data rate configurations for the MT90840 serial port.

In addition the user can specify the placement and polarity of the output frame pulse F0o as ST-BUS or GCI compatible, using the SPFP bit in the GPM register. In TM1, the MT90840 automatically detects ST-BUS or GCI serial bus modes, based on the polarity of F0i. The user can also specify which of the two input clock pins - C48R1 or C48R2 - to use as the serial port clock source, using the C4/8R bit in the TIM register.

The user can define the direction of each time slot of the serial port. This per-channel direction control feature is controlled by the DC bit in the Rx Path Connection Memory High. This is ideal for applications in Computer Telephony Integration (CTI) where per-channel direction control is required within telephony servers.

2.048 Mbps Balanced Mode

The 2.048 Mbps Balanced mode has 8 inputs and 8 outputs active during each serial-byte-period or “time slot”. At 2.048 Mbps, each STi/o pin has 32 8-bit channels per 125 μsec frame, with each individual channel at 64 kbps. (1/125μsec X 8 bits = 64 kbps, 32 x 64 kbps = 2.048 Mbps). This mode supports 256 serial input channels and 256 serial output channels. This mode is “balanced” in that there are always 8 inputs and 8 outputs during a time slot. If a specific time slot in an output stream (e.g. STo0-channel7) is programmed in the Rx Path Connection Memory as an input, the corresponding time slot on the equivalent input stream (i.e. STi0-channel7) is automatically an output. The serial clock for this mode is 4.096 MHz.

2.048 Mbps Add/Drop Mode

The 2.048 Mbps Add/Drop mode (FDC bit high) has 16 bidirectional streams active during each time slot. This mode allows up to 512 input channels, or up to 512 output channels, or any mix of channels totalling 512 channels. Per-channel direction control in the Rx Connection Memory specifies the direction of all 512 serial channels from STo0-channel0 up to STi7-channel31.

4.096 Mbps Mode

The 4.096 Mbps mode has 8 inputs and 8 outputs active during each time slot. At 4.096 Mbps each STi/o pin has 64 channels of 64 kbps. This mode supports 512 serial input channels and 512 serial output channels. The serial clock is 4.096 MHz. Per-channel direction control in this mode is the same as the 2.048 Mbps balanced mode.

8.192 Mbps Mode

The 8.192 Mbps mode has 4 inputs and 4 outputs active during each serial byte period. At 8.192 Mbps, each STi/o pin has 128 channels. This mode supports 512 serial input channels and 512 serial output channels. The serial clock for this mode is 8.192 MHz. Per-channel direction control in this mode is the same as the 2.048 Mbps balanced mode.

Serial Port Clock Signals

Depending on the Timing Mode selected, the serial port clock is either an input, or an output derived from a reference clock. In modes where the serial clock is derived by the MT90840 from a reference clock, the serial port clock output appears at SPCKo. The reference clock is either PCKR (if INTCLK is high), or one of C4/8R1 or C4/8R2. The C4/8R bit of the Timing Mode Register is used to select which of C4/8R1 or C4/8R2 will be the clock source or reference pin. Switching between clock sources during device operation will cause temporary TDM data errors.

Internal 4.096 MHz Clock Generator

For TM2 applications running at 19.44 or 16.384 MHz rates on the parallel port, an internal divider can be used to generate a 4.096 MHz clock from the PCKR clock input. The internal divider can not be used in applications where the parallel port operates at 6.480 Mbyte/s rates. The INTCLK bit in the TIM Register enables the internal divider, and the SPCKo output (and internal 4.096 MHz clocks) are driven by the clock divided-down from PCKR. At 16.384 MHz, this is a simple divide-by-4, and the SPCKo output jitter will depend on the PCKR input jitter. At 19.44 MHz, the SPCKo output jitter will be larger as the divider switches between rising and falling edges of PCKR. The serial port timing and F0o frame pulse are tightly slaved to PPFRi when INTCLK is set high.

Serial Frame Pulse

In TM1, the MT90840 receives the frame reference (F0i) from an external source, and the MT90840 senses the polarity of the frame pulse and adapts the device timing to the appropriate (ST-BUS or GCI) format.

In TM2 and TM3, the MT90840 outputs the serial port frame pulse (F0o). Positive (GCI) or negative (ST-BUS) frame pulse formats, and the associated clock polarity, can be selected for the F0o signal by programming the SPFP bit in the GPM Register. This flexibility allows the MT90840 to be employed with different serial bus formats.

In applications which require a large number of serial channels in TM2, it is possible to operate multiple MT90840s in parallel using the SFDI control bit (in the TIM register). To allow the MT90840s to synchronize their internal timing, all of the MT90840s are connected to the same C4/8 reference source, and one MT90840 in normal TM2 (SFDI set low) supplies F0 to one or more MT90840s in TM2 with SFDI set high. With SFDI set high, F0 becomes an input, and this allows the MT90840 driving F0 to control the timing of one or more other MT90840s. If the internal 4.096 MHz clock divider is used (INTCLK high) it is not necessary to use the SFDI control, as the serial port timing and F0o frame pulse of each parallel MT90840 will be tightly slaved to PPFRi when INTCLK is set high.

Should the input framing at F0i cease while the C4/8 clock continues to run, the MT90840 will continue to function as if the frame pulse was asserted after the normal number of clock cycles (free run). If F0i re-commences the MT90840 will immediately sync to F0i, but changes in the F0i interval will temporarily disrupt the TDM data streams. If the F0i input is held asserted, the serial I/O will “lock up” and operation will be disrupted.

Parallel Data Port

The MT90840 parallel port is composed of an 8-bit wide Parallel Data Output Port (PDo0-7), a 4-bit wide Control output port (CTo0-3), an 8-bit wide Parallel Data Input Port (PDi0-7), a Receive Frame sync signal (PPFRi) and a Transmit Frame sync signal (PPFT), and Transmit (PCKT) and Receive (PCKR) Clocks.

The Parallel Port Rates are controlled by the PPS bits in the IMS register, and are:

- 19.44 Mbyte/s (2430 channels),
- 16.384 Mbyte/s (2048 channels), and
- 6.48 Mbyte/s (810 channels).

The user can further specify the features of the parallel TDM port, including:

- the edge of the parallel port clock used to transmit data and PPFTo (see TCP bit in the TIM register),
- the polarity of the Parallel Port Frame Transmit pulse PPFT (see PPFP bit in the GPM register),

- the use of PPFT (normally an output) as an input in TM1, if the application requires multiple MT90840 devices to operate in parallel (see PFDI bit in the TIM register).

The parallel port of the MT90840 is flexible enough to interface to a variety of applications. It can be connected to a framer to access a serial transport backbone running at up to 155 Mbps. It can be connected to a backplane-type parallel bus. It can share a parallel bus with other devices, using the control outputs (CTo0-3) and the per-channel tristate function to share access to the bus.

Parallel Port Clock Signals and Framing

The MT90840's PPFRi (Parallel Port Frame pulse Receive input) and PPFTi/o (Parallel Port Frame pulse Transmit i/o) signals synchronize the MT90840 to the high speed data frame. Receive data is clocked in at the Parallel Data inputs (PDi0-7) by the Parallel port Receive ClocK (PCKR), as framed by Receive Parallel Port Frame input (PPFRi). In TM2, TM3 and TM4, PCKR also clocks the Parallel Data outputs (PDo0-7), with the framing in TM2 and TM4 indicated by the PPFTo output. In TM1, the Parallel Data outputs are clocked out by PCKT, with the framing indicated by PPFTo. Alternatively, the Transmit framing can be controlled by the PPFTi input if the PFDI bit in the TIM register has been set high, to enable multiple MT90840s to operate in parallel in TM1.

Should the input framing at PPFRi cease while the PCKR clock continues to run, the MT90840 will continue to function as if the frame pulse was asserted after the normal number of clock cycles (free run). If PPFRi re-commences, the MT90840 will immediately sync to PPFRi, but any change in the framing interval will temporarily disrupt the TDM data streams, and trigger the PPCE interrupt bit. PPCE will be triggered by PPFRi moving from the expected time, but PPCE will not be triggered by a missing PPFRi. If the PPFRi input is held asserted, the parallel I/O will “lock up” and operation will be disrupted (including CPU access to the TPCM).

The PPFTi framing in TM1 with PFDI=1 operates similarly, using PCKT, but the PPCE interrupt does not monitor PPFTi. Instead, the TXPAA bit indicates that the PPFTi input is out of phase with F0i.

Output Driver Enable Control Capability

The MT90840 provides a bit (ODE) in the IMS Register that places all data outputs of the device (parallel and serial) in a high impedance state. The ODE bit (Output Drive Enable) is automatically set low by the reset input pulse applied to the device during system power up. When low, the ODE bit disables all TDM outputs of the MT90840 while Connection Memory initialization is performed by the CPU. This function is useful to avoid data collision when the MT90840 is sharing a transmit parallel bus with other devices. When ODE is set high, individual parallel and serial port time slots are controlled by the OE bits in TPCM High and RPCM High.

Timing and Switching Control

The MT90840 supports four major timing/switching modes:

- TM1/Ring Master: PDo timing slaved to STi/o timing, Receive Path has elastic buffer enabled;
- TM2/Ring Slave: STi/o timing slaved to PDi timing, fixed delay in Receive Path;
- TM3/Bus Slave: PDo and PDi tied together, STi/o timing slaved to parallel bus timing;
- TM4/Parallel Switching: 2430 (or 2048) channel switching from PDi to PDo.

The TM1-0 bits in the TIM Register are used to select the timing modes. The PFDI and SFDI bits in the same register can be used to enable parallel-device sub-modes of TM1 and TM2 respectively. In all MT90840 timing modes, the throughput delay when performing time interchange functions of grouped channel data is constant, maintaining the frame integrity of the input and output data.

Timing Mode 1 (TM1) - Ring Master

Asynchronous Parallel Port With ST-BUS Clock Master

Timing Mode 1 is used where the main TDM clock reference resides on the serial port side of the system. (An example is a node which is the clock master on a ring network.) Timing on the transmit parallel port is tightly tied to the serial port. The receive parallel port timing is elastic; there is an elastic buffer in the Receive Path and the Bypass Path. See Figure 5a for a connection example.

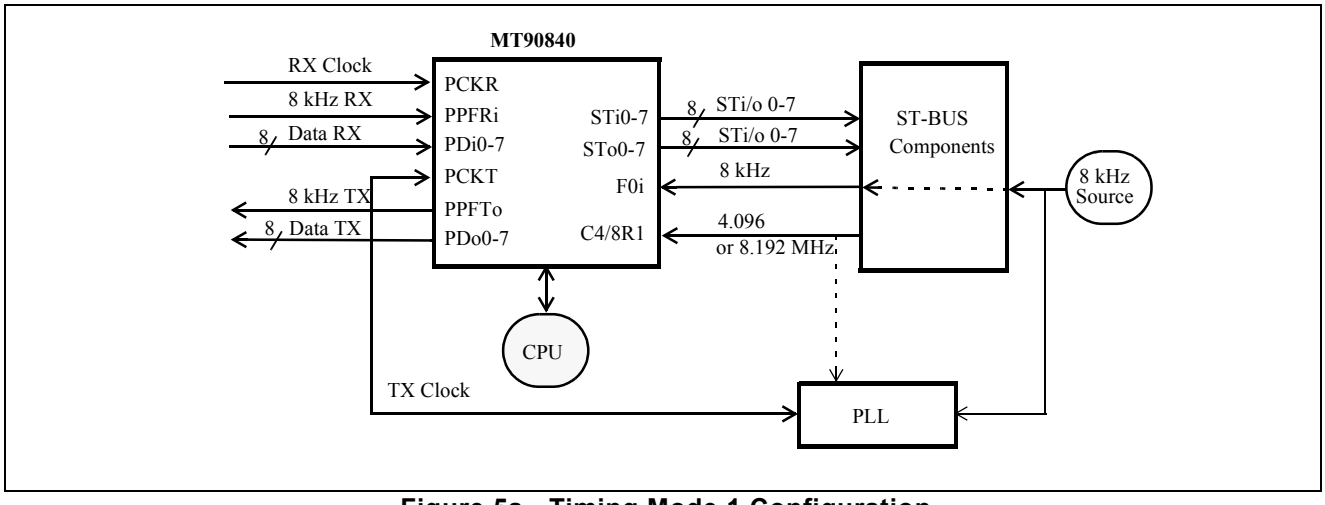


Figure 5a - Timing Mode 1 Configuration

In TM1, the MT90840 receives the serial port frame pulse (F0i) and serial clock (C4/8R1 or C4/8R2). The MT90840 then generates the parallel port output frame pulse (PPFTo) synchronized to F0i. The transmit parallel port is fixed in phase relative to the serial port. (A fixed offset of 3.8 μsec exists between F0i and PPFTo due to serial-to-parallel conversion.) The transmit path does not provide an elastic buffer, and therefore the parallel port TX clock (PCKT) must be tightly locked (in frequency) to the serial port C4/8 and F0i clocks. (Jitter less than +/- 100nsec.)

The receive parallel port timing may be of any phase relative to the serial and transmit-parallel ports in TM1. This allows for flexible round-trip data delays in star or ring type networks. An elastic buffer on the receive parallel port compensates for the difference in phase between PPFRi/PCKR and F0i/C4. The elastic buffer can also tolerate up to 50 μsec +/- 25 μsec) of clock drift and jitter before the buffer re-syncs and Rx Path data is corrupted. (Data corruption is flagged by the FSA interrupt source.) The Bypass Path data (PDi to PDo) also passes through the elastic buffer in TM1.

In TM1, the MT90840's SPCKo clock output is not used.

TM1 Multiple-MT90840 Sub-Mode (PFDI)

For TM1 applications which require more serial channels than are provided by a single MT90840, it is possible to operate multiple MT90840 in parallel. To do this, one MT90840 must control the F0i-to-PPFTo timing (normal TM1), and the remaining MT90840s must synchronize to the first by using PPFTi as an input reference. The device providing the reference will have the PFDI bit in the TIM Register set low (normal TM1). All other MT90840s will have PFDI set high (forcing PPFT to be an input).

Figure 5b shows this mode using two MT90840s; additional MT90840s (with PFDI set high) may be added. This sub-mode allows the serial ports of the multiple MT90840 to share one timing source, and the synchronized parallel output ports to be connected together on one bus.

The TM1 Multiple-MT90840 sub-mode is not available for operation at 6.48 Mbyte/s.

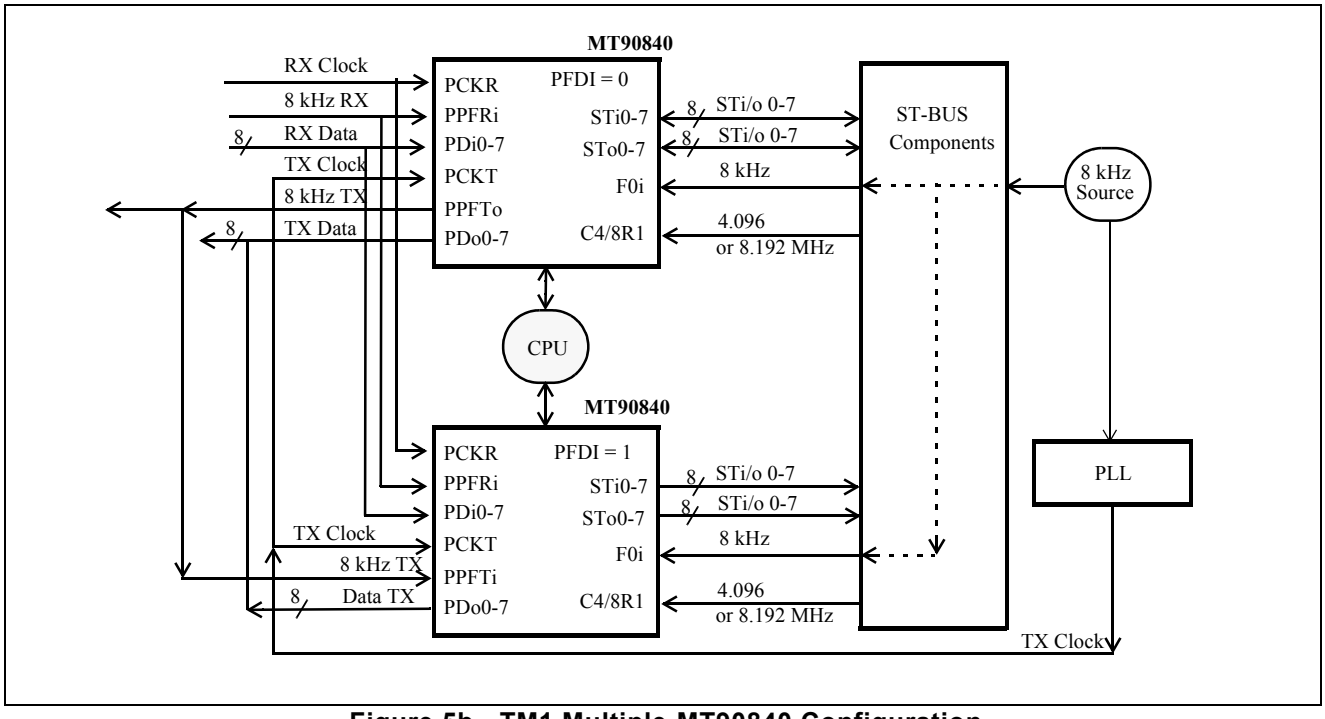


Figure 5b - TM1 Multiple-MT90840 Configuration

Timing Mode 2 (TM2) - Ring Slave

Asynchronous Parallel Port With ST-BUS Clock Slave

Timing Mode 2 is used where the main TDM clock reference resides on the parallel port side of the system. (An example is a node on a ring which is slaved to the ring clock.) Timing on the serial port is tightly tied (slaved) to the receive parallel port, and the transmit parallel port is clocked by the receive parallel port clock. In TM2, the PCKT input is not used. See Figure 6a for a connection example.

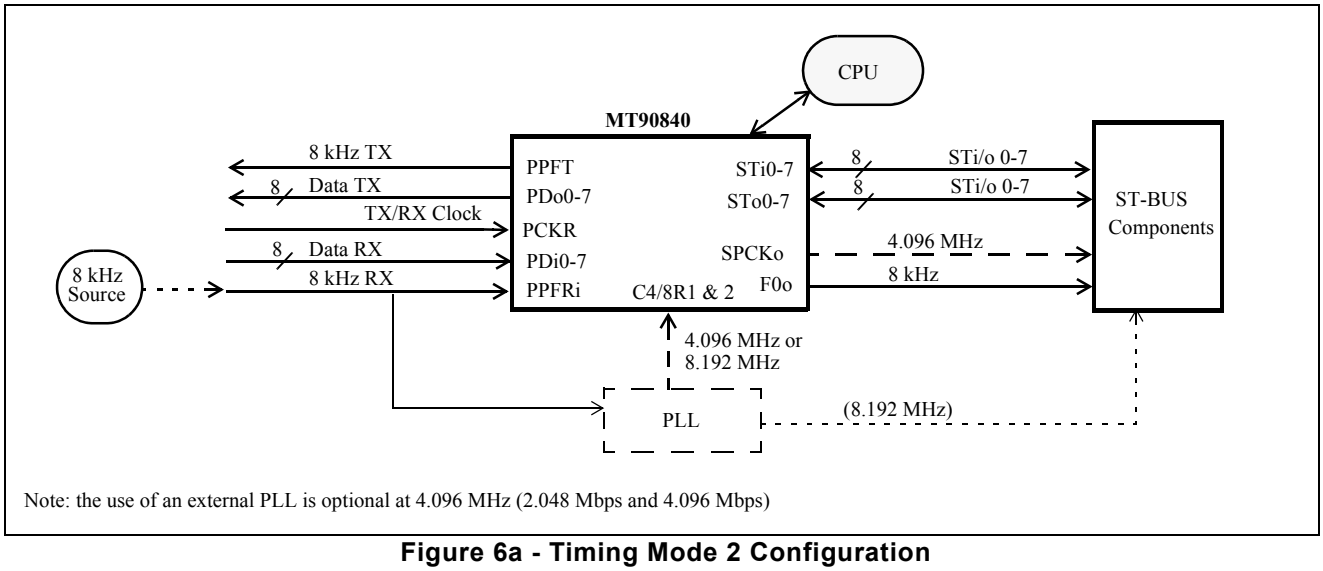


Figure 6a - Timing Mode 2 Configuration

In TM2, the MT90840 timing is controlled by the parallel port frame pulse (PPFRi) and clock (PCKR). The MT90840 generates the parallel port output frame pulse (PPFTo) and the serial port output frame pulse (F0o) locked to PPFRi. Both the transmit parallel port and the serial port are fixed in phase relative to the receive parallel port, and therefore no elastic buffer is required. A fixed offset exists between PPFRi and F0o due to parallel-to-serial conversion, and between F0o and PPFTo due to serial-to-parallel conversion delay. Total offset between PPFRi and PPFRo is about 12 μsec (and the Bypass Path data delay is therefore also about 12 μsec).

The transmit path does not provide an elastic buffer, and therefore the serial port clock must be tightly locked (in frequency) to the parallel port clock (PCKR). (Jitter less than +/- 100nsec.) This may be achieved in one of two ways: use of the internal clock divider (INTCLK set high), or use of an external PLL or DPLL, with C4 phase-correction performed by the MT90840.

Internal 4.096 MHz Clock Divider

For TM2 applications at 19.44 or 16.384 MHz rates on the parallel port, and 4.096 MHz on the serial port, the internal clock divider can be enabled. The clock divider can generate the required serial port clock outputs from the parallel port clock inputs. When enabled in TM2, the clock divider will provide 4.096 MHz (SPCKo) and 8 kHz (F0o) timing to the serial port that is rigidly locked to the PCKR and PPFRi clocks at the parallel port. The clock divider is enabled by setting the INTCLK bit high (in the TIM Register). The clock divider can not be used in applications where the parallel port operates at 6.480 Mbyte/s rates.

External PLL and C4 Phase-Correction

The MT90840 also supports the use of an external PLL (e.g. MT9041/2) to generate 4.096 or 8.192 MHz from the parallel port timing reference. At 4.096 MHz the generated clock must be input to the MT90840 (at C4/8R1 or C4/8R2) for phase monitoring and correction. The phase-corrected 4.096 MHz clock is then output on the SPCKo pin. Should the phase of the C4clock input (relative to the PPFRi framing input) drift more than approximately +/- 100nsec, the MT90840 will apply an additional correction and indicate possible data corruption with the RXPAA interrupt source. At 8.192 MHz, the generated clock is input to the MT90840 (at C4/8R1 or C4/8R2), and is also supplied directly to the serial bus (the SPCKo output is not used at 8.192 MHz). The serial port frame pulse (F0o) will be slaved to the parallel port frame pulse (PPFRi), and will be clocked out by SPCKo, or the 8.192 MHz clock, as appropriate.

TM2 Multiple-MT90840 Sub-Mode (SFDI)

For TM2 applications which require more serial channels than are provided by a single MT90840, it is possible to operate multiple MT90840s in parallel. Multiple-MT90840 operation is automatic if INTCLK is selected, but if an external PLL is used, the serial port timing of the MT90840s must be synchronized. To do this, one MT90840 controls the PPFRi-to-F0o timing and C4 phase-control (normal TM2), and the remaining MT90840s must synchronize to the first by using F0 as an input reference. The device providing the reference will have the SFDI bit in the TIM Register set low (normal TM2). All other MT90840s will have SFDI set high (forcing F0 to be an input).

Figure 6b shows this mode using two MT90840s; additional MT90840s (with SFDI set high) may be added. This sub-mode allows the serial ports of the multiple TM2 MT90840s to share one timing source. The transmit parallel port outputs are always synchronized to PPFRi in TM2, so the multiple MT90840s can also be connected together on one parallel output bus.

The TM2 Multiple-MT90840 sub-mode is not available for operation at 6.48 Mbyte/s.

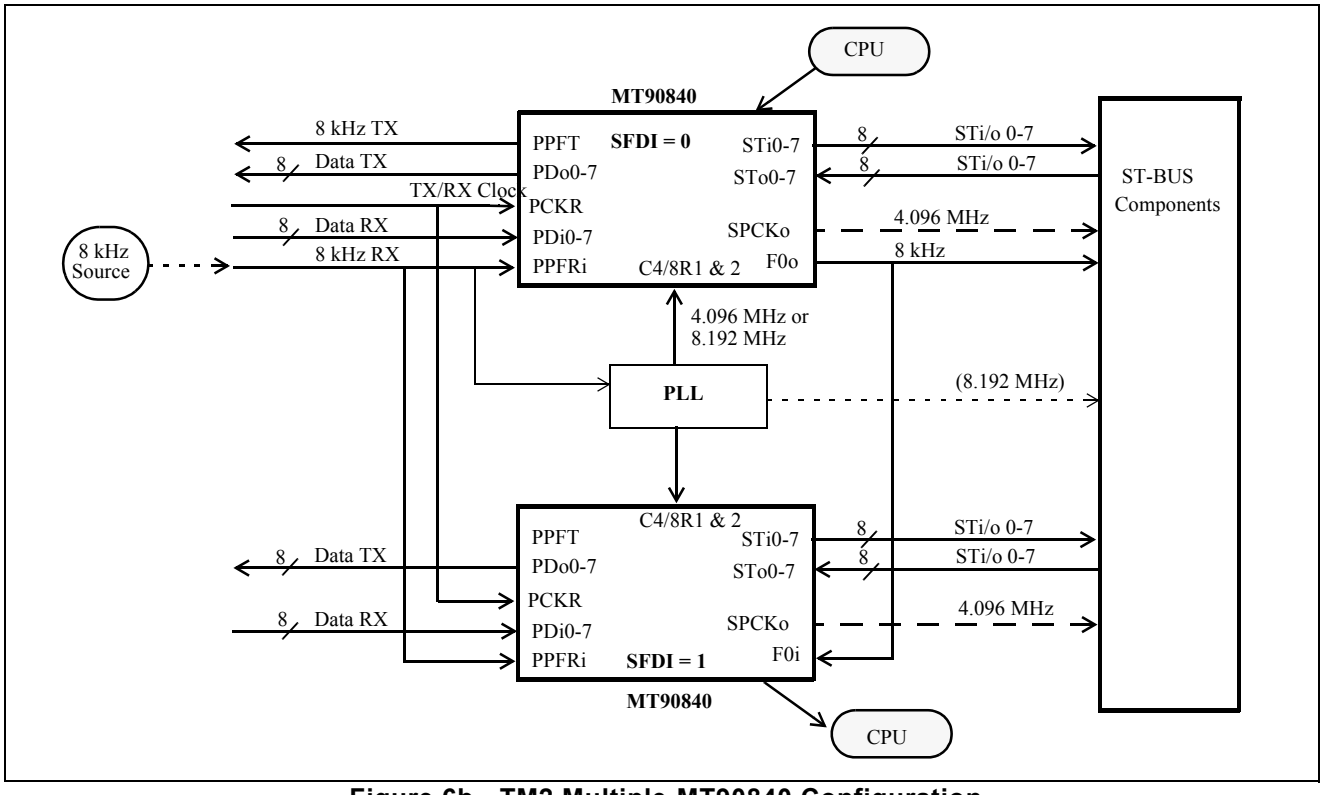


Figure 6b - TM2 Multiple-MT90840 Configuration

Timing Mode 3 (TM3) - Bus Slave

Synchronous Parallel Port With ST-BUS Clock Slave

Timing Mode 3 is used where the main TDM clock reference resides on the parallel port side of the system, and where the receive parallel port and the transmit parallel port are aligned. (An example is a node on a backplane.) Timing on the serial port is tightly tied to the receive parallel port, and the transmit parallel port is clocked by the receive parallel port clock. In TM3, PCKT and PPFTo are not used. See Figure 7 for a connection example.

In TM3, the MT90840 timing is controlled by the parallel port frame pulse (PPFRi) and clock (PCKR). The MT90840 generates the serial port output frame pulse (F0o) locked to PPFRi. TM3 is similar to TM2 with two main differences: the parallel Bypass Path is disabled, and the parallel port receive and transmit buses are synchronized and both aligned with PPFRi. A fixed offset exists between F0o and PPFRi due to serial-to-parallel conversion. The MT90840 will align F0o so that it proceeds PPFRi by 3.8 μsec.

In TM3 the internal clock divider circuit is always enabled, regardless of the state of the INTCLK bit (C4/8R1 and C4/8R2 are unused). Therefore TM3 is limited to 19.44 and 16.384 Mbyte/s parallel port rates, and 2.048 and 4.096 Mbps serial port rates.

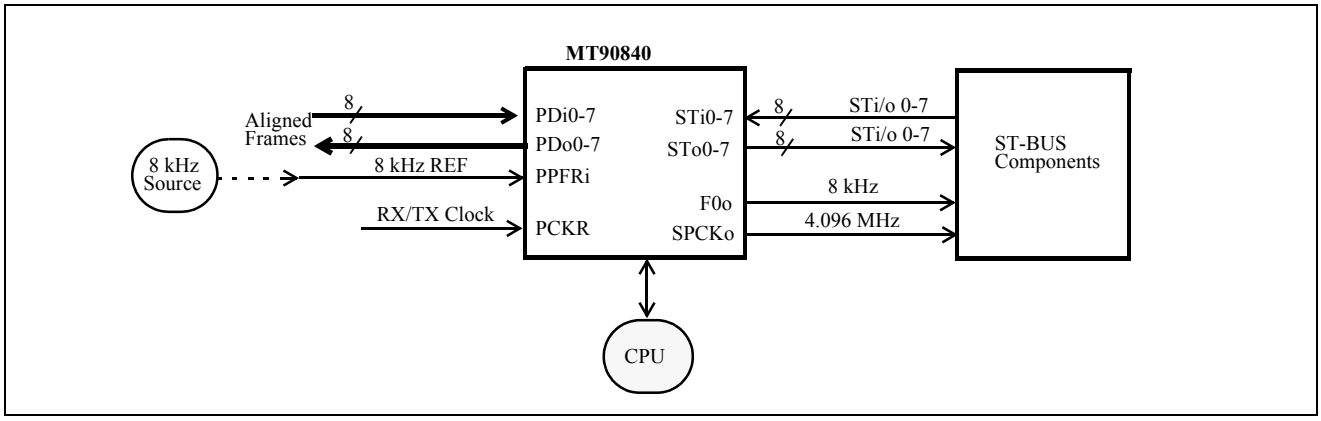


Figure 7 - Timing Mode 3 Configuration

Timing Mode 4 (TM4) - Parallel Data Switching

Timing Mode 4 is used to provide switching of up to 2430 parallel input channels to the same number of parallel output channels. Parallel TDM data is clocked in at PDi0-7 by PCKR, framed by PPFRi. Switching is performed as programmed in the Tx Path Connection Memory, and data is output on PDo0-7, framed by PPFTo and clocked by PCKR. See Figure 8 for connection details.

In TM4, PPFTo and PDo0-7 are offset (delayed) from PPFRi and PDi0-7 by a fixed 4 clock cycles (3.5 clock cycles if the TCP bit is high). All the serial port data and timing signals, and PCKT, are unused in TM4. The internal clock divider is used to generate an internal C4 clock to allow CPU reads from the RPDM. TM4 is only available for 19.44 and 16.384 Mbyte/s rates.

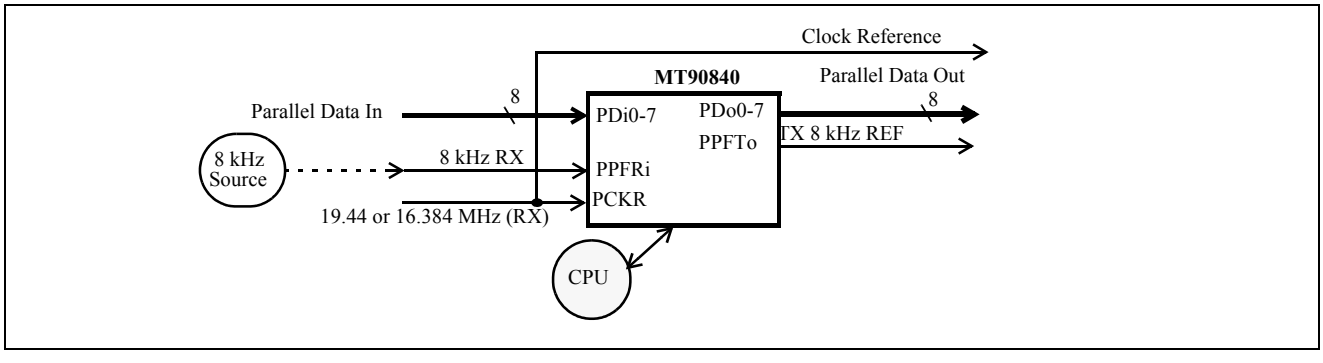


Figure 8 - Timing Mode 4 Configuration

MT90840 Throughput Delay

In many isochronous applications it is important to know and/or limit the delay of data. Table 1 summarizes the data throughput delay values for all timing modes of the MT90840. It is worth noting that the worst-case “round-trip” delays are not as large as the sum of the worst-case delays on the individual links. This is shown by the last 5 rows of Table 1, which give the delays for some representative two MT90840 setups.

MT90840 Per-channel Functions

Several functions of the MT90840 are programmable for each individual parallel channel or serial channel. Per-channel functions on the parallel port side are programmed in the Transmit Path Connection Memory High (TPCM High), and per-channel functions on the serial port interface are programmed in the Receive Path Connection Memory High (RPCM High). On the parallel port these per-channel features are Bypass, Control Outputs, Output

Enable, and Message Mode. On the serial port the per-channel features are Output Enable, Message Mode and Direction Control. These functions are generally available in all of the data rates and timing/switching modes.

Per-channel Bypass on the Parallel Port

This feature, when enabled, causes the specific individual parallel output channel at PDo to transmit the data received at the same number input channel at PDi. This can be used to perform a bypass (on a ring) or a loopback (in a star). This feature is only provided in Timing Modes 1 and 2. In TM2 the data-delay from PDi to PDo is fixed (as is the delay between PPFRi and PPFT). In TM1 the data-delay is elastic (and dependent on the timing of PPFRi and F0i).

The per-channel bypass feature is controlled by the PPBY bits of the TPCM High as explained in the register section. If the PPBY bit is HIGH at a specific TPCM address, the corresponding parallel output will transmit the data received in the corresponding input channel. When the PPBY bit is LOW, the corresponding output channel can be used for message-mode data, or for switched-data from the serial port. A bypass input channel is still copied to the Receive Path Data Memory, and may also be switched to the serial port, or read by the CPU from the Receive Path Data Memory.

The MT90840 per-channel output-enable and message-mode bits have higher priority than the PPBY bit.

Mode	Data Rates	Minimum Delay	Total Throughput Delay
TM1, TM2, or TM3 S/P	All	Dmin = 7.7 µsec Note 1	D = Dmin + 1 frame + Po - Si = 132.7 µsec + Po - Si Min. 7.7 µsec, Avg. 133 µsec, Max. 258 µsec
TM1P/S	All	Dmin = ELDmin = 4.4 µsec Note 2	D = 1 frame + ELD + So - Pi = 125 µsec + ELD + So - Pi Min. 4.4 µsec, Max. 379 µsec
TM2 P/S	All	Dmin = 4.3 µsec Note 1	D = Dmin + 1 frame + So - Pi = 129.3 µsec + So - Pi Min. 4.3 µsec, Avg. 129 µsec, Max. 254 µsec
TM3 P/S	All	Dmin = 1 frame - 7.7 µsec = 117.3 µsec	T = Dmin + 1 frame + So - Pi = 242.3 µsec + So - Pi Min. 117 µsec, Avg. 242 µsec, Max. 367 µsec
TM1 P/P (Bypass)	All	Dmin = 12 µsec + 1 frame = 137 µsec Note 2	D = 7.7 µsec + 1 frame + ELD Min.137 µsec, Max. 262 µsec
TM2 P/P (Bypass)	19.44 Mbyte/s 16.384 Mbyte/s 6.480 Mbyte/s	Note 3	D = {235 or 235.5} PCKR cycles = 12 µsec D = {199 or 199.5} PCKR cycles = 12 µsec D = {80 or 80.5} PCKR cycles = 12 µsec
TM4 P/P (Switching)	19.44 & 16.384 Mbyte/s	Dmin = {3.5 or 4} PCKR cycles (TCP bit = 1 or 0)	D = Dmin + 1 frame + Po - Pi Min. < 0.3 µsec, Avg. 125 µsec, Max. 250 µsec
TM1 S/P + TM2 P/S	All	Dmin = 12 µsec + 1 frame = 137 µsec	D = 12 µs + 2 frames + Transmission + So - Si = 262 µsec + Transmission + So - Si
TM2 S/P + TM1 P/S	All	Dmin = 12 µsec + 1 frame = 137.4 µsec	D = 12 µsec + 2 frames + Transmission + ELD + So - Si = 262 µsec + Transmission + ELD + So - Si

Mode	Data Rates	Minimum Delay	Total Throughput Delay
TM1 S/P + TM2 P/S + TM2 S/P + TM1 P/S	All	Dmin = 4 frames = 500 µsec	D = (2 X 12) µsec + 4 frames + 2 X Transmission + ELD + So - Si = {5 or more integral frames} + So - Si (Note 4)
TM1 S/P + TM2 Bypass + TM1 P/S	All	Dmin = 2 frames = 250 µsec	D = (3 X 12) µsec + 2 frames + 2 X Transmission + ELD + So - Si = {3 or more integral frames} + So - Si (Note 4)
TM3 S/P + TM3 P/S	All	Dmin = 250 µsec	D = (7.7 + 117.3) µsec + 2 frames + So - Si = 375 µsec + So - Si Min. 250 µsec, Avg. 375 µsec, Max. 500 µsec (Note 4)

Table 1 - MT90840 Throughput Delay Summary

Naming rules:
ELD: ELastic Delay, measured from PPFRi to F0i (4.4 to 129.4 µsec).
P/S: Parallel-to-Serial data path.
Pi: Parallel Input channel time, expressed in delay after PPFRi (0 to 125 µsec).
Po: Parallel Output channel time, expressed in delay after PPFTi/o (0 to 125 µsec).
S/P: Serial-to-Parallel data path.
Si: Serial Input channel time, expressed in delay after F0i/o (0 to 125 µsec).
So: Serial Output channel time, expressed in delay after F0i/o (0 to 125 µsec).
Transmission: The delay due to electronic circuits and physical media connecting the parallel ports of two MT90840s. (Assumed to be negligible in TM3.)

Note 1: Exact P/S or S/P delay depends on relative positions of PPFRi and F0 +/- 120 nsec tolerance).
Note 2: Actual TM1 P/S and P/P delay depends on elastic position of PPFRi with respect to F0i (see ELD definition).
Note 3: Bypass delay in TM2: PPFT and PDo ch.0 are co-incident with PDi ch.235 at 19.44 MHz, ch.199 at 16 MHz, and ch.80 at 6.48 MHz. (TCP = 1 delays PDo ch.0 an extra half clock-cycle in TM2).
Note 4: “Round-trip” delay from/to serial ports with the same F0 is always an integral number of frames (plus switching: So - Si).

Per-channel Control Outputs on the Parallel Port

The MT90840 provides four control outputs (CTo0-CTo3) which are synchronized to the parallel port output timing. Each of the CTo output pins is controlled by the CT0-3 bits of the TPCM High. (The CTo0 pin and bit are programmed with the Output Enable data.) The contents of the CTo bit in each TPCM High location is output on the corresponding CTo pin once every frame. See Figure 9. The control outputs can be used to control other devices, such as buffers, to allow sharing of the parallel port data bus.

Per-channel Tri-state (Serial and Parallel)

The MT90840 provides per-channel tri-state of the output pins on both the serial and parallel port. The OE bit in each address of the TPCM and RPCM determines if data will be driven during a particular time slot, or if the pin will be placed in a high-impedance state during that time slot. The OE bit overrides all other per-channel control bits.

Per-channel Message Mode (Serial and Parallel)

The MT90840 provides per-channel message mode capability on both the serial and parallel port. The MC bit in each address of the TPCM and RPCM determines if the Connection Memory Low byte is to be used as an address, or as data to be output on the particular channel (message mode). When the MC bit is HIGH, the Connection Memory Low byte is used as message data. As well as driving message data on the serial (RPCM) and parallel (TPCM) ports, the MT90840 allows the CPU to read serial or parallel data channels from the TPDM or RPDM. Applications for message mode include digital silence, proprietary signalling, and creating fixed 8 kHz framing patterns.

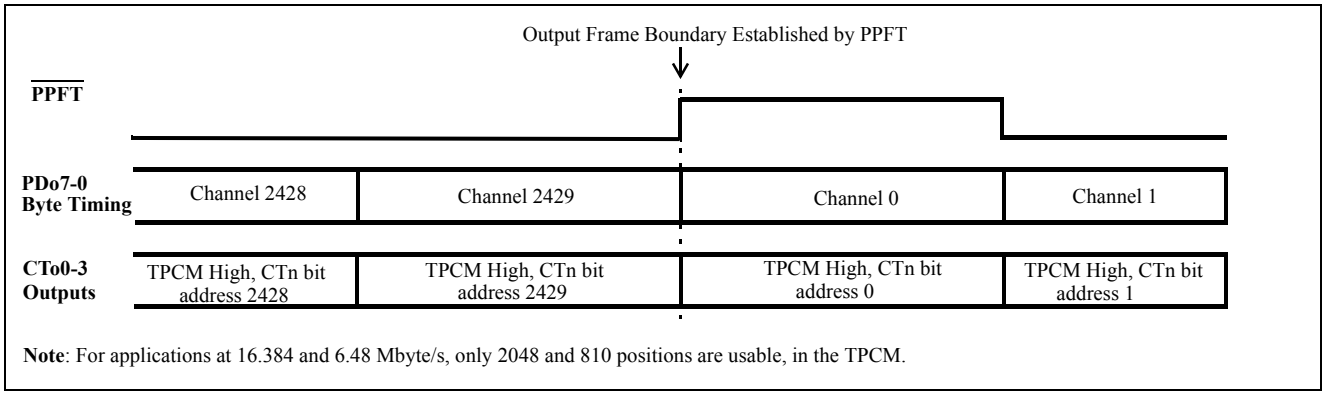


Figure 9 - Parallel Port Control Outputs, CTo0-3

Per-channel Direction Control on the Serial Port

The MT90840 provides the ability to use any nominal output serial channel as an input or as an output. The direction of each output serial channel is controlled by the DC bit in the appropriate byte of the Receive Path Connection Memory High (RPCM High). When DC is HIGH the matching channel is an output. The per-channel direction control feature of the MT90840 can be activated in one two modes: balanced, or add/drop operation.

- Balanced Operation (all serial data rates)

This mode is enabled when the FDC bit in the IMS Register is LOW. In this mode, each of the DC bits controls two serial channels: the nominal output and the nominal input. If a channel on a nominal output serial stream (STo0-7) is re-defined as an input, the same-number channel on the matching input stream (STi0-7) will be defined as an output. For example, if channel 0 on STo7 is programmed as an input (DC=0), then channel 0 on STi7 is defined as an output. Each DC-bit's state controls the direction of a channel on the nominal output stream (DC is HIGH for output), and inverse-sense controls a channel on the nominal input stream (DC is LOW for output). This is shown in Figure 10.

- Add/Drop Operation (2.048 Mbps only)

This mode is enabled when the FDC bit in the IMS Register is HIGH. In Add/Drop mode all channels on all 16 serial streams can be individually controlled, so that up to 512 channels can be either transmitted or received. As an example, if all DC bit locations of RPCM High are set HIGH, all 512 channels on STo0-7 and STi0-7 will be configured as outputs. If all DC bits are LOW, then all 512 channels will be configured as inputs. In Add/Drop mode all 512 serial channels are copied into the Transmit Path Data Memory, as inputs, regardless of the DC or OE bits. This has the effect of a "copy-back" of all serial outputs.

For more details on per-channel control functions for the serial and parallel data ports, see the TPCM High and RPCM High bits definition in the Register Description section.

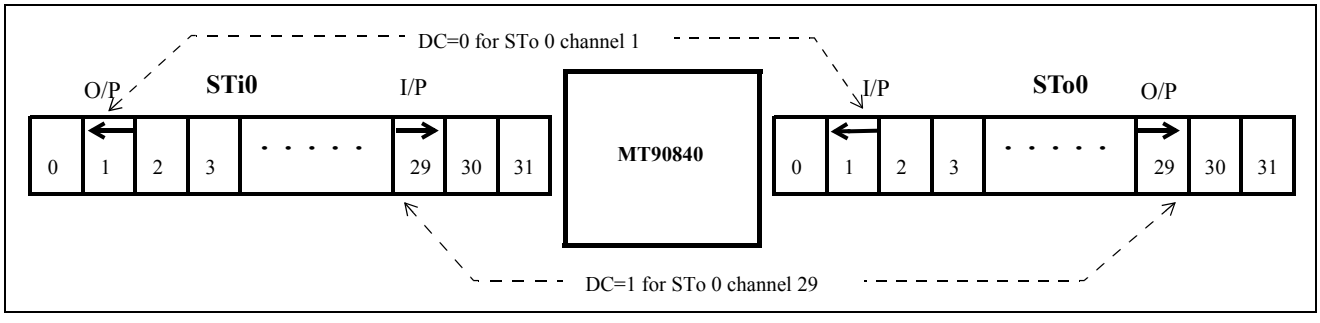


Figure 10 - Balanced Per-Channel Serial Direction Control as Determined by DC Bit

Serial Data Memory Addressing

The serial port mode determines the number of channels per stream, the number of streams, and the direction-control operation. Therefore the way in which serial data is addressed in the internal memory space must change with the serial port mode. Because of this, it is necessary to select the serial port mode (with DR1-0 and FDC in the IMS register) before programming the Receive Path Connection Memory.

2.048 Mbps Balanced Mode

The 2.048 Mbps Balanced mode has 8 serial input and 8 serial output streams, and 32 channels per stream. Therefore 3 bits are used to address the 8 streams, and 5 bits are used to address the 32 channels. Figure 11a shows how the Transmit Path Data Memory is read in this mode, by the CPU, or by the Transmit Path Connection Memory. Each of the 256 input channels is mapped to an address in the TPDM. CPU reads require the LSB (Least Significant Bit) of the CAR Register, and the 7 LSBs of the address bus. The source-channel address-value written in the TPCM requires 8 bits.

Figure 11b shows how the Receive Path Connection Memory is addressed by the CPU. Each of the 256 output channels has a control-address in the RPCM. CPU accesses require the LSB of the CAR Register, and the 7 LSBs of the address bus. When the DC bit for a specific output channel is LOW, that channel is output on the STi pin rather than the STo pin, and the data at the STo pin is input to the TPDM. When the DC bit is HIGH, the output channel appears at the normal STo pin.

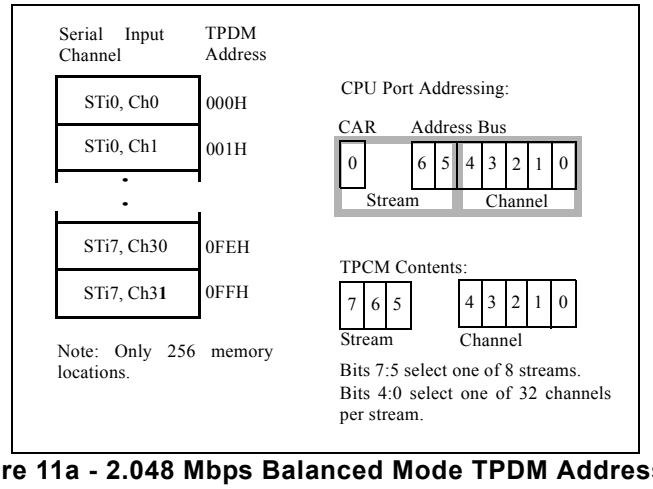


Figure 11a - 2.048 Mbps Balanced Mode TPDM Addressing

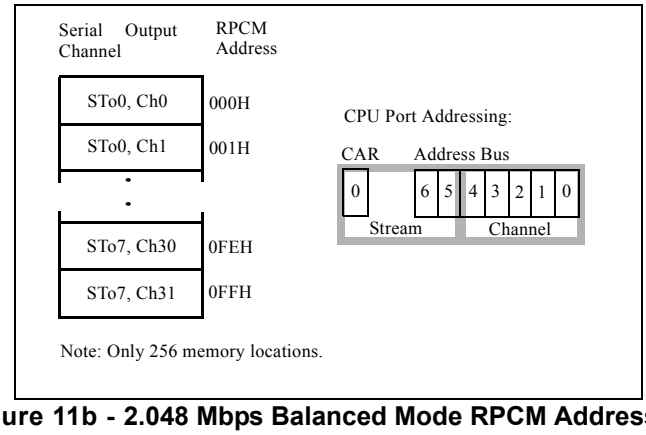


Figure 11b - 2.048 Mbps Balanced Mode RPCM Addressing

2.048 Mbps Add/Drop Mode

The 2.048 Mbps Add/Drop mode has 16 serial input/output streams, and 32 channels per stream. Therefore 4 bits are used to address the 16 streams, and 5 bits are used to address the 32 channels. Figure 12a shows how the Transmit Path Data Memory is read in this mode. Each of the 512 possible input channels is mapped to an address in the TPDM. CPU reads require the 2 LSBs of the CAR Register, and the 7 LSBs of the address bus. The source-channel address-value written in the TPCM requires 9 bits. In this mode the TPDM reads all 512 serial channels as inputs. When a specific channel is driven by the MT90840 as an output, the output data is also copied back into the TPDM.

Figure 12b shows how the Receive Path Connection Memory is addressed by the CPU in 2.048 Mbps Add/Drop mode. Each of the 512 possible output channels has a control-address in the RPCM. CPU accesses require the 2 LSBs of the CAR Register, and the 7 LSBs of the address bus. When the DC bit or the OE bit at a specific control-address is LOW, no data is driven out for that channel, and the input data at the pin is written to the TPDM.

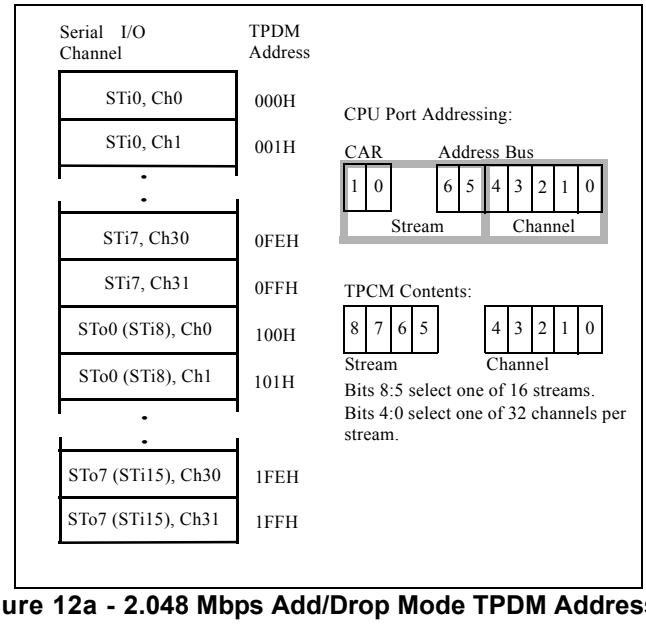


Figure 12a - 2.048 Mbps Add/Drop Mode TPDM Addressing

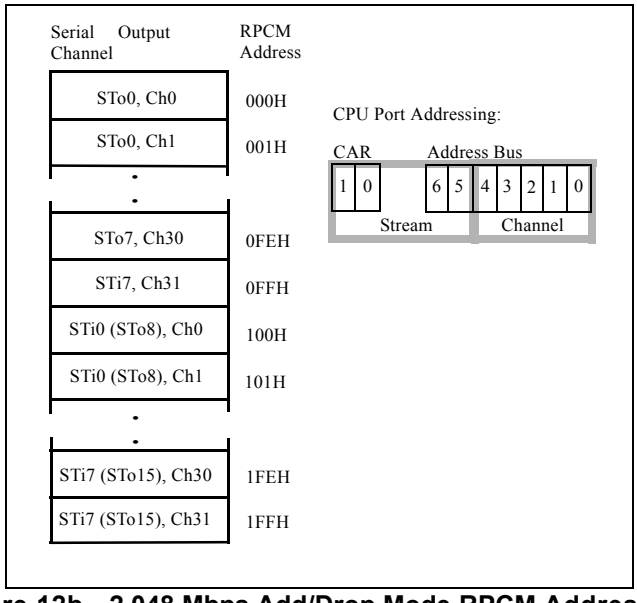


Figure 12b - 2.048 Mbps Add/Drop Mode RPCM Addressing

4.096 Mbps Mode

The 4.096 Mbps mode has 8 input and 8 output streams, and 64 channels per stream. Therefore 3 bits are used to address the 8 streams, and 6 bits are used to address the 64 channels. Figure 13a shows how the Transmit Path Data Memory is read in this mode. Each of the 512 input channels is mapped to an address in the TPDM. CPU reads require the 2 LSBs of the CAR Register, and the 7 LSBs of the address bus. The source-channel address-value written in the TPCM requires 9 bits.

Figure 13b shows how the Receive Path Connection Memory is addressed by the CPU in 4.096 Mbps mode. Each of the 512 output channels has a control-address in the RPCM. CPU accesses require the 2 LSBs of the CAR Register, and the 7 LSBs of the address bus. Per-channel direction control in this mode is the same as the 2.048 Mbps Balanced mode.

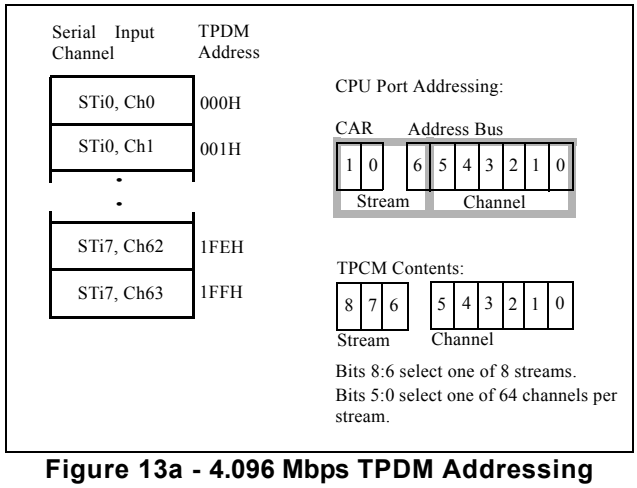


Figure 13a - 4.096 Mbps TPDM Addressing

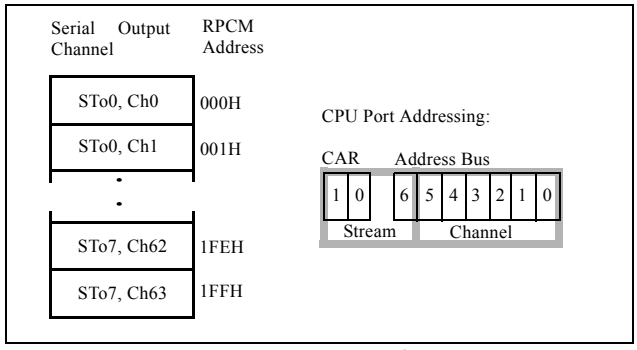


Figure 13b - 4.096 Mbps RPCM Addressing

8.192 Mbps Mode

The 8.192 Mbps mode has 4 input and 4 output streams, and 128 channels per stream. Therefore 2 bits are used to address the 4 streams, and 7 bits are used to address the 128 channels. Figure 14a shows how the Transmit Path Data Memory is read in this mode. Each of the 512 input channels is mapped to an address in the TPDM. CPU reads require the 2 LSBs of the CAR Register, and the 7 LSBs of the address bus. The source-channel address-value written in the TPCM requires 9 bits.

Figure 14b shows how the Receive Path Connection Memory is addressed by the CPU in 8.192 Mbps mode. Each of the 512 output channels has a control-address in the RPCM. CPU accesses require the 2 LSBs of the CAR Register, and the 7 LSBs of the address bus. Per-channel direction control in this mode is the same as the 2.048 Mbps Balanced mode.

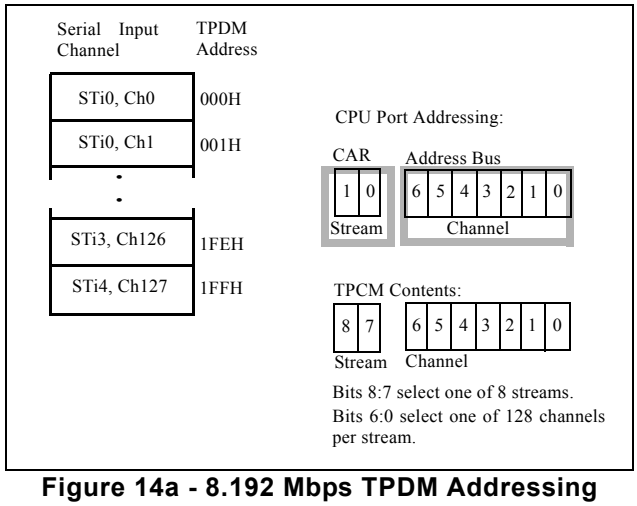


Figure 14a - 8.192 Mbps TPDM Addressing

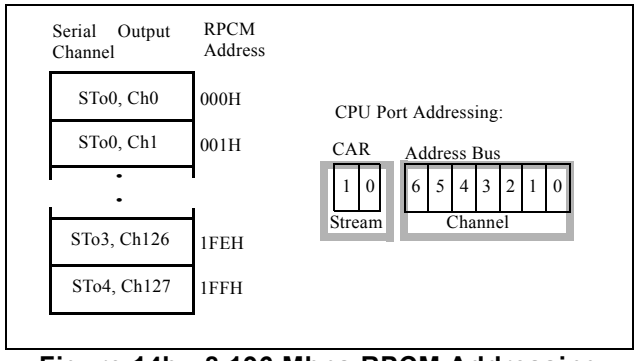


Figure 14b - 8.196 Mbps RPCM Addressing

Microprocessor Port

An 8-bit multiplexed parallel microprocessor port is provided on the MT90840 to allow an attached CPU to configure and read internal registers and memories. The MT90840 CPU interface is compatible with Motorola, National and Intel Multiplexed Bus CPUs and adapts itself to the appropriate bus-type control signal timing without any mode selection.

The MT90840 CPU interface signals are AD0-7 (Data and Address), ALE/AS, DS/$\overline{RD}$, R/$\overline{W\backslash WR}$, $\overline{CS}$ and $\overline{DTA}$. The parallel microprocessor interface provides the CPU with access to the internal configuration registers, and the Connection and Data Memories for both the transmit and receive paths. Connection memories are read/write, Data Memories are read only, and the control register senses are shown in Table 2.

Accesses from the microport to the Connection and Data Memories are multiplexed with accesses from the input and output TDM ports. This can cause variable data acknowledge delays which are communicated to the CPU by the $\overline{DTA}$ output signal. Note that if the parallel port clocks PCKR & PCKT or serial port clocks C4/8R1 & C4/8R2 are not present during an internal memory access, the $\overline{DTA}$ output signal may be held HIGH until the clocks are applied again.

For complete details on the Microprocessor Interface timing signals, refer to the AC Electrical Characteristics section.

Address Mapping of the Internal Registers

The MT90840 provides internal registers which are used by the CPU to configure the device in the various operation modes. The IMS, TIM, GPM and ALS Registers should be initialized by the CPU on every system power-up before any internal memory access is performed. In the MT90840, the AD7 address pin must be kept LOW when addressing the internal registers, as depicted in Table 2.

When input address pin AD7 is HIGH, input address pins AD0-AD6 are used together with bits HA7-HA11 in the Control Register to form a 12-bit address to access the MT90840 internal memory selected by the SEL2-SEL0 bits. See Internal Memory Description for memory address mapping.

IRQ Interrupt Pin

The MT90840 provides the output pin IRQ (Interrupt Request) which is active HIGH and indicates the occurrence of one or more error conditions in the MT90840 timing operations. The occurrences are indicated by bits PPCE, RXPAA, TXPAA and FSA in the ALS Register.

Except for cases where the indications are masked by the MSK3-0 bits in the ALS Register, the occurrence of any indication causes an IRQ interrupt to be generated to the CPU. When an interrupt is masked by MSK3-0 bits, the IRQ output will not be activated. However, the interrupt indication will still be provided in the ALS bits.

To cause the IRQ output signal or the indication bits to return to LOW again, the CPU can write any value to the ALS Register (normally the Mask bits are re-written to clear the IRQ pin).

A7	A3	A2	A1	A0	#	Type	LOCATION	Reset Value (Hex)
0	0	0	0	0	0	R/W	IMS Register	60
0	0	0	0	1	1	R/W	Control Register	00
0	0	0	1	0	2	R/W	TIM Register	00
0	0	0	1	1	3	R/W	GPM Register	00
0	0	1	0	0	4	R/W	ALS Register	0X
0	0	1	0	1	5	R/W	Test (leave 00hx)	00
0	0	1	1	0	6	-	reserved	
0	0	1	1	1	7	-	reserved	
0	1	0	0	0	8	RO	Phase Status (Low byte)	XX
0	1	0	0	1	9	RO	Phase Status (High 3 bits)	0X
0	1	0	1	0	10	-	reserved	

Table 2 - MT90840 Register Address Mapping

$\overline{\text{DTA}}$ Data Transfer Acknowledgment Pin

The $\overline{\text{DTA}}$ pin is driven LOW by internal logic, to indicate to the CPU that a data bus transfer is complete. When the bus cycle ends, this pin drives HIGH and then switches to high-impedance. If a short, or a signal contention, prevents the $\overline{\text{DTA}}$ pin from reaching a valid logic HIGH, it will continue to drive for approximately 15 nsec before switching to high-impedance.

Accessing Internal Memories

The Data and Connection memories of the MT90840 are connected to the various TDM data ports, and synchronized to the TDM clocks (PCKR, PCKT, and C4/8R1 or C4/8R2). Therefore all CPU accesses to the Data and Connection memories are synchronized to, and dependent upon, the TDM clocks. The TDM clocks supplied to the MT90840 must meet the requirements given in the AC Electrical Characteristics section for reliable operation of both the data switch and the CPU port. Faulty clocks can result in data corruption at the TDM ports, or on CPU accesses.

If there is no PCKR clock (PCKT in TM1), the CPU cannot access the Transmit Path Connection Memory. If there is no C4/8 clock, the CPU cannot access the Transmit Path Data Memory, Receive Path Data Memory, or Receive Path Connection Memory. If the PPFRi or F0 frame pulse is absent, but the other clocks are present, the MT90840 will free-run and allow normal CPU access. (In TM2 with the INTCLK bit asserted, or in TM3 or TM4, all clocks and all CPU memory accesses are tied to the PCKR clock.)

CPU Memory Read Operation

To perform a read, the Control Register must first be written to specify the memory and page to be read. Then the CPU can read the specified memory and page by latching an address into the MT90840, with address pin AD7 HIGH to indicate a memory access. When chip-select and read signals are asserted, data is transferred to the CPU port on the next free TDM clock edge, and then the $\overline{\text{DTA}}$ pin is asserted to indicate that the CPU port data pins hold valid read- data. Numerous reads within the same memory page can be performed without having to re-write the Control Register. CPU reads of the Data and Connection memories must be multiplexed with the TDM port accesses, resulting in the varying $\overline{\text{DTA}}$ response times given in the AC Electrical Characteristics section.

CPU Memory Write Operation (Write Pipeline)

CPU write access to the Connection Memories (TPCM and RPCM) must also be multiplexed with the TDM port accesses. To allow faster CPU write operations, the MT90840 has a transparent single-byte write pipeline. CPU write accesses are performed in the same manner as reads, with the Control Register programmed to specify the memory and page. The $\overline{DTA}$ pin is asserted by the MT90840 to indicate that the CPU data has been latched into the device. An isolated write operation will receive a register-speed $\overline{DTA}$, as the data is latched into the transparent write pipeline to await the next free TDM clock edge. A second write will not receive a $\overline{DTA}$ acknowledgment until the first write has exited the internal write pipeline. The $\overline{DTA}$ response time on the second write is a function of the memory chosen for the write currently in the pipeline, and is given in the AC Electrical Characteristics section.

$\overline{DTA}$ Operation and TDM Clocks

If the CPU tries to read a memory for which the necessary TDM clock is not present, the $\overline{DTA}$ pin will not be asserted. If the CPU tries to write a memory for which the necessary TDM clock is not present, the $\overline{DTA}$ pin will be asserted (as the data is stored in the write-pipeline) but the next CPU access will not see $\overline{DTA}$ asserted. No clocks are necessary for register accesses (but if the write-pipeline is hung, the registers cannot be accessed). If the MT90840 is hung due to a CPU read of a memory with a missing clock, the hang can be cleared by ending the read access. If the MT90840 is hung due to a CPU write to a memory with a missing clock, the hang can be cleared by applying a hardware RESET to the MT90840.

Detecting Clock Presence

After it is set, the BPE bit is cleared within 2 frames of the C4/8 clock (i.e. within 250 μsec). If this bit is cleared by the MT90840, the CPU can deduce that the C4/8 clock is present. In TM3, in TM4, and in TM2 with INTCLK asserted, C4/8 is internally generated from PCKR, and if the BPE bit is cleared by the MT90840, the CPU can deduce that the PCKR clock is present.

Clock Quality and TM1 TPCM Access Integrity

In Timing Mode 1 the parallel transmit frame pulse PPFTo must be held in phase with the serial bus frame pulse input (F0i). This is performed automatically by the MT90840 with an internal correction event, which moves the PPFTo output. In normal TM1 operation the correction happens once on initialization, and does not happen again as long as the C4/8 and PCKT clocks stay phase-locked.

If the clocks lose their phase lock, the MT90840 will assert an automatic correction, and set the TXPAA interrupt bit high. The transmit parallel port data, the CTO control data and the TX frame pulse (PPFTo) will all jump phase due to this correction, causing one errored TDM frame.

If a CPU write to the Transmit Path Connection Memory is occurring during the one PCKT clock cycle that clocks the correction, there is a chance that the write data will go to address 0, rather than the intended address. To avoid this it is necessary to keep clocks stable during TPCM programming in TM1 (including not using DIN while programming). If there is some doubt about the quality of the clocks in a particular application, options include:

-1- Program the TPCM in TM2, or TM2 with internal clocks (INTCLK=1), where this clock correction does not occur.

-2- Monitor the TXPAA interrupt bit during TPCM programming, and check the intended address, and address 0, if a TXPAA alarm occurs.

-4- Read/verify address 0 after a block of TPCM writes. If address 0 is corrupted, one of the writes occurred during a clock correction.

Clock Quality and TM2 RPCM Access Integrity

In Timing Mode 2 the serial frame pulse F0o must be held in phase with the parallel port RX frame pulse (PPFRi). This is performed automatically by the MT90840 with an internal correction event, which inverts the phase of the SPCKo output. In normal operation the correction happens once on initialization, and does not happen again as long as the C4/8 and PCKR clocks stay phase-locked.

If the clocks lose their phase lock, the MT90840 will assert an automatic correction, and set the RXPAA interrupt bit high. The serial port data and the ST bus frame pulse (F0o) will jump phase due to this correction, causing one errored TDM frame. The PPCE bit indicates a change in framing at the receive parallel port which may cause a “cascade” correction at SPCKo.

If a CPU write to the Receive Path Connection Memory is occurring during the one 4.096 MHz clock cycle that clocks the correction, there is a chance that the write data will go to Stream0-Channel0, or Stream1-Channel0, rather than the intended address. To avoid this it is necessary to keep clocks stable during RPCM programming in TM2 (including not using DIN while programming). If there is some doubt about the quality of the clocks in a particular application, options include:

-1- Program RPCM in TM1, where this correction does not occur.

-2- Program RPCM in TM2 with Internal Clock mode, (INTCLK=1) where this correction does not occur.

-3- Monitor the RXPAA interrupt bit during RPCM programming, and check the ST0-Ch0 and ST1-Ch0 addresses if an alarm occurs.

-4- Read/verify ST0-Ch0 and ST1-Ch0 after a block of RPCM writes. If either is corrupted, one of the writes occurred during a clock correction.

Memory Block-Programming

The MT90840 allows the user to program one value into the entire Transmit Path Connect Memory High, or Receive Path Connect Memory High, with a single register write. This feature allows the four most significant bits of each byte in the TPCM High, or RPCM High, to be automatically programmed with the value of the 4 PBD bits of the GPM register. This eases system initialization by allowing all channels to be placed in high-impedance, or all channels to be placed in bypass. The procedure works as follows:

a) The SEL2-0 bits in the Control Register are used to select Block-Programming for either the TPCM High, or the RPCM High blocks. It is also necessary to select the serial port mode (with DR1-0 and FDC in the IMS register) before programming the RPCM.

b) The GPM Register is written. The CPU sets the Block-Programming Enable (BPE) bit to HIGH and the Block-Programming Data (BPD7-4) bits to the desired value. This action causes the contents of the BPD7-4 bits to be loaded into the four most significant bits of all addresses in TPCM High, or RPCM High (as set by the Control Register).

c) The user waits 250 μsec (two frames) to allow the TPCM High (2430 positions) or RPCM High (512 positions) to be entirely loaded with the new pattern.

d) After 250 μsec, the user should check that the BPE bit is LOW, indicating that the Block Program completed successfully. If the BPE bit does not return to LOW, the necessary TDM clock input may not be available. The BPE bit can be written LOW to force an end to the Block Programming.

Procedures a, b, c, and d must be performed twice if both TPCM and RPCM have to be initialized.

Block-programming requires stable F0 and PPFRi framing to function properly. If the framing jumps during block-programming, a section of memory may be missed. RPCM block-programming is dependent on the C4/8 serial port clock and F0 framing. TPCM block programming is dependent on the PCKT clock, and F0 framing (PCKR, PPFRi and F0 in TM2). DIN should not be active during block programming.

If there is some doubt about the quality of the clocks in a particular application, block-programming options include:

-1- If a stable C4/8 serial port clock is not available, or if a stable F0i frame is not available, use TM2 with Internal Clocks (INTCLK=1) to perform block-programming of RPCM.

-2- If stable PPFRi framing is not available in TM2, disable the external gate driving PPFRi and use free-running framing to perform block-programming of TPCM (and/or Internal Clocks mode to block-program RPCM).

The interrupt source bits can also be monitored during block-programming. If PPCE, or RXPAA (in TM2), or TXPAA (in TM1), is asserted during block-programming, a framing error has occurred and the block-programming should be repeated.

Timing Mode Initialization

On system power-up, the CPU should program the MT90840 IMS, GPM, and TIM registers to establish the data rates, the Timing Mode (1,2,3,4), and the framing polarity of the device. The MT90840 will then adjust its internal rate conversion and time interchange circuits to accommodate the different rates set at both data ports.

To perform the rate conversions between the serial and the parallel ports, the MT90840 provides a phase alignment circuit, monitored by the RXPAA and TXPAA interrupt bits. In TM1 and in TM2 with external clocks (INTCLK=0) the phase alignment circuit works automatically to maintain the relative phase of the serial and parallel ports. The DIN bit in the GPM register works with this circuit by reducing the window, forcing the phase alignment circuit to center the relative phases.

After the parallel and serial port reference clocks (PCKT/PCKR and C4/8R1/C4/8R2) are stable, the DIN bit in the GPM Register can be set HIGH. The DIN bit will auto-reset itself after 8 frames, returning to LOW. (It can also be written LOW by the CPU.) The DIN bit procedure is especially useful in TM2. In TM1 the DIN bit also centers the phase relation, but the movement of the transmit parallel port timing during the 8 frames that DIN is asserted may cause data or framing errors in connected devices. The RPCM and TPCM should not be written to by the CPU while DIN is asserted.

JTAG Support

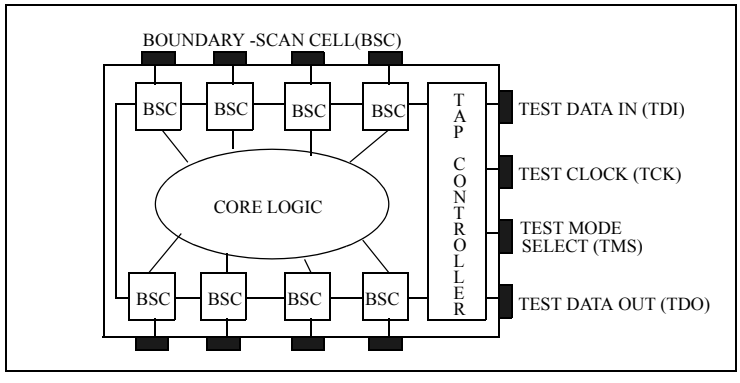


Figure 15 - A Typical Boundary-Scan IC

The MT90840 boundary-scan circuitry functions in accordance with IEEE Std 1149.1a (often referred to as JTAG boundary-scan). The standard specifies a design-for-testability technique called Boundary-Scan Test (BST). A boundary-scan IC has a shift-register stage or 'Boundary-Scan Cell' (BSC) in between the core logic and the I/O buffers adjacent to each I/O pin. The boundary-scan cellscan control and observe what happens at each I/O pin of the IC. The operation of the boundary-scan circuitry is controlled by a Test Access Port (TAP) Controller.

Test Access Port (TAP)

The Test Access Port (TAP) has five signals and provides access to the test logic defined by the JTAG standard.

The TAP has the following connections:

- Test Clock Input (TCK)

TCK provides the clock for the test logic. TCK is independent of the MT90840 functional clocks; this permits serial shifting of test data along the Boundary-Scan chain concurrent with the normal operation of the MT90840.

- Test Mode Select Input (TMS)

The signal at TMS selects the operational mode of the TAP Controller. The TMS signals are sampled on the rising edge of TCK. This pin is pulled high internally when not driven.

- The Test Data Input (TDI)

Serial instructions and test-data are shifted in at this pin. Serial information is passed to the instruction register, the boundary scan (test) register, or the bypass register, depending on the present mode of the TAP controller. TDI is sampled on the rising edge of TCK. This pin is pulled high internally when not driven.

- The Test Data Output (TDO)

Serial data is shifted out on this pin. Depending on the present mode of the TAP controller, data will come from one of: the instruction register, the boundary scan register or the bypass register. TDO is clocked out on the falling edge of TCK. When no data is being shifted, the TDO driver is set to a high-impedance state.

- $\overline{\text{TRST}}$:(Test reset input)

Asynchronously initializes the TAP controller by putting it in the *Test-Logic-Reset* state. This pin is pulled high internally when not driven.

One additional pin influences the boundary scan test operation:

- IC: (Manufacturing test pin)

This pin is an IEEE 1149 compliance-enable pin, and must be connected to Vss for proper boundary scan operation (and normal chip operation).

Boundary-Scan Instruction Register

In accordance with the IEEE 1149.1 standard, the MT90840 uses public instructions listed in Table 3 - “Instruction Register”. The MT90840 JTAG Interface contains a two bit instruction register. Instructions are serially loaded into the Instruction Register from the TDI pin when the TAP Controller is in its Shift-IR state. Subsequently, the instructions are decoded to achieve two basic functions: to select the test data register that may operate while the instruction is current and to define the serial test data register path that is used to shift data between TDI and TDO during data register scanning.

I[0:1]	Instruction	Description	
[00]	EXTEST	Boundary-Scan Register selected, Test enabled	This instruction is specifically provided to allow board-level interconnect testing of opens, bridging errors etc. When the EXTEST instruction is executed, the MT90840 core logic is isolated from the I/O pins, and the state of the I/O pins is determined by the boundary-scan register. I/O data for this instruction is pre-loaded into the boundary-scan register with the SAMPLE/PRELOAD instruction.
[01] [10]	SAMPLE/PRELOAD	Boundary-Scan Register selected, Test disabled	Two functions can be performed by the use of this instruction. It allows a SAMPLE (‘snapshot’) of the normal operation of the MT90840 to be taken for examination. And, prior to the selection of another test operation, a PRELOAD can place data values into the latched parallel outputs of the Boundary-Scan cells. During the execution of the instruction, the on-chip logic operation is not hampered in any way.
[11]	BYPASS	Bypass Register selected, Test disabled	This instruction is used to BYPASS the MT90840 while performing boundary-scan testing on other devices with scan registers in the same serial register chain. The MT90840 is allowed to function normally. This instruction is automatically loaded upon $\overline{\text{TRST}}$, as specified in IEEE1149.1

Table 3 - Boundary-Scan Instruction Register

Test Data Registers

As specified in the IEEE 1149.1 Standard, the MT90840 JTAG interface contains two test data registers:

- The Boundary Scan Register consists of a series of Boundary-Scan Cells arranged to form a scan path around the boundary of the core logic of the MT90840.
- The Bypass Register is a single stage shift-register that provides a one-bit path that minimizes the distance for test data shifting from the MT90840's TDI to its TDO.

The MT90840 Boundary-Scan register contains 107 bits. The suffix ('in', 'out', or 'en') indicates the nature and direction of the BSC. Bit 1 in Table 4 is the first bit clocked out. All tristate enable bits are asserted HIGH (i.e. a logic 1 enables the corresponding group of output/bidirectional pins). Note that clocking all zeros into the scan path register will set all outputs to tristate (outputs disabled).

Cells	Definition	Note
1	ppfri_in	first bit out
2	pckt_in	
3	pckr_in	
4:11	pdi<0:7>_in	
12:14	ppft_en, ppft_out, ppft_in	
15:22	pdo<0:7>_out	
23	pdo_en	enables pdo<0:7> outputs
24:27	cto<0:3>_out	always enabled
28	c48r2_in	
29:31	$\overline{\text{f0\_en, f0\_out, f0\_in}}$	
32	c48r1_in	
33:35	sti<7>_en, sti<7>_out, sti<7>_in	
36:53	sti<6>, sti<5>, ... sti<1>	
54:56	sti<0>_en, sti<0>_out, sti<0>_in	
57	$\overline{\text{res\_in}}$	
58	irq_en	tied HIGH internally
59	irq_out	
60	$\overline{\text{dta}}$_out	'pseudo' open-drain
61	$\overline{\text{cs}}$_in	

Table 4 - Boundary-Scan Register

Cells	Definition	Note
62	asale_in	
63	dsrdb_in	pin: ds/$\overline{rd}$
64	wrb_in	pin: r/$\overline{w}$\$\overline{wr}$
65:66	ad<7>_out, ad<7>_in	
67:78	ad<6>, ad<5>, ... ad<1>	
79:80	ad<0>_out, ad<0>_in	
81	ad_en	enables ad<0:7> outputs
82:84	sto<0>_en, sto<0>_out, sto<0>_in	
85:102	sto<1>, sto<2>, ... sto<6>	
103:105	sto<7>_en, sto<7>_out, sto<7>_in	
106:107	spcko_en, spcko_out	

Table 4 - Boundary-Scan Register

Please visit our web site at www.semicon.Zarlink.com to download a BSDL file for the MT90840.

Register Description

Interface Mode Selection Register (IMS) - READ/WRITE

DR1	DR0	PPS1	PPS0	ODE	0	0	FDC
7	6	5	4	3	2	1	0

DR1-0 Serial Port Data Rate Selection. Select one of three different data rates at the serial inputs and outputs of the MT90840.

DR1	DR0	Data Rate
0	0	2.048 Mbps
0	1	4.096 Mbps
1	0	8.192 Mbps
1	1	reserved

PPS1-0 Parallel Port Data Rate Selection. Select one of three different data rates for the parallel port of the MT90840.

PPS1	PPS0	Data Rate
0	0	reserved. Do not use.
0	1	6.480 Mbyte/s.
1	0	19.44 Mbyte/s.
1	1	16.384 Mbyte/s.

ODE Output Drive Enable. When LOW, forces the MT90840 output-buffers on the serial and parallel data ports into the high impedance state (STo0-STo7, STi0-STi7, and PDo0-7). If this output is HIGH, all channels have their output drive enable controlled by the per-channel OE bits of Transmit Connection Memory High, or Receive Connection Memory High.

FDC Full Direction Control. This bit should only be set HIGH at the 2.048 Mbps serial rate. When FDC is set HIGH, each time slot on each of the 16 ST-BUS pins can be individually configured as input or output. Up to 512 serial channels can be “inserted” onto the Transmit parallel port, or up to 512 parallel channels can be “dropped” to the serial port. Individual channel direction is controlled by the DC bits in the RPCM High. When FDC is LOW, the number of input and output time slots are “balanced”, and setting a nominal input to be an output causes the same-number output time slot on the same-number STo pin to become an input. For applications at 4.096 and 8.192 Mbps, this bit should be LOW.

Note: Bits 1 & 2 must be set to 0 by the CPU.

Timing Mode Register (TIM) - READ/WRITE

0	TM1	TM0	C4/8R	TCP	INTCLK	SFDI	PFDI
7	6	5	4	3	2	1	0

TM1-0 Timing Mode control bits. Define the four different timing modes described in the Timing and Switching Control section.

0 0 Timing Mode 1
0 1 Timing Mode 2
1 0 Timing Mode 3
1 1 Timing Mode 4

C4/8R C4/8R Input Reference Select. If set high, this bit enables the 4.096 or 8.192 MHz serial port reference clock to be taken from input pin C4/8R1. If LOW, the reference is taken from input pin C4/8R2 (default).

TCP Parallel Port Transmit Clock Polarity. To allow the MT90840 parallel port transmit clock to comply with different 155 Mbps framer backplanes, TCP controls which edge of the clock is used to transmit data at the parallel port. (The clock is PCKT in TM1 or PCKR in TM2, 3, & 4). The TCP bit allows the rising (TCP=LOW) or the falling (TCP=HIGH) edges of the transmit clock to be selected.

INTCLK Internal 4.096 MHz Clock Divider. For use in TM2, in 19.44 or 16.384 MHz parallel-port applications. This bit controls the operation of the internal clock divider driven by PCKR. When INTCLK is set HIGH the internal 4.096 MHz clock (and the SPCKo output) are generated by dividing down the PCKR clock. When INTCLK is set LOW, the C4/8R bit controls the source for the serial clock reference. In TM3 and TM4 the MT90840 automatically sets itself in the internal divider mode and the state of INTCLK has no effect. In TM1 this bit is must be set LOW.

SFDI Serial Frame Pulse Direction Control. Normally LOW, unless it is necessary to operate multiple parallel MT90840 devices in Timing Mode 2. When set HIGH, the F0 line becomes an input and this MT90840 is synchronized to the timing of another MT90840 generating the F0o, and using the same 4.096 or 8.192 MHz reference input. One MT90840 in TM2 with SFDI LOW can control several MT80940s with SFDI HIGH. When SFDI is set HIGH, INTCLK is ignored, and SPFP in the GPM register must be set to the expected F0i polarity.

PFDI Parallel Frame Pulse Direction Control. Normally LOW, unless it is necessary to operate multiple parallel MT90840 devices in Timing Mode 1. When set HIGH, the PPFT pin becomes an input and this MT90840 is synchronized to the timing of another MT90840 generating the PPFTo. One MT90840 in TM1 with PFDI LOW can control several MT80940s with PFDI HIGH. When PFDI is HIGH, PPFP in the GPM register must be set to the expected PPFTi polarity.

Note: Bit 7 must be set to 0 by the CPU.

General Purpose Mode Register (GPM) - READ/WRITE

BPD7	BPD6	BPD5	BPD4	PPFP	DIN	SPFP	BPE
7	6	5	4	3	2	1	0

BPD7-4 Block-Programming Data bits 7-4. These bits carry the value to be loaded into the TPCM-High or RPCM-High memory when the Memory Block-Programming feature is activated. When BPE is set HIGH, the contents of bits BPD7-4 are loaded into the four most significant bits of TPCM-High or RPCM-High, and the four least significant bits of TPCM-High or RPCM-High are zeroed.

PPFP Parallel Port Frame pulse Polarity. Used to program the polarity of the PPFT frame pulse. If PPFP is set HIGH, the frame boundaries at the Parallel Port output will occur when PPFT pulse signal is HIGH. If PPFP is set LOW, the PPFT output will indicate frame boundaries with a LOW active pulse. The transmit edge for the generation of PPFT, as well as PDo and CTo, is determined by TCP in the TIM Register.

DIN Device Initialization. This bit is used in TM1 and TM2 to center the phase relation between the parallel port clocks and the serial port clock. It can be set HIGH by the CPU after the serial and parallel port rates are written in the IMS Register, and the input clocks are stable. If the MT90840 internal divider is used (INTCLK bit = HIGH), or if TM4 or TM3 is selected, this bit is not used. This bit is automatically returned low after 8 frames, and clears all interrupt source bits in the ALS register as long as it is HIGH. The Connect Memories should not be programmed while DIN is asserted.

SPFP Serial Port Framing Polarity. In TM2 and TM3 this bit defines the format of the serial port frame pulse F0o, and the clock SPCKo. If SPFP is HIGH, F0o is set as a positive pulse with GCI timing. If SPFP is LOW, F0o is set as a negative pulse with ST-BUS timing. In TM2 with SFDI set HIGH, this bit specifies the expected F0i input polarity. In TM1, the F0i input polarity is automatically detected, and this bit is ignored. See the interface timing specifications.

BPE Block-Programming Enable. This bit activates the memory block-programming feature. It can be set high after the SEL0-2 bits in the Control Register are set to select the memory to be programmed. The BPE and BPD7-4 bits in this register must be defined in the same write operation. Once BPE is set HIGH, the user should wait at least 250 µs and then check BPE = LOW to see that the operation completed successfully. This bit can also be written low to force the end of the block-program operation.

Note: The CPU must maintain the required settings of the PPFP and SPFP bits when BPE is written. The DIN function and the BPE function should not be used simultaneously.

Alarm Status Register (ALS) - READ/WRITE

MSK3	MSK2	MSK1	MSK0	PPCE	RXPAA	TXPAA	FSA
7	6	5	4	3	2	1	0

MSK3-0 Mask Alarm Bits 3-0. These bits mask the specific interrupt source bits. MSK3 masks PPCE, MSK2 masks RXPAA, etc. If MSKn is set HIGH, the corresponding interrupt source is enabled, and the IRQ pin will respond to that interrupt source; if set LOW, the corresponding interrupt source is masked. When masked, an interrupt source will not assert the IRQ pin, but will still set the ALS register bit. On system power-up, all interrupts are masked. Writes to the ALS register clear the low nibble (interrupt source bits) regardless of the data written.

PPCE Parallel Port Frame Counter Error. Used in all timing modes. The PPCE bit goes HIGH whenever there is an incorrect number of PCKR clock cycles between PPFRi frame sync signals on the Receive parallel port. The numbers of clock cycles expected depends on the parallel port rate selected in the IMS Register (2430, 2048, or 810 clock cycles). The absence of PPFRi for one or more frames will not cause an interrupt (allowing free-run operation), but the PPCE bit will go HIGH if PPFRi occurs anywhere but on an expected frame boundary.

RXPAA RX Phase Alignment Alarm. Used in TM2 operation, when INTCLK = 0. The RXPAA bit goes HIGH whenever the C4/8 input reference goes out of phase relative to the parallel port clock (PCKR). A rising edge on the RXPAA bit indicates that the MT90840 has adjusted the position of F0o and SPCKo, and a data slip at the serial port has occurred. Note that a CPU write to the RPCM memory as RXPAA goes HIGH (in TM2) may be corrupted. In TM2 with SFDI = 1, a rising edge on the RXPAA bit indicates that the F0i input is out of phase with PPFRi, implying a failure in the timing supplied by the controlling (TM2 with SFDI = 0) MT90840. When not in TM2 the RXPAA bit may be continuously asserted, and therefore should be masked by setting MSK2 LOW, and ignored.

TXPAA TX Phase Alignment Alarm. Used in TM1 operation. The TXPAA bit goes HIGH whenever the PCKT clock input goes out of phase relative to the C4/8 clock. A rising edge on the TXPAA bit indicates that the MT90840 has adjusted the position of PPFTo, and a data slip at the TX parallel port output has occurred. Note that a CPU write to the TPCM memory as TXPAA goes HIGH (in TM1) may be corrupted. In TM1 with PFDI = 1, a rising edge on the TXPAA bit indicates that the PPFTi input is out of phase with F0i, implying a failure in the timing supplied by the controlling (TM1 with PFDI=0) MT90840.

FSA Frame Slip on Elastic Buffer. Used in TM1 operation. The FSA bit goes HIGH when either an overflow or underun condition on the Receive parallel port's elastic buffer has been detected. A rising edge on the FSA bit indicates that a frame of data from the RX parallel port has been dropped, or repeated. In TM2, TM3, and TM4 the user should mask this bit by setting MSK0 LOW.

Note: The interrupt source bits are latched, and remain high until cleared by the CPU. The interrupt source bits (ALS low nibble) are cleared by writing the mask bits (ALS high nibble), regardless of the data written.

Control Register (CR) - READ/WRITE

SEL2	SEL1	SEL0	HA11	HA10	HA9	HA8	HA7
7	6	5	4	3	2	1	0

This register selects which 128 byte page of which internal memory will be accessed by the CPU when the address bit AD<7> is high. (When address bit AD<7> is low, the control registers are accessed.)

SEL2-0 Memory Select bits. Used by the CPU to select the internal memories of the MT90840 for read or write operations. SEL2-0 bits have to be written before any READ/WRITE operation is performed on the internal memories.

SEL2	SEL1	SEL0	Memory Selected for RD/$\overline{WR}$ operation
0	0	0	Receive Path Connection Memory Low (RPCM Low)
0	0	1	Receive Path Connection Memory High (RPCM High)
0	1	0	Receive Path Data Memory (RPDM)
0	1	1	Enable Memory Block-Programming feature for RPCM High
1	0	0	Transmit Path Connection Memory Low (TPCM Low)
1	0	1	Transmit Path Connection Memory High (TPCM High)
1	1	0	Transmit Path Data Memory (TPDM)
1	1	1	Enable Memory Block-Programming feature for TPCM High

HA11-7 High Address Bits 11-7. These bits select which 128 byte page of the selected memory (see SEL2-0 bits) will be accessed by the CPU. Used along with AD0-AD6 input lines to address the MT90840 internal memories when the address bit AD<7> is high. See RPCM, TPCM, RPDM and TPDM Address Mapping section for more details.

To address serial time slots in TPDM or RPCM:

Serial Port Data Rate	Number of Serial Port Input and Output Streams	HA bits and input address lines, or TPCM address bits, used to select ST stream.	HA bits and input address lines, or TPCM address bits, used to select the time slot.
2 Mbps Balanced	8i x 8o (256 channels)	HA7 + AD6-AD5 / AB7-AB5	AD4-AD0 / AB4-AB0 (32 time slots)
2 Mbps Add/Drop	16 i/o (512 channels)	HA8-HA7 + AD6-AD5 / AB8-AB5	AD4-AD0 / AB4-AB0 (32 time slots)
4 Mbps	8i x 8o (512 channels)	HA8-HA7 + AD6 / AB8-AB6	AD5-AD0 / AB5-AB0 (64 time slots)
8 Mbps	4i x 4o (512 channels)	HA8-HA7 / AB8-AB7	AD6-AD0 / AB6-AB0 (128 time slots)

To address parallel time slots in RPDM or TPCM:

Parallel Port Data Rate	Number of Channels	HA bits and input address lines used to select channel in TPCM.	RPCM address bits used to select channel.
19.44 Mbyte/s	2430	HA11-HA7 + AD6-AD0	AB11-AB0
16.384 Mbyte/s	2048	HA10-HA7 + AD6-AD0	AB10-AB0
6.480 Mbyte/s	810	HA9-HA7 + AD6-AD0	AB9-AB0

Phase Status Registers (PSD) - READ Only

PSD7	PSD6	PSD5	PSD4	PSD3	PSD2	PSD1	PSD0	Register Address 8 (Low Byte)
7	6	5	4	3	2	1	0	
0	0	0	0	0	PSD10	PSD9	PSD8	Register Address 9 (High 3-bits)
7	6	5	4	3	2	1	0	

PSD10-0 Phase Status Data 10-0. The PSD bits represent the phase status of the serial port, as sampled at every second PPFRi frame (every 250 µsec). PSD0 is the phase of the internal 4.096 MHz clock, PSD1-9 count the cycles of the 4.096 MHz within a frame, and PSD10 toggles each frame (even/odd frame bit). The PSD bits enable the CPU to monitor the relative phases of the Receive parallel port and the serial port. This is especially useful in TM1, where the PSD bits might be used by the CPU to monitor a PLL control loop, since the elastic buffer in the Receive parallel port allows great variation in phase. These registers should be read twice in succession, in case the CPU access occurs close to the sampling edge.

Internal Memory Description

Transmit Path Connection Memory High (TPCM High) - This is an 8-bit x 2430-position memory.

OE/ CTo0	PPBY	MC	CTo1	CTo2/ AB11	CTo3/ AB10	AB9	AB8	(TX Path CM High)
7	6	5	4	3	2	1	0	

OE/CTo0 Output Enable. Provides per channel tristate control on the parallel port side. It controls the MT90840 parallel output drivers to disable (tristate, when LOW) or enable (when HIGH) the transmission of data from the device. The contents of this bit will also be clocked out on the CTo0 output pin at the parallel port rate.

PPBY Parallel Port Bypass Enable. Indicates that the parallel output channel is going to contain bypassed (PPBY=HIGH) data from the Receive parallel port of the MT90840. The channels that are not bypassed (PPBY=LOW) can be used for switching of data from the serial port side, or for message-mode data. The use of this bit is only allowed in Timing Modes 1 and 2. The PPBY bit is overridden by MC set HIGH.

MC Message Channel. The message channel contents are programmed by the CPU into the TP Connection Memory Low. If MC=1 the contents of the corresponding location of TPCM Low are output on the corresponding channel at the Transmit parallel port. If MC=LOW, the contents of the programmed location in TPCM Low act as an address for the Data Memory, and so determine the source channel for this output channel. Depending on the timing mode selected, the source of the connection can be an input channel from either serial (TM1, 2, or 3) or parallel (TM4) data ports. This bit overrides PPBY if both are set HIGH.

CTo1-3 External Control Lines 1-3. These three bits are used by the CPU to program the three external control pins CTo1-3. Like OE/CTo0, the contents of these lines will be transmitted to pins CTo1-3 at the parallel port rate. **Note**: CTo2 and CTo3 cannot be used in Timing Mode 4.

AB8-11 Source Channel Address Bits 8-11. These bits are used along with bits AB0-7 in TPCM Low to select the source channel for this output channel. In all timing modes except TM4, only bit AB8 is used, along with bits AB0-7 in TPCM Low, to select one of 512 serial source channels from the serial port side to be transmitted on this output channel.

Transmit Path Connection Memory Low (TPCM Low) - This is an 8-bit x 2430-position memory.

AB7	AB6	AB5	AB4	AB3	AB2	AB1	AB0
7	6	5	4	3	2	1	0

(TX Path CM Low)

AB7-0 Source Channel Address Bits. In Timing Modes 1, 2, and 3, these 8 bits are used along with bit AB8 in the TPCM High to select up to 512 serial source channels from the serial port side to be connected to any 512 (out of 2430) output channels available on the parallel port side. See table for details.

In Timing Mode 4, these 8 bits are used along with bits AB8-11 in the TPCM High memory to select up to 2430 source channels from the parallel port input to be connected to any of the 2430 channels available on the parallel port output side.

If message mode is selected at TPCM High bits, the contents of the AB0-7 bits in the TPCM Low locations are transmitted to the corresponding channels at the PDo0-7 lines until the mode is changed by the CPU.

USE OF THE TPCM HIGH AND LOW ADDRESS BITS WHEN SELECTING SOURCE SERIAL-PORT CHANNELS (TM1, TM2 and TM3)			
SERIAL STREAM and CHANNEL ALLOCATION		SOURCE STREAM ADDRESSING	SOURCE CHANNEL ADDRESSING
2 Mbps	16 i/o (512 channels)	AB5,AB6,AB7,AB8 (up to 16 streams)	AB0 to AB4 used to select up to 32 channels per stream
4 Mbps	8i x 8o (512 channels)	AB6, AB7, AB8 used to select up to 8 streams	AB0 to AB5 used to select up to 64 channels per stream
8 Mbps	4i x 4o (512 channels)	AB7, AB8 used to select up to 4 streams	AB0 to AB6 used to select up to 128 channels per stream

SOURCE CHANNEL ADDRESSING IN TM4	
6.48 Mbyte/s	AB0-AB9 (one of 810 input channels)
16.384 Mbyte/s	AB0 - AB10 (one of 2048 input channels)
19.44 Mbyte/s	AB0 - AB11 (one of 2430 input channels)

Receive Path Connection Memory High (RPCM High) - This is a 7-bit x 512-position memory. Used only in TM1, 2, & 3.

-	MC	DC	OE	AB11	AB10	AB9	AB8	(RX Path CM High)
7	6	5	4	3	2	1	0	

MC Message Channel: The message channel contents are provided by the CPU in bits AB0-7 in the Rx Path Connection Memory Low. If MC is HIGH, the contents of the corresponding location of RPCM Low are output on this serial port channel. If MC is LOW, the contents of the corresponding location in RPCM Low act as an address for the Rx Path Data Memory and so determine the source of the connection (input channels from the PDi0-7 port).

DC Direction Control: DC set HIGH indicates this channel is an output. DC set LOW indicates this channel is an input. The operation of this bit is modified by the state of FDC in the IMS Register.

When FDC = LOW (2.048, 4.096 or 8.192 Mbps) the 512 DC bits (256 at 2.048) each define the direction of a pair of pins for each channel. When DC is set LOW the associated channel on the STo pin becomes an input, and the corresponding channel on the same-number STi pin is automatically used as the output for this time slot. When DC is set HIGH, STo is the output, and STi is the input for this time slot (default).

When FDC = HIGH (2.048 Mbps), the 512 DC bits can be used to control the direction of each individual 64 kbps time slot present on the 16 serial I/O lines on a non-symmetrical basis; i.e. all 512 channels can be configured as outputs or inputs or any mixed combination. If DC is LOW, this serial port channel is defined as input. If DC is HIGH, this channel is defined as output. Note that the CPU still has to set OE to enable the output buffers on each channel defined as an output.

OE Output Enable. Per-channel tristate control for each channel on the serial port side. If FDC is HIGH, the 512 OE bits enable the output for each of the 512 ST channels, unless the channel is defined as an input by the DC bit. In 4.096 and 8.192 Mbps modes, the OE bit enables the output buffer either on a STo pin, or an STi pin, as defined by the accompanying DC bit.

AB8-11 Source Channel Address. These 4 bits are used along with AB0-7 to select any of the 2430 parallel incoming channels from the parallel port and determine the switch connection to the 512 possible destination channels on the serial port.

Receive Path Connection Memory Low (RPCM Low) - This is an 8-bit x 512-position memory. Used only in TM1, 2 &3.

AB7	AB6	AB5	AB4	AB3	AB2	AB1	AB0	(RX Path CM Low)
7	6	5	4	3	2	1	0	

AB0-7 Source Channel Address. In switching mode (MC=LOW), these 8 bits are used along with AB8-11 to select one of the 2430 incoming channels from the parallel port. In message mode (MC=HIGH), these 8 bits are programmed by the CPU with the message patterns desired on the corresponding serial output channel.

Applications

Distributed Isochronous Network

Low latency isochronous backbones provide for the deployment of systems that require cost effective implementation, high bandwidth, predictable data transfer delays and direct synchronization with the wide area network.

Some applications in Computer Telephony Integration (CTI) require a large amount of bandwidth to be transported between multiple chassis within the same location, or between separate locations. The MT90840 is ideal for implementing physically distributed transport and switching systems for multi-chassis or inter-shelf communications.

The MT90840 bridges existing Zarlink ST-BUS components into a new networking environment where mixed data, voice and video signals can be time-interchanged or multiplexed from serial PCM streams onto serial high-speed time-division- multiplex (TDM) isochronous backbones operating at SONET rates such as 51 (STS-1) or 155 Mbps (STS-3).

Today, transmission links operating at SONET rates utilize serial-to-parallel and parallel-to-serial converters (or framers) which perform embedded framing functions and give the user access to the payload of the high speed frame. The MT90840 provides an 8-bit bidirectional parallel data port which directly interfaces to a high-speed framer parallel data interface, allowing designers to build distributed networking systems with interconnection speeds up to 155 Mbps. Figure 16 shows an example of a distributed networking application in a CTI system.

The MT90840's clock synchronization and reference options allow many applications and topologies when isochronous TDM backbones are required. Two major clock synchronization schemes provided by the MT90840 allow the serial port interface (ST-BUS) to provide the master clock and frame reference signals for the distributed high speed backbone (master operation) or to derive the entire ST-BUS clock and frame reference signals from the high speed backbone (slave operation). This type of synchronization scheme may be used in applications such as the proposed MVIP multi-chassis level 3 interface (MC-3 system) utilizing point-to-point or point-to-multipoint switching connections.

When the MT90840 operates in a ring application, the Parallel Data Bypass mode is provided to allow all or part of the received input parallel data to be bypassed to the output parallel port feeding the ring back with the data which is not destined for the local station. The data destined for the local station can be dropped through CPU programming. In this mode, the CPU has full control of the outgoing bandwidth (from the serial interface to the high speed link) so that it does not contend with the bypassed data.

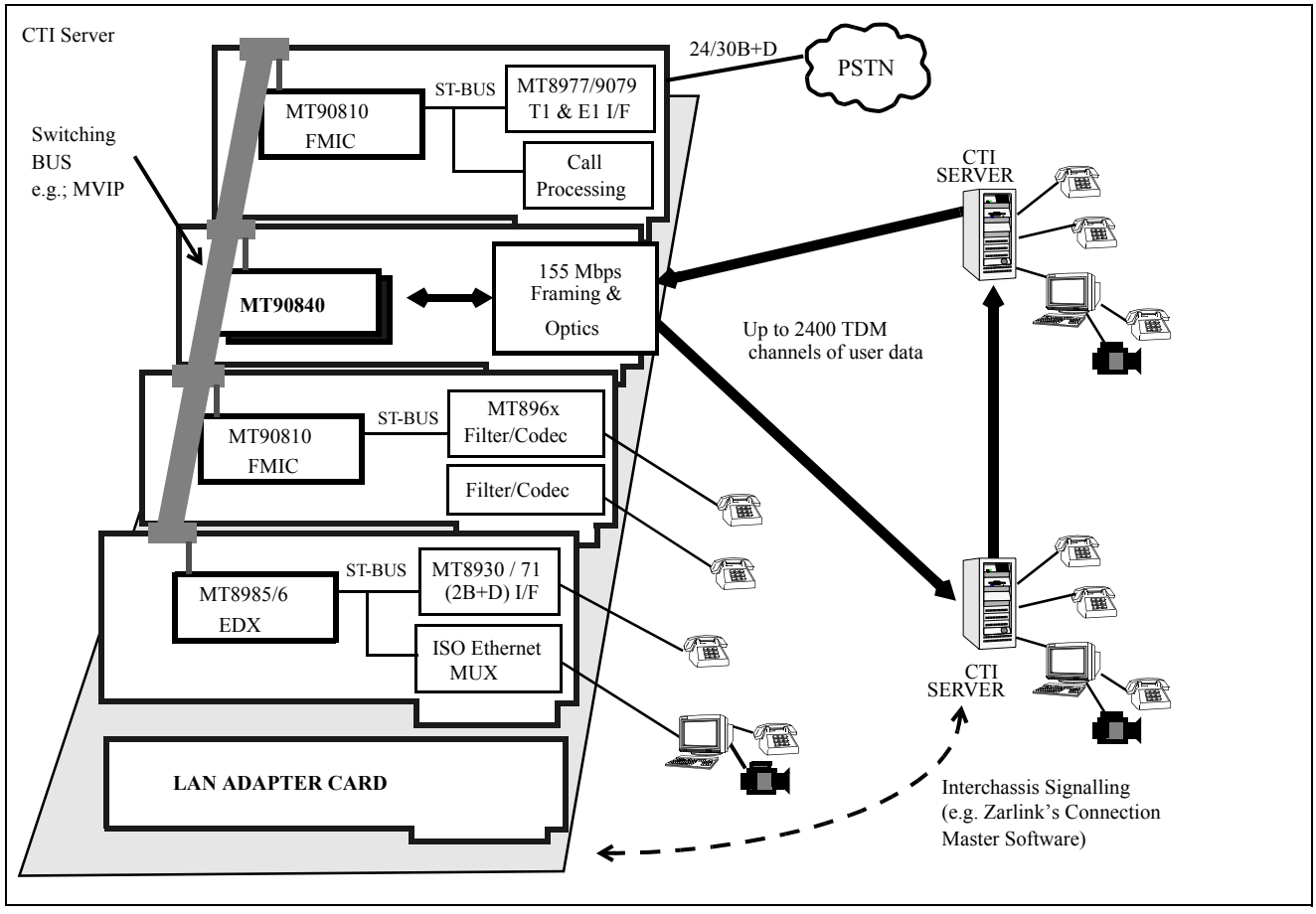


Figure 16 - CTI Distributed Architecture Implemented with the MT90840

Absolute Maximum Ratings*

	Parameter	Symbol	Min.	Max.	Units
1	Supply Voltage	V_{DD}	0	6	V
2	Voltage on any I/O pin	V_I	V_{SS}-0.3	V_{DD}+0.3	V
3	Continuous Current at Digital Outputs	I_O		40	mA
4	Storage Temperature	T_S	-65	+125	°C
5	Package Power Dissipation	P_D		2	W

* Exceeding these values may cause permanent damage. Functional operation under these conditions is not implied.

Recommended Operating Conditions - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.	Max.	Units	Test Conditions
1	Operating Temperature	T_{OP}	-40		+85	°C	
2	Positive Supply	V_{DD}	4.75	5.0	5.25	V	
3	Input Voltage	V_I	0		V_{DD}	V	

DC Electrical Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

		Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions/Pins
1		Supply Current at 19.44 Mbyte/sec & 4 Mbps	I_{DD}		100	160	mA	Outputs unloaded
2	INPUTS	Input High Voltage	V_{IH}	2.0			V	TTL inputs (most pins)
3		Input Low Voltage	V_{IL}			0.8	V	TTL inputs (most pins)
4		Input High-Going Threshold	V_{T+}		2.8	4.2	V	Schmitt inputs
5		Input Low-Going Threshold	V_{T-}	0.9	1.8		V	Schmitt inputs
6		Input Leakage (I/O pins)	I_{IL}			50	µA	V_I between V_{SS} and V_{DD}
7		Input Pin Capacitance	C_I			10	pF	
8	OUTPUTS	Output High Voltage	V_{OH}	2.4			V	Sourcing I_{OH}
9		Output Low Voltage	V_{OL}			0.4	V	Sinking I_{OL}
10		Output High Current (sourcing at V_{OH}) or Output Low Current (sinking at V_{OL})	I_{OH} or I_{OL}	9			mA	Pins: STi4-7, STo4-7
				16			mA	TDO, RPA, $\overline{DTA}$, AD7-0, F0, SPCKo, STi0-3, STo0-3
				28			mA	PDo0-7, CTo3-0, PPFTo
11		High Impedance Leakage	I_{OZ}			5	µA	V_O between V_{SS} and V_{DD}. Pins: PDo0-7, CTo3-0
12		Output Pin Capacitance	C_O			10	pF	

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

AC Electrical Characteristics - **Voltages are with respect to ground (V_{SS}) unless otherwise stated.**

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	C4/8 Input - Clock Period: 4.096 MHz (2.048 & 4.096 Mbps) 8.192 MHz (8.192 Mbps) SPCKo Output - Clock Period from internal divider (2.048 & 4.096 Mbps) SPCKo Output - Clock Period generated from external C4/8 reference (2.048 and 4.096 Mbps)	t_{clk}	 200 100 224 241	 244 122	 259 245	 ns ns ns ns	C4/8R1 or C4/8R2 19.44 MHz 60/40% duty-cycle clock at PCKR C4/8R1 input with 244 ns cycle
2	C4/8 Input Clock Width HIGH 4.096 MHz (2.048 & 4.096 Mbps) 8.192 MHz (8.192 Mbps) SPCKo Output - Clock Width HIGH from internal divider (2.048 & 4.096 Mbps) SPCKo Output - Clock Width HIGH generated from external C4/8 reference (2.048 and 4.096 Mbps)	t_{clkh}	 85 50 101 110	 122 61	 135 	 ns ns ns ns	C4/8R1 or C4/8R2 19.44 MHz 60/40% duty-cycle clock at PCKR C4/8R1 input with min. 115 ns semi-cycle
3	C4/8 Input - Clock Width LOW 4.096 MHz (2.048 & 4.096 Mbps) 8.192 MHz (8.192 Mbps) SPCKo Output - Clock Width LOW from internal divider (2.048 & 4.096 Mbps) SPCKo Output - Clock Width LOW generated from external C4/8 reference (2.048 and 4.096 Mbps)	t_{clkl}	 85 50 101 110	 122 61	 135 	 ns ns ns ns	C4/8R1 or C4/8R2 PCKR with 60/40% duty cycle C4/8R1 input with minimum 115 ns half-cycle
4	CLK rise/fall time	t_t		5		ns	
5	F0 output delay from SPCKo (TM2 & TM3, 2.048 and 4.096 Mbps) F0 output delay from C4/8 input (TM2 & TM3, 8.192 Mbps)	t_{df}			32 51 30 46	ns ns	C_L=30pF C_L=150pF C_L=30pF C_L=150pF
6	F0i Setup Time from C4/8 input edge TM1 TM2 with SFDI =1	t_{frs}	 0 28			 ns ns	 C4/8 falling edge
7	F0i Hold Time from C4/8 input edge TM1 TM2 with SFDI =1	t_{frh}	 8 0			 ns ns	 C4/8 falling edge C4/8 rising or falling
8	F0i Input Frame Pulse Width 2.048, 4.096, 8.192 Mbps	t_{frw}	 35			 ns	

AC Electrical Characteristics - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
9	STo Delay - Active to High-Z, 2.048 and 4.096 Mbps (TM2 &TM3) 2.048 and 4.096 Mbps (TM1) 8.192 Mbps (STio0-3)	t_{az}			 38 50 26	 ns ns ns	C_L=30pF, R_L=1K
10	STo Delay from High-Z to Active 2.048 and 4.096 Mbps (TM2 &TM3) 2.048 and 4.096 Mbps (TM1) 8.192 Mbps (STio0-3)	t_{za}			 38 50 26	 ns ns ns	C_L=30pF, R_L=1K
11	STo Output Delay from SPCKo (TM2 & TM3, 2.048 and 4.096 Mbps) STo Output Delay from 4.096 MHz C4/8 input (TM1) STo 8.192 Mbps Output Delay from C4/8 input (TM1, 2 & 3; STi/o0-3)	t_{sod}			40 64 52 72 28 43	ns ns ns ns ns ns	C_L=30pF C_L=150pF C_L=30pF C_L=150pF C_L=30pF C_L=150pF
12	STi Input Setup Time from SPCKo output edge (2.048 and 4.096 Mbps) STi Input Setup Time from C4/8 input edge in TM1 (2.048 and 4.096 Mbps) STi Input Setup Time from C4/8 input edge at 8.192 Mbps (STi/o0-3)	t_{stis}	28 41 0 0			ns ns ns	SPCKo C_L=30pF SPCKo C_L=150pF TM1 and TM2, STi0-3, STo0-3
13	STi Input Hold Time from SPCKo output edge (2.048 and 4.096 Mbps) STi Input Hold Time from C4/8 input edge in TM1 (2.048 and 4.096 Mbps) STi Input Hold Time from C4/8 input edge at 8.192 Mbps	t_{stih}	9 2 20 13			ns ns ns	SPCKo C_L=30pF SPCKo C_L=150pF TM1 and TM2, STi0-3, STo0-3

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

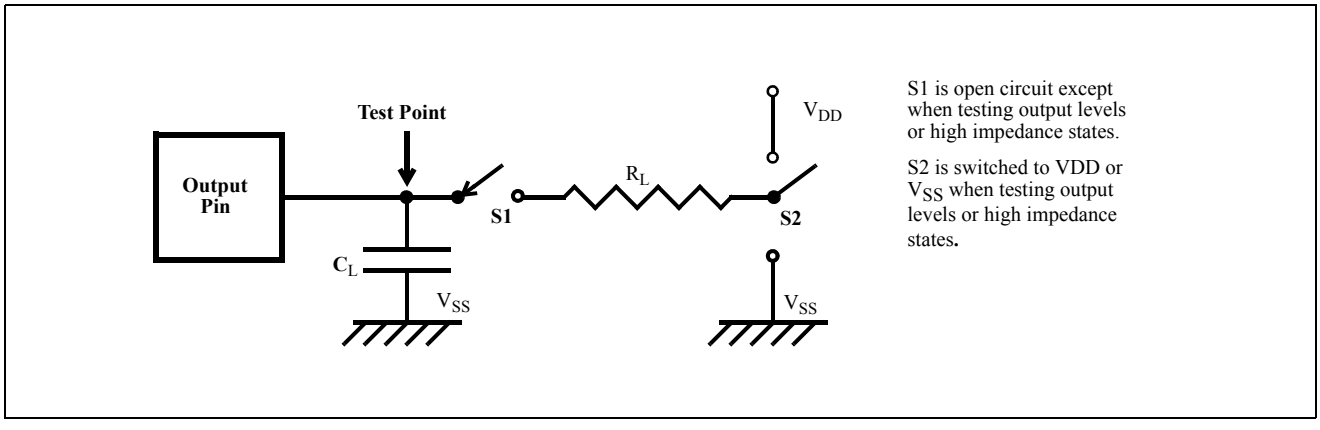
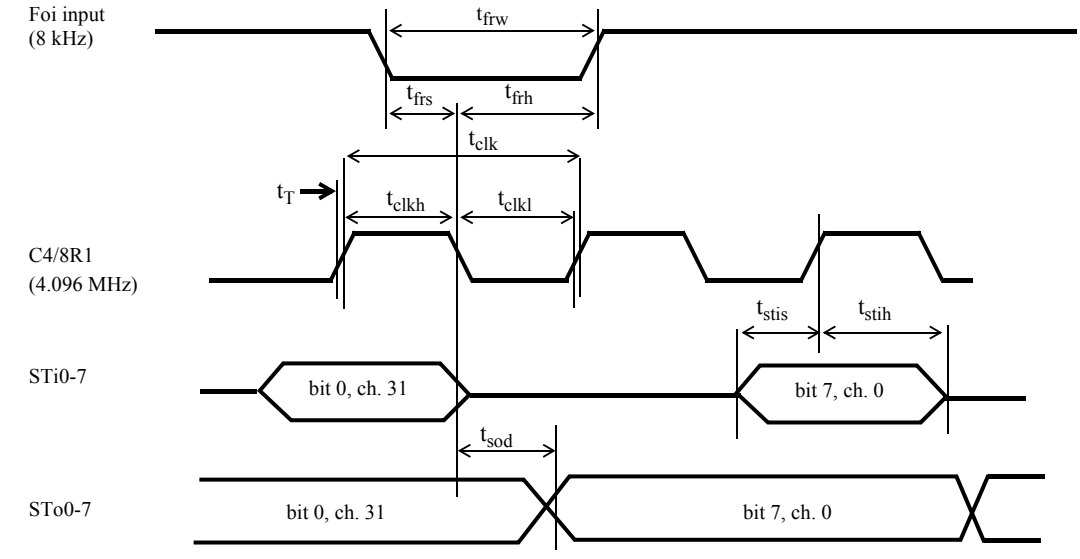
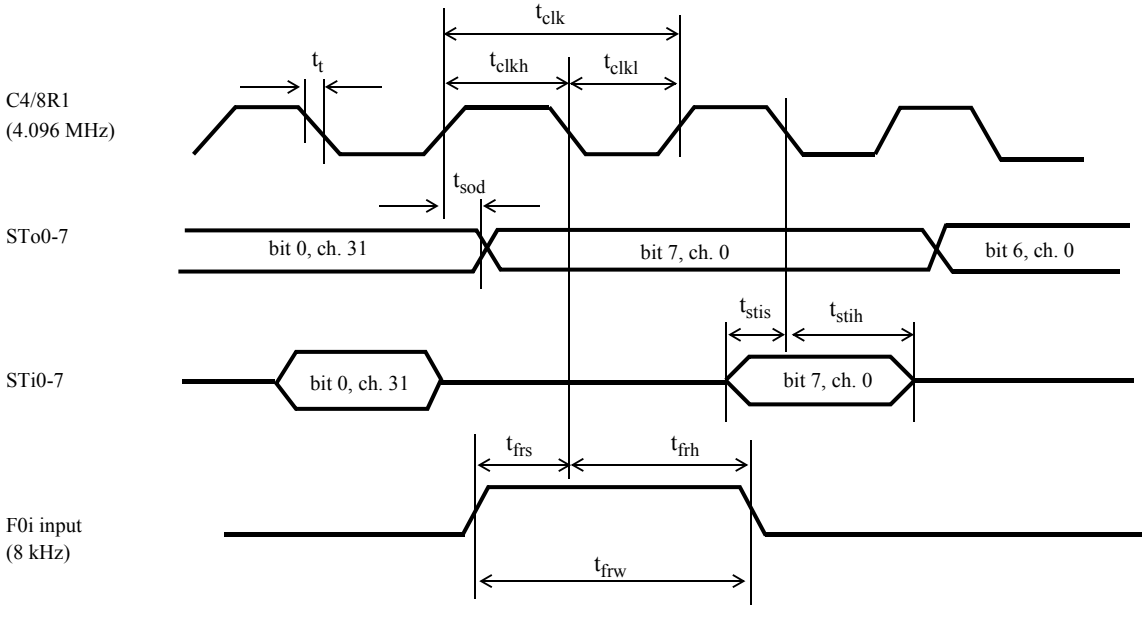


Figure 17 - Output Test Load



Serial Port with Negative Polarity F0 (ST-BUS)



Serial Port with Positive Polarity F0 (GCI)

Note: In TM2 with SFDI=1, C4/8R1 may have reversed polarity from that shown.

Figure 18 - Serial Port Timing for 2.048 Mbps Operation - TM2 (SFDi = 1) and TM1

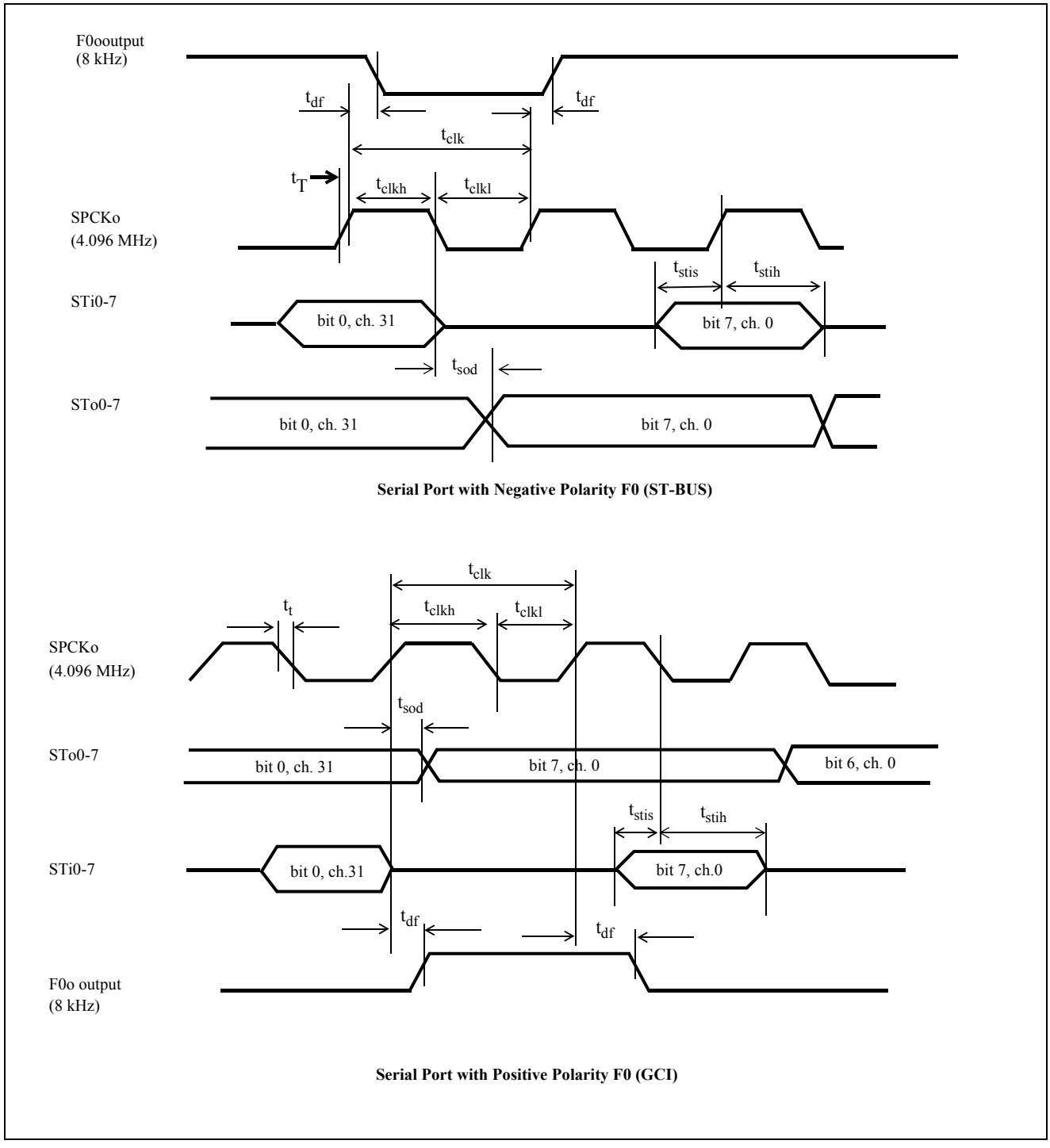
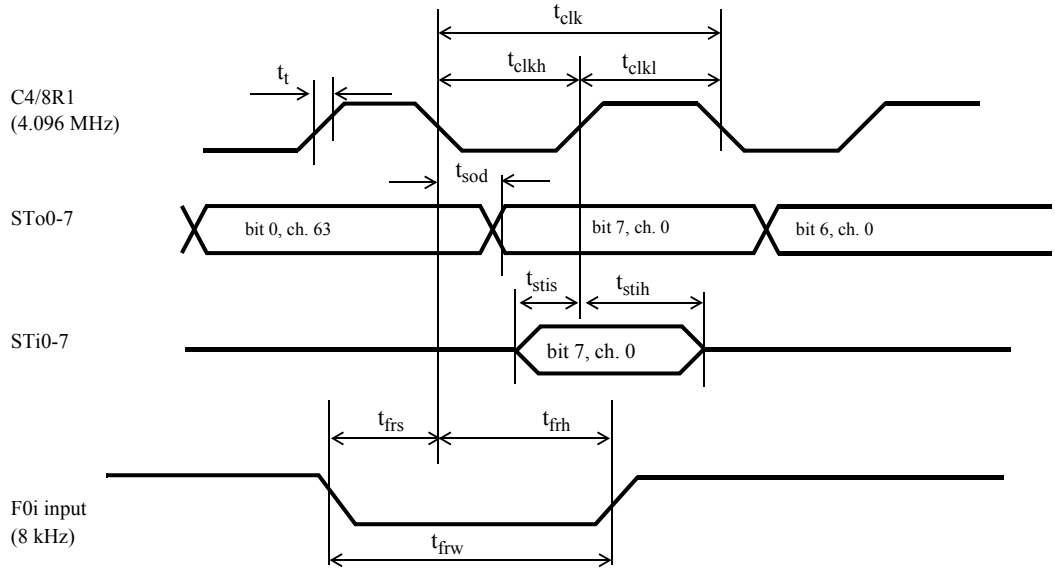
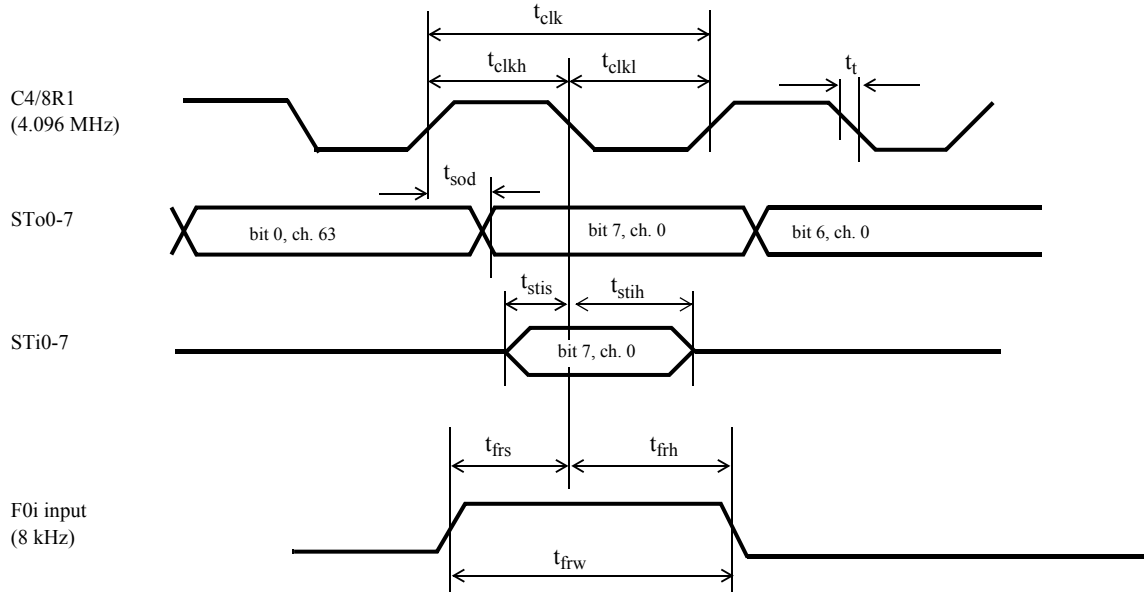


Figure 19 - Serial Port Timing for 2.048 Mbps - TM2 (SFDi = 0) and TM3



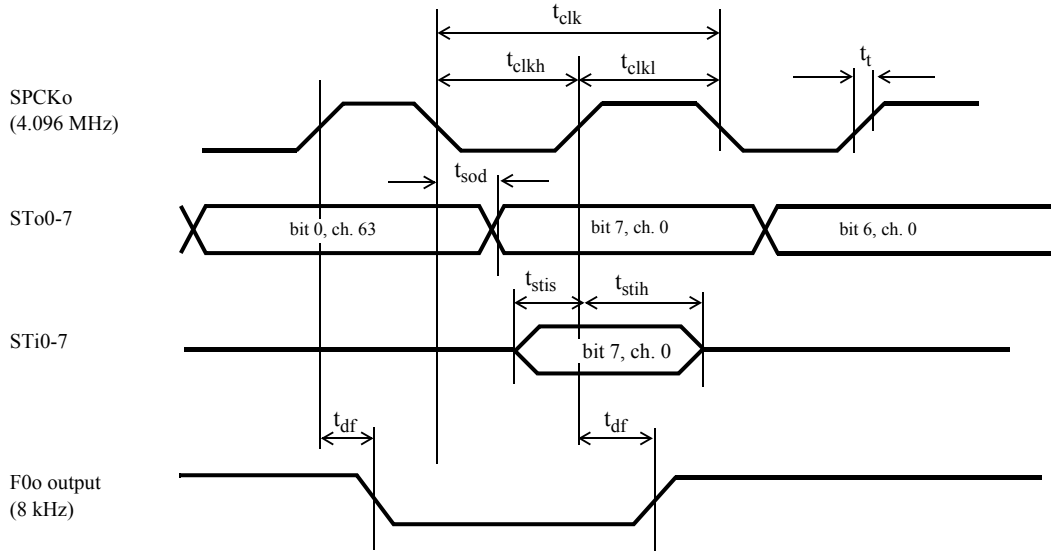
Serial Port with Negative Polarity F0 (ST-BUS)



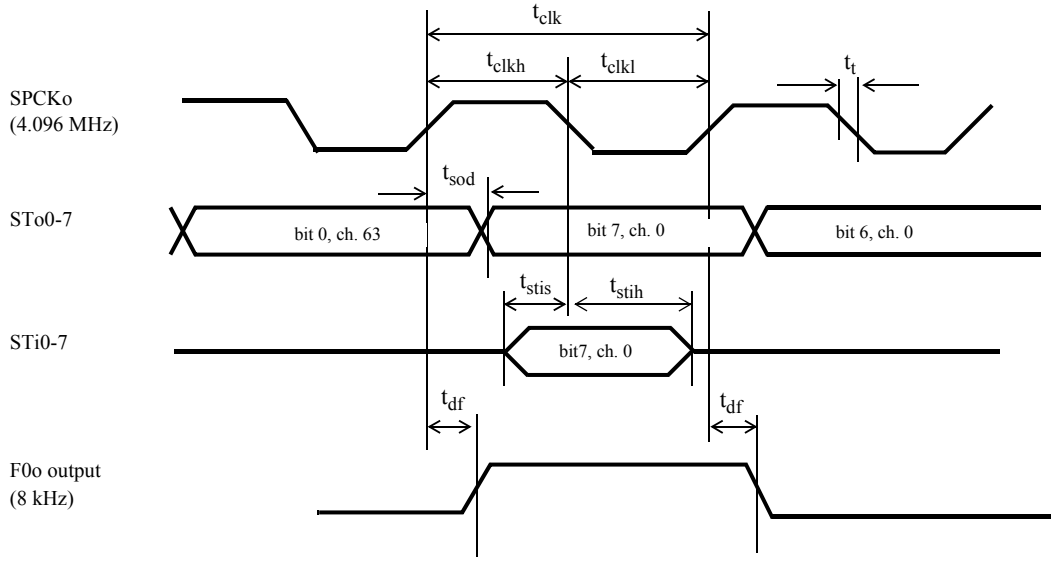
Serial Port with Positive Polarity F0 (GCI)

Note: In TM2 with SFDI=1, C4/8R1 may have reversed polarity from that shown.

Figure 20 - Serial Port Timing for 4.096 Mbps Operation - TM2 (SFDi = 1) and TM1

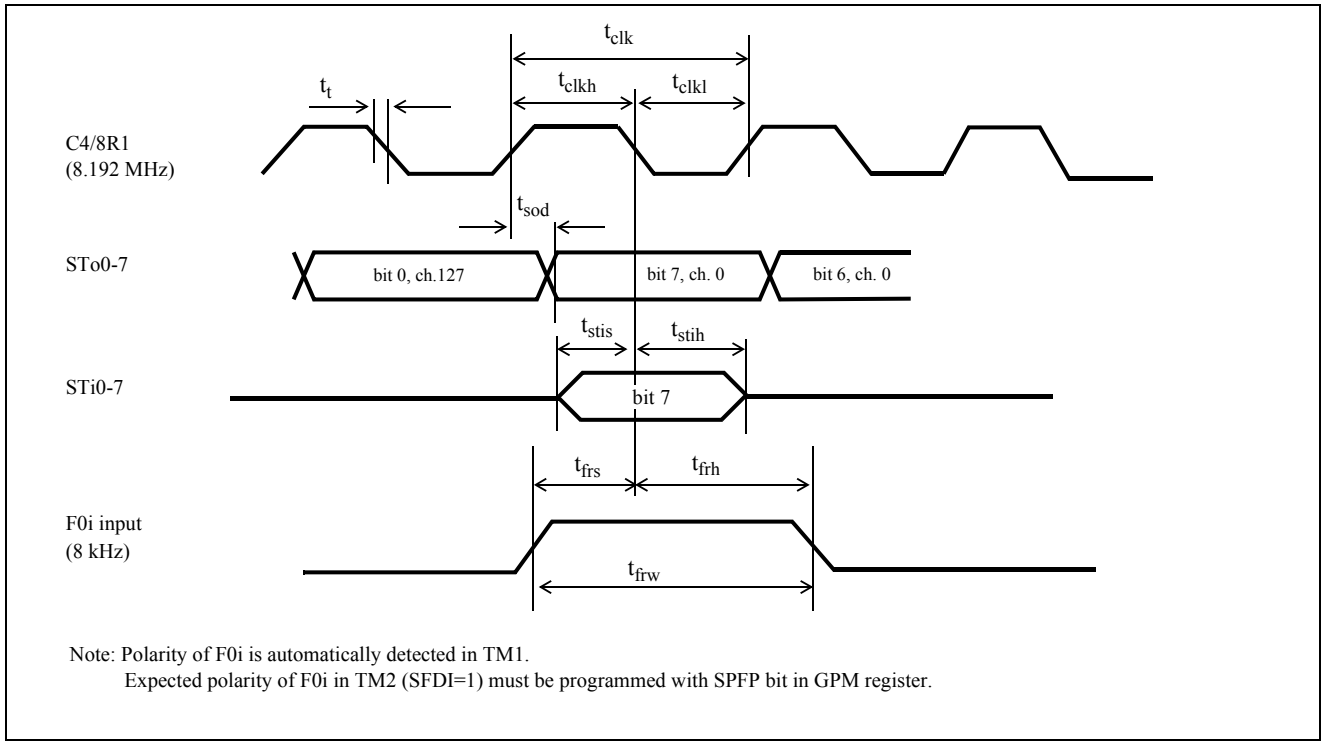


F0 Frame Sync with Negative Polarity (SPFP = 0)



F0 Frame Sync with Positive Polarity (SPFP = 1)

Figure 21 - Serial Port Timing for 4.096 Mbps Operation - TM2 (SFDi = 0) and TM3



Note: Polarity of F0i is automatically detected in TM1.
Expected polarity of F0i in TM2 (SFDI=1) must be programmed with SPFP bit in GPM register.

Figure 22 - Serial Port Timing for 8.192 Mbps - TM1 and TM2 (SFDi = 1)

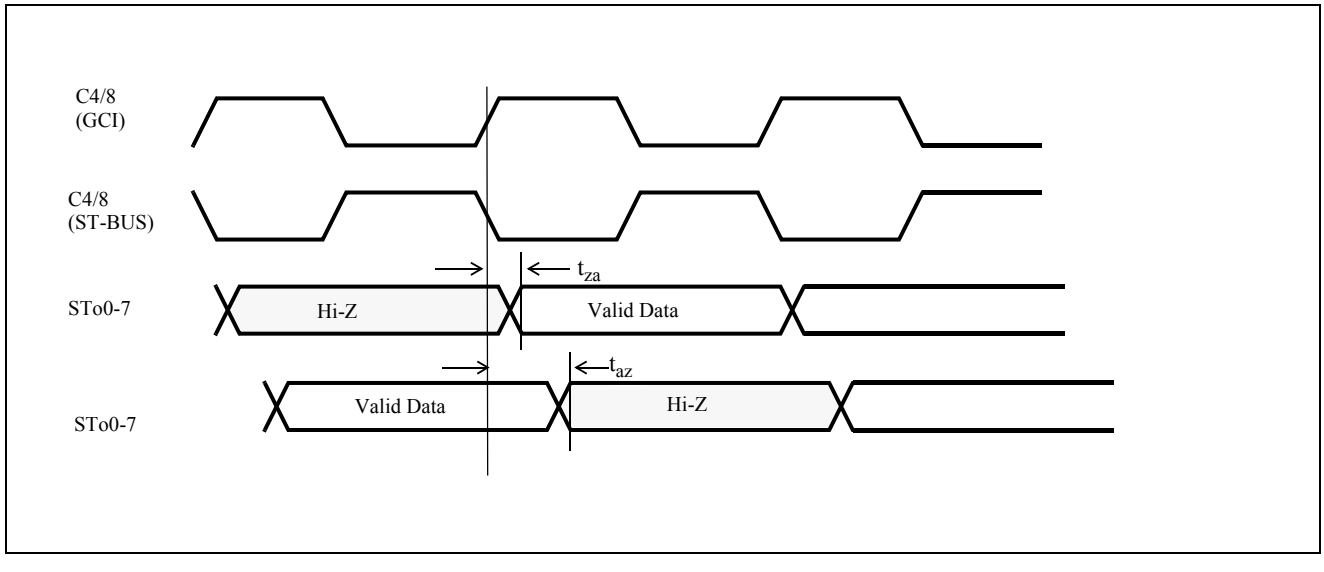
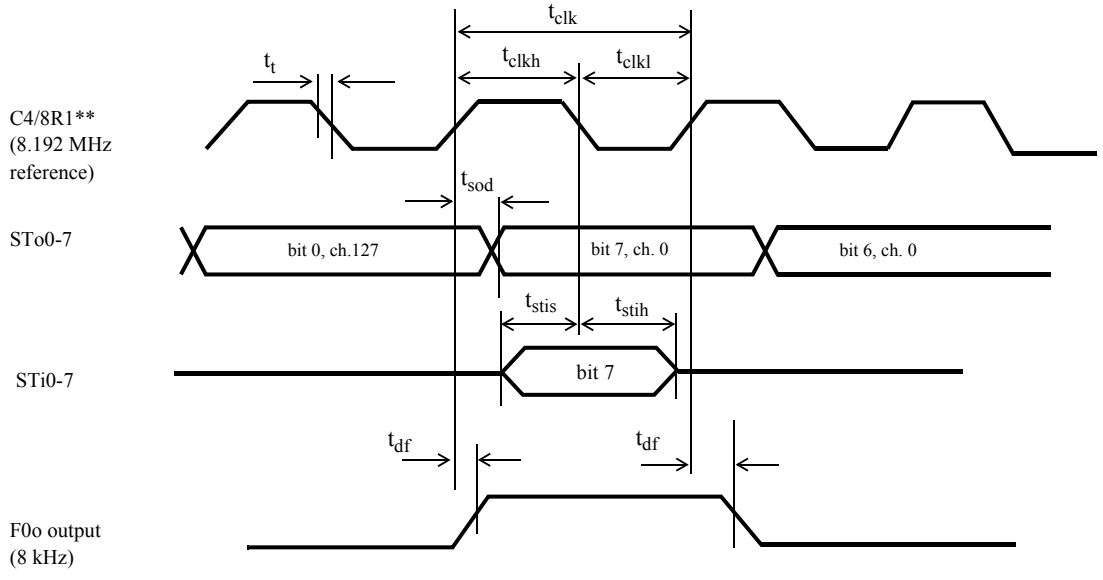
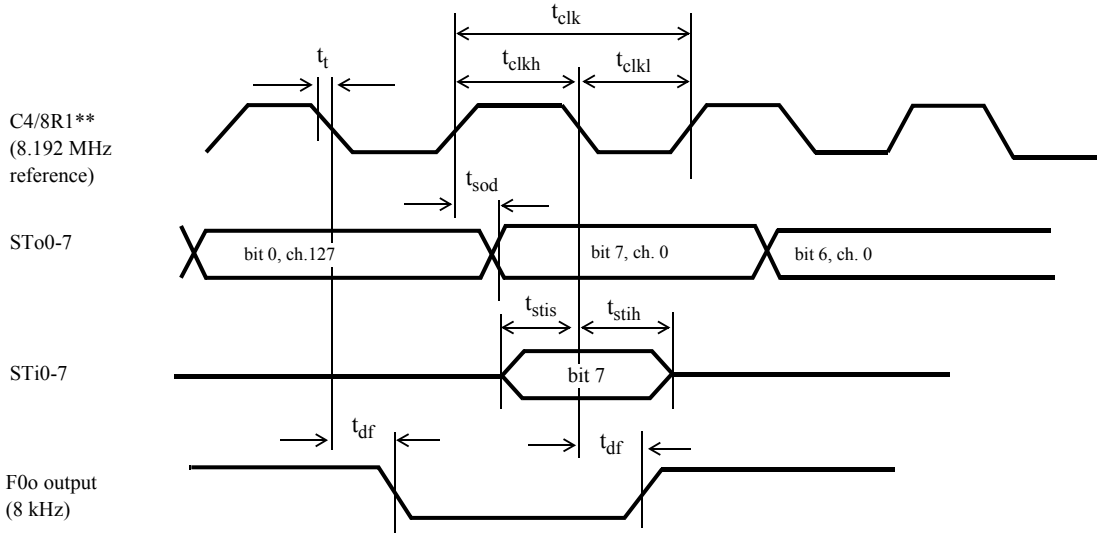


Figure 23 - Per-Channel Tristate Characteristics at all Data Rates



Frame Sync with Positive Polarity (SPFP = 1)



Frame Sync with Negative Polarity (SPFP = 0)

** In TM2 and TM3 operation at 8.192 Mbps, the F0 output signal is clocked by the C4/8R1 input reference provided by the user. (In 8.192 Mbps applications, the SPCKo output signal is not used.)

Figure 24 - Serial Port Timing for 8.192 Mbps - Timing Modes 2 and 3

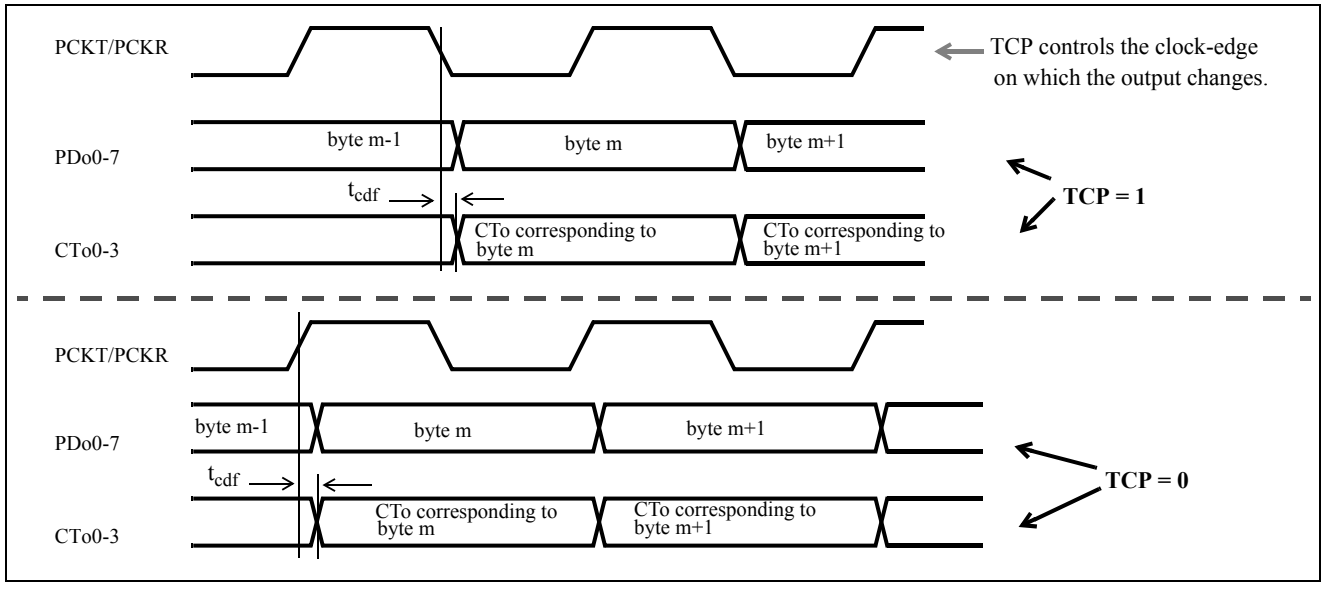


Figure 25 - Timing for the Parallel Port External Control Lines CTo0-3

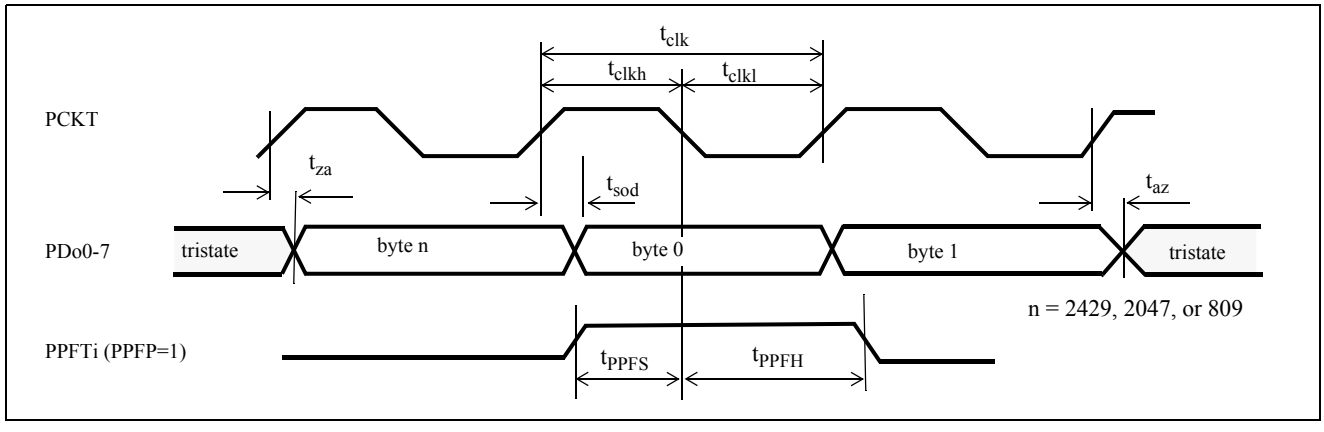
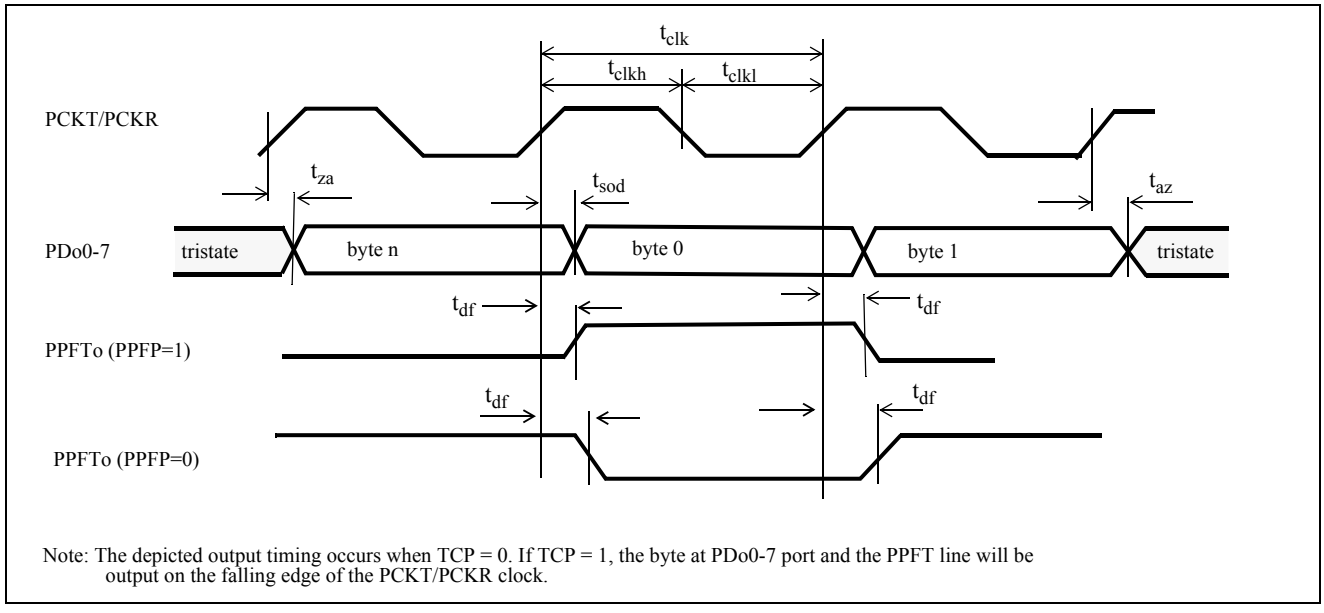


Figure 26 - TM1 Parallel Port Transmit Timing (TM1 & PFDI = 1, PPFT is an input)



Note: The depicted output timing occurs when TCP = 0. If TCP = 1, the byte at PDo0-7 port and the PPFT line will be output on the falling edge of the PCKT/PCKR clock.

Figure 27 - Parallel Port Transmit Timing (PFDI = 0, PPFT is an output)

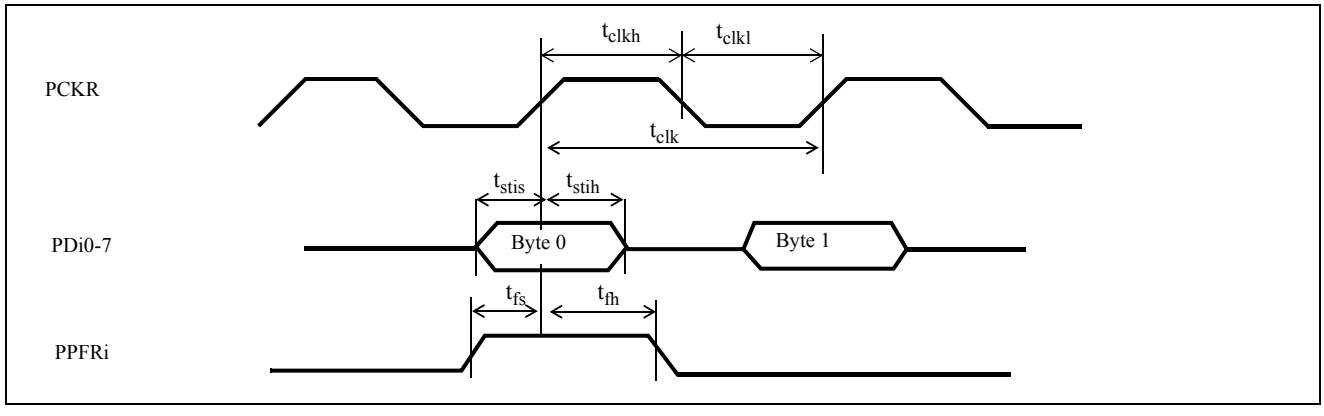
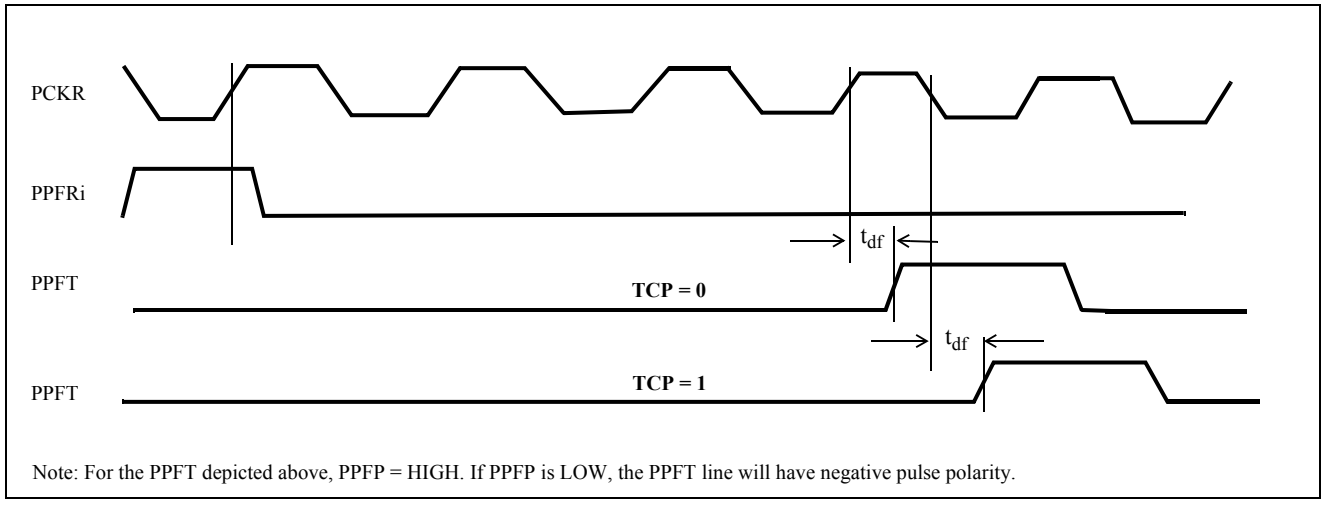


Figure 28 - Parallel Port Receive Timing

AC Electrical Characteristics - Parallel Data Port

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions
1	PCKT/PCKR clock period	t_{clk}	50			ns	
2	PCKT/PCKR HIGH time	t_{clkh}	20			ns	
3	PCKT/PCKR LOW time	t_{clkl}	20			ns	
4	PPFTo output delay from PCKR/PCKT transmit edge	t_{df}			28 30	ns	C_L=30pF C_L=50pF
5	PDo output delay from PCKR/PCKT transmit edge	t_{sod}			28 30	ns	C_L=30pF C_L=50pF
6	CTo0-3 output delay from PCKR/PCKT transmit edge	t_{cdf}			26 28	ns	C_L=30pF C_L=50pF
7	PDo delay from Active to High-Z	t_{za}			26	ns	C_L=30pF, R_L=1K
8	PDo delay from High-Z to Active	t_{az}			28	ns	C_L=30pF, R_L=1K
9	PPFRi Setup Time from PCKR sampling edge	t_{frs}	5			ns	
10	PPFRi Hold Time from PCKR sampling edge	t_{frh}	8			ns	
11	PDi Set-up Time from PCKR sampling edge	t_{stis}	5			ns	
12	PDi Hold Time from PCKR sampling edge	t_{stih}	8			ns	
13	PPFTi Input Setup Time from PCKT sampling edge	t_{ppfs}	5			ns	TM1, PFDI = 1
14	PPFTi Input Hold Time from PCKT sampling edge	t_{ppfh}	5			ns	TM1, PFDI = 1
15	Jitter between PCKT/PCKR and C4 serial port clock.	t_{pv}	-100		+100	ns	C4/8R1 or C4/8R2 at 4.096 MHz with 50% duty cycle

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.



Note: For the PPFT depicted above, PPFP = HIGH. If PPFP is LOW, the PPFT line will have negative pulse polarity.

Figure 29 - Parallel Port in Timing Mode 4

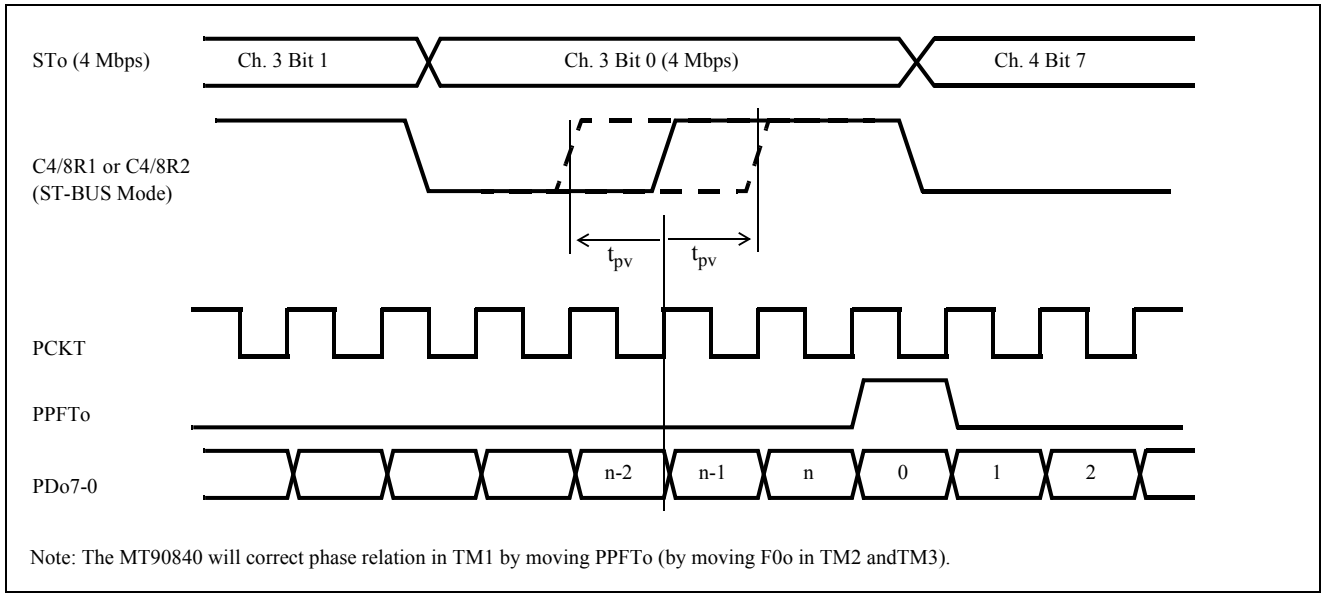


Figure 30 - Phase Variation Between C4/8R1 & C4/8R2 and PCKT Inputs for TM1 Operation

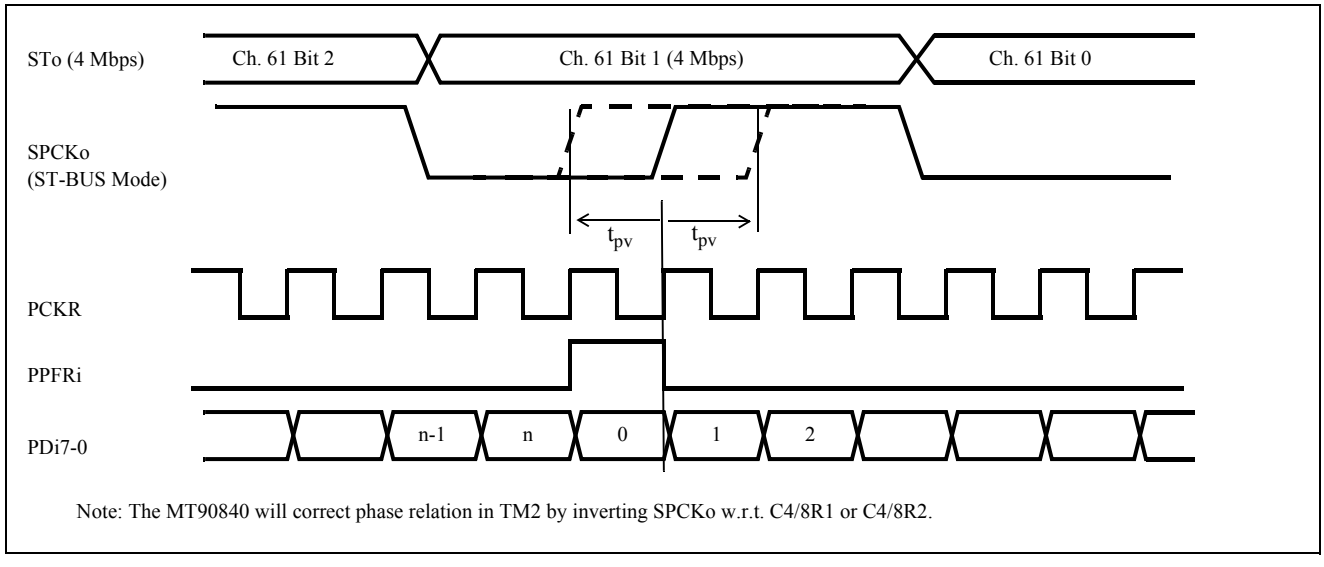


Figure 31 - Phase Variation Between C4 and PCKR Inputs for TM2 Operation

AC Electrical Characteristics† - Intel/National- HPC Multiplexed Bus Mode - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions/Notes
1	ALE pulse width	t_{alw}	10			ns	
2	Address setup from ALE falling	t_{ads}	5			ns	
3	Address hold from ALE falling	t_{adh}	5			ns	
4	$\overline{RD}$ Active after ALE falling	t_{alrd}	15			ns	
5	Data setup from $\overline{DTA}$ LOW on read	t_{ddr}	0			ns	C_L=150 pF on $\overline{DTA}$, and 30 pF on AD0-7.
6	$\overline{CS}$ hold after $\overline{RD}$/$\overline{WR}$	t_{csrw}	0			ns	
7	$\overline{CS}$ setup from $\overline{RD}$	t_{csr}	0			ns	
8	Data hold after $\overline{RD}$	t_{dhr}	10 15		22 30	ns ns	C_L=30 pF C_L=150 pF
9	$\overline{WR}$ delay after ALE falling	t_{alwr}	15			ns	
10	$\overline{CS}$ setup from $\overline{WR}$	t_{csw}	0			ns	
11	Data setup from $\overline{WR}$	t_{dsw}	10			ns	
12	Data hold after $\overline{WR}$ Inactive	t_{dhw}	0			ns	
13	$\overline{RD}$/$\overline{WR}$ Inactive to ALE Falling Edge	t_{rst}	23			ns	
14	Acknowledgment hold time	t_{akh}	0		20	ns	C_L=150 pF, R_L=1kΩ*
15	Data Delay on Reading Registers	t_{rdd}			47 68	ns ns	C_L=30 pF C_L=150 pF
16	Acknowledgment Delay Reading Registers	t_{akd-rd}			73 85	ns ns	C_L=30 pF C_L=150 pF
	Acknowledgment Delay Writing Registers	t_{akd-wr}			32 41	ns ns	C_L=30 pF C_L=150 pF
17	Acknowledgment Delay - Memories:	$t_{akd-mem}$					
	Reading TP Data Memory		244	488	1306	ns	1 to 5 C4 cycles + register t_{akd-rd}
	Reading RP Data Memory		122	366	1062	ns	.5 to 4 C4 cycles + register t_{akd-rd}
	Reading TP Connection Memory		1 clock cycle	2 clock cycles	3 clk cyc + t_{akd-rd}		1 to 3 PCKT/R cycles + register t_{akd-rd}
	Reading RP Connection Memory		244	488	817	ns	1 to 3 C4 cycles + register t_{akd-rd}
	Writing TP Connection Memory**		t_{akd-wr}		3 clk cyc + t_{akd-wr}		Up to 3 PCKT/R cyc. + register t_{akd-wr}
	Writing RP Connection Memory**		t_{akd-wr}		774	ns	Up to 3 C4 cycles + register t_{akd-wr}

† Timing is over recommended temperature & power supply voltages.
‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.
* High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.
** Individual writes to Connection Memories will have Register Acknowledgment Delay. Burst writes to Connection Memories will have Read Connection Memory Acknowledgment Delay.

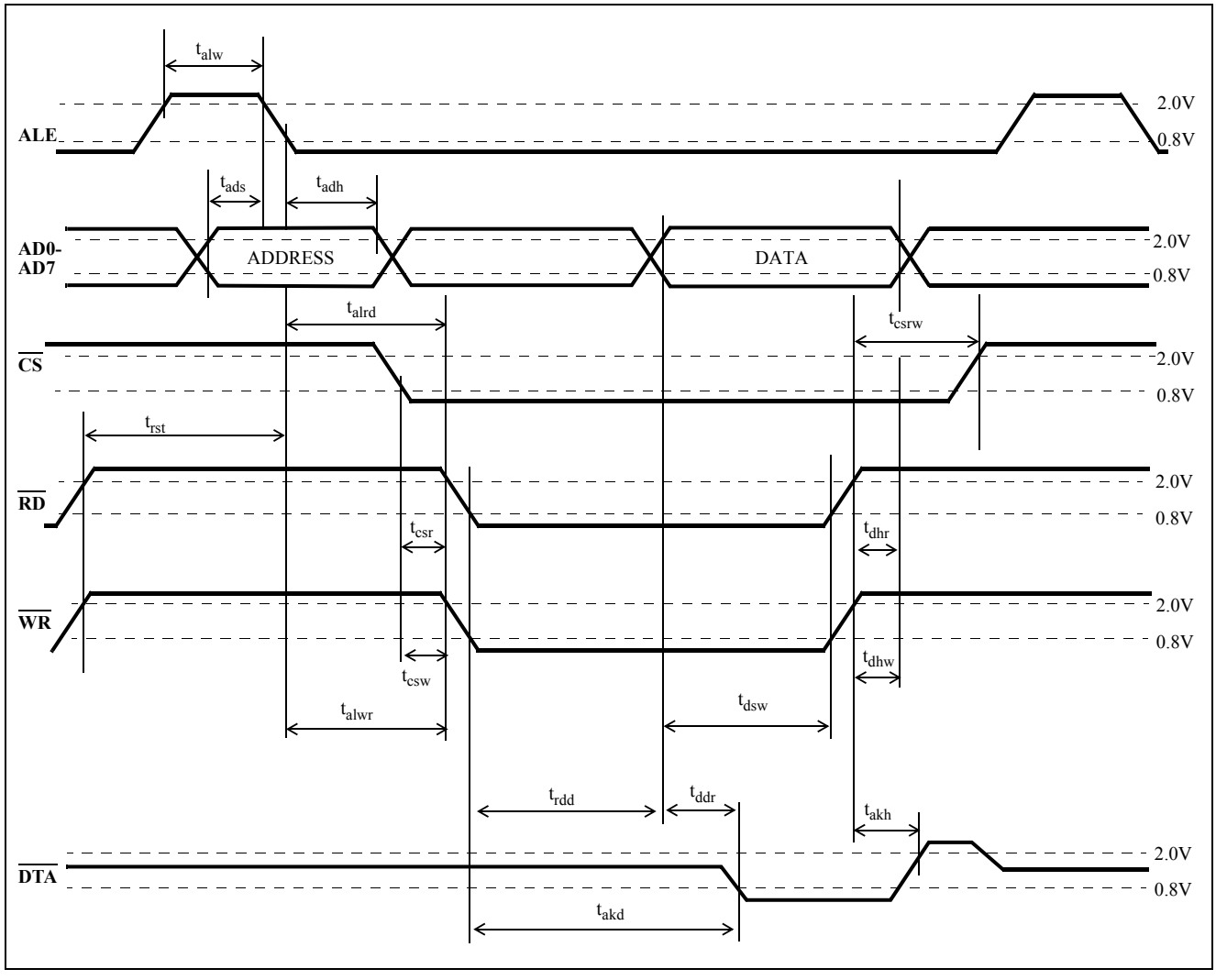


Figure 32 - Intel/National Multiplexed Bus Timing

AC Electrical Characteristics† - Motorola Multiplexed Bus Mode - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions/Notes
1	AS pulse width	t_{asw}	10			ns	
2	Address setup from AS falling	t_{ads}	5			ns	
3	Address hold from AS falling	t_{adh}	5			ns	
4	Data setup from $\overline{DTA}$ LOW on read	t_{ddr}	0			ns	C_L=150 pF on $\overline{DTA}$, 30 pF on AD0-7.
5	$\overline{CS}$ hold after DS falling	t_{csh}	0			ns	
6	$\overline{CS}$ setup from DS rising	t_{css}	0			ns	
7	Data setup on write	t_{dsw}	10				
8	Data hold after write	t_{dhw}	0			ns	
9	DS Inactive to AS Falling Edge	t_{dss}	23			ns	
10	R/$\overline{W}$ setup from DS rising	t_{rws}	5			ns	
11	R/$\overline{W}$ hold after DS falling	t_{rwh}	5			ns	
12	Data hold after read	t_{dhr}	10 15		22 30	ns ns	C_L=30 pF C_L=150 pF
13	DS delay after AS falling	t_{dsh}	15			ns	
14	Acknowledgment hold time	t_{akh}	0		20	ns	C_L=150 pF, R_L=1kW*
15	Acknowledgment Delay: Writing Registers Acknowledgment Delay: Reading Registers	t_{akd-wr} t_{akd-rd}			32 41 73 85	ns ns ns ns	C_L=30 pF C_L=150 pF C_L=30 pF C_L=150 pF

AC Electrical Characteristics† - Motorola Multiplexed Bus Mode - Voltages are with respect to ground (V_{SS}) unless otherwise stated.

	Characteristics	Sym.	Min.	Typ.‡	Max.	Units	Test Conditions/Notes
16	Memory Acknowledgment Delay	$t_{akd-mem}$					
	Reading TP Data Memory		244	488	1306	ns	1 to 5 C4 cycles + register t_{akd-rd}
	Reading RP Data Memory		122	366	1062	ns	.5 to 4 C4 cycles + register t_{akd-rd}
	Reading TP Connection Memory		1 clock cycle	2 clock cycles	3 clk cyc + t_{akd-rd}		1 to 3 PCKT/R cycles + register t_{akd-rd}
	Reading RP Connection Memory		244	488	817	ns	1 to 3 C4 cycles + register t_{akd-rd}
	Writing TP Connection Memory**		t_{akd-wr}		3 clk cyc + t_{akd-wr}		Up to 3 PCKT/R cyc. + register t_{akd-wr}
	Writing RP Connection Memory**		t_{akd-wr}		774	ns	Up to 3 C4 cycles + register t_{akd-wr}

† Timing is over recommended temperature & power supply voltages.

‡ Typical figures are at 25°C and are for design aid only: not guaranteed and not subject to production testing.

* High Impedance is measured by pulling to the appropriate rail with R_L, with timing corrected to cancel time taken to discharge C_L.

** Individual writes to Connection Memories will have Register Acknowledgment Delay. Burst writes to Connection Memories will have Read Connection Memory Acknowledgment Delay.

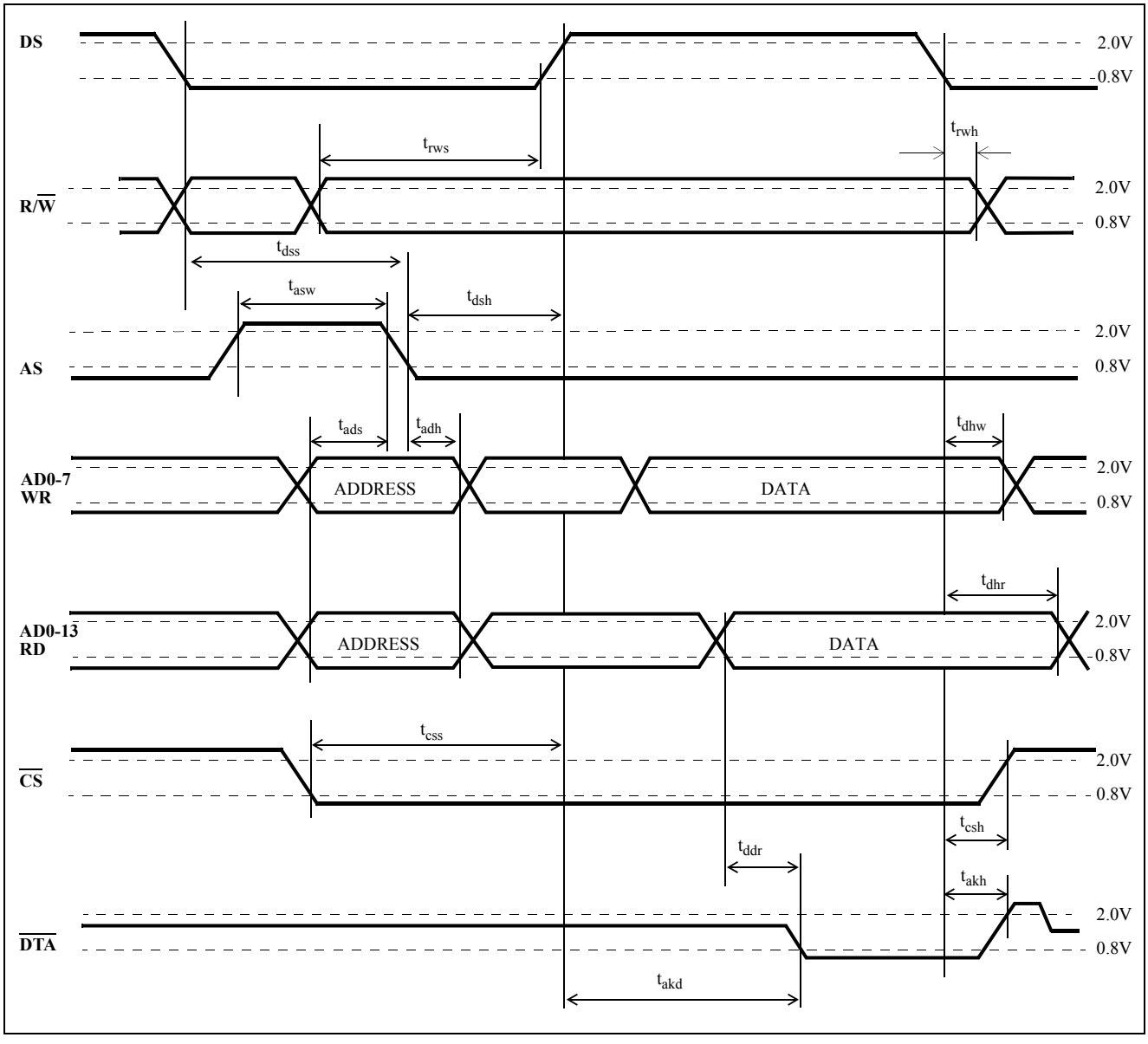


Figure 33 - Motorola Multiplexed Bus Timing

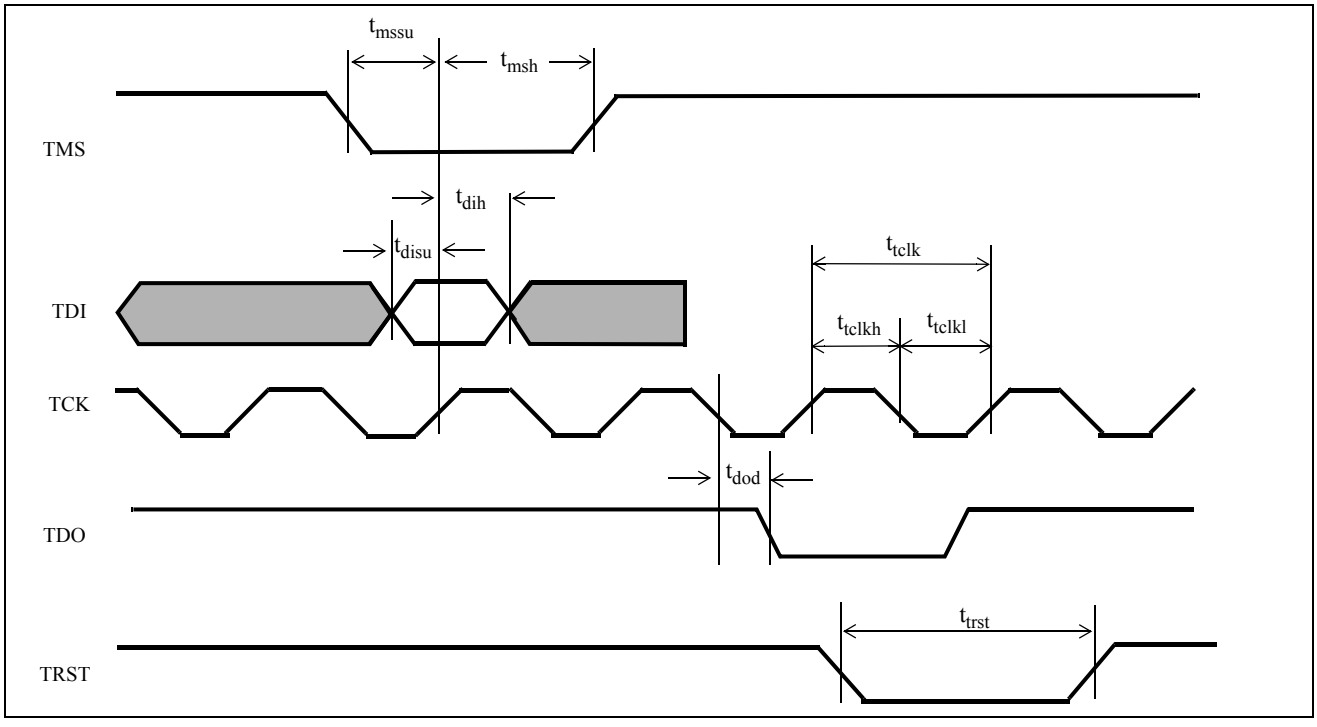


Figure 34 - Boundary Scan Test Port Timing

AC Electrical Characteristics - Boundary-Scan Test Port and RESET Pin

	Parameter	Symbol	Min.	Max.	Units	Test Conditions
1	TCK period width	t_{tclk}	100		ns	
2	TCK period width LOW	t_{tclkl}	40		ns	
3	TCK period width HIGH	t_{tclkh}	40		ns	
4	TDI setup time to TCK rising	t_{disu}	2		ns	
5	TDI hold time after TCK rising	t_{dih}	33		ns	
6	TMS setup time to TCK rising	t_{mssu}	2		ns	
7	TMS hold time after TCK rising	t_{msh}	5		ns	
8	TDO delay from TCK falling	t_{dod}		20	ns	C_L = 30 pF
9	$\overline{\text{TRST}}$ pulse width	t_{trst}	15		ns	
10	RESET pulse width	t_{rst}	15		ns	

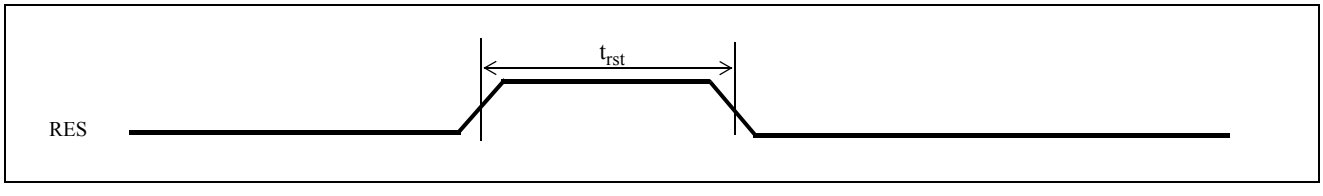
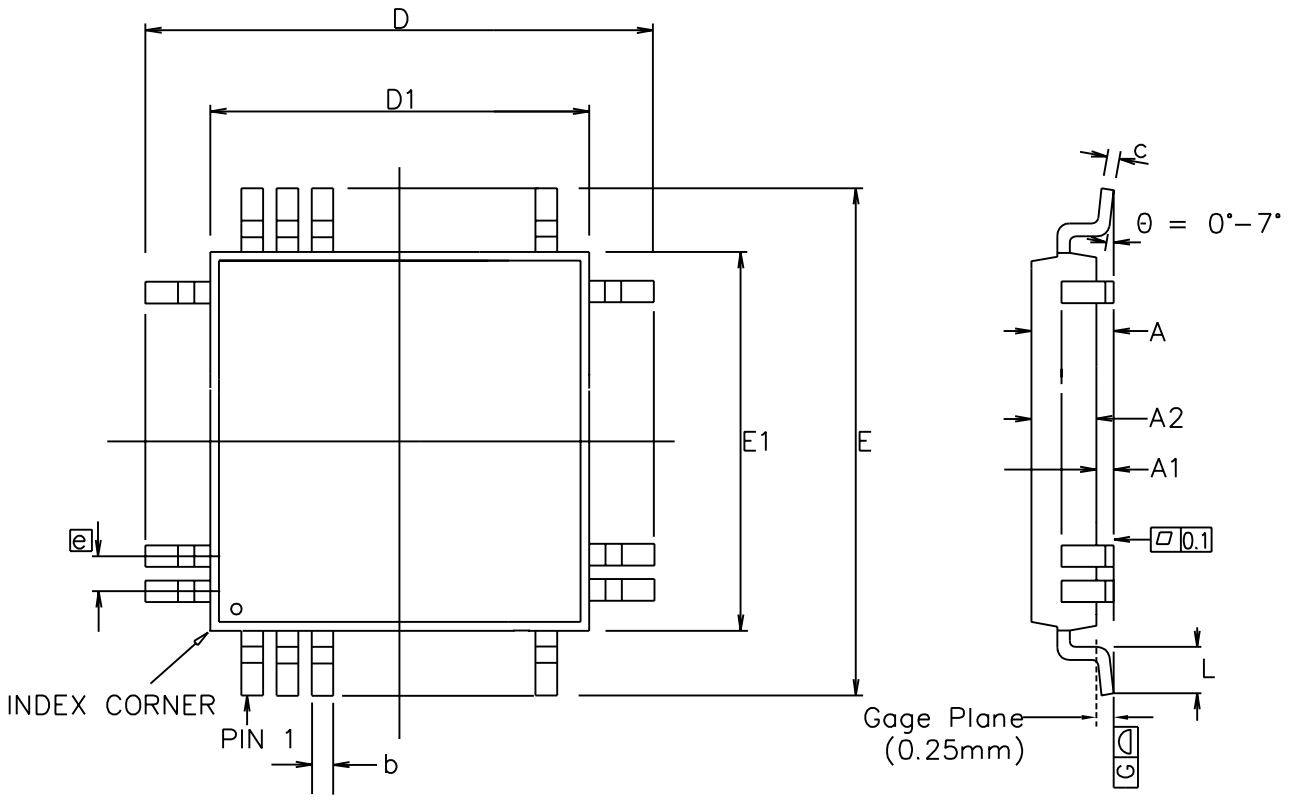


Figure 35 - RESET Timing



Symbol	Control Dimensions in millimetres			Altern. Dimensions in inches	
	MIN	MAX		MIN	MAX
A	– – –	3.40		– – –	0.134
A1	0.25	– – –		0.010	– – –
A2	2.55	3.05		0.100	0.120
D	23.90 BSC			0.941 BSC	
D1	20.00 BSC			0.787 BSC	
E	17.90 BSC			0.705 BSC	
E1	14.00 BSC			0.551 BSC	
L	0.73	1.03		0.029	0.041
e	0.65 BSC			0.026 BSC	
b	0.22	0.38		0.009	0.015
c	0.11	0.23		0.004	0.009
	Pin features				
N	100				
ND	30				
NE	20				
NOTE	RECTANGULAR				

Conforms to JEDEC MO-112 CC-1 Iss. B

Notes:
1. Pin 1 indicator may be a corner chamfer, dot or both.
2. Controlling dimensions are in millimeters.
3. The top package body size may be smaller than the bottom package body size by a max. of 0.15 mm.
4. Dimension D1 and E1 do not include mould protusion.
5. Dimension b does not include dambar prorusion.
6. Coplanarity, measured at seating plane G, to be 0.10 mm max.

This drawing supersedes 418/ED/51210/005 (Swindon)

ISSUE	2	3	4	5
ACN	203201	204759	207063	212834
DATE	20Oct97	24Jun98	1Jul99	21May02
APPRD.				

ZARLINK SEMICONDUCTOR

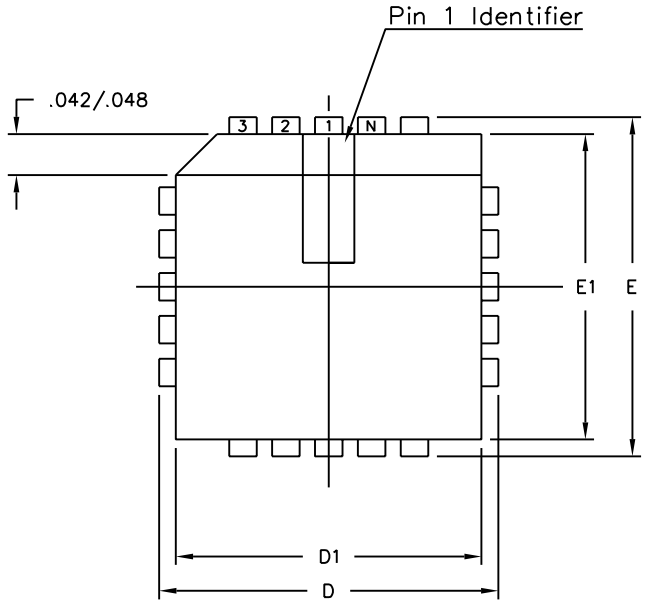
Previous package codes

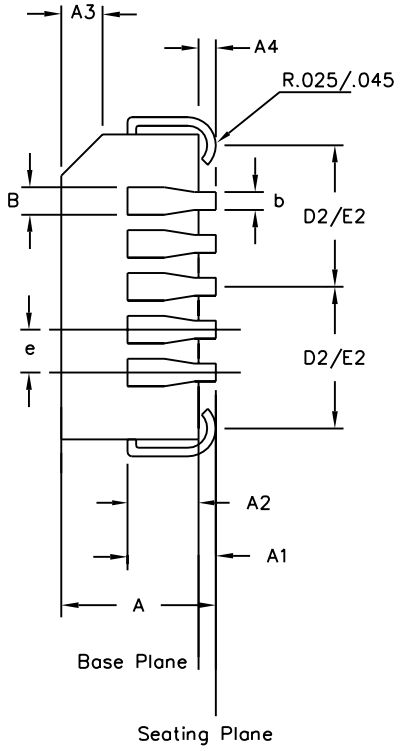
GP / L

Package Code QB

Package Outline for 100 lead MQFP (14 x 20 x 2.8mm) 3.9mm Footprint

GPD00241





Symbol	Control Dimensions in inches		Altern. Dimensions in millimetres	
	MIN	MAX	MIN	MAX
A	0.165	0.180	4.19	4.57
A1	0.090	0.120	2.29	3.05
A2	0.059	0.080	1.57	2.11
A3	0.042	0.056	1.07	1.42
A4	0.020	–	0.51	–
D	1.185	1.195	30.10	30.35
D1	1.150	1.158	29.21	29.41
D2	0.541	0.569	13.74	14.45
E	1.185	1.195	30.10	30.35
E1	1.150	1.158	29.21	29.41
E2	0.541	0.569	13.74	14.45
B	0.026	0.032	0.66	0.81
b	0.013	0.021	0.33	0.53
e	0.050 BSC		1.27 BSC	
	Pin features			
ND	21			
NE	21			
N	84			
Note	Square			
Conforms to JEDEC MS-018AF Iss. A				

Notes:
1. All dimensions and tolerances conform to ANSI Y14.5M–1982
2. Dimensions D1 and E1 do not include mould protrusions. Allowable mould protrusion is 0.010" per side. Dimensions D1 and E1 include mould protrusion mismatch and are determined at the parting line, that is D1 and E1 are measured at the extreme material condition at the upper or lower parting line.
3. Controlling dimensions in Inches.
4. "N" is the number of terminals.
5. Not To Scale
6. Dimension R required for 120° minimum bend.

ISSUE	1	2	3	
ACN	5958	207471	213096	
DATE	15Aug94	10Sep99	15Jul02	
APPRD.				

ZARLINK SEMICONDUCTOR

Previous package codes

HP / P

Package Code QA

Package Outline for 84 lead PLCC

GPD00006

For more information about all Zarlink products
visit our Web Site at

www.zarlink.com

TECHNICAL DOCUMENTATION - NOT FOR RESALE