Preliminary Data Sheet, DS1, July 2002

SLIC-S/-S2

Subscriber Line Interface Circuit Standard Feature Set

PEB 4264 Version 1.2

PEB 4264-2 Version 1.2

Wired
Communications

Never stop thinking.

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Page	Subjects (major changes since last revision)

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Preface

This document describes the High Voltage Subscriber Line Interface Circuit Standard Feature Set PEB 4264/-2 (SLIC-S/-S2) which is part of the DuSLIC and VINETIC chip set family.
For more DuSLIC or VINETIC related documents please see our webpages at http://www.infineon.com/duslic or http://www.infineon.com/vinetic.

Organization of this Document

This Preliminary Data Sheet is divided into six chapters. It is organized as follows:

- **Chapter 1**, **Overview**
  A general description of the product, its key features, and pin configuration.
- **Chapter 2**, **Functional Description**
  The main functions and operating modes are presented.
- **Chapter 3**, **Typical Application Circuit for DuSLIC and VINETIC**
  Application circuit including bill of material and protection.
- **Chapter 4**, **Electrical Characteristics**
  Parameters, symbols and limit values.
- **Chapter 5**, **Test Figures**
  Test figures including external components.
- **Chapter 6**, **Package Outlines**
  Illustrations and dimensions of the package outlines.

1 Overview

The High Voltage Subscriber Line Interface Circuit PEB 4264/-2 (SLIC-S/-S2) is a reliable interface between the telephone line and the codec devices of the DuSLIC or VINETIC chip sets. It is fabricated using Infineon Technologies proven Smart Power Technology SPT4.

The PEB 4264/-2 provides battery feeding between –15 V and –65 V and internal balanced ringing up to 45 Vrms. In order to achieve this, an auxiliary positive battery voltage is used during ringing to enhance the useable voltage range to 90 V.

The SLIC is designed for a voltage-feeding/current-sensing line interface concept and senses the transversal and longitudinal current.

To minimize system power dissipation, a power-down mode can be used; the SLIC-S/-S2 is switched off and the line outputs go to a high-impedance mode. Off-hook supervision is provided by activating a simple line current sensor with negligible power consumption.

For saving power in active mode an integrated switch enables the use of a lower battery voltage in short loop applications.

The PEB 4264/-2 is compatible with both 3.3 V and 5 V V_{DD} supplies.

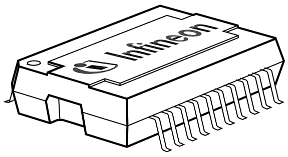
SLIC-S/-S2
Subscriber Line Interface Circuit Standard Feature Set

PEB 4264
PEB 4264-2

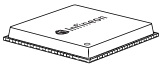
Version 1.2

1.1 Features

- High-voltage line feeding
- Two battery voltages (–15 V … –65 V)
- Integrated balanced ringing up to 45 Vrms
- Power-saving active mode (ACTL) with reduced battery voltage
- Sensing of transversal and longitudinal line currents
- Package options:
  - P-DSO-20-5
  - P-VQFN-48-4
- High longitudinal balance performance with PEB 4264-2
- Compatible with 3.3 V and 5 V V_{DD}
- Enables high packing densities on board



P-DSO-20-5



P-VQFN-48-4

Type	Package
SLIC-S/-S2	P-DSO-20-5 / P-VQFN-48-4

1.2 Logic Symbol

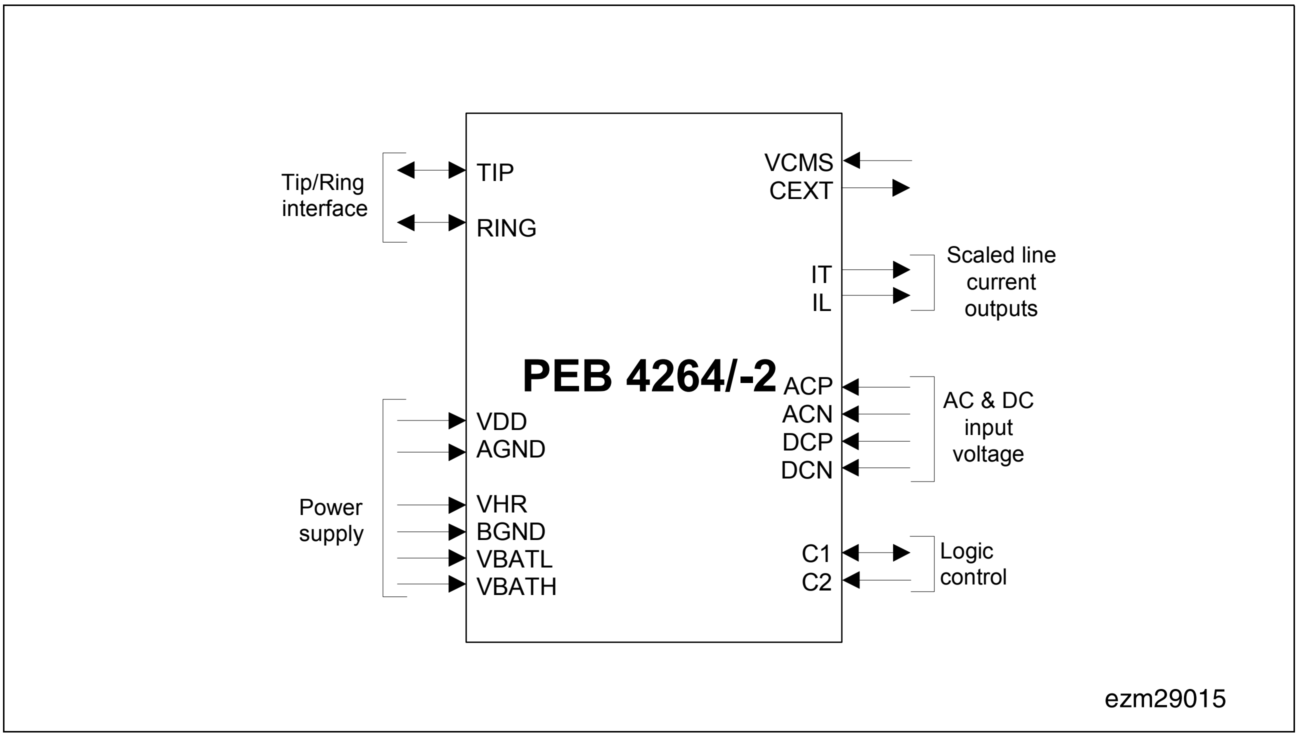


Figure 1 Logic Symbol

1.3 Pin Configuration

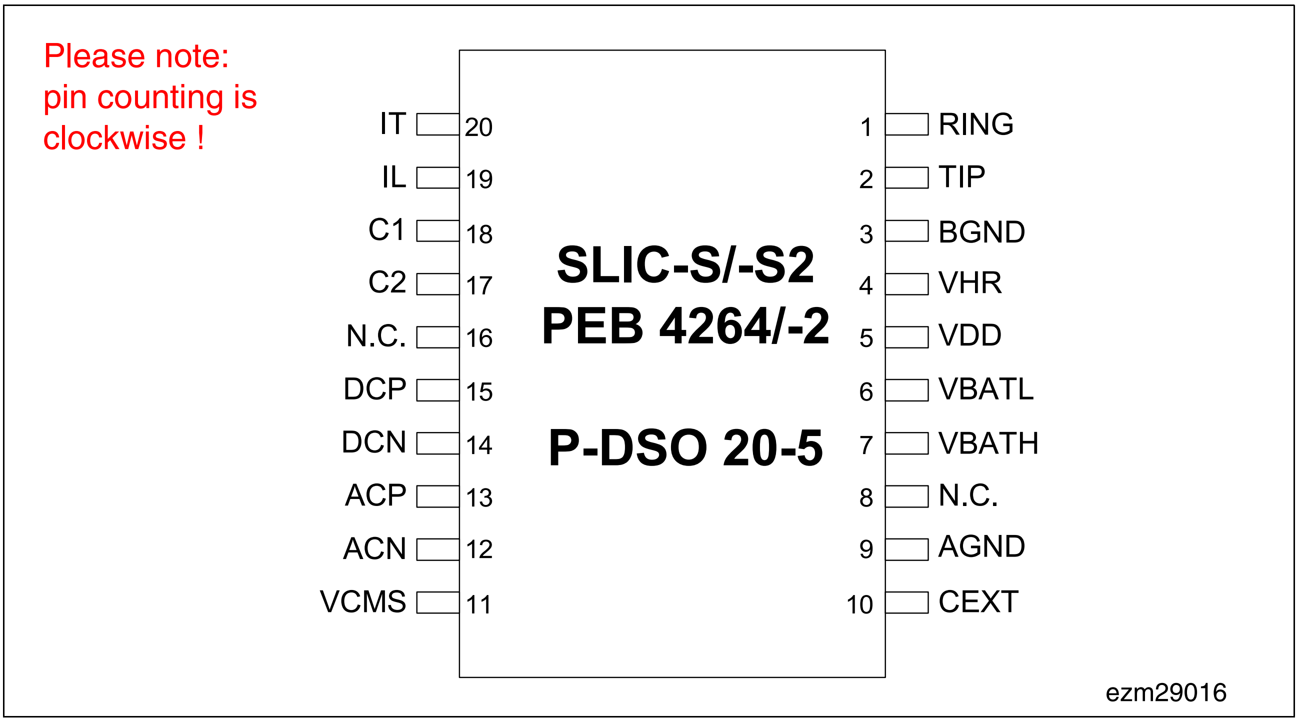


Figure 2 Pin Configuration P-DSO-20-5 Package (top view)

Note: The P-DSO-20-5 package is designed with heatsink on top. The pin counting for this package is clockwise (top view).

Attention: The heatsink (see Figure 20) is connected to VBATH via the chip substrate. Due to the high voltage of up to 90 V between VHR and VBATH, touching of the heatsink or any attached conducting part can be hazardous.

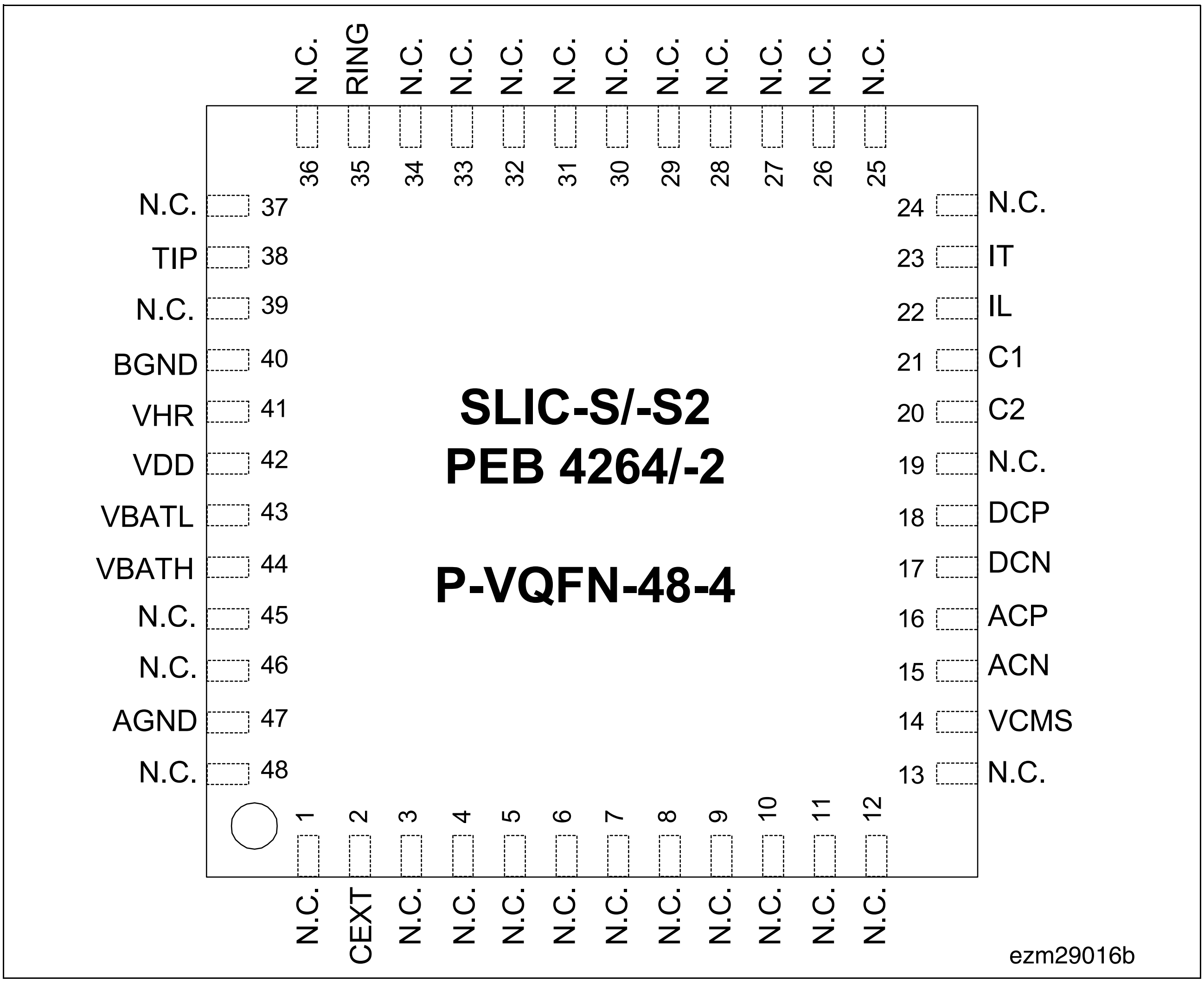


Figure 3 **Pin Configuration P-VQFN-48-4 Package** (top view)

Attention: The exposed die pad and die pad edges are connected to VBATH via the chip substrate. Due to the high voltage of up to 90 V between VHR and VBATH, touching of the die pad or any attached conducting part can be hazardous.

1.4 Pin Definitions and Functions SLIC-S/-S2

Table 1 Pin Definitions and Functions SLIC-S/-S2

Pin No.		Symbol	Input (I) Output (O)	Function
P-DSO -20-5	P-VQFN-48-4			
1	35	RING	I/O	Subscriber loop connection RING.
2	38	TIP	I/O	Subscriber loop connection TIP.
3	40	BGND	Power	Battery ground: TIP, RING, V_{BATH}, V_{BATL} and V_{HR} refer to this pin.
4	41	VHR	Power	Auxiliary positive battery supply voltage ($5\ V \leq V_{HR} \leq 45\ V$) used in ringing mode.
5	42	VDD	Power	Positive supply voltage ($3.1\ V \leq V_{DD} \leq 5.5\ V$), referred to AGND.
6	43	VBATL	Power	Negative battery supply voltage ($-15\ V \geq V_{BATL} \geq V_{BATH}$)
7	44	VBATH	Power	Negative battery supply voltage ($-20\ V \geq V_{BATH} \geq -65\ V$)
9	47	AGND	Power	Analog ground: V_{DD}, and all signal and control pins with the exception of TIP and RING refer to AGND.
10	2	CEXT	O	Output of voltage divider defining DC line potentials; an external capacitance allows supply voltage filtering (output resistance 50 kΩ).
11	14	VCMS	I	Reference voltage for differential two wire interface of typically 1.5 V.
12, 13	15, 16	ACN, ACP	I	Differential two-wire AC input voltage; multiplied by –6 and related to $(V_{HI} + V_{BI})/2$[1), ACN appears at TIP and ACP at RING output, respectively.
14, 15	17, 18	DCN, DCP	I	Differential two-wire DC input voltage; multiplied by –30 (ACTH and ACTL mode) or –60 (ACTR mode) and related to $(V_{HI} + V_{BI})/2$[1), DCN appears at TIP and DCP at RING output, respectively.

Table 1 Pin Definitions and Functions SLIC-S/-S2 (cont'd)

Pin No.		Symbol	Input (I) Output (O)	Function
P-DSO -20-5	P-VQFN-48-4			
17	20	C2	I	Ternary logic input, controlling the operation mode.
18	21	C1	I/O	Ternary logic input, controlling the operation mode; in case of thermal overload (chip temperature exceeding 165 °C), this pin sinks a current of typically 150 μA.
19	22	IL	O	Current output: longitudinal line current scaled down by a factor of 100.
20	23	IT	O	Current output: transversal line current scaled down by a factor of 50.
8, 16	[2]	N.C.		Not connected.

[1] V_{HI} is the output voltage of the positive battery switch,
V_{BI} is the output voltage of the negative battery switch (see **Figure 4**).

[2] For the P-VQFN-48-4 the following pins are not connected: 1, 3, 4, 5, 6, 7, 8, 9, 10, 11, 12, 13, 24, 25, 26, 27, 28, 29, 30, 31, 32, 33, 34, 36, 37, 39, 45, 46, 48.

1.5 Functional Block Diagram

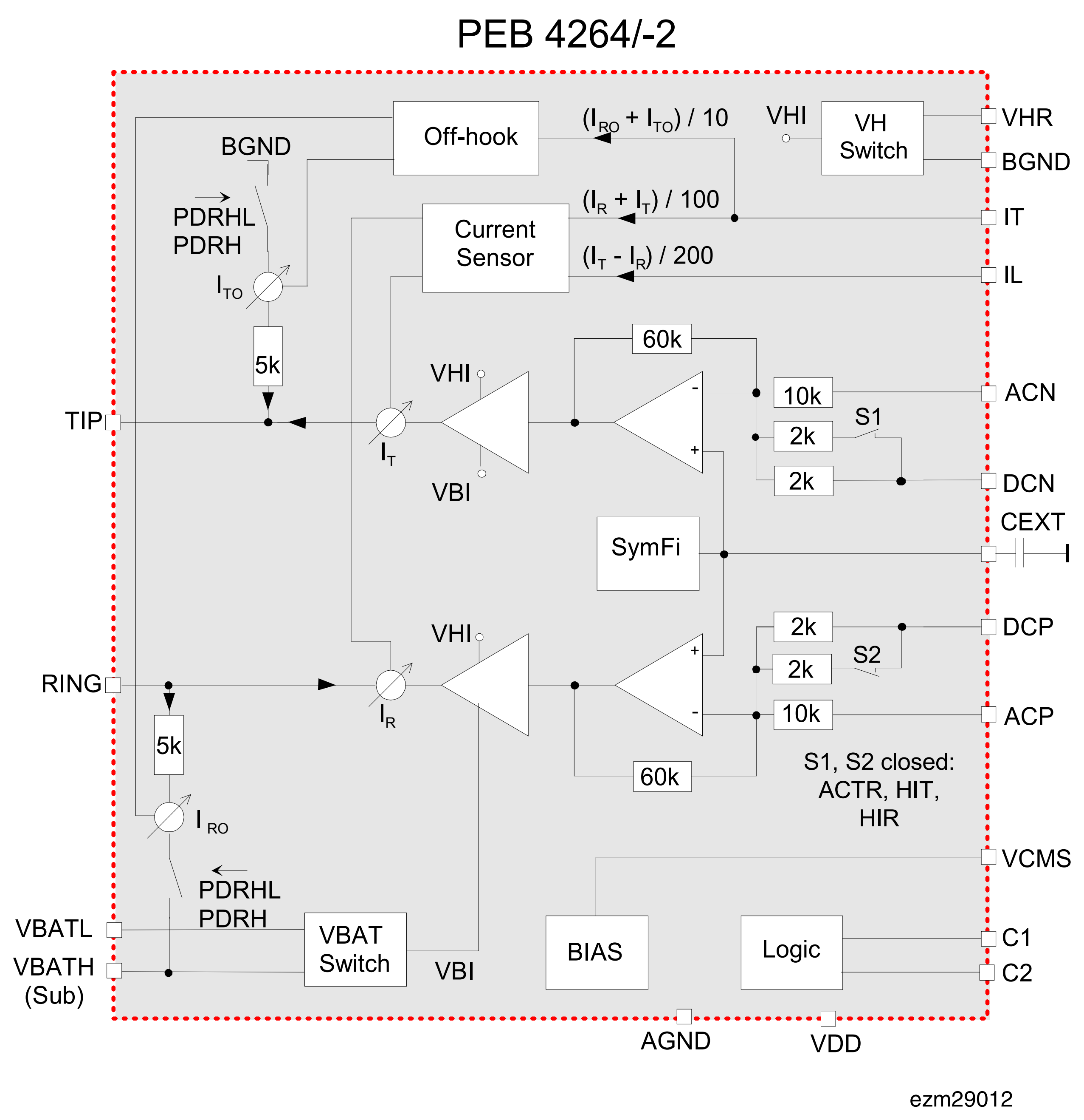


Figure 4 Block Diagram

2 Functional Description

The PEB 4264/-2 supports AC and DC control loops based on feeding a voltage V_{TR} to the line and sensing the transversal line current I_{Trans} and the longitudinal current I_{Long} (**Figure 5**).

In receive direction DC and AC voltages are handled separately with different gains on the SLIC-S/-S2. Both are applied differentially via pins DCP and DCN or ACP and ACN, respectively.

The line voltages V_R and V_T are the amplified input voltages, related to the mean supply voltage $V_M = (V_{HI} + V_{BI})/2$. Depending on the operation mode, V_{HI} is switched either to V_{HR} or to BGND via the VH switch and V_{BI} is switched either to V_{BATL} or to V_{BATH} via the VBAT switch (see **Figure 4**).

In the active modes ACTH with $V_M = V_{BATH}/2$ and ACTL with $V_M = V_{BATL}/2$, the line voltages are given by

$$V_T = V_{TIP} = V_M - 30 \times (V_{DCN} - V_{CMS}) - 6 \times (V_{ACN} - V_{CMS})$$
$$V_R = V_{RING} = V_M - 30 \times (V_{DCP} - V_{CMS}) - 6 \times (V_{ACP} - V_{CMS}),$$

while in ringing mode ACTR with $V_M = [V_{HR} + V_{BATH}]/2$,

$$V_T = V_{TIP} = V_M - 60 \times (V_{DCN} - V_{CMS}) - 6 \times (V_{ACN} - V_{CMS})$$
$$V_R = V_{RING} = V_M - 60 \times (V_{DCP} - V_{CMS}) - 6 \times (V_{ACP} - V_{CMS})$$

The transversal line voltage $V_{TR} = V_T - V_R$ is simply related to the input voltages:

$V_{TR} = V_{TIP} - V_{RING} = V_{ab} =$

$= 30 \times (V_{DCP} - V_{DCN}) + 6 \times (V_{ACP} - V_{ACN})$ for mode ACTH, ACTL

$= 60 \times (V_{DCP} - V_{DCN}) + 6 \times (V_{ACP} - V_{ACN})$ for mode ACTR

A reversed polarity of V_{TR} is easily obtained by changing the sign of $(V_{DCP} - V_{DCN})$.

In transmit direction the transversal and longitudinal currents are measured and scaled images are provided at the IT and IL pin, respectively:

$I_{IT} = (I_T + I_R)/100 = I_{Trans}/50$	$I_{IL} = (I_T - I_R)/200 = I_{Long}/100$
$I_{Trans} = (I_T + I_R)/2$	$I_{Long} = (I_T - I_R)/2$

For off-hook detection, in PDRH mode 5 kΩ resistors are connected from TIP to BGND and from RING to VBATH, respectively.

The currents through these resistors, I_{T0} and I_{R0} are sensed, scaled and provided at the IT pin (see **Figure 4**):

$I_{IT0} = (I_{T0} + I_{R0})/10 = I_{TRANS0}/5$

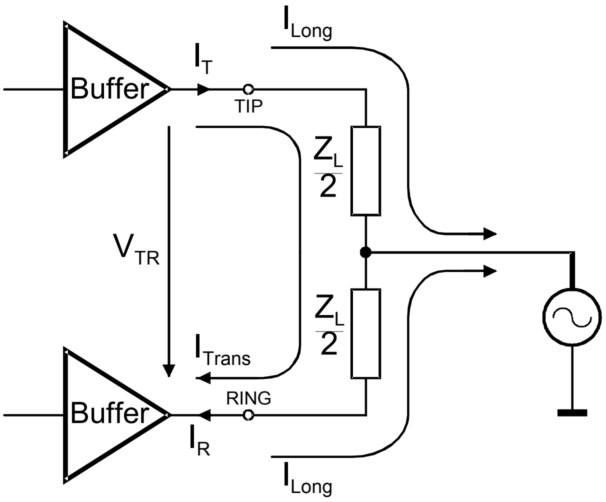


Figure 5 Definition of Output Current Directions

2.1 Operating Modes

The PEB 4264/-2 (SLIC-S/-S2) operates in the following modes controlled by ternary logic signals at the C1 and C2 inputs:

Table 2 SLIC-S/-S2 Interface Code

		C2		
		L	**M**	**H**
C1	**L**1)	PDH	PDRHL	PDRH
	M	ACTL	ACTH	ACTR
	H	HIRT	HIT	HIR

1) No ‘Overtemp’ signaling possible via pin C1 if C1 is low.

Table 3 SLIC-S/-S2 Modes

SLIC-S/-S2 Mode	**Mode Description**	**Internal Supply Voltages V_{BI}, V_{HI}**
PDH	Power Down High Impedance	(supply switches open)
PDRH	Power Down Resistive High	(supply switches open)
PDRHL	Power Down Resistive High Load	(supply switches open)
ACTL	Active Low	V_{BATL}, BGND
ACTH	Active High	V_{BATH}, BGND
ACTR	Active Ring	V_{BATH}, V_{HR}
HIRT	High Impedance on RING and TIP	V_{BATH}, V_{HR}
HIT	High Impedance on TIP	V_{BATH}, V_{HR}
HIR	High Impedance on RING	V_{BATH}, V_{HR}

Power Down High Impedance (PDH)

PDH offers high impedance at TIP and RING; it can be used for testing purposes or when an error condition occurs. In PDH mode all functions are switched off. Off-hook detection is not available.

Power Down Resistive High (PDRH)

Power consumption is reduced to a minimum by switching completely off all voice transmission functions. To allow off-hook detection, PDRH provides a connection of 5 kΩ each from TIP to BGND and RING to VBATH , respectively, while the output buffers show high impedance (see **Figure 4**). The current through these resistors is sensed and transferred to the IT pin for off-hook supervision.

Power Down Resistive High Load (PDRHL)

PDRHL is used as a transition state at a mode change from PDRH or PDH to ACTH mode (automatically initiated by the codec device at a mode change). It causes fast preloading of C_{EXT} in order to suppress line voltage transients.

Active Low (ACTL), Active High (ACTH)

These are the regular transmission modes for voiceband. The line-driving section is operated between V_{BATL} or V_{BATH} and BGND.

Active Ring (ACTR)

Utilizing an additional positive battery voltage V_{HR}, this mode allows balanced ringing of up to 45 Vrms or feeding of very long telephone lines.

High Impedance (HIR, HIT, HIRT)

In these modes each of the line outputs can be programmed to show high impedance. HIT switches off the TIP buffer, while HIR switches off the RING buffer. The current through the active buffer can still be measured by IT or IL. In the HIRT mode both buffers show high impedance. The current sensor remains active thus allowing sensor offset calibration (for test purposes).

2.2 Current Limitation / Overtemperature

In any operating mode (except Power Down) the total current delivered by the output drivers is limited to approximately 100 mA.

If, however, the chip temperature exceeds a threshold of typically 165 °C, this current limit is further reduced in order to keep temperature constant.

Besides, pin C1 sinks a signalling current I_{therm}. The temperature threshold for switching on I_{therm} depends on V_{DD}:

- if operated at 5 V, both signalling and current limit reduction start simultaneously
- at 3.3 V, the temperature threshold for signalling is about 5 - 10 °C higher than for the onset of current reduction.

3 Typical Application Circuit for DuSLIC and VINETIC

Figure 6 (**Figure 7**) shows one channel of an application circuit including a SLIC-S/-S2 and a SLICOFI-2/-2S or VINETIC-4VIP/-4M/-8M chip (for latest information please refer to the DuSLIC or VINETIC Data Sheet).

Table 4 shows the external passive components needed for a dual-channel solution as shown in **Figure 6** and **Figure 7**.

Table 4 External Components DuSLIC / VINETIC for 2 Channels

No.	Symbol	Value	Unit	Relat. Tol.	Rating	DuSLIC Systems	VINETIC Systems
2	R_{IT1}	470	Ω	1 %		x	
2	R_{IT1}	510	Ω	1 %			x
2	R_{IT2}	680	Ω	1 %		x	x
2	R_{IL}	1.6	kΩ	1 %		x	x
4	R_{STAB}	30	Ω	1 %[1]		x	x
4	R_{PROT}[2]	20 ... 50	Ω	1 %[1]		x	x
4	C_{STAB}	15 (typ.)	nF	10 %	100 V	x	x
2	C_{DC}	120	nF	10 %	10 V	x	
2	C_{DC}	220	nF	10 %	10 V		x
2	C_{ITAC}	680	nF	10 %	10 V	x	
2	C_{ITAC}	1	µF	10 %	10 V		x
1	C_{PRE}[3]	18	nF	5 %	10 V		x
2	C_{VCMIT}	680	nF	10 %	10 V	x	
1	C_{REF}	68	nF	20 %	10 V	x	x
2	C_{EXT}	470	nF	20 %	10 V	x	x
12	C_1	typ. 100	nF	10 %		x	x
1	C_2	4.7	µF	20 %	10 V, Tantal	x	
2	D_1	BAS 21	–	–	–	x	x
4	D_2	BAS 21	–	–	–	x	x
2	U_1[2]	Overvoltage Protection Element	–	–	–	x	x

[1] Matching tolerance dependent on longitudinal balance requirements (for details see the Application Note *External Components*).

[2] See Application Note *Protection of DuSLIC / VINETIC Linecard Chip Sets against Overvoltages and Overcurrents*.

[3] C_{PRE} is only necessary when TTX (12 or 16 kHz metering) is used.

Typical Application Circuit for DuSLIC and VINETIC

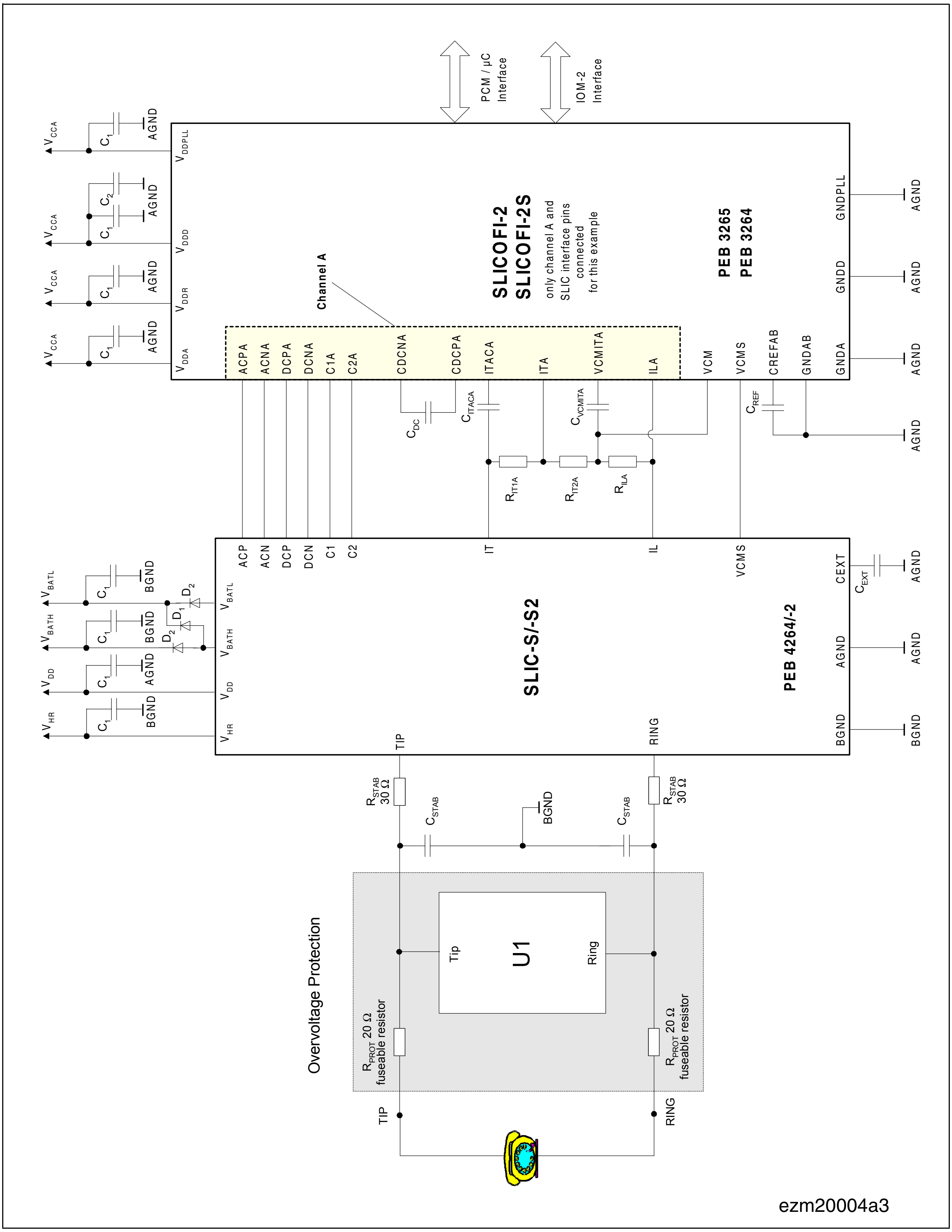


Figure 6 Application Circuit DuSLIC

Typical Application Circuit for DuSLIC and VINETIC

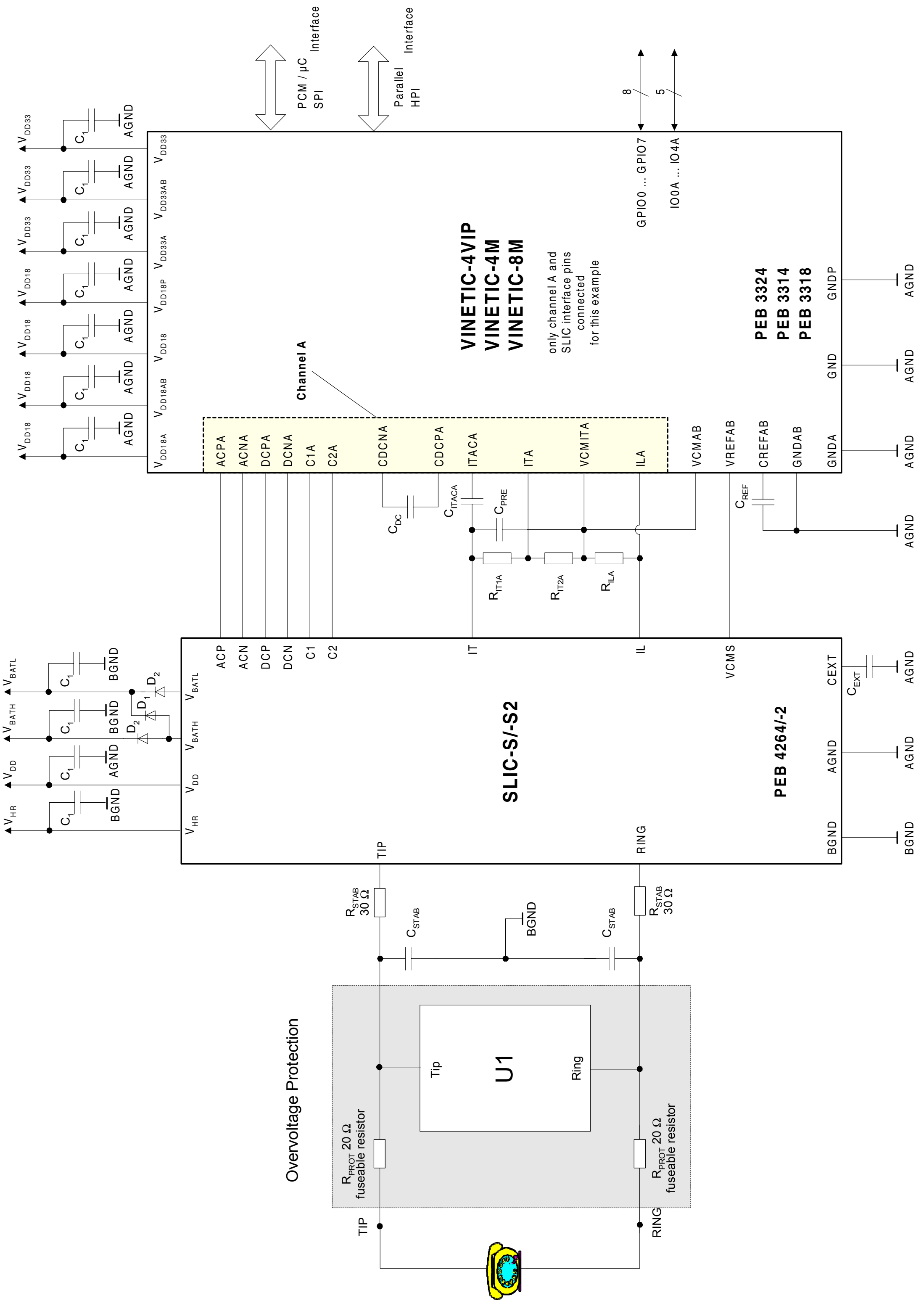


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Figure 7 Application Circuit VINETIC

4 Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 5 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Battery voltage low	V_{BATL}	–65	0.4	V	Referred to BGND
Battery voltage high	V_{BATH}	–70	0.4	V	Referred to BGND
Battery voltage difference	$V_{BATL} - V_{BATH}$	–0.4	–	V	–
Auxiliary supply voltage	V_{HR}	–0.4	50	V	Referred to BGND
Total battery supply voltage, continuous	$V_{HR} - V_{BATH}$	–0.4	90	V	–
V_{DD} supply voltage	V_{DD}	–0.4	7	V	Referred to AGND
Ground voltage difference BGND, AGND	–	–0.4	0.4	V	–
Input voltages	V_{DCP}, V_{DCN}, V_{ACP}, V_{ACN}, V_{C1}, V_{C2}, V_{CMS}	–0.4	$V_{DD} + 0.4$	V	Referred to AGND
Voltages on current outputs	V_{IT}, V_{IL}	–0.4	$V_{DD} + 0.4$	V	Referred to AGND
Junction temperature	T_j	–	150	°C	–
ESD voltage, all pins	–	–	1	kV	SDM (Socketed Device Model)[1]

[1] EOS/ESD Assn. Standard DS5.3-1993.

Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect the reliability of the device.

4.2 Foreign Line Voltages

External voltages applied at the line outputs cause a current flow in the SLIC-S/-S2. The resulting on-chip power dissipation has to be limited to avoid thermal destruction, because overtemperature protection cannot react fast enough at high local power density. The value of allowed power dissipation strongly depends on its duration. It can be expressed in terms of voltage and current limits directly at the TIP/RING outputs.

Table 6 Voltage Limits on Output Pins

Duration of Voltage	Pins	Min. voltage [V]	Max. Voltage [V]
continuous	TIP, RING	$V_{BATH} - 0.4$	$V_{HR} + 5$
< 10 ms	TIP, RING	$V_{BATH} - 5$	$V_{HR} + 10$
< 100 µs	TIP, RING	$V_{BATH} - 10$	$V_{HR} + 20$
< 1 µs	TIP, RING	$V_{BATH} - 10$	$V_{HR} + 20$

Table 7 Current Limits on Output Pins

Duration of Current	Pins	Min. Current [A]	Max. Current[A]
continuous	TIP, RING	– 0.1	0.1
< 10 ms	TIP, RING	– 0.5	0.5
< 100 µs	TIP, RING	– 1	1.0
< 1 µs	TIP, RING	– 1.5	1.5

The above limits (**Table 6** and **Table 7**) have to be regarded as typical. They are valid simultaneously. Together with external circuitry they determine protection requirements (see Application Note of the DuSLIC/VINETIC chip set on overvoltages and overcurrents).

4.3 Power Up Sequence of Supply Voltages

It is recommended to apply the SLIC-S/-S2 supply voltages in the following order to the respective pins:

1) AGND, BGND
2) V_{DD}
3) V_{BATH}
4) V_{HR}
5) V_{BATL}

When powering down the SLIC-S/-S2, the supply voltages have to be removed in reverse order.

With the use of the diodes D_1 and D_2 (see application circuits **Figure 6** and **Figure 7**) it is not necessary to keep the recommended power up sequence.

4.4 Operating Range

Table 8 Operating Range

Parameter	Symbol	Limit Values		Unit	Notes
		min.	max.		
Battery voltage L [1]	V_{BATL}	–60	–15	V	Referred to BGND
Battery voltage H [1]	V_{BATH}	–65	–20	V	Referred to BGND
Auxiliary supply voltage	V_{HR}	3.1	45	V	Referred to BGND
Total battery supply voltage	$V_{HR} - V_{BATH}$	–	90	V	–
V_{DD} supply voltage	V_{DD}	3.1	5.5	V	Referred to AGND
Ground voltage difference BGND, AGND	–	–0.4	0.4	V	–
Voltage at pins IT, IL	V_{IT}, V_{IL}	–0.4	V_{DD}	V	Referred to AGND
Input range V_{DCP}, V_{DCN}, V_{ACP}, V_{ACN}	V_{ACDC}	0	3.3	V	Referred to AGND
Ambient temperature	T_{amb}	–40	85	°C	–
Junction temperature	T_J	–	125[2]	°C	–

[1] If the battery switch is not used, pins VBATL and VBATH should be connected externally. In this case the full voltage range of –15 V to –65 V can be used.

[2] Operation up to T_J = 150 °C possible. However, a permanent junction temperature exceeding 125 °C could degrade device reliability.

4.5 Thermal Resistances

Table 9 Thermal Resistances

Parameter	Symbol	Typical Value	Unit	Condition
Junction to case	$R_{th, jC}$	2	K/W	P-DSO-20-5, P-VQFN-48-4
Junction to ambient	$R_{th, jA}$	50 20	K/W K/W	P-DSO-20-5, without additional heatsink P-DSO-20-5, with heatsink
Junction to ambient	$R_{th, jA}$	25	K/W	P-VQFN-48-4, 4-layer PCB; die pad soldered to 20 x 20 mm² cooling area (footprint see **Chapter 6.1**)

4.6 Electrical Parameters

Minimum and maximum values are valid within the full operating range.

Testing is performed according to the specific test figures at V_{BATH} = –48 V, V_{BATL} = –24 V, V_{HR} = +32 V and V_{DD} = +3.3 V.

Functionality and performance is guaranteed for T_A = 0 to 70 °C by production testing. Extended temperature range operation at –40 °C < T_A < 85 °C is guaranteed by design, characterization and periodically sampling and testing production devices at the temperature extremes.

4.6.1 Supply Currents and Power Dissipation

Table 10 Supply Currents, Power Dissipation ($I_R = I_T$ = 0 A; V_{RT} = 0 V)

No.	Parameter	Symbol	Mode	Limit Values			Unit
				min.	**typ.**	**max.**	
Power Down High Impedance, Power Down Resistive High							
1.	V_{DD} current	I_{DD}	PDx	–	200	300	µA
2.	V_{BATH} current	I_{BATH}	PDH	–	50	100	µA
3.			PDRH	–	120	200	µA
4.	V_{BATL} current	I_{BATL}	PDx	–	0	10	µA
5.	V_{HR} current	I_{HR}	PDx	–	10	20	µA
Active Low							
6.	V_{DD} current	I_{DD}	ACTL	–	1	1.3	mA
7.	V_{BATH} current	I_{BATH}	ACTL	–	100	150	µA
8.	V_{BATL} current[1)]	I_{BATL}	ACTL	–	2.5	3.2	mA
9.	V_{HR} current	I_{HR}	ACTL	–	10	20	µA

Table 10 Supply Currents, Power Dissipation ($I_R = I_T = 0$ A; $V_{RT} = 0$ V) (cont'd)

No.	Parameter	Symbol	Mode	Limit Values			Unit
				min.	typ.	max.	
Active High							
10.	V_{DD} current	I_{DD}	ACTH	–	1	1.3	mA
11.	V_{BATH} current[1]	I_{BATH}	ACTH	–	3	4	mA
12.	V_{BATL} current	I_{BATL}	ACTH	–	0	10	µA
13.	V_{HR} current	I_{HR}	ACTH	–	10	20	µA
Active Ring							
14.	V_{DD} current	I_{DD}	ACTR	–	0.6	0.8	mA
15.	V_{BATH} current[1]	I_{BATH}	ACTR	–	2.2	3.2	mA
16.	V_{BATL} current	I_{BATL}	ACTR	–	0	10	µA
17.	V_{HR} current[1]	I_{HR}	ACTR	–	1.4	2	mA
High Impedance on RING, High Impedance on TIP							
18.	V_{DD} current	I_{DD}	HIR, HIT	–	0.6	0.8	mA
19.	V_{BATH} current[1]	I_{BATH}	HIR, HIT	–	1.8	2.5	mA
20.	V_{BATL} current	I_{BATL}	HIR, HIT	–	0	10	µA
21.	V_{HR} current[1]	I_{HR}	HIR, HIT	–	1.1	1.6	mA

[1] Current depending on supply voltage (see **Table 11**)

The total power dissipated in the SLIC consists of the quiescent power P_Q due to the supply currents and the output stage power P_O caused by any line current I_{TRANS} (see **Table 12**).

$$P_{tot} = P_Q + P_O$$

with $P_Q = V_{DD} \times I_{DD} + |V_{BATH}| \times I_{BATH} + |V_{BATL}| \times I_{BATL} + V_{HR} \times I_{HR}$

The supply currents I_{BATL}, I_{BATH} and I_{HR} are dependent on the respective supply voltages. They can be calculated from the specified values I_{BATL} (–24 V), I_{BATH} (–48 V) and I_{HR} (32 V) by the formulas in **Table 11**.

Table 11 Voltage Dependance of Supply Currents

Operating Mode	Equation for I Calculation
ACTL	I_{BATL} (V_{BATL}) = I_{BATL} (-24V) + (|V_{BATL}| - 24)/50 kΩ
ACTH	I_{BATH} (V_{BATH}) = I_{BATH} (-48V) + (|V_{BATH}| - 48)/50 kΩ
ACTR[1]	I_{BATH} (V_{BATH}) = I_{BATH} (-48V) + (|V_{BATH}| - 48)/50 kΩ I_{HR} (V_{HR}) = I_{HR} (32V) + (V_{HR} - 32)/200 kΩ

[1] valid for $|V_{BATH}| > V_{HR}$

Table 12 Output Stage Power Dissipation

Operating Mode	Equation for P_O Calculation
ACTL	$P_O = (1.05 \times \|V_{BATL}\| - V_{TR}) \times I_{Trans}$
ACTH	$P_O = (1.05 \times \|V_{BATH}\| - V_{TR}) \times I_{Trans}$
ACTR	$P_O = (1.02 \times V_{HR} + 1.05 \times \|V_{BATH}\| - V_{TR}) \times I_{Trans}$ (ohmic load) $P_O = [4 \times (V_H + \|V_{BATH}\|) - \pi \times V_P \times \cos\varphi] \times V_P / (2 \times \pi \times Z_L)$ (complex load $Z = Z_L e^{i\varphi}$, V_P ... peak ring voltage)

4.6.2 DC Characteristics

Table 13 DC Characteristics

No.	Parameter	Symbol	Mode	Limit Values			Unit	Test Condition
				min.	typ.	max.		
Line Termination TIP, RING								
22.	DC line voltage	$V_{TR, DC}$	ACTL, ACTH, ACTR	–0.4		0.4	V	$V_{DCP} = V_{DCN} = V_{ACP} = V_{ACN} = 1.5$ V
23.		$V_{TIP, DC}$	ACTL	–13	–12	–11	V	
24.			ACTH	–25	–24	–23	V	
25.			ACTR	–10.5	–9.5	–8.5	V	
26.		$V_{TR, DC}$	ACTH	23.5	24	24.5	V	$V_{DCP} - V_{DCN} = 0.8$ V, $V_{ACP} = V_{ACN} = 1.5$ V
27.				–24.5	–24	–23.5	V	$V_{DCP} - V_{DCN} = -0.8$ V, $V_{ACP} = V_{ACN} = 1.5$ V
28.	DC line voltage drop (see **Figure 8**)	$-V_{BATH} - V_{TR, max}$	ACTH	–	2	3	V	$I_{Trans,DC} = 20$ mA, $V_{DCP} - V_{DCN} = 2.5$ V, $V_{ACP} = V_{ACN} = 1.5$ V
29.	Output current limit (see **Figure 12**)	$\|I_{R, max}\|$, $\|I_{T, max}\|$	ACTL, ACTH, ACTR, HIR HIT	75		115	mA	
30.	Open loop resistance TIP to V_{BGND} (see **Figure 13**)	R_{TG}	PDRH	4.7	5.5	6.3	kΩ	$I_T = 2$ mA, Temp = 25 °C[1]
31.	Open loop resistance RING to V_{BATH} (see **Figure 13**)	R_{RB}	PDRH	4.7	5.5	6.3	kΩ	$I_R = 2$ mA, Temp = 25 °C[1]
32.	Open loop line voltage	V_{TR}	PDRH		47		V	
33.	Power down output leakage current	$I_{Leak,R}$, $I_{Leak,T}$	PDH	–30		30	µA	$V_{R,T} = V_{BATH}$
34.					50	80	µA	$V_{R,T} = V_{HR}$

Table 13 DC Characteristics (cont'd)

No.	Parameter	Symbol	Mode	Limit Values			Unit	Test Condition
				min.	typ.	max.		
35.	High impedance output leakage current	$I_{\text{Leak,R}}$	HIR, HIRT	–30		30	µA	$V_{\text{BATH}} < V_{\text{R}} < V_{\text{HR}} - 3$
36.		$I_{\text{Leak,T}}$	HIT, HIRT	–30		30	µA	$V_{\text{BATH}} < V_{\text{T}} < V_{\text{HR}} - 3$
Inputs DCP, DCN, ACP, ACN, Output C_{EXT}								
37.	Input resistance DCP, DCN	R_{DC}	ACTR, HIR, HIT	–	1	–	kΩ	
38.			ACTL, ACTH	–	2	–	kΩ	
39.	Input resistance ACP, ACN	R_{AC}	all	–	10	–	kΩ	
40.	Output resistance on C_{EXT}		all	–	50	–	kΩ	
Current Outputs IT, IL								
41.	IT output current (see **Figure 14**)	I_{IT}	ACTx	–15	0	15	µA	$I_{\text{R}} = I_{\text{T}} = 0$ mA
42.				380	400	420	µA	$I_{\text{R}} = I_{\text{T}} = 20$ mA
43.				–420	–400	–380	µA	$I_{\text{R}} = I_{\text{T}} = -20$ mA
44.	Transversal current ratio (guaranteed by design, see **Figure 14**)	$1/G_{\text{IT,DC}}$ [2]	ACTx	49	50	51	–	$I_{\text{R}} = I_{\text{T}} = 20$ mA, $I_{\text{R}} = I_{\text{T}} = -20$ mA
45.	Off-hook output current on IT		PDRH	650	800	950	µA	TIP/RING shorted Temp = 25 °C[3]
46.	IL output current (see **Figure 14**)	I_{IL}	ACTx	–20	0	20	µA	$I_{\text{R}} = I_{\text{T}} = 20$ mA
47.				30	50	70	µA	$I_{\text{R}} = 15$ mA, $I_{\text{T}} = 25$ mA
48.				–160	–125	–90	µA	$I_{\text{R}} = 62.5$ mA, $I_{\text{T}} = 37.5$ mA

Table 13 DC Characteristics (cont'd)

No.	Parameter	Symbol	Mode	Limit Values			Unit	Test Condition
				min.	typ.	max.		
Control Inputs C1, C2								
49.	H-input voltage	V_{IH}	–	2.7	–	V_{DD} + 0.3	V	–
50.	M-input voltage	V_{IM}	–	1.2	–	2.1	V	–
51.	L-input voltage	V_{IL}	–	–0.3	–	0.6	V	–
52.	Input leakage current	I_{Leak}	–	–5	0	5	µA	–
53.	Thermal overload current C1	I_{therm}	ACTx, HIx	120	150	250	µA	V_{C1} = 1.20 V
54.	Max. junction temperature[4]	T_{jLIM}	ACTx, HIx	–	165	–	°C	–

[1] The systematic temperature dependency of this resistance is +0.1 %/°C.

[2] The offset (I_R = I_T = 0 mA) has to be taken into account.

[3] The systematic temperature dependency of this current is –0.1 %/°C.

[4] Overtemperature protection (guaranteed by design)

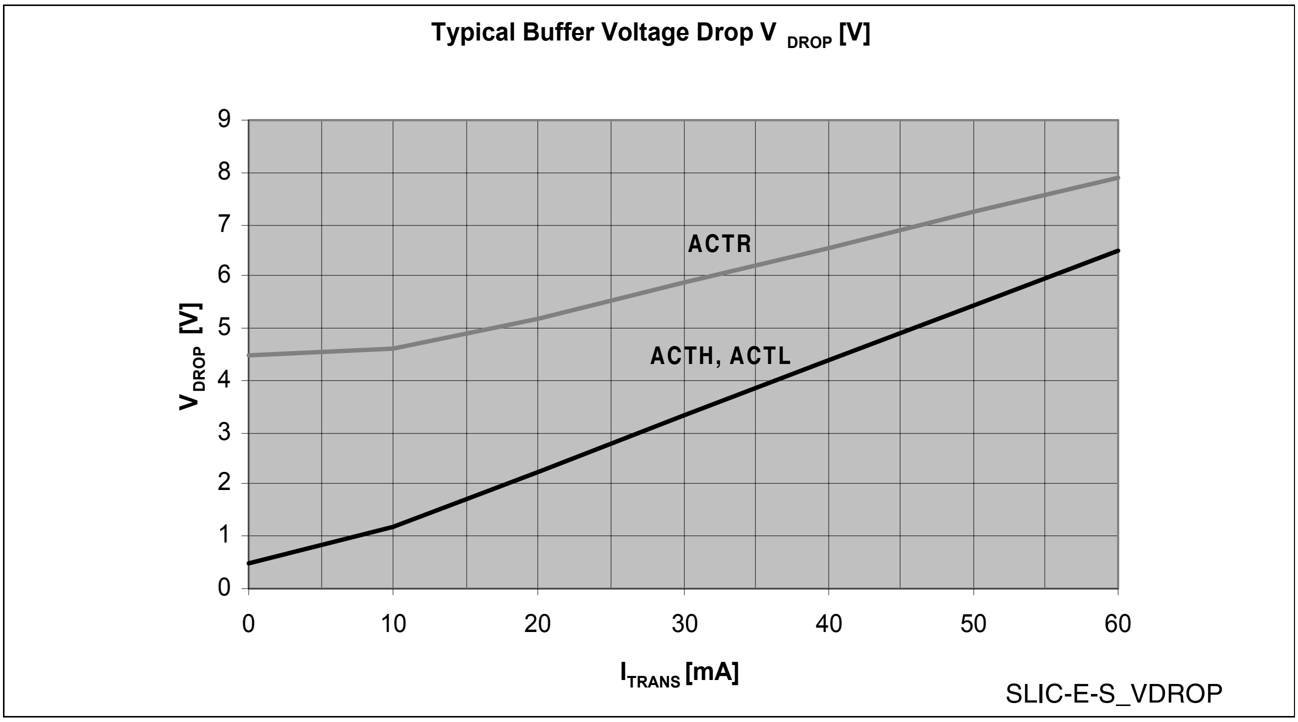


Figure 8 Typical Buffer Voltage Drop in Operating Modes ACTL, ACTH, ACTR

4.6.3 AC Characteristics

If not otherwise stated, AC characteristics are tested at a DC line current of 25 mA and –25 mA, respectively; they are valid in all active modes.

Table 14 AC Characteristics

No.	Parameter	Symbol	Mode	Limit Values			Unit	Test Condition
				min.	typ.	max.		
Line Termination TIP, RING								
55.	Receive gain (see **Figure 15**)	G_r		5.925	6.0	6.075	–	$V_{ACP} - V_{ACN}$ = 640 mVrms f = 1015 Hz
56.	Total harmonic distortion V_{TR} (see **Figure 15**)	THD		–	0.03	0.3	%	$V_{ACP} - V_{ACN}$ = 640 mVrms f = 1015 Hz
57.	Teletax distortion	$THDTTX$		–	0.1	1	%	$V_{TR,AC}$ = 5 Vrms f = 16 kHz, R_L = 200 Ω
58.				–	1	3	%	$V_{TR,AC}$ = 5 Vrms f = 16 kHz, R_L = 200 Ω, $I_{Trans,DC}$ = 0 mA
59.	Psophometric noise (see **Figure 15**)	N_{pVTR}		–	–80	–76	dBmp	
60.	Longitudinal to transversal rejection ratio V_{long}/V_{TR} (see **Figure 16**)	$LTRR$		60	70	–	dB	V_{long} = 3 Vrms 300 Hz < f < 3.4 kHz
61.	Longitudinal to transversal rejection ratio V_{long}/V_{TR} (loop) (see **Figure 17**)	*LTRR-1 loop*1)		54	58	–	dB	V_{long} = 3 Vrms 300 Hz < f < 1 kHz
62.				52	56	–	dB	3.4 kHz
63.		*LTRR-2 loop*2)		61	65	–	dB	300 Hz < f < 1 kHz
64.				56	60	–	dB	3.4 kHz
65.	Transversal to longitudinal rejection ratio V_{TR}/V_{long} (see **Figure 18**)	$TLRR$		48	58	–	dB	$V_{ACP} - V_{ACN}$ = 1920 mVrms 300 Hz < f < 3.4 kHz

Table 14 AC Characteristics (cont'd)

No.	Parameter	Symbol	Mode	Limit Values			Unit	Test Condition
				min.	typ.	max.		
	Power supply rejection ratio	*PSRR*						V_{SupplyAC} = 100 mVp 300 Hz < f < 3.4 kHz
66.	$V_{\text{BATL}}/V_{\text{TR}}$			40	60		dB	
67.	$V_{\text{BATH}}/V_{\text{TR}}$			40	60		dB	
68.	$V_{\text{HR}}/V_{\text{TR}}$			33	50		dB	
69.	$V_{\text{DD}}/V_{\text{TR}}$ (see **Figure 9**, **10**, **11**)			33	50		dB	
70.	Ringing amplitude TIP/RING	V_{RNG0}	ACTR		51		Vrms	$V_{\text{DCP}} - V_{\text{DCN}}$ = 0.15 V (DC) + 0.85 Vrms (sine wave), V_{HR} = 42 V R_{R} = 450 Ω, C_{R} = 3.4 µF, f = 20 Hz
71.	Ringing distortion (see **Figure 19**)	*RD*		–	0.1	2	%	

Transversal Current IT

No.	Parameter	Symbol	Mode	min.	typ.	max.	Unit	Test Condition
	Transversal current ratio	$1/G_{\text{it}}$					–	$V_{\text{ACP}} - V_{\text{ACN}}$ = 640 mVrms f = 1015 Hz
72.	(see **Figure 15**)			49.5	50	50.5		$I_{\text{Trans,DC}}$ = 25 mA
73.				49	50	51		$I_{\text{Trans,DC}}$ = –25 mA
74.	Total harmonic distortion V_{IT}	THD_{IT}		–	0.02	0.3	%	$I_{\text{Trans,DC}}$ = 25 mA $V_{\text{ACP}} - V_{\text{ACN}}$ = 640 mVrms f = 1015 Hz
75.	Psophometric noise (see **Figure 15**)	N_{pVIT}		–	–110	–105	dBmp	
76.	Longitudinal to transversal current output rejection ratio $V_{\text{long}}/V_{\text{IT}}$ (see **Figure 16**)	*LITRR*		78			dB	V_{long} = 3 Vrms 300 Hz < f < 3.4 kHz
	Power supply rejection ratio	*PSRR*						V_{SupplyAC} = 100 mVp 300 Hz < f < 3.4 kHz
77.	$V_{\text{BATL}}/V_{\text{IT}}$			50	70	–	dB	
78.	$V_{\text{BATH}}/V_{\text{IT}}$			50	70	–	dB	
79.	$V_{\text{HR}}/V_{\text{IT}}$			50	70	–	dB	
80.	$V_{\text{DD}}/V_{\text{IT}}$			50	70	–	dB	

[1] Longitudinal to transversal rejection ratio for PEB 4264

[2] Longitudinal to transversal rejection ratio for PEB 4264-2

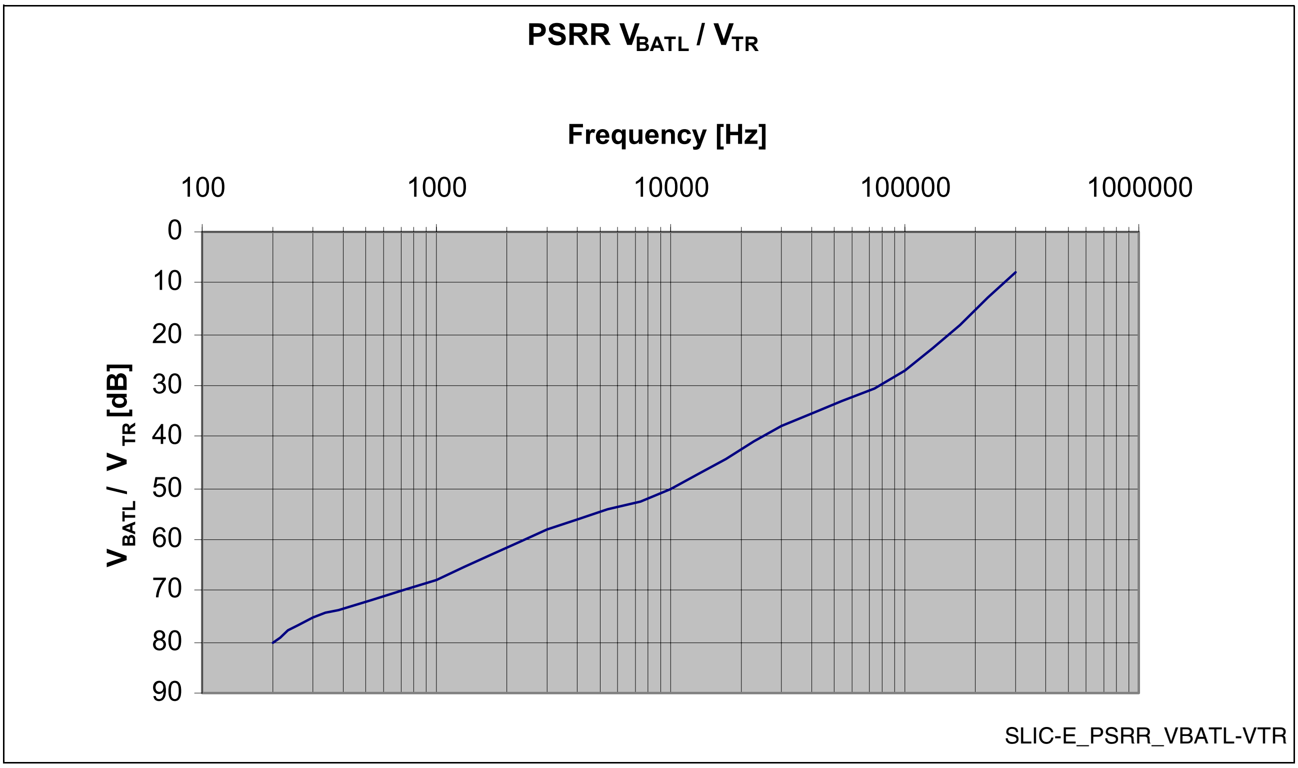


Figure 9 Typical Frequency Dependence of PSRR VBATL/VTR

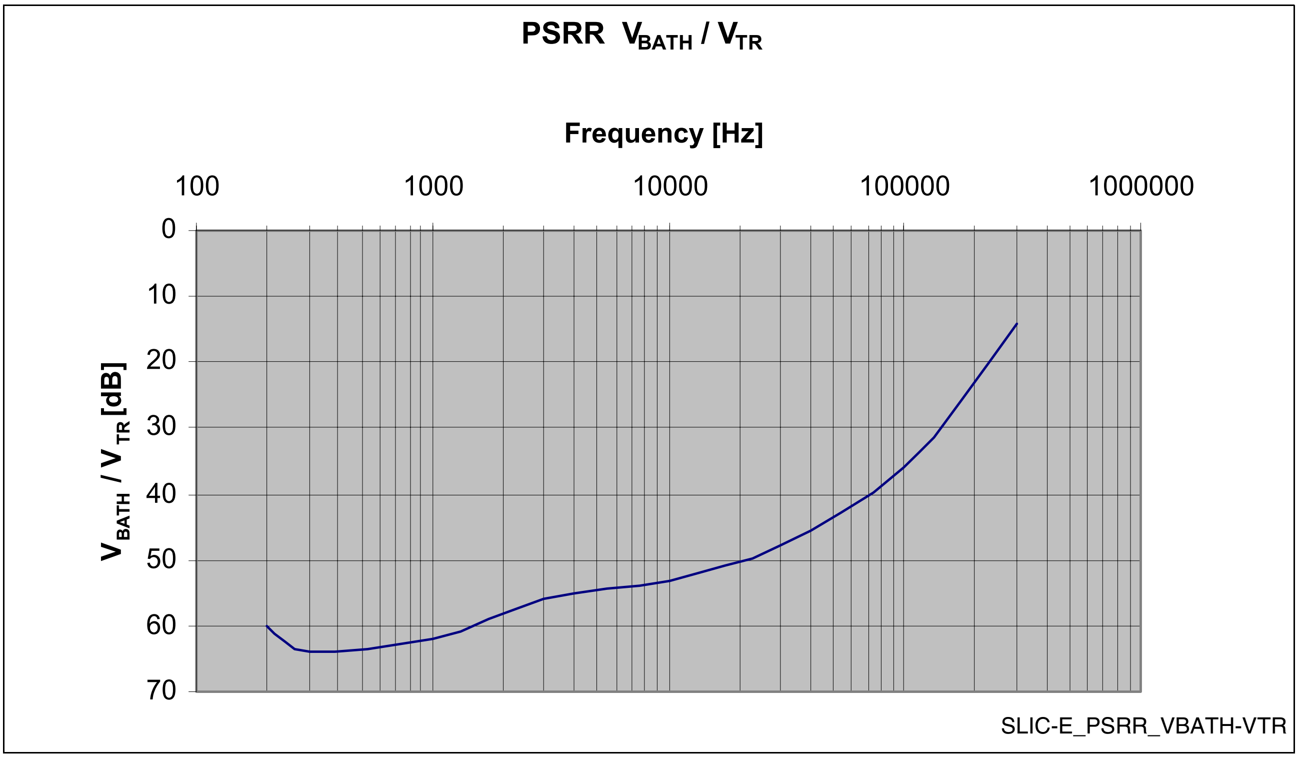


Figure 10 Typical Frequency Dependence of PSRR VBATH/VTR

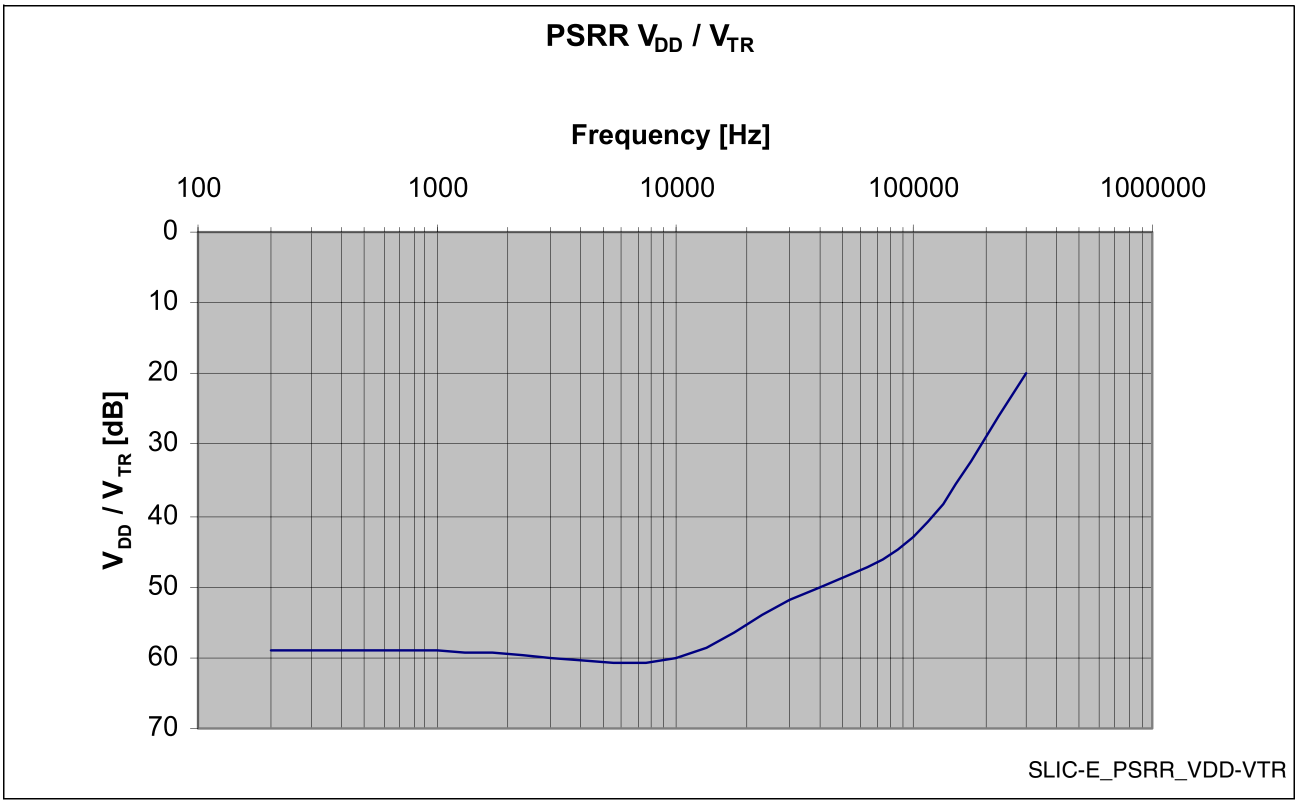


Figure 11 Typical Frequency Dependence of PSRR VDD/VTR

5 Test Figures

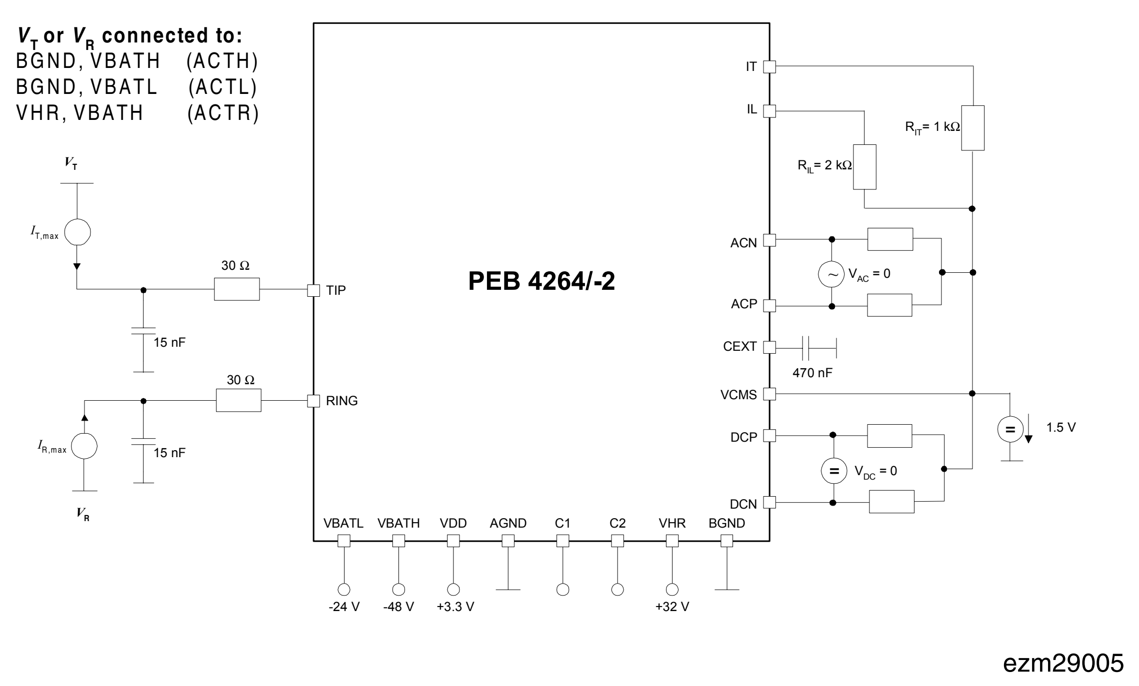


Figure 12 Output Current Limit

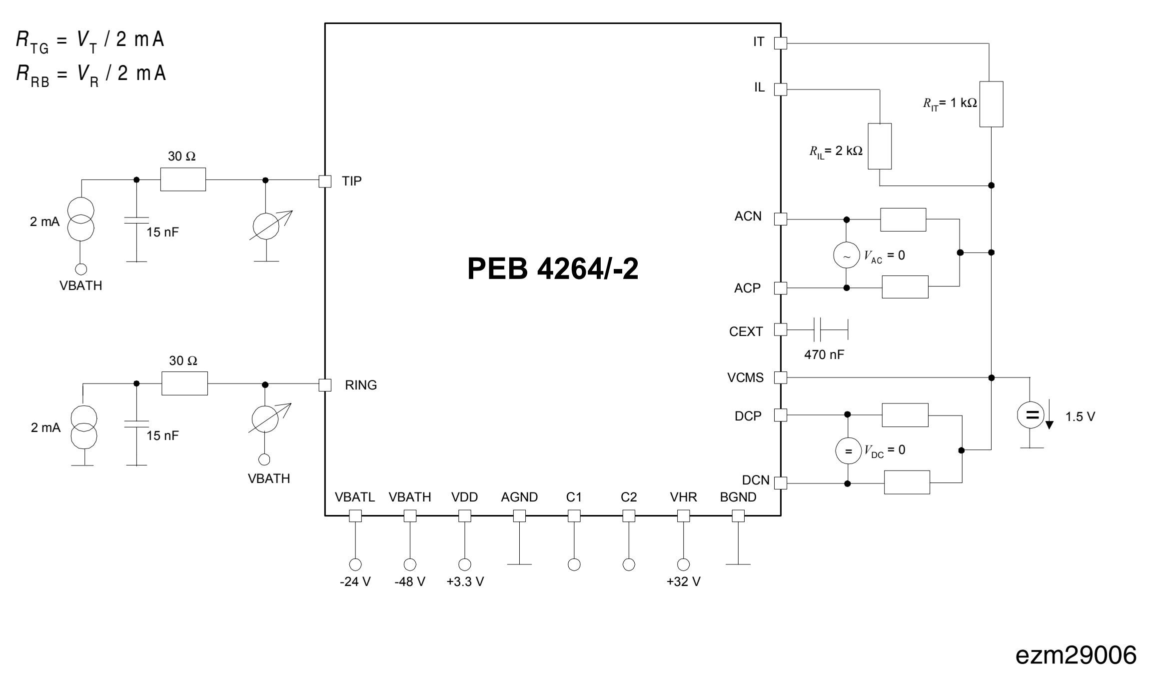


Figure 13 Output Resistance PDRH, PDRHL

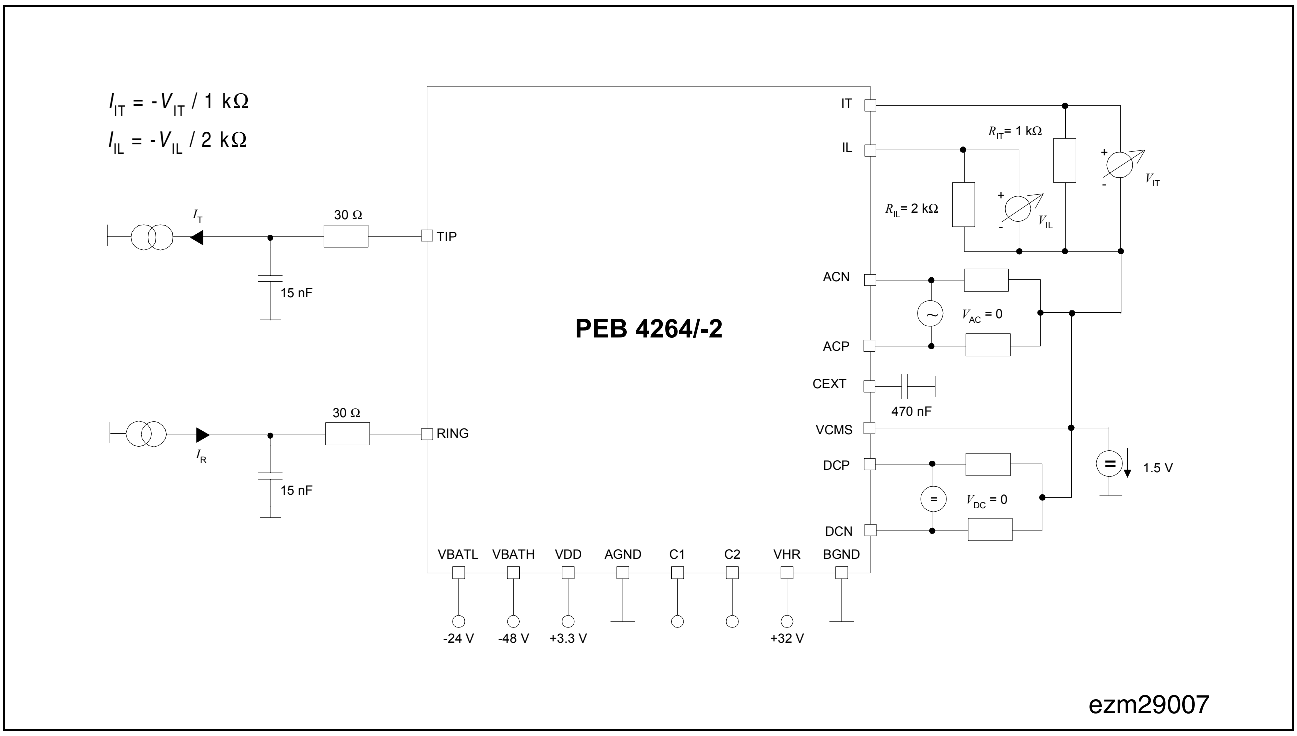


Figure 14 Current Outputs IT, IL

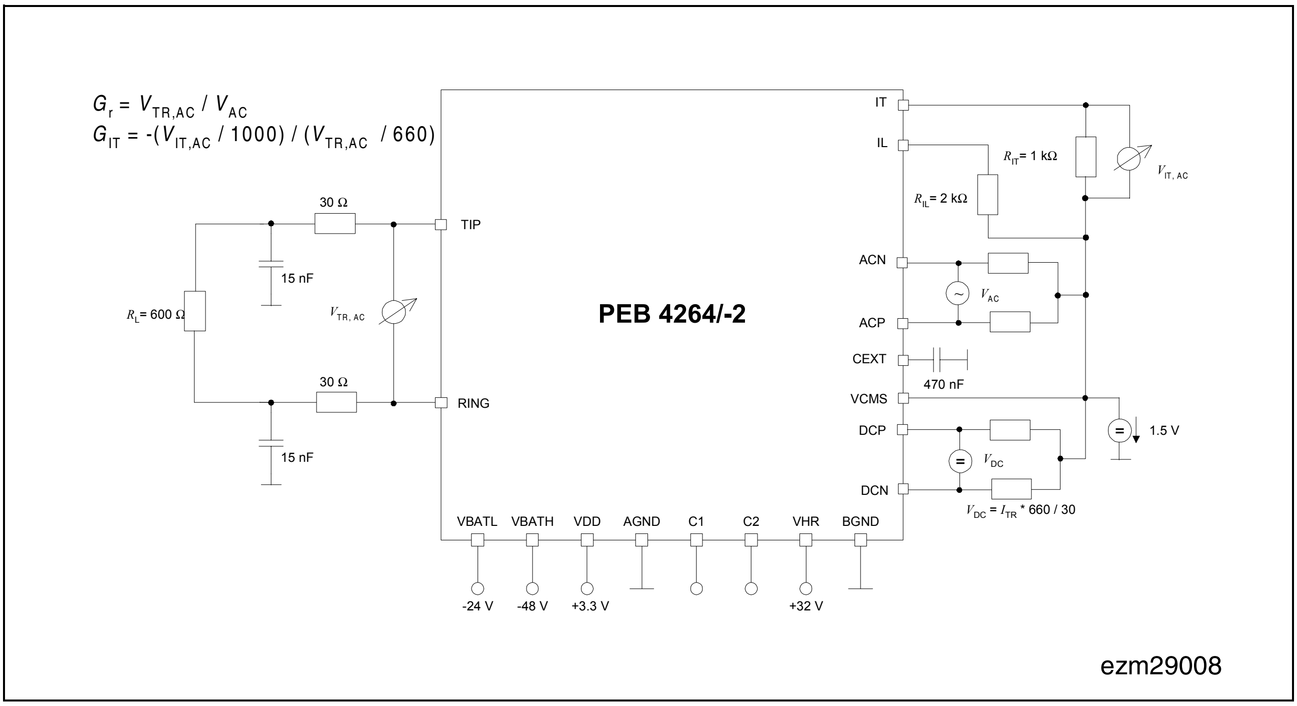


Figure 15 Transmission Characteristics

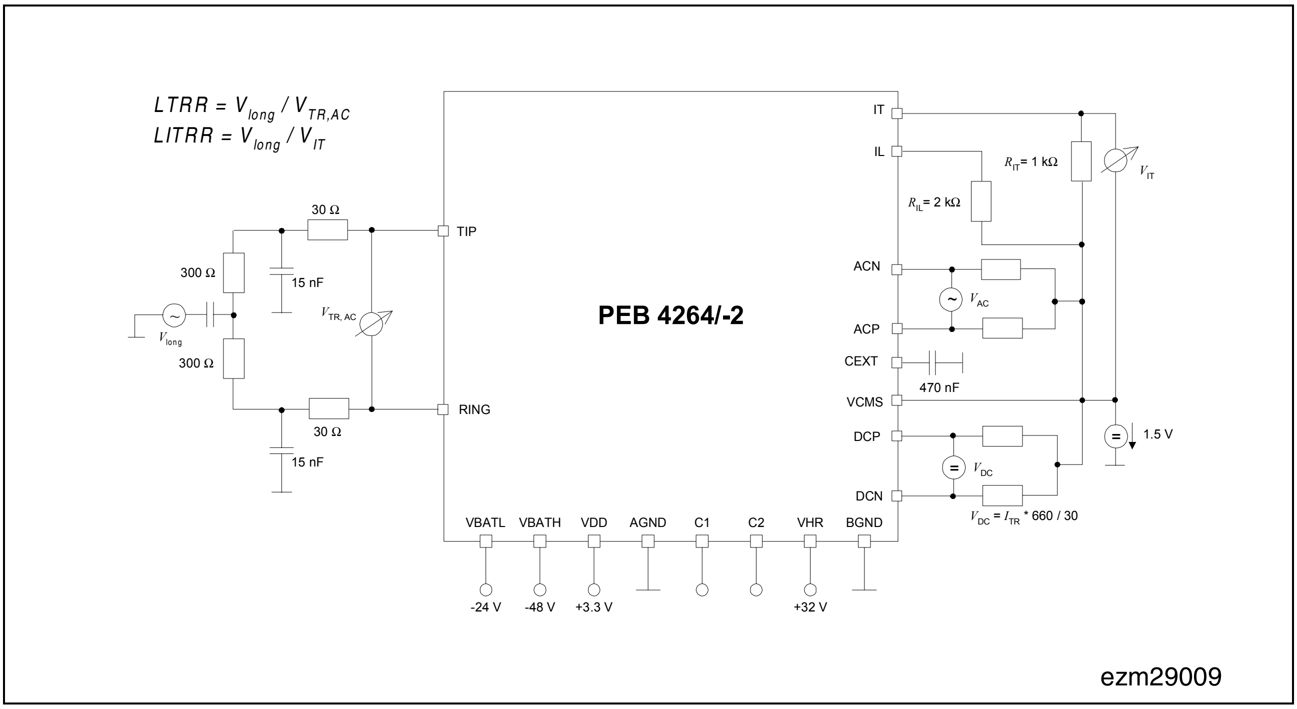


Figure 16 Longitudinal to Transversal Rejection

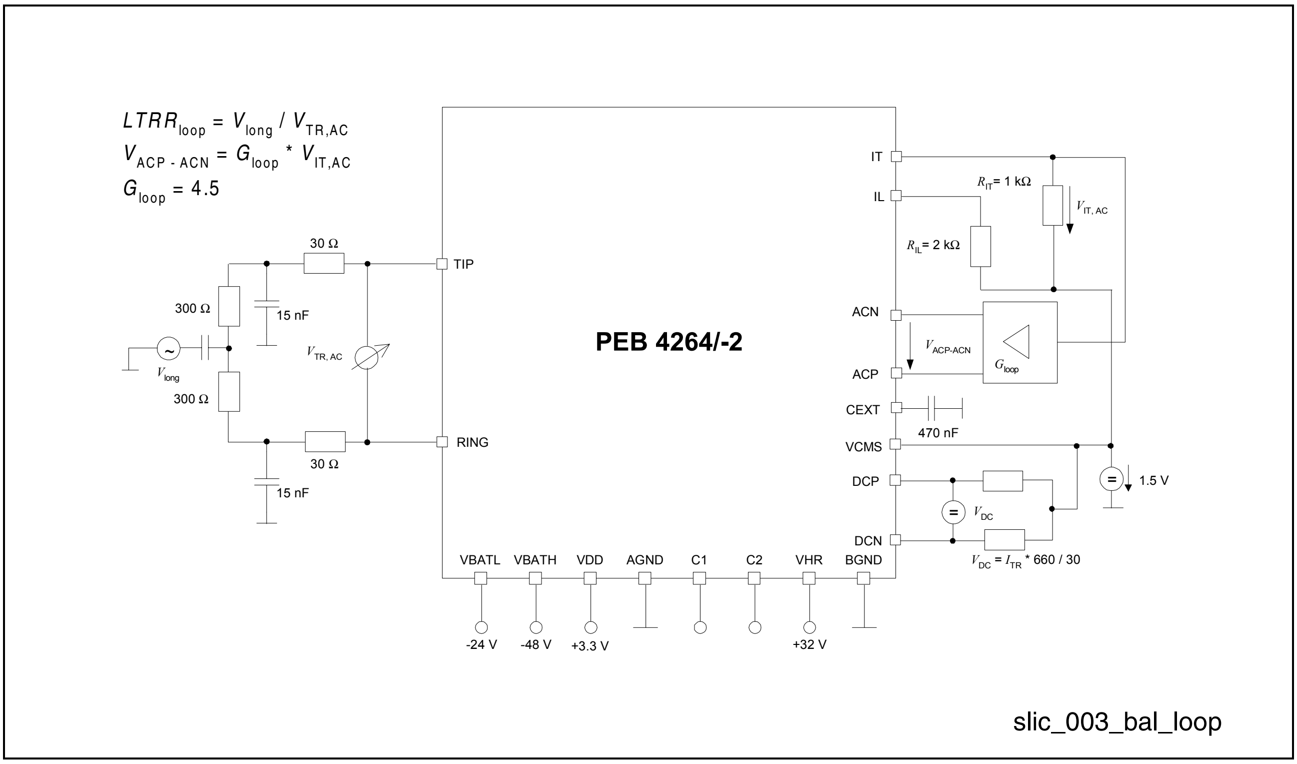


Figure 17 Longitudinal to Transversal Rejection Loop

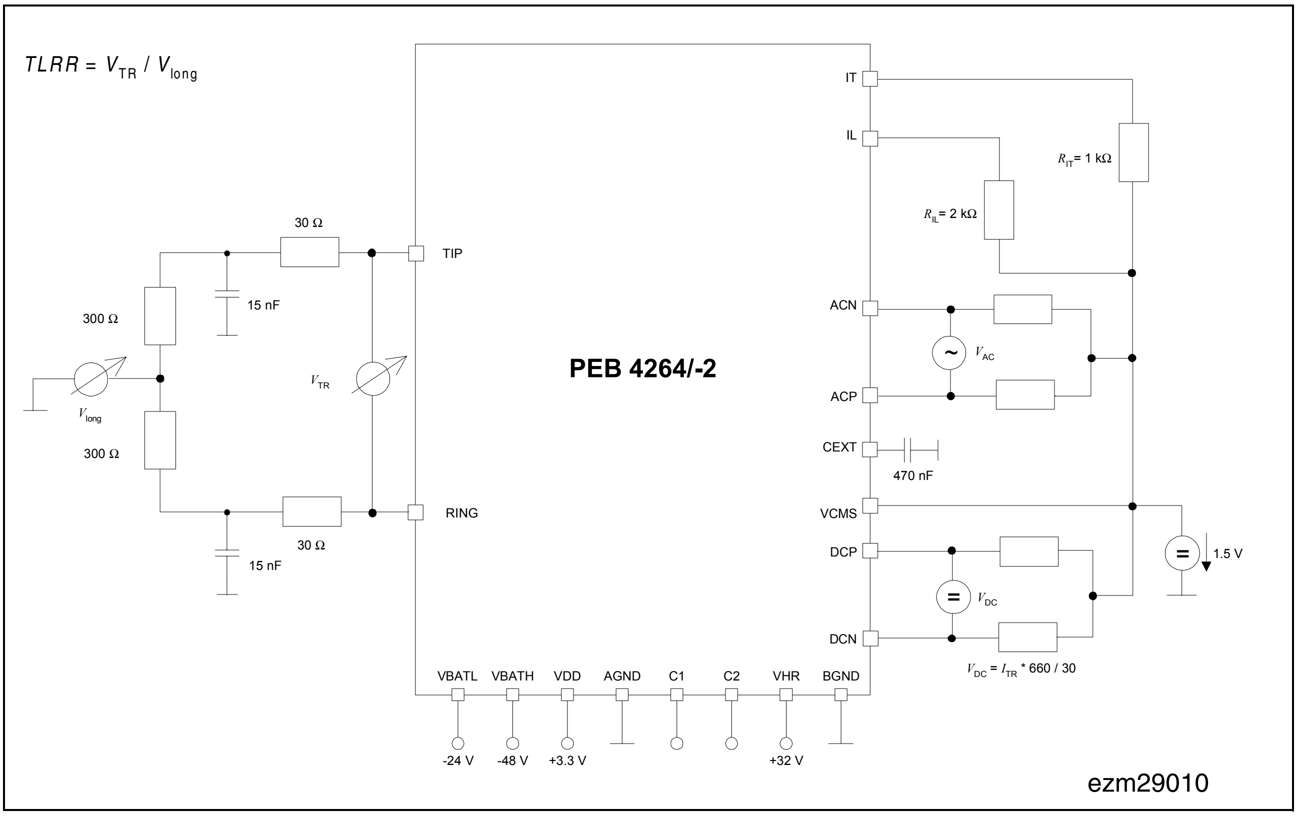


Figure 18 Transversal to Longitudinal Rejection

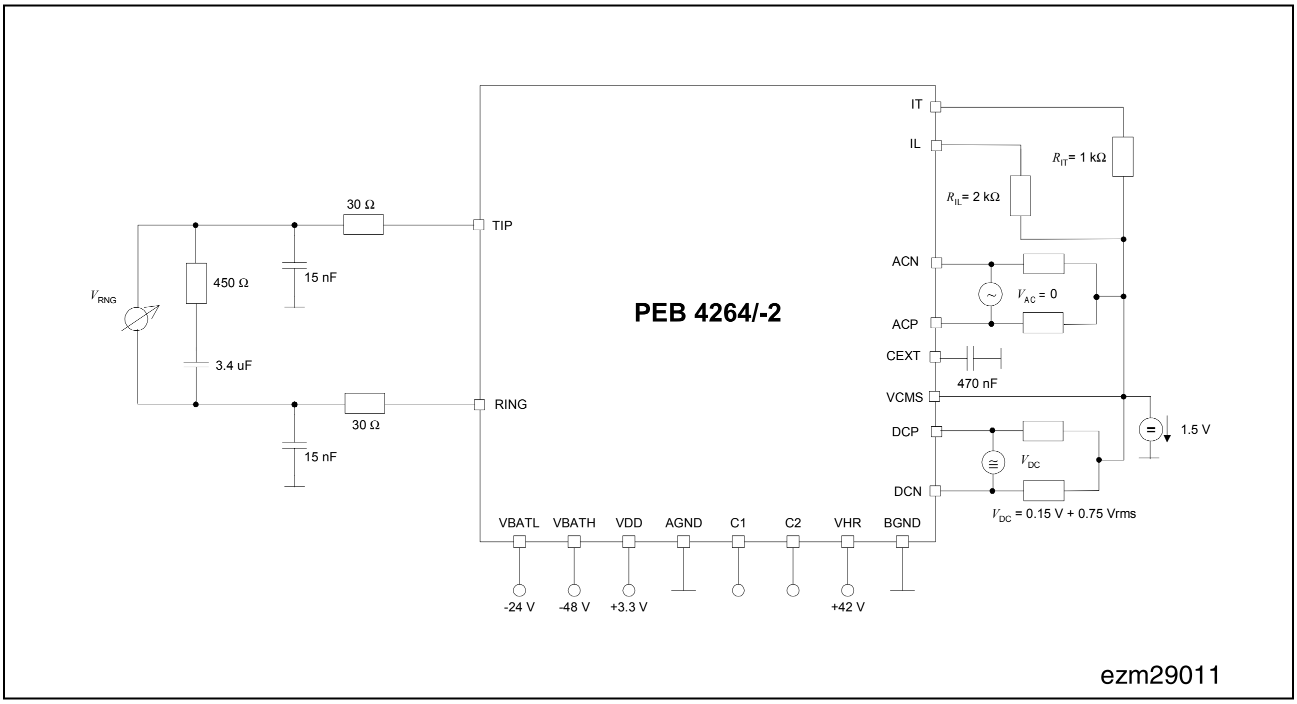
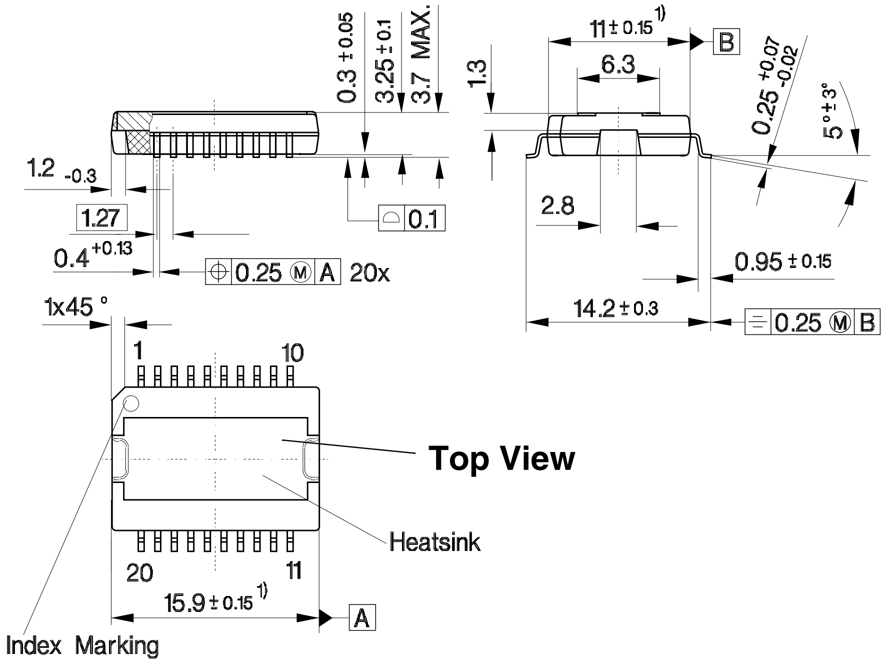


Figure 19 Ring Amplitude

6 Package Outlines

P-DSO-20-5 (SLIC-S/-S2)
(Plastic Dual Small Outline)



1) Does not include plastic or metal protrusion of 0.15 max. per side

gps05755

Figure 20 Packet Outline for P-DSO-20-5

Note: The P-DSO-20-5 package is designed with heatsink on top. The pin counting for this package is clockwise (top view).

Attention: The heatsink (see Figure 20) is connected to VBATH via the chip substrate. Due to the high voltage of up to 90 V between VHR and VBATH, touching of the heatsink or any attached conducting part can be hazardous.

You can find all of our packages, sorts of packing and others in our Infineon Internet Page “Products”: http://www.infineon.com/products.

SMD = Surface Mounted Device

Dimensions in mm

P-VQFN-48-4 (SLIC-S/-S2)
(Very thin Profile Quad Flatpack No-lead)

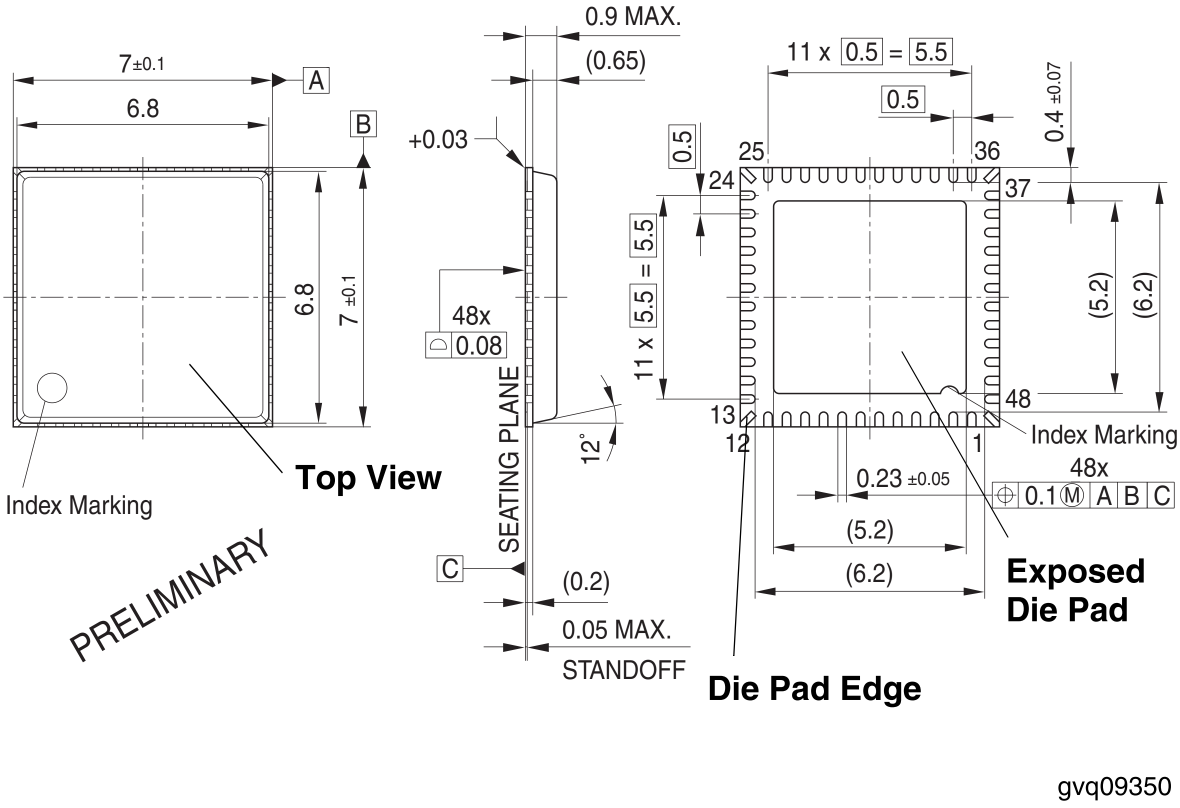


Figure 21 Packet Outline for P-VQFN-48-4

Attention: ***The exposed die pad and die pad edges are connected to VBATH via the chip substrate. Due to the high voltage of up to 90 V between VHR and VBATH, touching of the die pad or any attached conducting part can be hazardous.***

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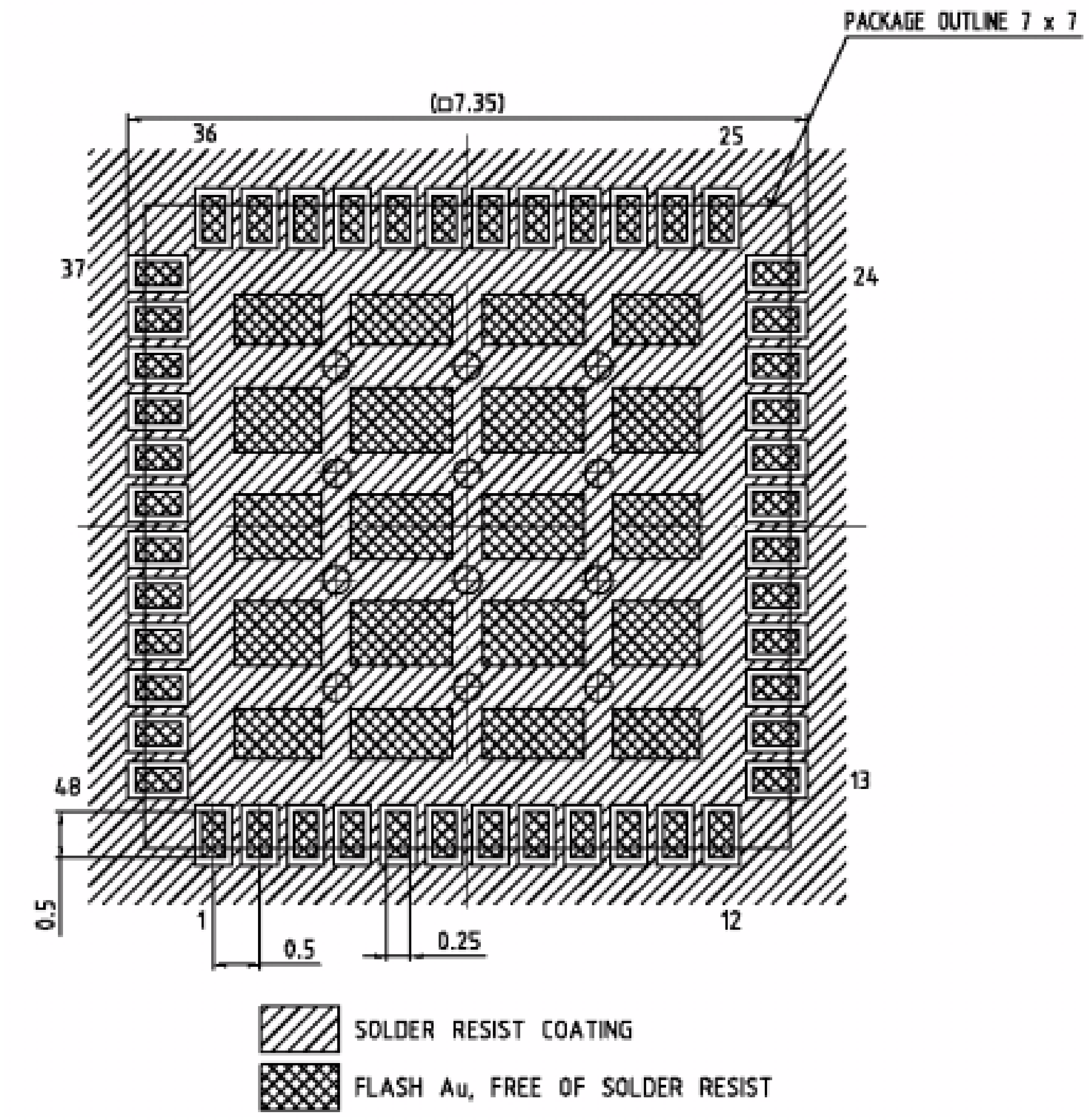
SMD = Surface Mounted Device

Dimensions in mm

6.1 Recommended PCB Foot Print Pattern for the P-VQFN-48-4



P-VQFN-48-4_foot

Figure 22 Foot Print for P-VQFN-48-4

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“Business excellence means intelligent approaches and clearly defined processes, which are both constantly under review and ultimately lead to good operating results.
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