KS54HCTLS/KS74HCTLS 590/591

8-Bit Binary Counters with Output Registers

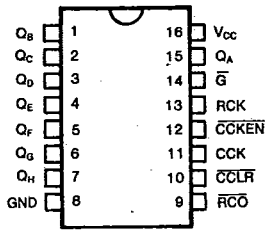
Preliminary Specifications

T-45-23-17

FEATURES

- Choice of 3-State ('590) and Open-Drain ('591) Outputs
- Function, pin-out, speed and drive compatibility with 54/74LS logic family
- Low power consumption characteristic of CMOS
- High-Drive-Current outputs (I_{OL} = 24mA @ V_{OL} = 0.5V) for direct bus interface
- Inputs and outputs interface directly with TTL, NMOS and CMOS devices
- Wide operating voltage range: 4.5V to 5.5V
- Characterized for operation over industrial and military temperature ranges:
  KS74HCTLS: −40°C to +85°C
  KS54HCTLS: −55°C to +125°C
- Package options include plastic "small outline" packages, standard plastic and ceramic 300-mil DIPs

PIN CONFIGURATION



DESCRIPTION

These devices each consist of an 8-bit counter which feeds an 8-bit register. The counter is incremented on the rising edge of the CCK input, provided that clock enable, $\overline{CCKEN}$, is low. When the counter increments to the all ones condition, ripple carry out, $\overline{RCO}$, will go low. This enables either synchronous cascading of the counters by connecting the $\overline{RCO}$ of the first stage to the $\overline{CCKEN}$ of the second, or clocking both circuits in parallel. Ripple cascading is accomplished by connecting the $\overline{RCO}$ of the first to the CCK of the second stage. A clear input is also provided which will reset the counter to the all zeros state.

The output register is loaded with the contents of the counter on the rising edge of the register clock, RCK. The outputs of this register feed the outputs which are enabled when the enable input, G, is taken low. This enables connection of this part to a system bus. The Q outputs of the '590 are 3-State and those for '591 are Open-drain.

These devices provide speeds and drive capability equivalent to their LSTTL counterparts and yet maintain CMOS power levels. The input and output voltage levels allow direct interface with TTL, NMOS and CMOS devices without any external components.

All inputs and outputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

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FUNCTION TABLE

INPUTS					FUNCTION
$\overline{G}$	RCK	$\overline{CCLR}$	$\overline{CCKEN}$	CCK	
H	X	X	X	X	Q Outputs disable
L	X	X	X	X	Q Outputs enable
L	↑	X	X	X	Counter data is stored into register
L	↓	X	X	X	Register state is not changed
L	X	L	X	X	Counter clear
L	X	H	L	↑	Advance one count
L	X	H	L	↓	No count
L	X	H	H	X	No count

X: Don't care

$$\overline{RCO} = Q_A' \bullet Q_B' Q_C' \bullet Q_D' Q_E' \bullet Q_F' Q_G' \bullet Q_H'$$

($Q_A' \sim Q_H'$: Internal outputs of the counter)

KS54HCTLS 590/591
KS74HCTLS

8-Bit Binary Counters with Output Registers

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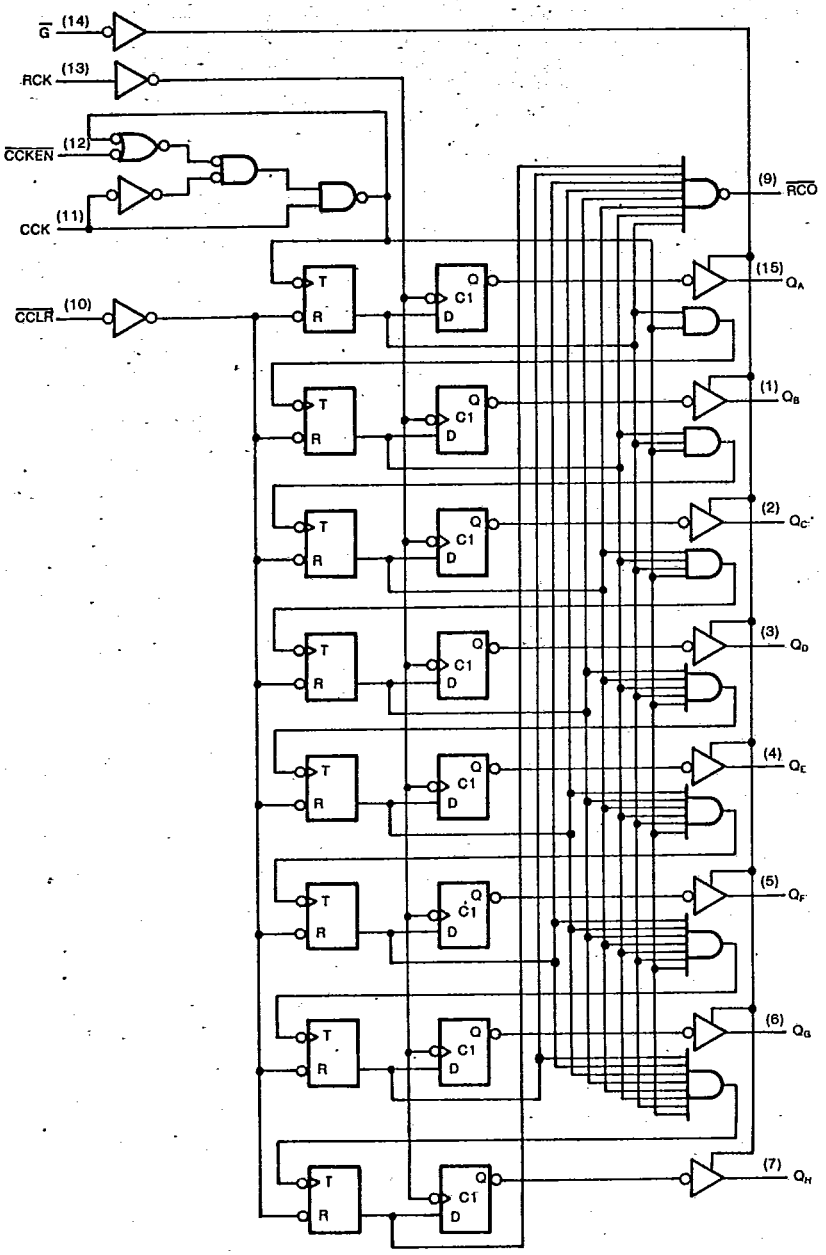
LOGIC DIAGRAM



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8-Bit Binary Counters with Output Registers

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Absolute Maximum Ratings*

Supply Voltage Range V_{CC} . . . . . −0.5V to +7V
DC Input Diode Current, I_{IK}
($V_I < -0.5V$ or $V_I > V_{CC} + 0.5V$) . . . . . ±20 mA
DC Output Diode Current, I_{OK}
($V_O < -0.5V$ or $V_O > V_{CC} + 0.5V$) . . . . ±20 mA
Continuous Output Current Per Pin, I_O
($-0.5V < V_O < V_{CC} + 0.5V$) . . . . . ±70 mA
Continuous Current Through
V_{CC} or GND pins . . . . . ±250 mA
Storage Temperature Range, T_{stg} . . . −65°C to +150°C
Power Dissipation Per Package, P_d† . . . . . 500 mW

* Absolute Maximum Ratings are those values beyond which permanent damage to the device may occur. These are stress ratings only and functional operation of the device at or beyond them is not implied. Long exposure to these conditions may affect device reliability.

† Power Dissipation temperature derating:
Plastic Package (N): −12mW/°C from 65°C to 85°C
Ceramic Package (J): −12mW/°C from 100°C to 125°C

Recommended Operating Conditions

Supply Voltage, V_{CC} . . . . . 4.5V to 5.5V
DC Input & Output Voltages*, V_{IN}, V_{OUT} . . 0V to V_{CC}
Operating Temperature
Range KS74HCTLS: −40°C to +85°C
KS54HCTLS: −55°C to +125°C
Input Rise & Fall Times, t_r, t_f . . . . . Max 500 ns

* Unused inputs must always be tied to an appropriate logic voltage level (either V_{CC} or GND)

DC ELECTRICAL CHARACTERISTICS (V_{CC}=5V±10% Unless Otherwise Specified)

Characteristic	Symbol	Test Conditions	T_a = 25°C	KS74HCTLS T_a = −40°C to +85°C	KS54HCTLS T_a = −55°C to +125°C	Unit
			Typ	Guaranteed Limits		
Minimum High-Level Input Voltage	V_{IH}			2.0	2.0	2.0	V
Maximum Low-Level Input Voltage	V_{IL}			0.8	0.8	0.8	V
Minimum High-Level Output Voltage (All '590 Outputs and '591 $\overline{RCO}$ Outputs)	V_{OH}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=-20\mu A$ $I_O=-6mA$	V_{CC} 4.2	$V_{CC}-0.1$ 3.98	$V_{CC}-0.1$ 3.84	$V_{CC}-0.1$ 3.7	V
Maximum Low-Level Output Voltage	V_{OL}	$V_{IN}=V_{IH}$ or V_{IL} $I_O=20\mu A$ $I_O=12mA$ $I_O=24mA$	0	0.1 0.26 0.39	0.1 0.33 0.5	0.1 0.4	V
Maximum Input Current	I_{IN}	$V_{IN}=V_{CC}$ or GND		±0.1	±1.0	±1.0	μA
Maximum 3-State Leakage Current	I_{OZ}	Output Enable $=V_{IH}$ $V_{OUT}=V_{CC}$ or GND		±0.5	±5.0	±10.0	μA
Maximum Quiescent Supply Current	I_{CC}	$V_{IN}=V_{CC}$ or GND $I_{OUT}=0\mu A$		8.0	80.0	160.0	μA
Additional Worst Case Supply Current	ΔI_{CC}	per input pin $V_I=2.4V$ other Inputs: at V_{CC} or GND $I_{OUT}=0\mu A$		2.7	2.9	3.0	mA

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS590

Characteristic		Symbol	Conditions†	$T_a = 25°C$ $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$ $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$	Unit
				Typ	Guaranteed Limits			
Maximum Clock Frequency		f_{max}		35	25	20	20	ns
Maximum Propagation Delay, CCK↑ to $\overline{RCO}$		t_{PLH}	$C_L = 50pF$	24	32	40	48	ns
		t_{PHL}		24	32	40	48	
Maximum Propagation Delay, $\overline{CCLR}$↓ to $\overline{RCO}$		t_{PLH}		26	35	44	52	ns
Maximum Propagation Delay, RCK↑ to Q		t_{PLH}		16	21	26	31	ns
		t_{PHL}		16	21	26	31	
Maximum Output Enable Time, $\overline{G}$↓ to Q		t_{PZH}	$R_L = 1k\Omega$ $C_L = 50pF$	18	24	30	36	ns
		t_{PZL}		18	24	30	36	
Maximum Output Disable Time, $\overline{G}$↑ to Q		t_{PHZ}		18	24	30	36	ns
		t_{PLZ}		18	24	30	36	
Minimum Pulse Width	CCK or RCK High or Low	t_w		12	16	20	24	ns
	$\overline{CCLR}$ Low			12	16	20	24	
Minimum Setup Time	$\overline{CCKEN}$↓ before CCK↑	t_{su}		12	16	20	24	ns
	$\overline{CCLR}$↑ before CCK↑			12	16	20	24	
	CCK↑ to RCK↑††			24	32	40	48	
Maximum Input Capacitance		C_{IN}		5				pF
Maximum Output Capacitance		C_{OUT}	Output Disabled	10				pF
Power Dissipation Capacitance*		C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

†† The RCK↑ to CCK↑ setup time ensures that the counter will see stable data from the register output.

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8-Bit Binary Counters with Output Registers

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AC ELECTRICAL CHARACTERISTICS (Input t_r, $t_f \leq 6$ ns), HCTLS591

Characteristic		Symbol	Conditions†	$T_a = 25°C$, $V_{CC} = 5.0V$	KS74HCTLS $T_a = -40°C$ to $+85°C$, $V_{CC} = 5.0V \pm 10\%$		KS54HCTLS $T_a = -55°C$ to $+125°C$, $V_{CC} = 5.0V \pm 10\%$	Unit
				Typ	Guaranteed Limits			
Maximum Clock Frequency		f_{max}		35	25	20	20	ns
Maximum Propagation Delay, CCK↑ to $\overline{RCO}$		t_{PLH}	$C_L = 50pF$, $R_L = 1k\Omega$	24	32	40	48	ns
		t_{PHL}		24	32	40	48	
Maximum Propagation Delay, $\overline{CCLR}$↓ to $\overline{RCO}$		t_{PLH}		26	35	44	52	ns
Maximum Propagation Delay, RCK↑ to Q		t_{PLH}		27	37	46	55	ns
		t_{PHL}		16	21	26	31	
Maximum Output Enable Time, $\overline{G}$↓ to Q		t_{PZL}		18	24	30	36	ns
Maximum Output Disable Time, $\overline{G}$↑ to Q		t_{PLZ}		18	24	30	36	ns
Minimum Pulse Duration	CCK or RCK High or Low	t_w		12	16	20	24	ns
	$\overline{CCLR}$ Low			12	16	20	24	
Minimum Setup Time	$\overline{CCKEN}$↓ before CCK↑	t_{su}		12	16	20	24	ns
	$\overline{CCLR}$↑ before CCK↑			12	16	20	24	
	CCK↑ to RCK↑††			24	32	40	48	
Maximum Input Capacitance		C_{IN}		5				pF
Maximum Output Capacitance		C_{OUT}	Output Disabled					pF
Power Dissipation Capacitance*		C_{PD}						pF

* C_{PD} determines the no-load dynamic power dissipation: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

† For AC switching test circuits and timing waveforms see section 2.

†† The clocks may be tied together, in which case the register state will be one clock pulse behind the counter.

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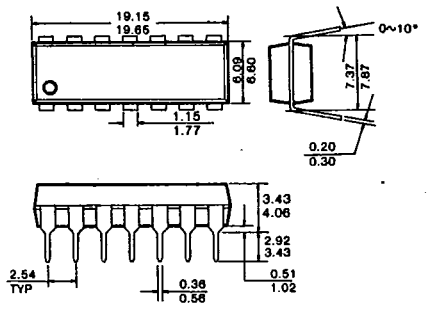
PACKAGE DIMENSIONS

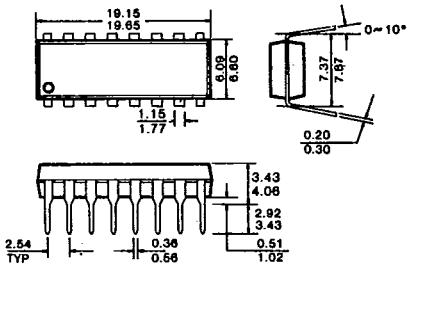
T-90-20

1. PLASTIC PACKAGES

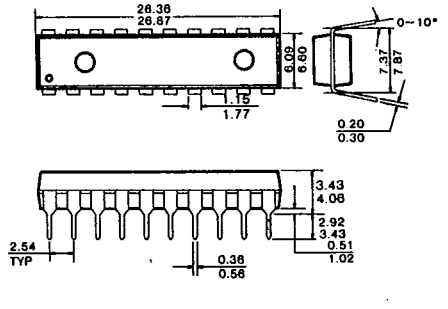
14-Pin Plastic DIP **Units: mm**



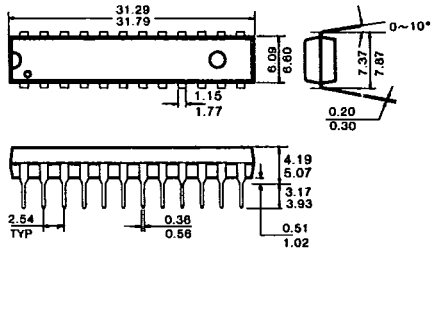
16-Pin Plastic DIP **Units: mm**



20-Pin Plastic DIP **Units: mm**



24-Pin Plastic DIP **Units: mm**



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PACKAGE DIMENSIONS

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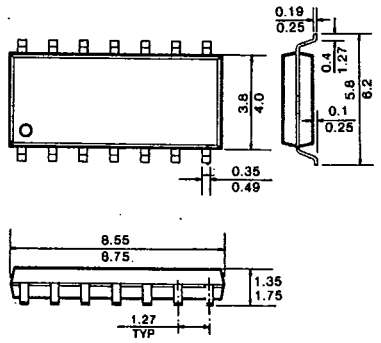
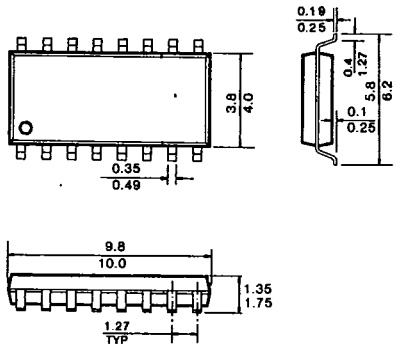
14-Pin SOP

Unit: mm



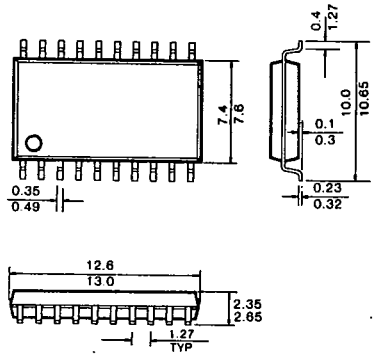
16-Pin SOP

Unit: mm



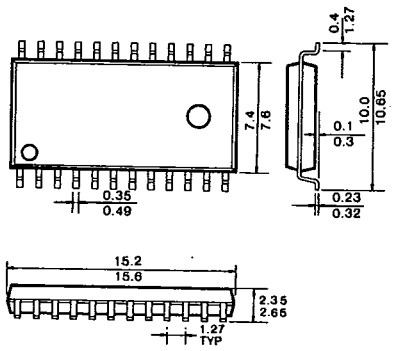
20-Pin SOP

Unit: mm



24-Pin SOP

Unit: mm

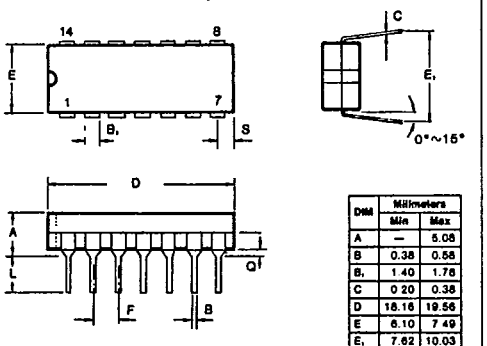


PACKAGE DIMENSIONS

T-90-20

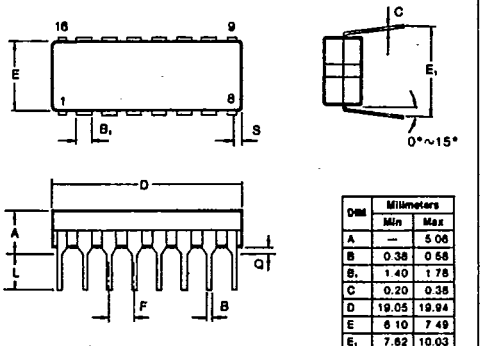
2. CERAMIC PACKAGES

14-Pin Ceramic DIP Units: mm



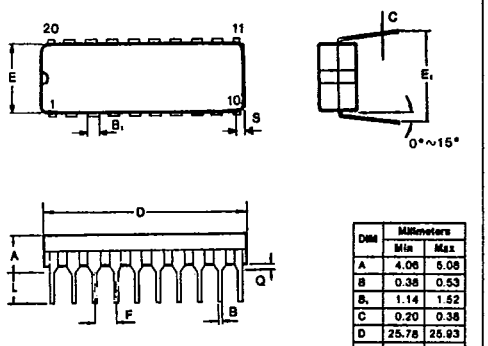
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B1	1.40	1.78
C	0.20	0.38
D	18.16	19.56
E	6.10	7.49
E1	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	1.91	2.29

16-Pin Ceramic DIP Units: mm



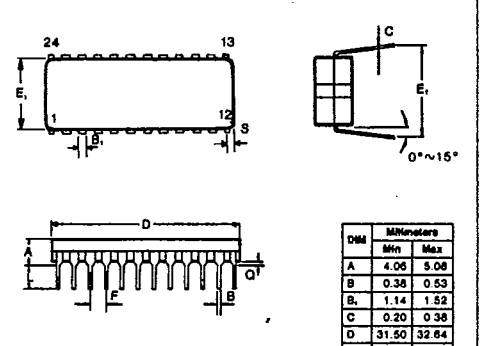
DIM	Millimeters	
	Min	Max
A	—	5.08
B	0.38	0.58
B1	1.40	1.78
C	0.20	0.38
D	19.05	19.94
E	6.10	7.49
E1	7.62	10.03
F	2.54	
L	3.18	4.19
Q	0.51	1.02
S	0.51	1.14

20-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B1	1.14	1.52
C	0.20	0.38
D	25.78	25.93
E	6.10	6.60
E1	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.38	0.89
S	0.51	1.14

24-Pin Ceramic DIP Units: mm



DIM	Millimeters	
	Min	Max
A	4.06	5.08
B	0.38	0.53
B1	1.14	1.52
C	0.20	0.38
D	31.50	32.64
E	7.24	7.75
E1	7.77	7.98
F	2.54	
L	3.73	4.01
Q	0.508	1.778
S	1.65	1.93

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