SSM-2110
TRUE RMS-TO-DC CONVERTER

FEATURES

- Multiple Output Options (Absolute Value, RMS, Log RMS, Log Absolute Value, Average Absolute Value)
- Wide Dynamic Range 100dB
- Prebias Option for Fast Response at Low Signal Levels
- On-Chip Log Output Amplifier
- Optional Internal Log Output Temperature Compensation
- Low Drift Internal Voltage Reference
- Low Cost

APPLICATIONS

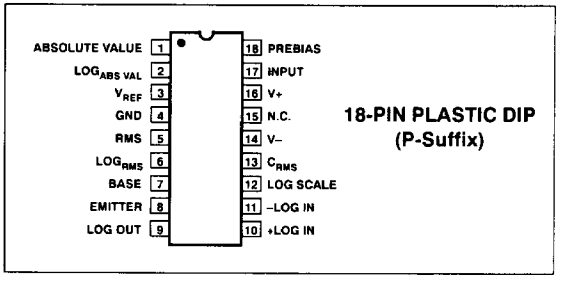
- Audio Dynamic Range Processors
- Audio Metering Systems
- Digital Multimeters
- Noise Testers
- Panel Meters
- Power Meters
- Process Control Systems

GENERAL DESCRIPTION

The SSM-2110 is a true RMS-to-DC converter designed to provide multiple linear and logarithmic output options. The linear outputs, true RMS and absolute value, can be obtained simultaneously with the absolute value output configurable to give a peak function. The logarithmic outputs can provide log RMS, log absolute value or log average absolute value. Full on-chip temperature compensation is available for each output option.

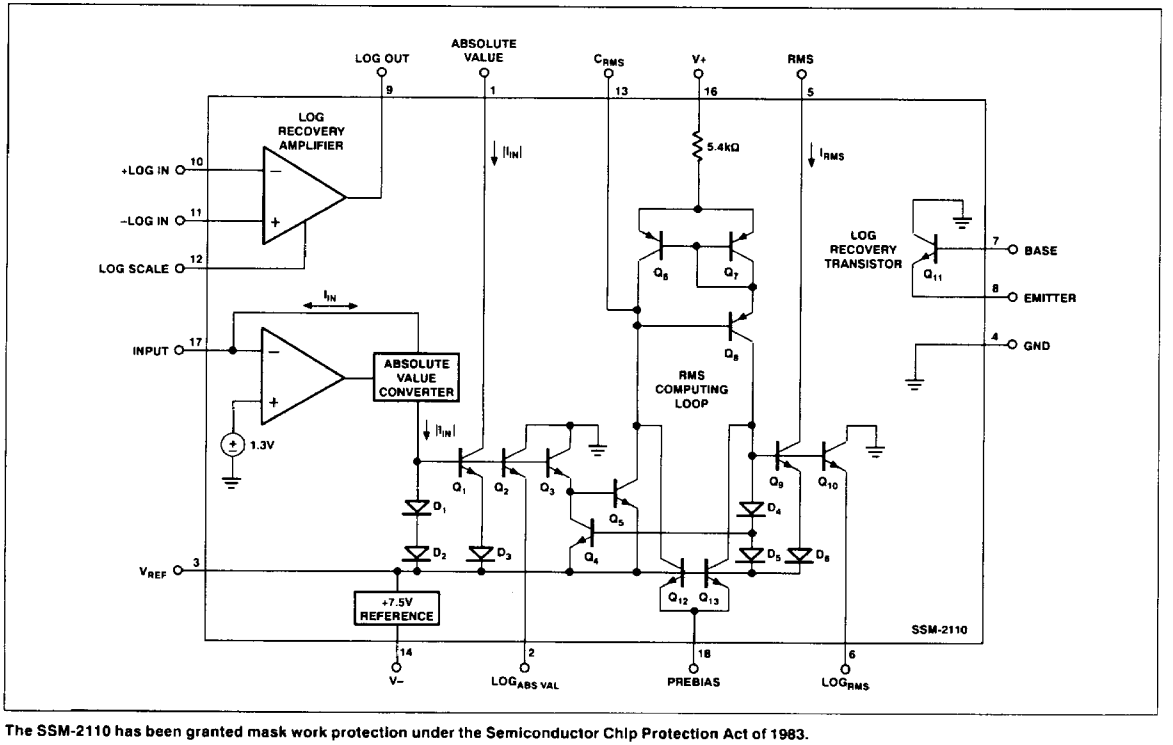
Continued

PIN CONNECTIONS



18-PIN PLASTIC DIP (P-Suffix)

FUNCTIONAL DIAGRAM



GENERAL DESCRIPTION *Continued*

The SSM-2110 has a dynamic range of 100dB. A unique on-chip prebias circuit enables the users to trade dynamic range at low signal levels for a faster response time. As a precision level detector, the SSM-2110 has applications in digital multimeters, panel meters, process control and audio systems.

ORDERING INFORMATION

PACKAGE	OPERATING TEMPERATURE RANGE
PLASTIC 18-PIN	
SSM2110P	–25°C to +75°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Storage Temperature Range ..... –65°C to +150°C
Lead Temperature Range
(Soldering, 60 sec) ..... +300°C
Junction Temperature ..... +150°C
Operating Temperature Range ..... –25°C to +75°C

PACKAGE TYPE	Θ_{JA} (Note 1)	Θ_{JC}	UNITS
18-Pin Plastic DIP (P)	75	33	°C/W

NOTE:
1. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for P-DIP.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$ and $R_{SCALE} = 4.7k\Omega$, unless otherwise noted.

			SSM-2110			
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Dynamic Range	DR	$30nA_{p-p} \le I_{INp-p} \le 3mA_{p-p}$	100	110	–	dB
Unadjusted Gain		$I_{IN} = \pm 1mA$	0.95	1.0	1.05	
Error (Mean or RMS)			–	–	±0.5	dB
Output Offset Current	I_{OOS}	$I_{IN} = \pm 1mA$	–	5	15	nA
I_{OS} Shift	ΔI_{OOS}	$R_{PREBIAS} = 3M\Omega$	–	50	120	nA
Crest Factor @ $1mA_{RMS}$	CF	For 0.1dB Additional Error For 0.5dB Additional Error For 1.0dB Additional Error	– – –	2.5 5 8	– – –	
RMS Filter Time Constant	t_{CON}	$I_{RMS} > 10\mu A_{RMS}$		$11k\Omega \times C_{INT}$		
Frequency Response (Sine Wave)						
For 0.1dB Additional Error		$I_{IN} > 1mA_{RMS}$ $I_{IN} > 10\mu A_{RMS}$ $I_{IN} > 1\mu A_{RMS}$	– – –	400 10 2	– – –	
For 0.5dB Additional Error	BW	$I_{IN} > 1mA_{RMS}$ $I_{IN} > 10\mu A_{RMS}$ $I_{IN} > 1\mu A_{RMS}$	– – –	1000 50 7.5	– – –	kHz
–3dB Bandwidth		$I_{IN} > 1mA_{RMS}$ $I_{IN} > 10\mu A_{RMS}$ $I_{IN} > 1\mu A_{RMS}$	– – –	1500 300 50	– – –	
Log Amp Output Offset Current (Pin 9)	$I_{OOS\ -LOG}$		–	±3.3	±13	µA
Max Log Amp Output (Pin 9)	$I_{OUT\ -LOG}$		±250	±265	±288	µA
Log Scale Factor (Pin 2 or Pin 6)			–	+6	–	mV/dB
Log Mode Zero Crossing (Mean or RMS, Pin 9)		RMS In To Get Zero Out (See Figure 7)	–	10	–	µA
Log Amp Linearity (Pin 9)		$-240mV < V_{PIN\ 10} - V_{PIN\ 11} < +240mV$	–	0.1	0.25	dB
Log Output Tempco	T_C	$0°C < T_A < +70°C$	–	±75	–	ppm/°C
V_{REF} (Pin 3 to V–)			6.7	7.5	7.8	V

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $T_A = +25°C$ and $R_{SCALE} = 4.7k\Omega$, unless otherwise noted. *Continued*

PARAMETER	SYMBOL	CONDITIONS	SSM-2110 MIN	TYP	MAX	UNITS
Positive Supply Current	I_S+	$I_{IN} = 0$	480	–	920	µA
Negative Supply Current	I_S-		2.1	–	3.3	mA
Supply Voltage Range	V_S		±12	–	±18	V

Specifications subject to change; consult latest data sheet.

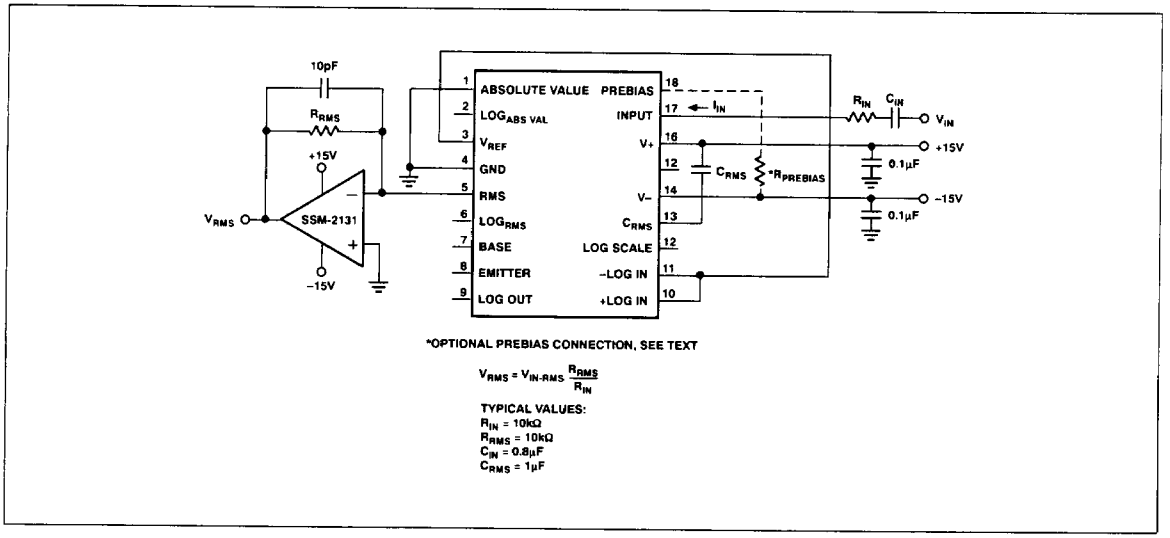


FIGURE 1: *RMS Output Circuit*

THE RMS COMPUTING LOOP

The RMS section of the SSM-2110 consists of an implicit RMS computing loop whose output follows the equation:

$$I_O = \frac{I_{IN}^2}{\overline{I_O}}$$

where $\overline{I_O}$ is the average of I_O

The time constant for averaging is determined by the value of the averaging cap C_{RMS} (on pin 13) and an internal resistor whose effective value is 10.8kΩ. A very low leakage capacitor must be used for C_{RMS} to prevent limiting the dynamic range.

Increasing the value of C_{RMS} will result in lower levels of ripple on the RMS Output at the expense of an increase in settling time for a step change in the input signal amplitude. This is a proportional relationship where increasing the value of C_{RMS} tenfold results in a tenfold increase in the settling time.

For the circuit in Figure 1, the peak-to-peak ripple approximately follows the equation:

$$V_{RIPPLE(p-p)} = \frac{2\sqrt{2} \times V_{RMS}}{4\pi f R_{INT} C_{RMS}} \times \frac{R_{RMS}}{R_{IN}}$$

where $R_{INT} \approx 10.8k\Omega$

The settling time of the SSM-2110 also depends on the frequency of the signal being processed. It takes approximately 100ms for a $300\mu A_{p-p}$, 50Hz signal to settle within 0.1% when $C_{RMS} = 1\mu F$, and it takes 10ms for a 500Hz signal to settle within the same value. The general rule is a tenfold increase in frequency causes a tenfold reduction in settling time. The settling time also varies with the amplitude of the signal. The larger the signal level the faster the settling time.

INPUT

The INPUT (pin 17) is an AC virtual ground with approximately +1.3V DC offset voltage. The useful dynamic range of input current the device can process is 100dB (3mA$_{p-p}$ to 30nA$_{p-p}$). The input RC network is usually chosen to allow close to 20dB of headroom in order to process high crest factor signals and provide a DC block below a given frequency band. Since in every case the ratio of R_{OUT} (R_{AV} and R_{RMS}) to R_{IN} determines the overall gain of the circuit, R_{OUT} must also be considered when selecting the low frequency breakpoint. The maximum recommended values for R_{OUT} vary from 4kΩ to 10kΩ for the circuits in Figures 1, 3, 4, and 5.

Referring to the circuit in Figure 3, and assuming a gain of 1 is desired, R_{IN} should be set to 4kΩ (R_{RMS} and R_{AV} = 4kΩ). Based on this value of R_{IN}, C_{IN} should be 2μF to place the subsonic filter pole at 20Hz. If you wish to limit the lower frequency to something other than 20 Hz then C_{IN} should be changed accordingly. The low frequency pole is governed by the simple equation

$$f_{MIN} = 1/2\pi R_{IN} C_{IN}$$

C_{IN} should be a very low leakage capacitor to avoid impairing the dynamic range at low signal levels (many electrolytic types will not work).

The choice of R_{IN} = 10kΩ in Figure 1 is good for processing 0dBV reference signals. Given a nominal signal level of 0dBV (2.828V$_{p-p}$ = 1 V_{RMS}), this voltage across the 10kΩ input resistor gives a nominal input current of 283μA$_{p-p}$, which allows 20dB of headroom. The three other common choices for R_{IN} are 4kΩ, 5kΩ and 8kΩ, which provide 12dB, 14dB, and 18dB respectively.

The values of C_{IN}, R_{IN} and R_{OUT} can be changed accordingly to vary output levels to system requirements.

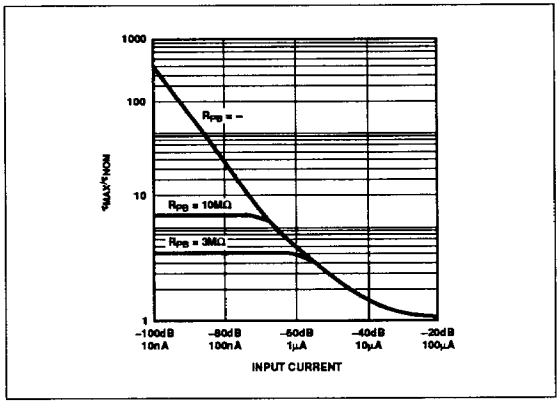


FIGURE 2: *Normalized Time Constant Relative to 1mA$_{RMS}$*

The PREBIAS pin (pin 18), can be used to increase the speed of the RMS computing loop at low signal levels at some expense to the dynamic range. Below a 10μA$_{RMS}$ input level, the time constant of the RMS loop will increase from its nominal value by a factor of 10 for every 20dB drop in level.

By use of the PREBIAS pin, one can ensure that the loop time constant will not increase above a chosen maximum as the signal level continues to decrease. The equation relating the maximum time constant increase to the value of $R_{PREBIAS}$ connected between pin 18 and V– is given by:

$$\frac{\tau_{MAX}}{\tau_{NOM}} = \frac{10\mu A \times R_{PREBIAS}}{6.8V} \quad \text{(See Figure 2)}$$

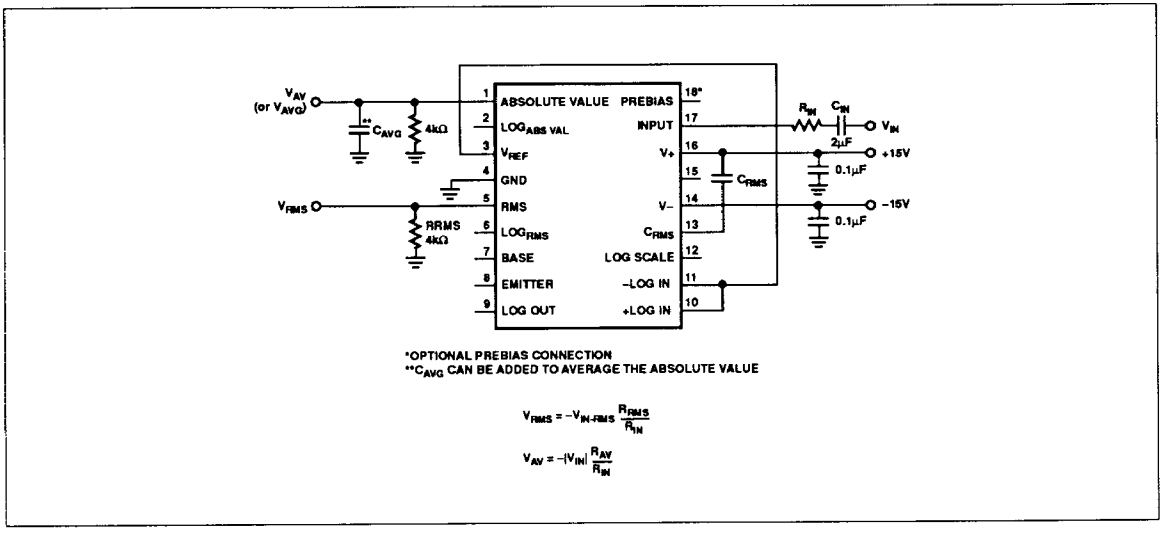


FIGURE 3: *Simple RMS/Absolute Value/Average Absolute Value Configuration*

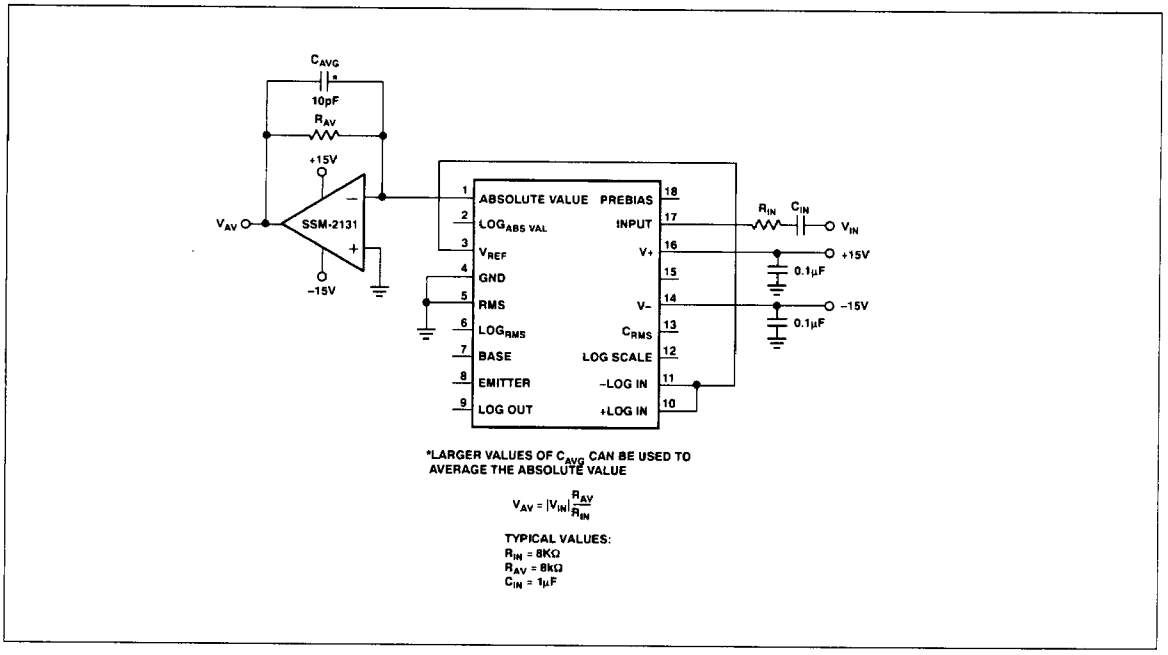


FIGURE 4: *Absolute Value and Average Absolute Value Output*

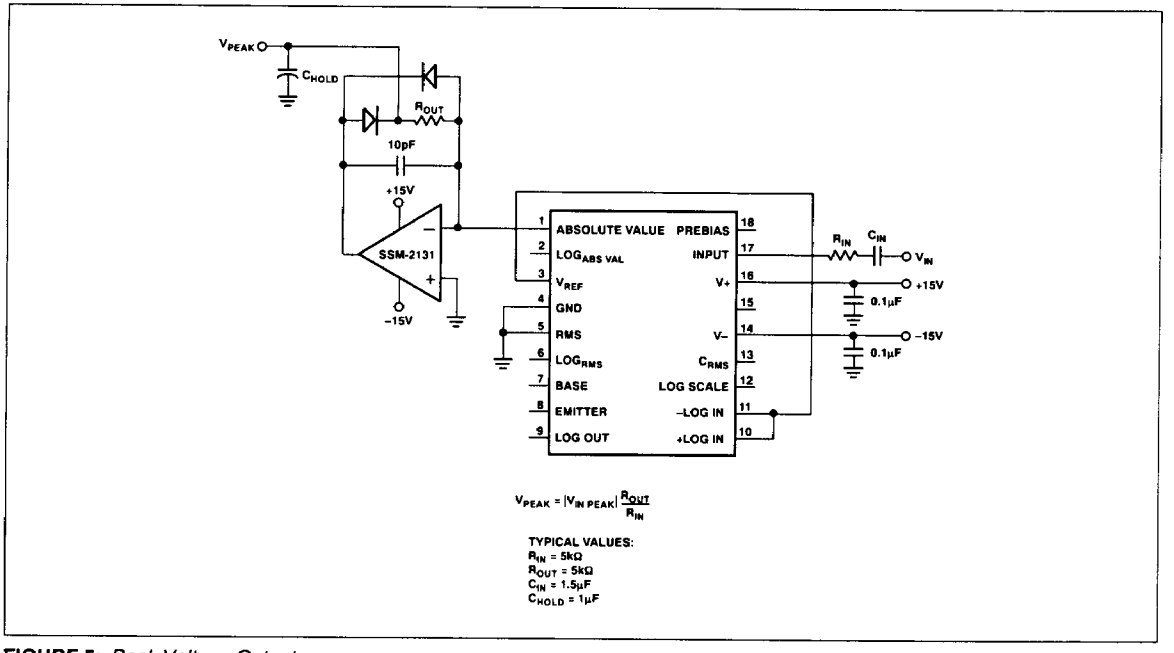


FIGURE 5: *Peak Voltage Output*

LINEAR OUTPUTS (ABSOLUTE VALUE AND RMS)

The instantaneous absolute value of the input signal appears as a current absolute value pin (pin 1). The true RMS value of the input signal similarly appears as a current into the RMS pin (pin 5). With ±15 volt supplies, the voltage compliance on these outputs is from +15 to −6 volts. For simple applications it is possible to convert these currents to negative output voltages by connecting a resistor in series with the pin(s) to ground (see Figure 3). For a maximum $3mA_{p-p}$ input signal, the resistor(s) value should be 4.0kΩ or less. To obtain an average of the absolute value output, capacitor C_{AVG} can be added in parallel with R_{AV}.

More commonly, a positive going voltage at low impedance is desired as an output. This can be accomplished by connecting a linear output pin to the virtual ground of an op amp configured as a current-to-voltage converter (see Figures 1 and 4). The scale factor for the conversion is determined by the value of R_{IN} and the feedback resistor (R_{RMS} or R_{AV}).

For the absolute value circuit in Figure 4, a maximum feedback resistor (R_{AV}) of 8kΩ allows maximum swing of the SSM-2131 output amplifier. Given a maximum output signal of $1.5mA_{PEAK}$ the SSM-2131 will be able to swing to +12V. If values larger than 8kΩ are used, then signal clipping may result.

For the RMS output circuit in Figure 1, the maximum feedback resistor (R_{RMS}) can be 10kΩ since the RMS level should never exceed 1.2mA.

A peak output can be implemented by using the circuit in Figure 5. The output scale factor is determined by R_{OUT}/R_{IN}. The decay time constant is equal to the product $R_{OUT}C_{HOLD}$. For this circuit, the feedback resistor (R_{OUT}) should be kept below 5kΩ.

A small capacitor (10pF) is usually added in parallel with the feedback resistor for stability particularly if a high slew rate JFET input op amp is used. In Figure 4, this capacitor (C_{AVG}) can be made large to obtain an average of the absolute value output. If the averaging circuit is implemented then R_{IN} can be increased to a maximum of 10kΩ since the 1.5mA peaks will no longer be present.

If the signal levels being processed are less than $3mA_{p-p}$ then the above mentioned feedback resistors can be increased accordingly.

The circuits in Figures 1 and 4 can be connected at the same time providing the user with multiple functions from a single SSM-2110. R_{IN}, R_{RMS} and R_{AV} should be set so that clipping does not occur.

The linear output pins must be kept within their voltage compliance range for proper device operations. An unused linear output must always be terminated, preferably to ground.

LOG OUTPUTS (LOG_{RMS} AND $LOG_{ABS\ VAL}$)

The log of the instantaneous absolute value and the log of true RMS of the input signal appears as voltages on pins 2 and 6 respectively. However, these outputs must be buffered, level shifted and, in many applications, temperature compensated in order to be made useful.

The log recovery transistor is an internal level shifting component which may be switched between the two log outputs. This will reference the log output(s) to the internal voltage regulator which is about 7.5V above the negative supply (see Figure 6).

Figures 6, 7, and 8 show the recommended connection between the log output transistor Q_2 or Q_{10}, and the log recovery transistor Q_{11}. Note that although the log recovery transistor can be switched between the two log outputs, only one log output can be recovered at a time. With the resistor values R_{REF1} and R_{REF2} shown, the output swing at the emitter of Q_{11} over the dynamic

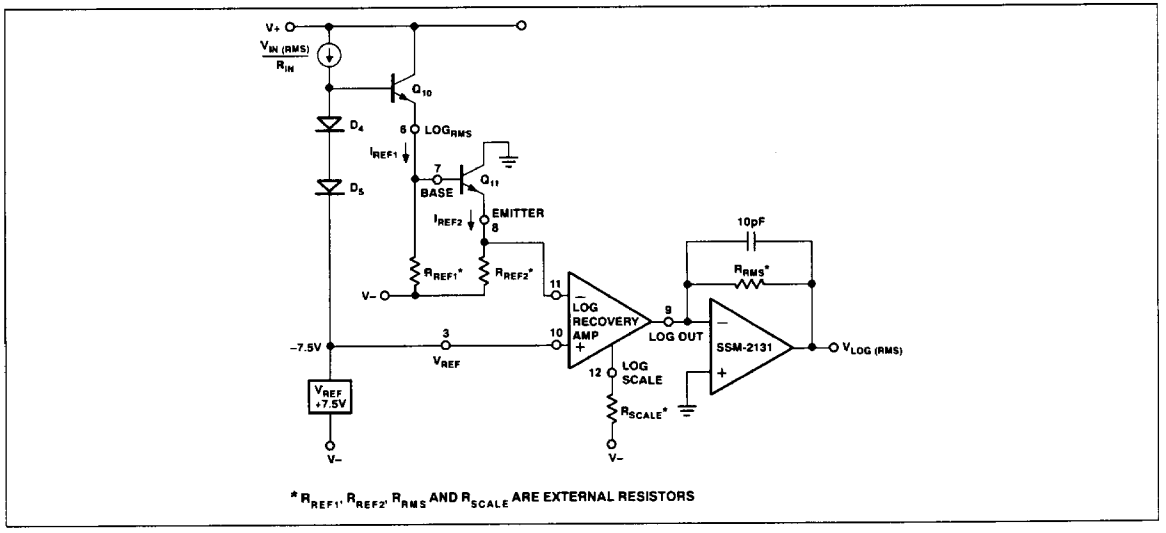
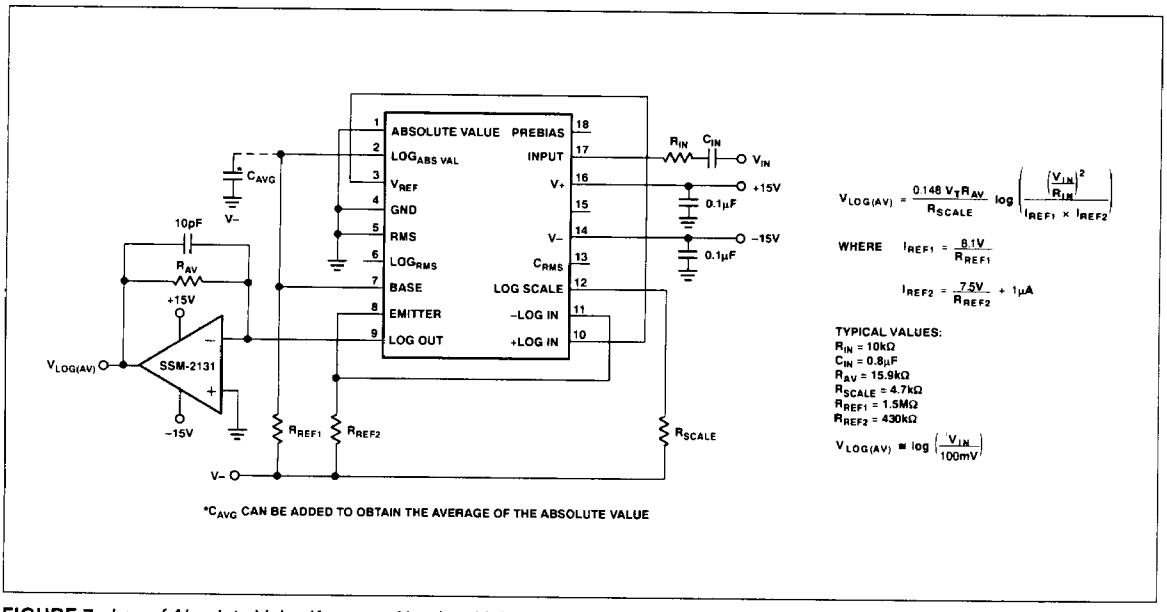


FIGURE 6: *Log Recovery Circuit*



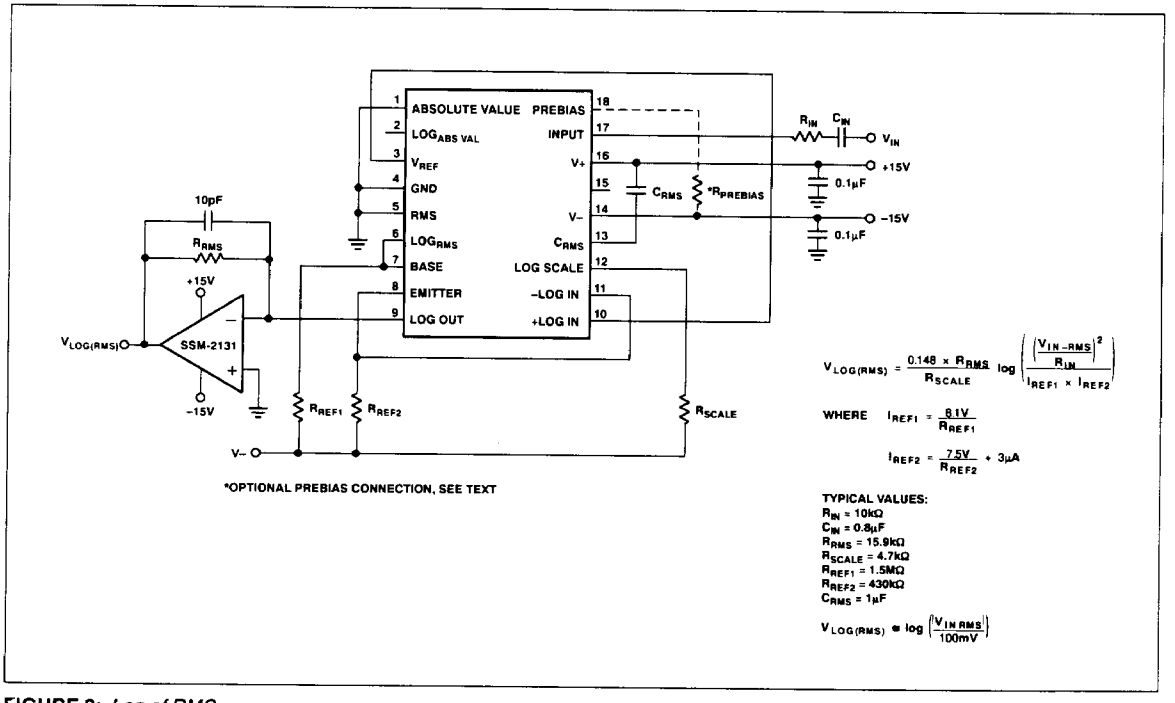
$$V_{LOG(AV)} = \frac{0.148\ V_T R_{AV}}{R_{SCALE}} \log\left(\frac{\left(\frac{V_{IN}}{R_{IN}}\right)^2}{I_{REF1} \times I_{REF2}}\right)$$

$$I_{REF1} = \frac{8.1V}{R_{REF1}}$$

$$I_{REF2} = \frac{7.5V}{R_{REF2}} + 1\mu A$$

$$V_{LOG(AV)} \approx \log\left(\frac{V_{IN}}{100mV}\right)$$

FIGURE 7: *Log of Absolute Value/Average Absolute Value*



$$V_{LOG(RMS)} = \frac{0.148 \times R_{RMS}}{R_{SCALE}} \log\left(\frac{\left(\frac{V_{IN-RMS}}{R_{IN}}\right)^2}{I_{REF1} \times I_{REF2}}\right)$$

$$I_{REF1} = \frac{8.1V}{R_{REF1}}$$

$$I_{REF2} = \frac{7.5V}{R_{REF2}} + 3\mu A$$

$$V_{LOG(RMS)} \approx \log\left(\frac{V_{IN\,RMS}}{100mV}\right)$$

FIGURE 8: *Log of RMS*

range of the device will be roughly symmetrical about the internal negative voltage reference. Also, the output impedance will be low enough to drive the log amplifier's input(s) without introducing significant errors. The bias current into the pins of the log amplifier is typically less than 1μA but can be as high as 2μA. For this reason the current through the log recovery transistor Q_{11} should always be set higher than 5μA. The current I_{REF1} should not be set too high (above 50μA) because the base current of Q_{10} induces errors in the RMS computing loop. If higher reference currents are required then they should be taken care of by changing the current through Q_{11}. This can be done by changing R_{REF2}. The Log Recovery Amplifier Section explains this in more detail.

The output sensitivity at EMITTER (pin 8) is about +60mV for every 10dB of signal level increase at 25°C. This sensitivity has a temperature coefficient of +3300ppm/°C.

The log of absolute value output can be converted to a log of mean value by connecting a capacitor between $LOG_{ABS\ VAL}$ (pin 2) and V– (see Figure 7). Since this is an emitter follower output, the response to a large-signal level increase will be fast while the time constant of the output following a large-signal level decrease will be determined by the product of capacitor C_{AVG} and resistor R_{REF1}.

One might think that connecting a capacitor to the log output would produce the average of the log of the absolute value. However, since the capacitor enforces an AC ground at the emitter of the output transistor, the capacitor charging currents are proportional to the antilog of the signal at the base. Since the base voltage is the log of the absolute value, the log and the antilog terms cancel, and the capacitor is charged as a linear integrator with a current directly proportional to the absolute value of the input current. This effectively inverts the order of the averaging and logging operations. The signal at the output, therefore, is the log of the average of the absolute value of the input signal.

LOG RECOVERY AMPLIFIER (PINS 9,10, 11 AND 12)

The log recovery amplifier is a linearized voltage-to-current transconductor whose gain can be made proportional to absolute temperature. It is used to reference the log output(s) to ground and also to temperature compensate the V_T (KT/q) terms in the log output recovery transistors (Q_2/Q_{10} and Q_{11}).

One input of the log recovery amplifier is usually connected to EMITTER (the emitter of the log recovery transistor–pin 8) while the other is connected to V_{REF} (pin 3).

Figure 6 shows the internal and external connections used to obtain an output voltage equal to $V_{LOG(RMS)}$. The transfer characteristic of the log recovery transistors is given by the following equation:

$$\Delta V_{IN} = V_T \times \ln\left(\frac{(V_{IN(RMS)}/R_{IN})^2}{I_{REF1} \times I_{REF2}}\right)$$

where, $I_{REF1} \approx \left(\frac{8.1V}{R_{REF1}}\right)$

$$I_{REF2} \approx \left(\frac{7.5V}{R_{REF2}}\right) + 1\mu A$$

The transfer characteristic of the log recovery amplifier is given by the following equation:

$$I_{OUT} = \frac{64mV\ \Delta V_{IN}}{R_{SCALE} V_T}$$

Combining the two equations yields the overall transfer characteristic for the ouput voltage $V_{LOG(RMS)}$:

$$V_{LOG(RMS)} = \frac{0.148 \times R_{RMS}}{R_{SCALE}} \times \log\left(\frac{(V_{IN}/R_{IN})^2}{I_{REF1} \times I_{REF2}}\right)$$

where, $I_{REF1} \approx \left(\frac{8.1V}{R_{REF1}}\right)$

$$I_{REF2} \approx \left(\frac{7.5V}{R_{REF2}}\right) + 1\mu A$$

Ideally this voltage is completely independent of temperature. However, due to the temperature coefficient of several transistors internal to the SSM-2110, this is not entirely true. The temperature coefficient is approximately ±75ppm/°C.

With the values shown in Figures 7 and 8, this transfer function corresponds to an output change of 50mV/dB. The reference current is set to 10μA to provide the widest possible dynamic range. The following results can be expected for the circuit in Figure 8:

$V_{IN\ (RMS)}$	100μV	1mV	10mA	100mV	1V	10V
$I_{IN\ (RMS)}$	10nA	100nA	1μA	10μA	100μA	1mA
$V_{LOG\ OUT}$	–3V	–2V	–1V	0V	1V	2V

An R_{SCALE} value of approximately 4.7kΩ gives the best overall linearity and temperature compensation performance. This is an improvement of about a factor of 40 over the uncompensated drift. A 2kΩ resistor in series with a silicon diode can be connected from LOG SCALE (pin 12) to the negative supply to defeat the temperature compensation for certain applications such as compressor/limiters where the log drift will cancel the thermal gain drift of a VCA's dB/volt control port.

The maximum output current for both the compensated and uncompensated examples above is ±250μA. This output current is converted to a voltage with the circuits in Figures 7 and 8. For these circuits this corresponds to a maximum output voltage of ±3.975V. If R_{SCALE} is changed from the nominal value of 4.7kΩ the maximum output current will also change by the following equation:

$$I_{LOG\ OUT\ (MAX)} = \frac{1.18V}{R_{SCALE}}$$

If the log recovery amplifier is not used, +LOG IN (pin 10) and –LOG IN (pin 11) must be connected to V_{REF} (pin 3) for proper operation of the rest of the circuit.

It is possible to use one of the log configurations in Figure 7 or 8 in conjunction with the linear output circuits (Figures 1, 3, 4 and 5) but care must be taken in choosing the appropriate resistor values. This provides the user with substantial flexibility from a single device.

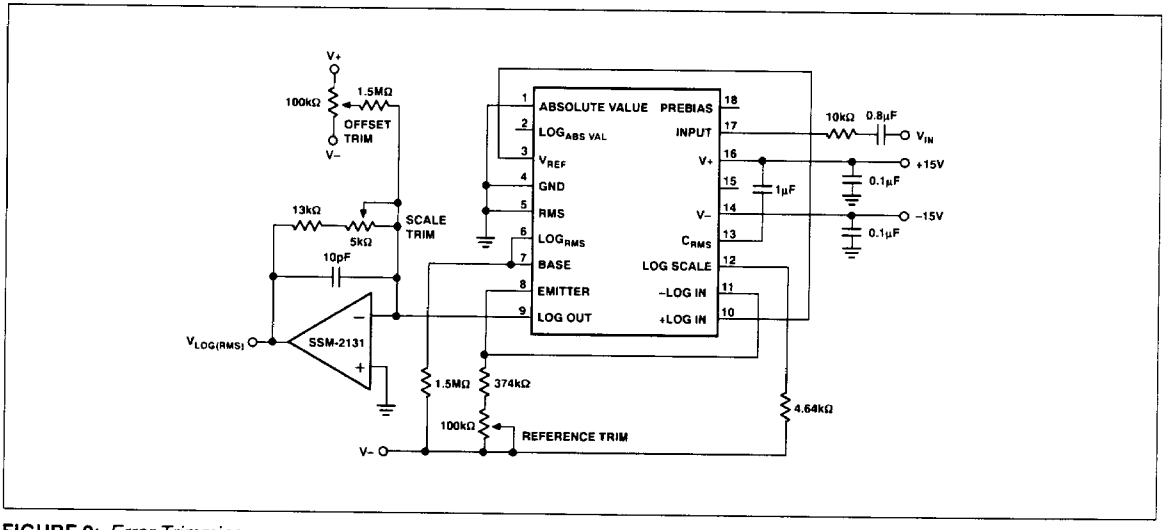


FIGURE 9: *Error Trimming*

ERROR TRIMMING

The offset, reference and scale factor trims (Figure 9) can be used to improve the overall accuracy of the device. The correct procedure for trimming out the various errors is as follows. First, +LOG IN (pin 10) and –LOG IN (pin 11) should be connected to V_{REF} (pin 3). The offset trim should be adjusted to achieve 0V at the $V_{LOG(RMS)}$ output. This nulls out any DC errors due to offsets in the log recovery amplifier. Second, reconnect the ±LOG IN pins as shown in Figure 9. Apply an input signal of $100mV_{RMS}$ ($10\mu A_{RMS}$). Adjust the reference trim to obtain 0V at the $V_{LOG(RMS)}$ output. This compensates for the input bias current of the log recovery amplifier and other errors. It sets the reference current to $10\mu A$. Third, change the input signal to $1V_{RMS}$ ($100\mu A_{RMS}$). Adjust the scale trim to obtain 1.000V at the $V_{LOG(RMS)}$ output. This adjusts the scale factor to obtain 1V/20dB (50mV/dB). If other reference currents or scale factors are used then steps 2 and 3 will have to be changed accordingly.

This same procedure can be used for the log absolute value and log average absolute value configurations. If the log recovery amplifier is not used then the circuit in Figure 10 should be used to trim the offsets.

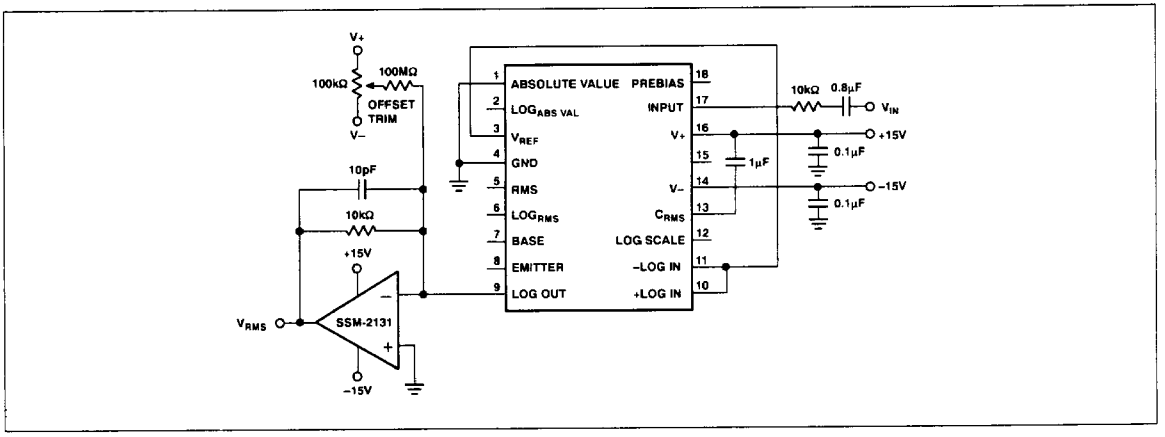
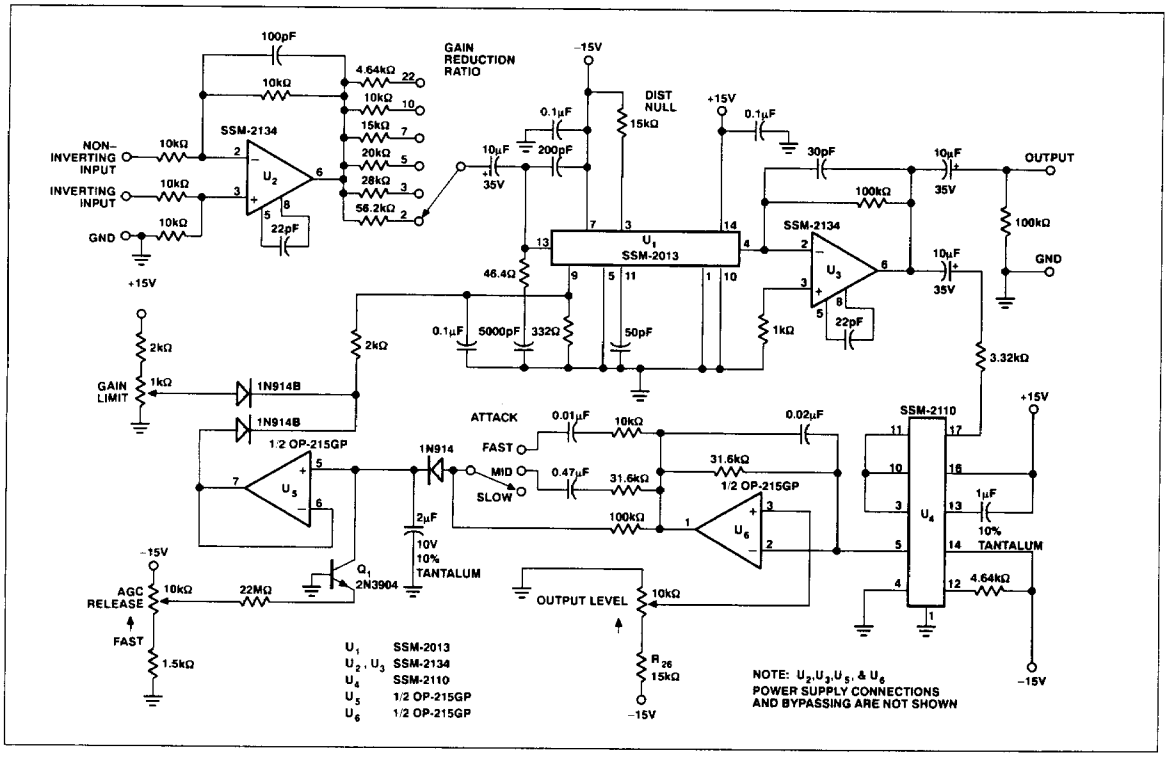


FIGURE 10: *Offset Trimming*

WAVEFORM	RMS	AVERAGE OF ABSOLUTE VALUE (A_{AV})	CREST FACTOR = $\frac{V_P}{RMS}$
V_P SINE WAVE	$\frac{V_P}{\sqrt{2}}$	$\frac{2 \cdot V_P}{\pi}$	$\sqrt{2} = 1.414$
V_P SQUARE WAVE	V_P	V_P	1
V_P TRIANGLE WAVE	$\frac{V_P}{\sqrt{3}}$	$\frac{V_P}{\sqrt{2}}$	$\sqrt{3} = 1.732$
$2V_P$ GAUSSIAN NOISE	RMS	$\sqrt{\frac{2}{\Pi}} \times RMS$	Typically varies from 1 to 6 depending on the characteristic of the noise. Theoretically, the crest factor is unlimited.

FIGURE11: *RMS, Average of Absolute Value and Crest Factors for Different Waveforms*



TYPICAL APPLICATIONS

AUTOMATIC GAIN CONTROL (AGC) AMPLIFIER

The automatic gain control amplifier shown below features selectable gain reduction compression ratios and time domain adjustable AGC attack and release. The design employs the SSM-2013 VCA, SSM-2110 true RMS-to-DC converter, two SSM-2134 low noise op amps and an OP-215 FET input op amp.

For additional information about this circuit, please see PMI application note AN-116.