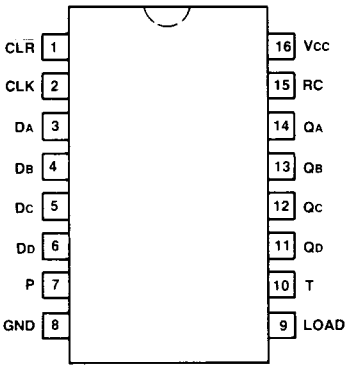
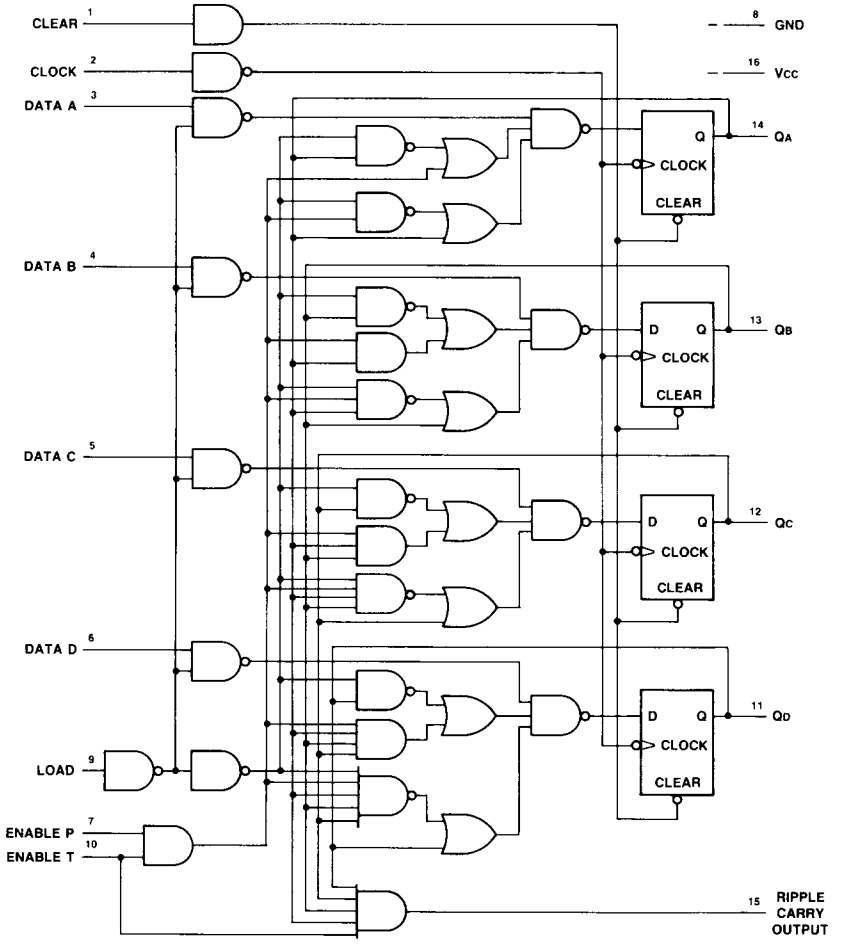
Binary Direct Clear Synchronous 4-Bit Counter

The LS161 is a bipolar, NPN, sealed-junction, silicon integrated circuit. It is manufactured in low-power Schottky technology and is available in a wire-bonded, 16-pin plastic DIP or surface mount package. This device is a high-speed, modulo-16 binary counter with synchronously preset outputs. It features look-ahead circuitry for use in cascadable counting applications.



Logic Diagram



Electrical Characteristics

V_{CC} = 5.0 ±0.5 V, T_A = −55 to +125°C (WA-LS)
V_{CC} = 5.0 ±0.25 V, T_A = 0 to 70°C (WP90349L1)
V_{CC} = 5.0 ±0.5 V, T_A = −40 to +85°C (WA-LSD, WP90405L1)

		WA-LS		WP, WA-LSD		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**
Output Voltage, V_{CC} = 4.5 V (WA-LS), 4.75 V (WP, WA-LSD)						
Low, I_{OL} = 4.0 mA	V_{OL}	—	0.4	—	0.4	V
I_{OL} = 8.0 mA	V_{OL}	—	0.5	—	0.5	V
High, I_{OH} = −0.4 mA	V_{OH}	2.5	—	2.7	—	V
Input Voltage, V_{CC} = 4.5 V (WA-LS), 4.75 V (WP, WA-LSD)						
Low	V_{IL}	—	0.7	—	0.8*	V
High	V_{IH}	2.0	7.5	2.0	5.5	V
Clamp, I_{IN} = −18.0 mA	V_{IK}	—	−1.5	—	−1.5	V
Input Current, V_{CC} = 5.5 V (WA-LS), 5.25 V (WP, WA-LSD)						
Low, V_{IL} = 0.4 V						
Data, Clear, Enable P	I_{IL}	—	−0.4	—	−0.4	mA
Enable T, Clock, Load	I_{IL}	—	−0.8	—	−0.8	mA
High, V_{IH} = 2.7 V						
Data, Clear, Enable P	I_{IH}	—	20.0	—	20.0	μA
Enable T, Clock, Load	I_{IH}	—	40.0	—	40.0	μA
@ V_I max, V_I = 7.0 V (WA-LS), 5.5 V (WP, WA-LSD)						
Data, Clear, Enable P	I_I	—	0.1	—	0.1	mA
Load, Clock, Enable T	I_I	—	0.2	—	0.2	mA
Output Current, V_{CC} = 5.5 V (WA-LS), 5.25 V (WP, WA-LSD)						
Short-Circuit	I_{OS}	−20.0	−100.0	−20.0	−100.0	mA
Supply Current, V_{CC} = 5.5 V (WA-LS), 5.25 V (WP, WA-LSD)						
Output Low	I_{CCL}	—	32.0	—	32.0	mA
Output High	I_{CCH}	—	31.0	—	31.0	mA

* WA-LSD, WP90405L1: V_{IL} = 0.7 V

Timing Characteristics

V_{CC} = 5.0 V, T_A = 25°C, C_L = 15 pF

		WA-LS		WP, WA-LSD		
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Units**
Propagation Delay						
Clock-to-Ripple Carry Output						
Low-to-High	t_{PLH}	—	30.0	—	35.0	ns
High-to-Low	t_{PHL}	—	28.0	—	35.0	ns
Clock-to-Any Q						
Low-to-High	t_{PLH}	—	24.0	—	24.0	ns
High-to-Low	t_{PHL}	—	27.0	—	27.0	ns
Enable T-to-Ripple Carry Output						
Low-to-High	t_{PLH}	—	14.0	—	14.0	ns
High-to-Low	t_{PHL}	—	14.0	—	14.0	ns
Clock-to-Any Q						
High-to-Low	t_{PHL}	—	28.0	—	28.0	ns
Operating Conditions						
Set-up Delay						
Data-to-Clock, Low	t_{DSL}	20.0	—	20.0	—	ns
High	t_{DSH}	20.0	—	20.0	—	ns
Parity Enable- or Reset-to-Clock, Low	t_{DSL}	20.0	—	20.0	—	ns
High	t_{DSH}	20.0	—	20.0	—	ns
Count Enable-to-Clock, Low	t_{DSL}	25.0	—	20.0	—	ns
High	t_{DSH}	25.0	—	20.0	—	ns
Hold Delay						
Data-to-Clock, Low	t_{DHL}	0	—	3.0	—	ns
High	t_{DHH}	0	—	3.0	—	ns
Parity Enable- or Reset-to-Clock, Low	t_{DHL}	0	—	3.0	—	ns
High	t_{DHH}	0	—	3.0	—	ns
Count Enable-to-Clock, Low	t_{DHL}	0	—	3.0	—	ns
High	t_{DHH}	0	—	3.0	—	ns
Minimum Pulse Width						
Clock Pulse Width, Low	$t_{W\varnothing L}$	25.0	—	25.0	—	ns
High	$t_{W\varnothing H}$	15.0	—	25.0	—	ns
Clear Pulse Width	t_W	15.0	—	20.0	—	ns
Clearing Time	t_{CL}	20.0	—	20.0	—	ns
Maximum Clock Frequency	f_{max}	30.0	—	25.0	—	MHz

Maximum Ratings

Power supply voltage (V_{CC}) . . . . . 7.0 V
Operating temperature (T_A) . . . . . WA-LS: −55 to +125°C
WP90349L1: 0 to 70°C
WA-LSD, WP90405L1: −40 to +85°C
Storage temperature (T_{stg}) . . . . . −65 to +150°C

Maximum ratings are defined as the limiting conditions that the user can apply to the device under all variations of circuit and environmental conditions. If any rating is exceeded, permanent damage to the device may result.

Bonding or soldering of the external leads of this device can be performed safely at temperatures up to 300°C.

Timing Diagrams

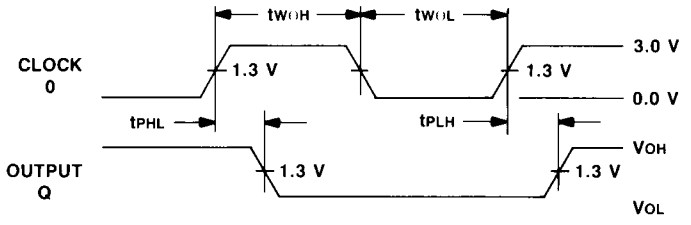


Figure 1. Clock to Output Delays, Count Frequency, and Clock Pulse Width

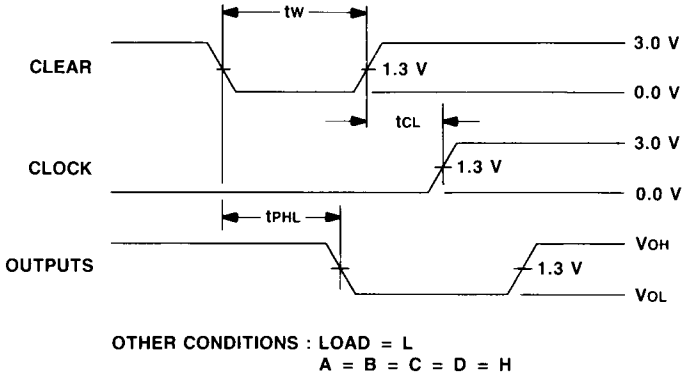


Figure 2. Clear to Output Delay, Clear Pulse Width, and Clearing Time

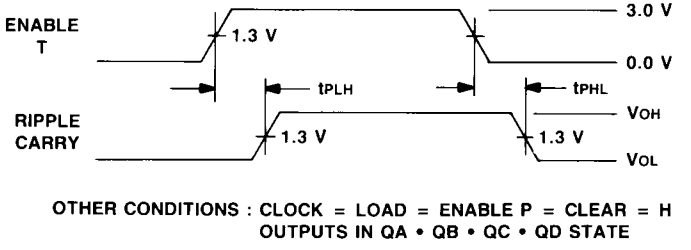
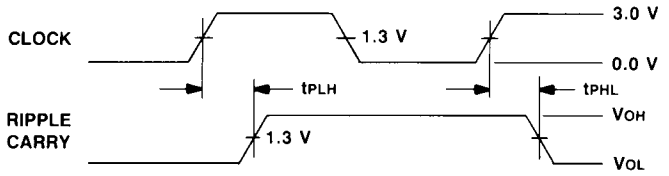
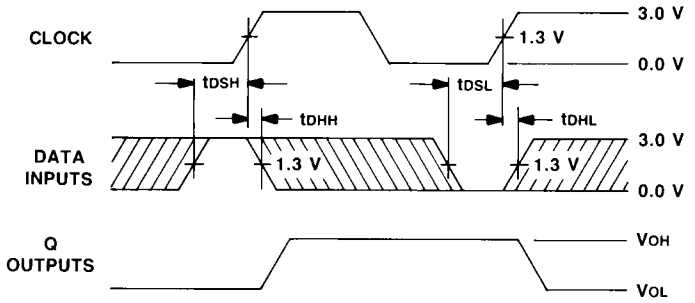


Figure 3. Enable Input to Ripple Carry Output Delays



OTHER CONDITIONS : LOAD = ENABLE P = ENABLE T = CLEAR = H
OUTPUTS IN QA • QB • QC • QD STATE

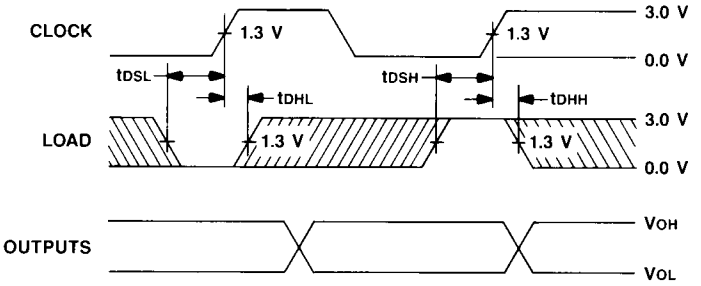
Figure 4. Clock to Ripple Carry Output Delays



OTHER CONDITIONS : LOAD = L, CLEAR = H

THE SHADED AREAS INDICATE WHEN THE INPUT IS PERMITTED
TO CHANGE FOR PREDICTABLE OUTPUT PERFORMANCE

Figure 5. Set-Up and Hold Times with Parallel Data Inputs



THE SHADED AREAS INDICATE WHEN THE INPUT IS PERMITTED
TO CHANGE FOR PREDICTABLE OUTPUT PERFORMANCE

Figure 6. Set-Up and Hold Times with Load Input