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GigaBit Logic

10G002
10G002M

Quad 2-Input XOR/XNOR/Line Receiver
1.8 GHz /600 ps Propagation Delay
10G PicoLogic™ Family

FEATURES

- -55°C to +125°C operation (10G002M)
- 150 ps typical output rise and fall times
- Differential DA inputs and true or inverted output
- ECL and 10G PicoLogic™ compatible I/O
- Temperature and voltage compensated design
- On-chip VBBS threshold reference voltage supply
- GHz small signal amplifier
- Wire-OR output capability
- Available in 40 Pin C- leaded or leadless chip carrier, or die form
- Packages contain internal decoupling capacitors for optimum high frequency performance

APPLICATIONS

- Code Generation
- Precision pulse generation
- Level Comparator
- Differential Line Receiver
- Digital Phase Detector
- High speed ECL to GaAs translator

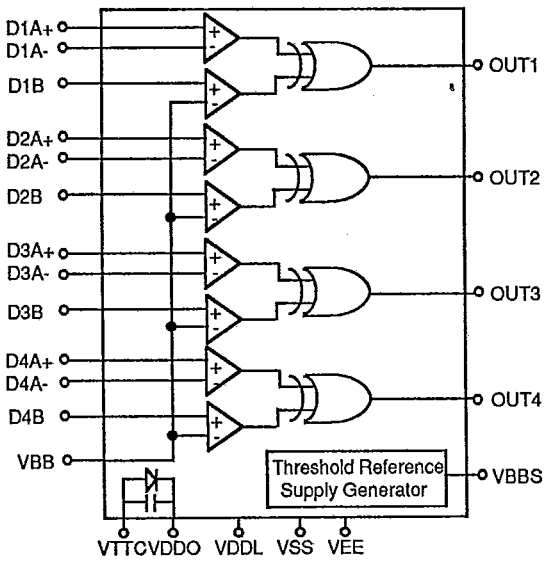
FUNCTIONAL DESCRIPTION

The 10G002 is an ECL or 10G PicoLogic™ compatible high speed quad XOR/XNOR gate. Because of its sensitive differential amplifier inputs, the 10G002 can also be used as a differential or single-ended line receiver or as a level comparator. In either application, the outputs can be inverted under control of the DB inputs. With the addition of an external low pass filter, the 10G002 can be used as a high frequency digital phase detector.

The 10G002 features a nominal -1.3V GaAs/ECL threshold reference supply voltage output on pin VBBS. Maximum propagation delay and minimum guaranteed operating frequency at 25°C are 600ps and 1.8 GHz respectively at 800 mW power dissipation. Typical room temp. operating freq. is 2.0 GHz and higher speed operation is possible with some reduction in output level swing. Output transition times are typically 150ps. For extended temperature applications, the 10G002M is specified for operation over the -55°C to +125°C case temperature range.

The 10G002 is fabricated using GigaBit's high volume, production proven GaAs MESFET process technology.

BLOCK DIAGRAM



10G002/10G002M ORDERING INFORMATION

PACKAGE TYPE	10G002 (0°C- 85°C)		10G002M (-55°C - 125°C)	
	1.6 GHz	1.3 GHz	1.4 GHz	1.1 GHz
C-Leaded CC	10G002-2C	10G002-3C	10G002M-2C	10G002M-3C
Leadless CC	10G002-2L	10G002-3L	10G002M-2L	10G002M-3L
Die		10G002-3X		10G002M-3X

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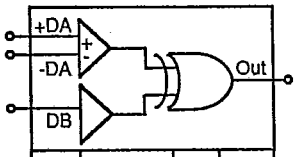
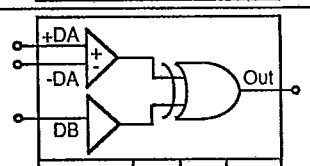
CONNECTION DIAGRAMS & TRUTH TABLES

XOR



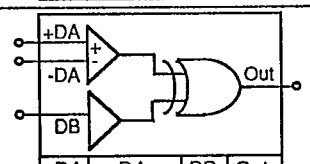
+DA	-DA	DB	Out
L	Vbb or H	L	L
L	Vbb or H	H	H
H	Vbb or L	L	H
H	Vbb or L	H	L

XNOR



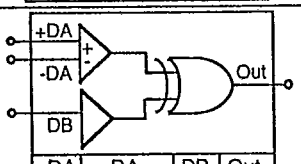
+DA	-DA	DB	Out
Vbb or H	L	L	H
Vbb or H	L	H	L
Vbb or L	H	L	L
Vbb or L	H	H	H

Line Receiver/ Comparator (Non-inverting)



	+DA	-DA	DB	Out
Receiver	H	L	L	H
	L	H	L	L
Comparator	V	Vth (<V)	L	H
	V	Vth (>V)	L	L
	V	V	X	U

Line Receiver/ Comparator (Inverting)



	+DA	-DA	DB	Out
Receiver	H	L	H	L
	L	H	H	H
Comparator	V	Vth (<V)	H	L
	V	Vth (>V)	H	H
	V	V	X	U

NOTES: X = Don't care, U = Undefined State
$-1.9V \le V \le -0.5V$
Vth = Threshold level, nominally VBB

FUNCTIONAL DESCRIPTION (cont.)

The operation of the 10G002 is illustrated in the adjacent connection diagrams and truth tables. The exclusive OR function of inputs DA+ and DB is formed by connecting the DA- input to the threshold reference level VBB or to the complement of the signal driving DA+ if this signal is differential. The exclusive NOR function utilizes the DA- and DB inputs and requires that the DA+ input be connected to VBB or the complement of the signal on DA-. As a differ- ential receiver, the10G002 accepts complementary signals on its DA inputs. The output is non-inverting when true and complement inputs are received on DA+ and DA- respectively with DB held low. An inverted output is obtained when either the DA connections are reversed or DB is held high. If one of the two DA inputs is replaced with a threshold reference level within the input's common mode range (-1.9V to -0.5V), the 10G002 performs a comparison between the other DA input and this level, producing an inverted or true output depending on the state of the B input.

When connected as either an XOR or XNOR gate, the 10G002 can function as a phase detector by producing an output binary signal whose duty cycle is proportional to the phase difference between the two inputs when the inputs are equal in frequency.

Since the output logic threshold level of various ECL and GaAs families will shift differently with temperature and supply voltage variation, the input threshold of the 10G002 is designed to track these movements. This is easily accomplished by connecting the interfacing logic family's threshold voltage to the 10G002's VBB input pin. This enables the 10G002's input threshold to track the threshold of devices connected to it, resulting in maximum noise immunity and minimum signal distortion over temperature and supply voltage variation. Some ECL devices (e.g. 10114,10115 100114,100125) and all second generation PicoLogic devices make the logic threshold level available on an output pin. In ECL it is termed VBB, and in PicoLogic it is referred to as VBBS. If unavailable, this voltage level can be generated by connecting the terminated output of an inverting gate back to its input with suitable filtering of the output to prevent oscillation.

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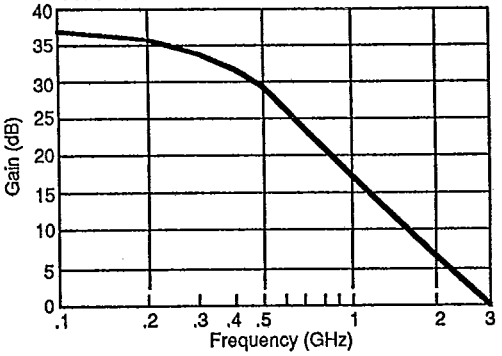
FUNCTIONAL DESCRIPTION (cont.)

When PicoLogic is used to drive the 10G002, the VBBS pin must be strapped to the VBB pin for proper device operation. Connecting VBBS to the VBB input is also appropriate, in some cases, for non-PicoLogic device interfaces. Examples of these are ECL-to-10G002 interface over a limited temperature range or when driving the10G002 from another GaAs device since GaAs logic output swings are generally much larger than ECL output swings. In any case, the VBB pin must always be connected to either the VBBS pin or to an external threshold reference voltage within the input's common mode range.

The 10G002 features two input clamp diodes which are brought out on pins VICH and VICL. These clamps can be used to internally limit a high peak-to-peak value input signal (i.e. when using the 10G002 as a phase detector and driving from a VCO with high output voltage), or to allow an improvement in an input sinewave signal edge speed by overdriving and clamping. When these pins are both connected to -1.3V, the internal input swing is limited to a range from approximately -.5V to -2.0V. When not used, VICH and VICL should be left unconnected.

Depending upon user choice of load resistor and termination voltage (VTT), the output high level (VOH) generated by the 10G002 (typically -0.4V to -0.5V) may require limiting when the 10G002 drives ECL logic. This is accomplished via an output driver clamp diode brought out on pin VDCH. For applications that require VOH limiting, consult GigaBit Application Note 4.

TYPICAL SMALL SIGNAL GAIN VS. FREQUENCY



PIN DESCRIPTIONS

D1A+ to D4A+	A differential data inputs, true
D1A- to D4A-	A differential data inputs, complement
D1-4B	B data inputs
OUT1-4	Outputs
VDDO	Output driver ground (0V)
VDDL	Internal logic ground (0V)
VSS	-3.4V power supply
VEE	-5.2V power supply
VTTC	VDDO internal decoupling capacitor return. VTTC is brought into the 10G002 package as the AC return lead for the internal VDDO output driver decoupling capacitor. It is not brought onto the10G002 die.VTTC is typically equal to VTT (nominally -2.0V).
VDCH	Output driver clamp supply.When VDCH is connected to VTT = -2.0V the output driver high level is limited to approximately -0.6V, thus providing ECL output compatibility. Consult Application Note #4 for details. When not used, VDCH should be connected to VDDO.
VICH, VICL	Input protection clamp voltages. When connected to -1.3V, these allow an overdriven sine wave input signal to be truncated to a square wave, thus providing faster rise and fall times to the internal XOR gate. When not used, the input clamps should be connected as follows: VICL to VSS and VICH to VDDO for transient protection. Inputs are internally clamped to VSS and VDDL.
VBB	Threshold reference level input. Provided to allow direct tracking of the driving logic family's output threshold voltage. Connect to VBBS when the 10G002 is driven from PicoLogic. When driving from ECL or other GaAs families, connect to that family's threshold voltage. This pin may not be left unconnected.
VBBS	PicoLogic threshold reference voltage output. Connect to VBB when interfacing with PicoLogic.

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DC CHARACTERISTICS

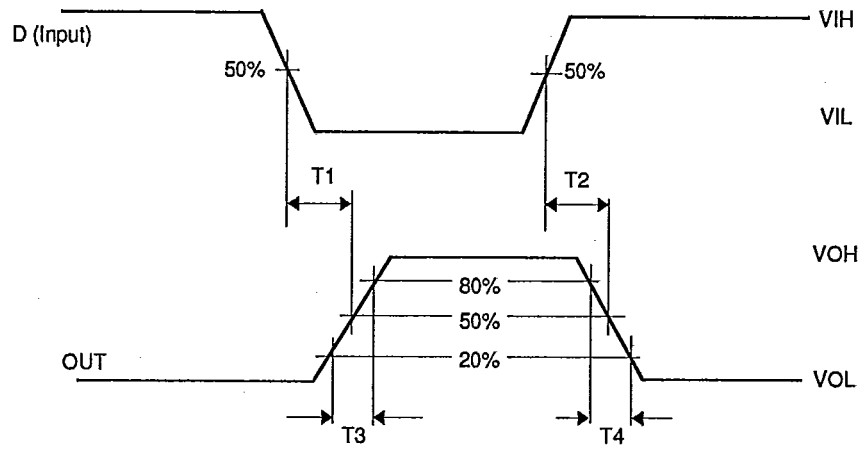
VSS = -3.5 V TO -3.3 V, VEE = -5.5 TO -5.1 V, VDDL = VDDO = Gnd., unless otherwise indicated

SYMBOL	PARAMETER	10G002 (0 to 85°C)			10G002M (-55 to +125°C)			Units
		Min	Typ.	Max	Min	Typ.	Max	
VOL	Ouput Voltage Low						-1.7	V
ISS	Power Supply Current		160	240		160	250	mA
IEE	Power Supply Current		55	75		55	75	mA
PD	Power Dissipation		800	1200		800	1200	mW

NOTE:

The remaining DC Characteristics are specified in the 10G PicoLogic™ Family Electrical Characteristics Table at the beginning of this section. This table notes parameter deviations to Family Characteristics and provides specific supplementary characteristics only.

SWITCHING WAVEFORMS



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AC CHARACTERISTICS (Note 1)

10G002-2

VSS = -3.5V to -3.3V, VEE = -5.5V to -5.1V, VDDL=VDDO = 0V, unless otherwise indicated.

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	Prop. Delay, Low to High	350	600	350	450	600	400	650	ps	
T2	Prop. Delay, High to Low	350	600	350	450	600	400	650	ps	
T3	Output Rise/Fall Times		175		125	175		200	ps	2
Fmax	Operating Frequency	1.8		1.8	2.0		1.6		GHz	

10G002-3

SYMBOL	PARAMETER	Tc = 0°C		Tc = +25°C			Tc = +85°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	Prop. Delay, Low to High	400	650	400	500	650	450	700	ps	
T2	Prop. Delay, High to Low	400	650	400	500	650	450	700	ps	
T3	Output Rise/Fall Times		210		150	210		225	ps	2
Fmax	Operating Frequency	1.5		1.5	1.8		1.3		GHz	

10G002-2M

SYMBOL	PARAMETER	Tc = -55°C		Tc = 25°C			Tc = 125°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	Prop. Delay, Low to High	350	600	350	450	600	450	700	ps	
T2	Prop. Delay, High to Low	350	600	350	450	600	450	700	ps	
T3	Output Rise/Fall Times		175		125	175		210	ps	2
Fmax	Operating Frequency	1.8		1.8	2.0		1.4		GHz	

10G002-3M

SYMBOL	PARAMETER	Tc = -55°C		Tc = 25°C			Tc = 125°C		UNITS	NOTES
		MIN	MAX	MIN	TYP	MAX	MIN	MAX		
T1	Prop. Delay, Low to High	400	650	400	500	650	500	750	ps	
T2	Prop. Delay, High to Low	400	650	400	500	650	500	750	ps	
T3	Output Rise/Fall Times		210		150	210		240	ps	2
Fmax	Operating Frequency	1.5		1.5	1.8		1.1		GHz	

Notes: 1. Test conditions (unless otherwise indicated) :

VBB = -1.2V VICH = N/C VIH = -0.7V VOH ≥ -0.7V
VTT = -2.0V VICL = N/C VIL = -1.7V VOL ≤ -1.7V
VTTC = VTT VDCH = VDDO
RLOAD = 50Ω to -2.0V
Input signal rise and fall times ≤ 150 ps

2. Rise and fall times are measured at the 20% and 80% points of the transition from VOL max to VOH min.

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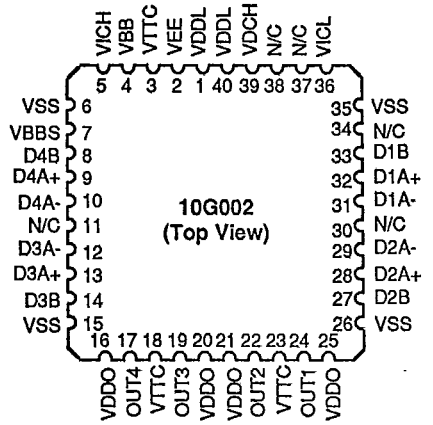
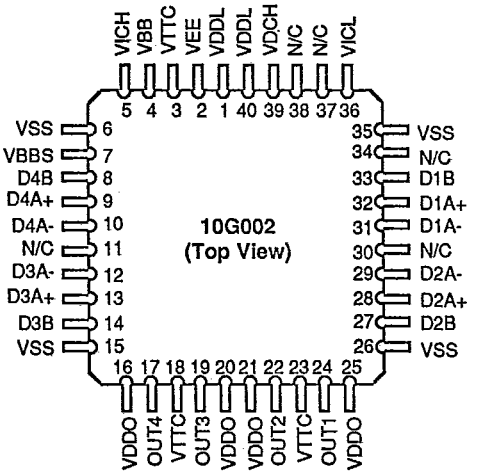
PACKAGE PINOUT DIAGRAMS

TYPE "L" PACKAGE



NOTES: Pin 1 is marked for orientation. N/C = No Connection.

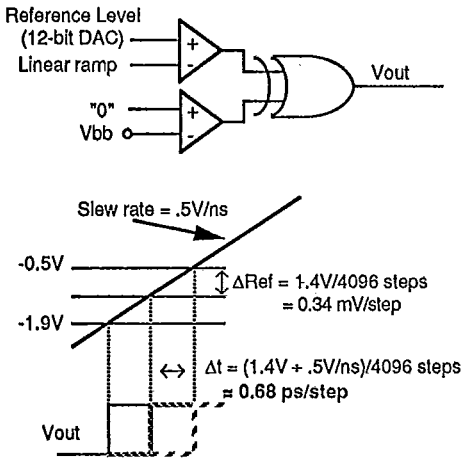
TYPE "C" PACKAGE



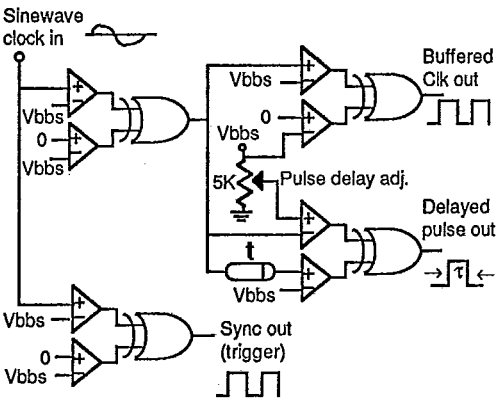
NOTES: Pin 1 is marked for orientation. N/C = No Connection.

TYPICAL APPLICATIONS

PRECISION TIME VERNIER



ADJUSTABLE DELAY PULSE GENERATOR



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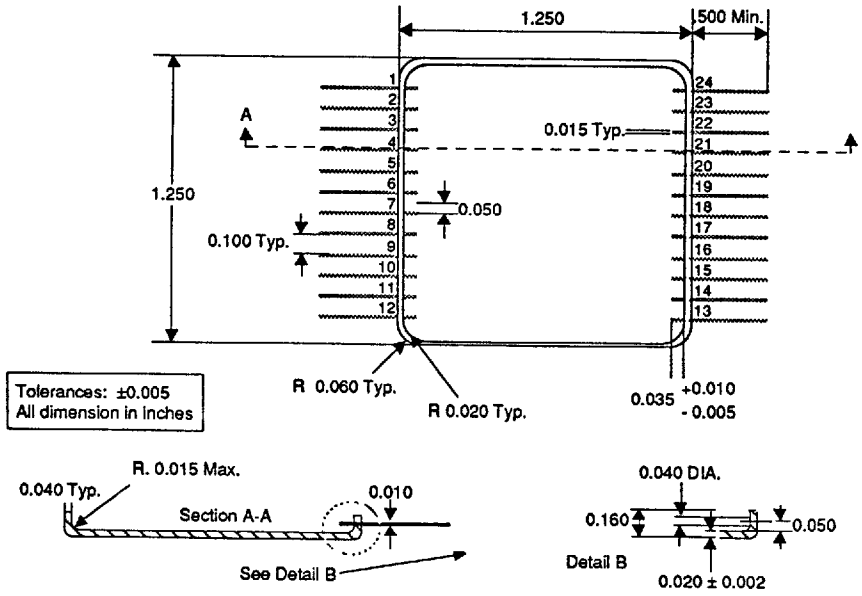
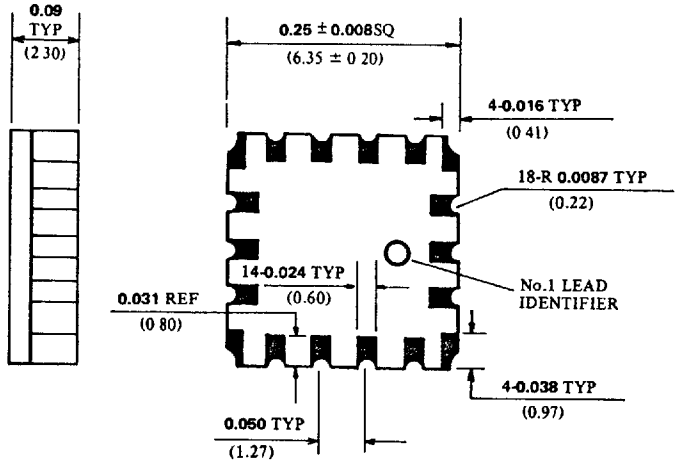
24 PIN METAL FLATPACK
18 PIN PACKAGE

24 PIN METAL FLATPACK
Type H



18 PIN LEADLESS CHIP CARRIER
TYPE L1



All dimensions shown in inches and (millimeters)

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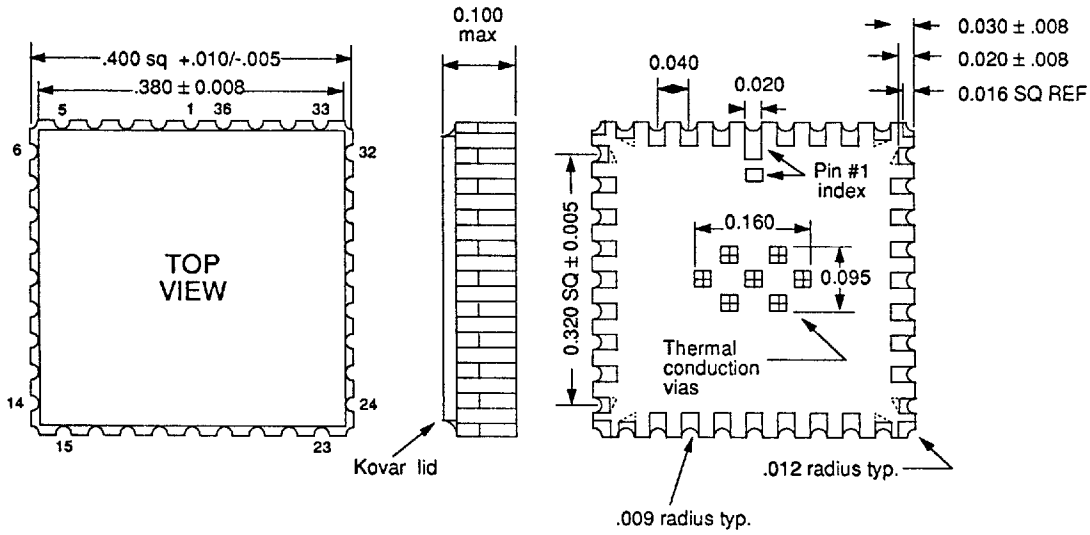
GigaBit Logic

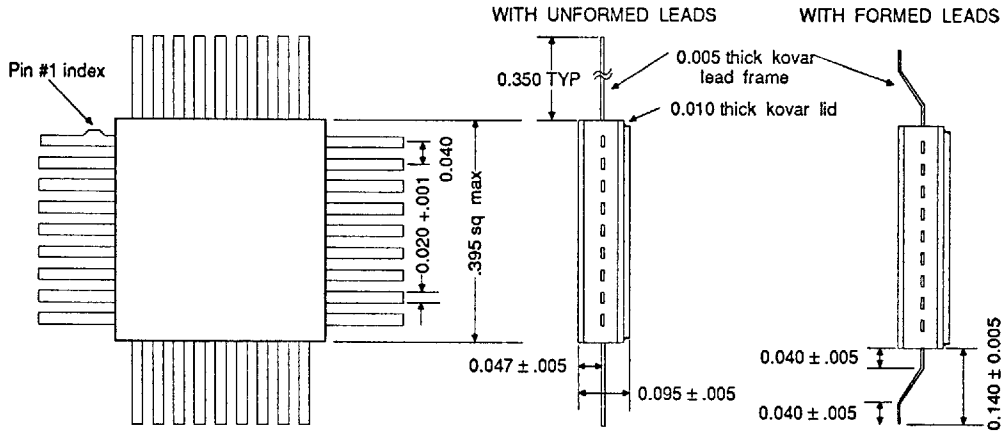
36 PIN PACKAGES

36 PIN LEADLESS CHIP CARRIER
TYPE L36



NOTES:
1) The package bottom thermal vias, top lid surface and 4 metallized corner castellations (when present) are all at Vss potential.
2) All dimensions in inches.
3) Plin #1 identifier may be an elongated pad or small, square gray marker.

36 I/O LEAD FLATPACK
TYPE F



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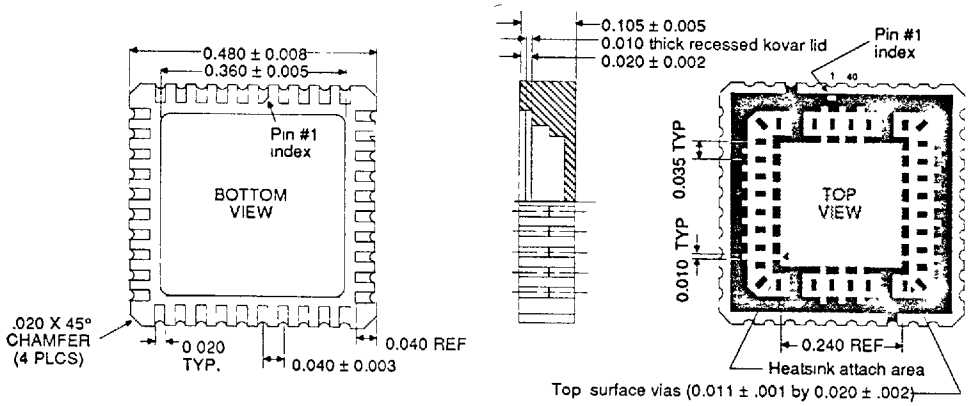
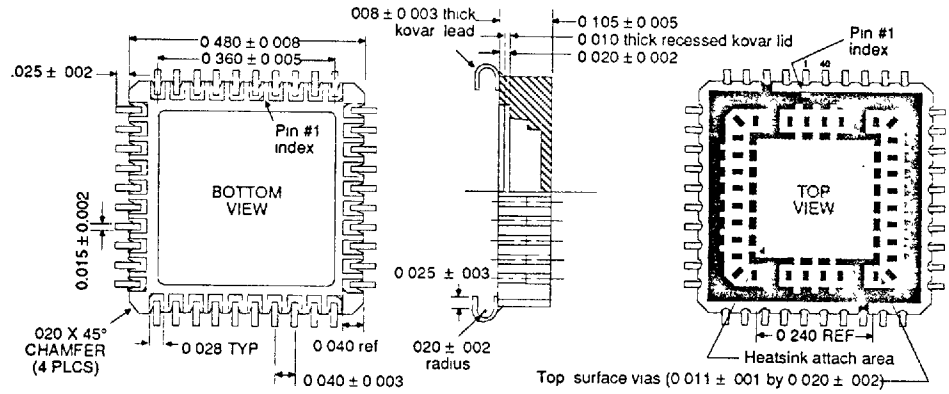
40 PIN PACKAGES

40 PIN LEADLESS CHIP CARRIER
TYPE L

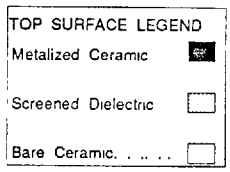


40 PIN LEADED CHIP CARRIER
TYPE C

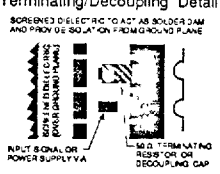


NOTES

(1) Footprint is JEDEC standard outline
(2) Top surface v as (for terminating resistors and decoupling capacitors) are not available on pins 3 4 17 18 23 24 37 and 38
(3) Top surface metal (not including vias) and p ns 3 and 23 are fixed at VTT potential
(4) Recommended top surface chip res stors are 0 040 long by 0 020 w de by 0 010 thick typ 100 mw min nominal power rating (M ni-Systems MSR 21 or equivalent)
(5) Recommended top surface ch p capac tors are 0 040 ong by 0 030 wide by 0 020 thick typ 25V VDCW 1000 pf min (Johanson R09 case or equivalent)
(6) Recommended heatsinks a e GBL P/Ns 90GHS 40 A and 90GHS 40 B
(7) Thermally conductive, e ectrically non-conductive epoxy is recommended for heatsink attachment (Ablestick 789 4 or 561K, or Thermalloy Thermalbond™ or equivalent.)
(8) L40 and C40 packages are dimensionally identical except for contact finger width



Top Surface Terminating/Decoupling Detail



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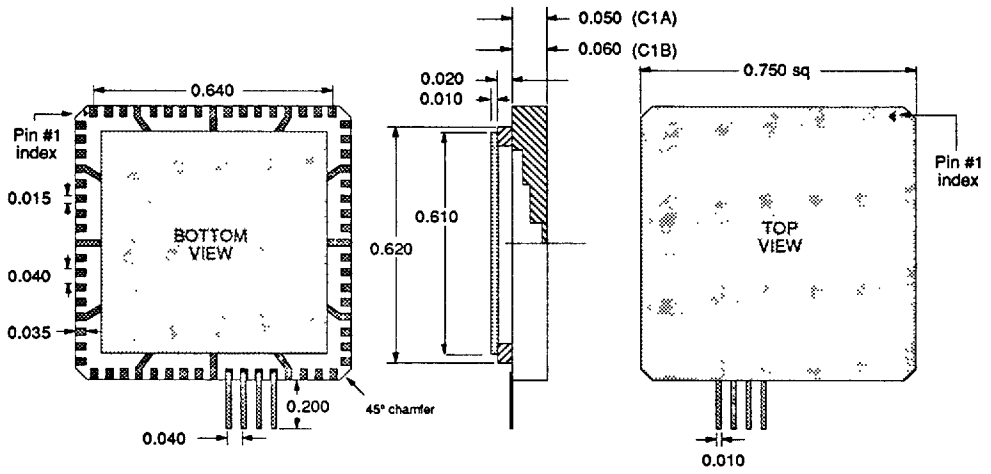
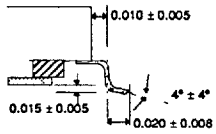
68 & 132 PIN PACKAGES

68 PIN LEADED CHIP CARRIER
TYPE C1



1. All dimensions in inches.
2. C1A PACKAGE: Package lid, top, and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
3. C1B PACKAGE: Package lid and pins 4, 9, 14, 21, 26, 31, 38, 43, 48, 55, 60, 65 are at common potential (system ground).
4. Tolerance on all dimensions is ± 1 % but not larger than ± 0.005. Tolerance on 0.640 end pad to end pad dimension is ± 0.003.

GULLWING LEADS



132 PIN LEADED CHIP CARRIER
TYPE C3