MOTOROLA

MC14528B

DUAL MONOSTABLE MULTIVIBRATOR

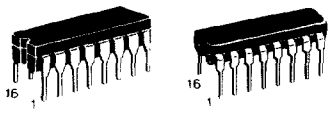
The MC14528B is a dual, retriggerable, resettable monostable multivibrator. It may be triggered from either edge of an input pulse, and produces an output pulse over a wide range of widths, the duration of which is determined by the external timing components, C_X and R_X.

- Separate Reset Available
- Diode Protection on All Inputs
- *Triggerable from Leading or Trailing Edge Pulse*
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Capable of Driving Two Low-power TTL Loads or One Low-power Schottky TTL Load Over the Rated Temperature Range
- Pin-for-Pin Replacement with the MC14538B and MC14548B.

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

DUAL RETRIGGERABLE/RESETTABLE MONOSTABLE MULTIVIBRATOR



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

A Series: −55°C to +125°C
MC14XXXBAL (Ceramic Package Only)

C Series: −40°C to +85°C
MC14XXXBCP (Plastic Package)
MC14XXXBCL (Ceramic Package)

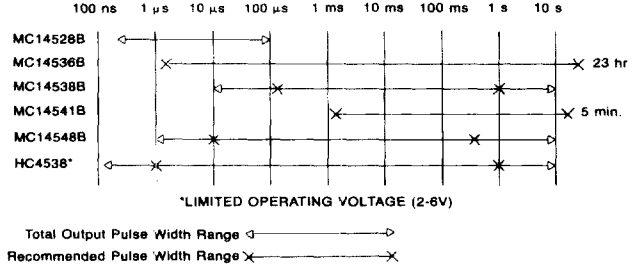
MAXIMUM RATINGS* (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage	−0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage (DC or Transient)	−0.5 to V_{DD} +0.5	V
I_{in}, I_{out}	Input or Output Current (DC or Transient), per Pin	±10	mA
P_D	Power Dissipation, per Package†	500	mW
T_{stg}	*Storage Temperature*	*−65 to +150*	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

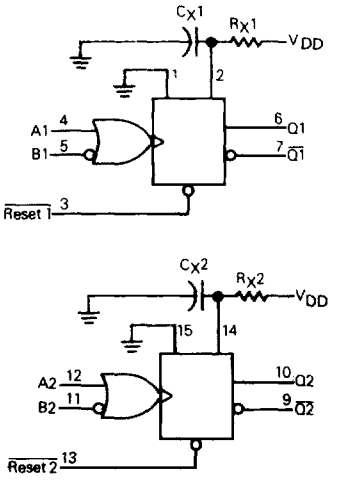
*Maximum Ratings are those values beyond which damage to the device may occur.
†Temperature Derating: Plastic "P" Package: −12mW/°C from 65°C to 85°C
Ceramic "L" Package: −12mW/°C from 100°C to 125°C

THE MC14528B IS NOT RECOMMENDED FOR NEW DESIGNS

ONE-SHOT SELECTION GUIDE



BLOCK DIAGRAM



V_{DD} = Pin 16
V_{SS} = Pin 1, Pin 8, Pin 15
R_X and C_X are external components

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ #	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	—	0.05	—	0	0.05	—	0.05	Vdc
V_{in} = V_{DD} or 0		10	—	0.05	—	0	0.05	—	0.05	
		15	—	0.05	—	0	0.05	—	0.05	
"1" Level	V_{OH}	5.0	4.95	—	4.95	5.0	—	4.95	—	Vdc
V_{in} = 0 or V_{DD}		10	9.95	—	9.95	10	—	9.95	—	
		15	14.95	—	14.95	15	—	14.95	—	
Input Voltage "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	—	1.5	—	2.25	1.5	—	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	—	3.0	—	4.50	3.0	—	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	—	4.0	—	6.75	4.0	—	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	—	3.5	2.75	—	3.5	—	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	—	7.0	5.50	—	7.0	—	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	—	11.0	8.25	—	11.0	—	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.2	—	−1.0	−1.7	—	−0.7	—	
(V_{OH} = 4.6 Vdc)		5.0	−0.64	—	−0.51	−0.88	—	−0.36	—	
(V_{OH} = 9.5 Vdc)		10	−1.6	—	−1.3	−2.25	—	−0.9	—	
(V_{OH} = 13.5 Vdc)		15	−4.2	—	−3.4	−8.8	—	−2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	—	0.51	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	—	1.3	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	4.2	—	3.4	8.8	—	2.4	—	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	−1.0	—	−0.8	−0.7	—	−0.6	—	
(V_{OH} = 4.6 Vdc)		5.0	−0.52	—	−0.44	−0.88	—	−0.36	—	
(V_{OH} = 9.5 Vdc)		10	−1.3	—	−1.1	−2.25	—	−0.9	—	
(V_{OH} = 13.5 Vdc)		15	−3.6	—	−3.0	−8.8	—	−2.4	—	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	—	0.44	0.88	—	0.36	—	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	—	1.1	2.25	—	0.9	—	
(V_{OL} = 1.5 Vdc)		15	3.6	—	3.0	8.8	—	2.4	—	
Input Current (AL Device)	I_{in}	15	—	±0.1	—	±0.00001	±0.1	—	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	—	±0.3	—	±0.00001	±0.3	—	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	—	—	—	—	5.0	7.5	—	—	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	—	5.0	—	0.005	5.0	—	150	μAdc
		10	—	10	—	0.010	10	—	300	
		15	—	20	—	0.015	20	—	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	—	20	—	0.005	20	—	150	μAdc
		10	—	40	—	0.010	40	—	300	
		15	—	80	—	0.015	80	—	600	
**Total Supply Current at an external load Capacitance (C_L) and at external timing capacitance (C_X), use the formula —	I_T	—	$I_T(C_L, C_X) = [(C_L + 0.36C_X)V_{DD}f + 2x10^{-8} R_X C_X(V_{DD}-2)2f] \times 10^{-3}$ where: I_T in μA (per circuit), C_L and C_X in pF, R_X in megohms, V_{DD} in Vdc, f in kHz is input frequency.							

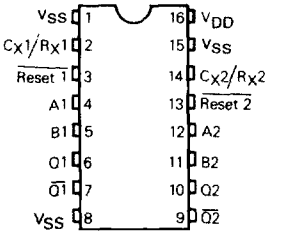
*T_{low} = −55°C for AL Device, −40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

** The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \le (V_{in}$ or $V_{out}) \le V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

PIN ASSIGNMENT



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SWITCHING CHARACTERISTICS** (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	C_X pF	R_X kΩ	V_{DD} Vdc	Min	Typ #	Max	Unit
Output Rise and Fall Time	t_{TLH}, t_{THL}	—	—					ns
t_{TLH}, t_{THL} = (1.5 ns/pF) C_L + 25 ns				5.0	—	100	200	
t_{TLH}, t_{THL} = (0.75 ns/pF) C_L + 12.5 ns				10	—	50	100	
t_{TLH}, t_{THL} = (0.55 ns/pF) C_L + 9.5 ns				15	—	40	80	
Turn-Off, Turn-On Delay Time — A or B to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	15	5.0					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 240 ns				5.0	—	325	650	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 87 ns				10	—	120	240	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 65 ns				15	—	90	180	
Turn-Off, Turn-On Delay Time — A or B to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	1000	10					ns
t_{PLH}, t_{PHL} = (1.7 ns/pF) C_L + 620 ns				5.0	—	705	—	
t_{PLH}, t_{PHL} = (0.66 ns/pF) C_L + 257 ns				10	—	290	—	
t_{PLH}, t_{PHL} = (0.5 ns/pF) C_L + 185 ns				15	—	210	—	
Input Pulse Width — A or B	t_{WH}	15	5.0	5.0	150	70	—	ns
				10	75	30	—	
				15	55	30	—	
	t_{WL}	1000	10	5.0	—	70	—	ns
				10	—	30	—	
				15	—	30	—	
Output Pulse Width — Q or $\overline{Q}$	t_W	15	5.0	5.0	—	550	—	ns
(For C_X < 0.01 μF use graph for appropriate V_{DD} level.)				10	—	350	—	
				15	—	300	—	
Output Pulse Width — Q or $\overline{Q}$	t_W	10,000	10	5.0	15	30	45	μs
(For C_X > 0.01 μF use formula:				10	10	50	90	
t_W = 0.2 R_X C_X Ln [V_{DD} − V_{SS}])†				15	15	55	95	
Pulse Width Match between Circuits in the same package	t1 - t2	10,000	10	5.0	—	6.0	25	%
				10	—	8.0	35	
				15	—	8.0	35	
Reset Propagation Delay — $\overline{Reset}$ to Q or $\overline{Q}$	t_{PLH}, t_{PHL}	15	5.0	5.0	—	325	600	ns
				10	—	90	225	
				15	—	60	170	
		1000	10	5.0	—	1000	—	ns
				10	—	300	—	
				15	—	250	—	
Retrigger Time	t_{rr}	15	5.0	5.0	0	—	—	ns
				10	0	—	—	
				15	0	—	—	
		1000	10	5.0	0	—	—	ns
				10	0	—	—	
				15	0	—	—	
External Timing Resistance	R_X	—	—	—	5.0	—	1000	kΩ
External Timing Capacitance	C_X	—	—	—	No Limits*			μF

† R_X is in Ohms, C_X is in farads, V_{DD} and V_{SS} in volts, PW_{out} in seconds.

* If C_X > 15 μF, Use Discharge Protection Diode D_X, per Fig. 9.

**The formulas given are for the typical characteristics only at 25°C.

#Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

FUNCTION TABLE

Inputs			Outputs	
$\overline{Reset}$	A	B	Q	$\overline{Q}$
H	↑	H	⎍	⎎
H	L	↓	⎍	⎎
H	↑↓	L	Not Triggered	
H	H	↑↓	Not Triggered	
H	L, H, ↓	H	Not Triggered	
H	L	L, H, ↑	Not Triggered	
L	X	X	L	H
↓↑	X	X	Not Triggered	

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FIGURE 1 – OUTPUT SOURCE CURRENT TEST CIRCUIT

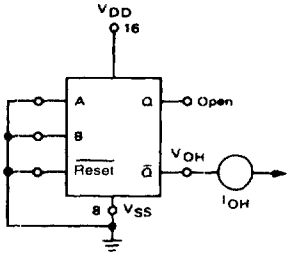


FIGURE 2 – OUTPUT SINK CURRENT TEST CIRCUIT

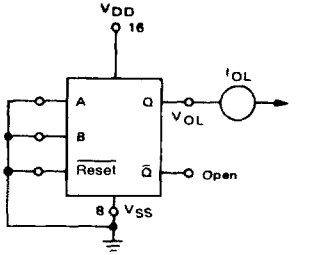
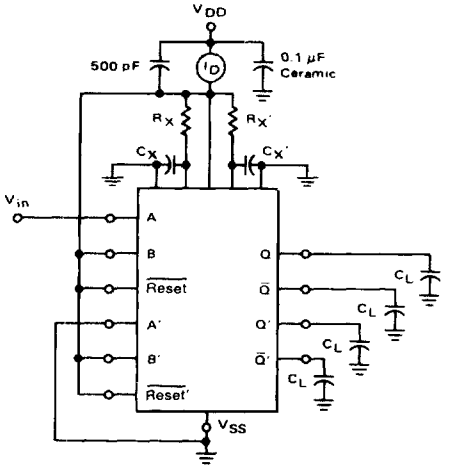
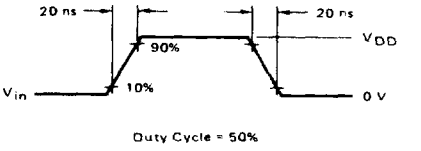


FIGURE 3 – POWER DISSIPATION TEST CIRCUIT AND WAVEFORMS





Duty Cycle = 50%

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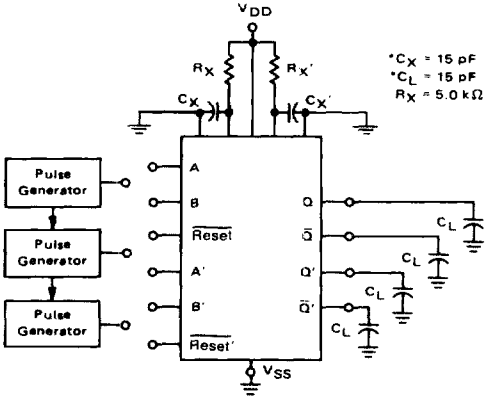
FIGURE 4 – AC TEST CIRCUIT



INPUT CONNECTIONS

CHARACTERISTICS	$\overline{\text{Reset}}$	A	B
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, t_W	V_{DD}	PG1	V_{DD}
t_{PLH}, t_{PHL}, t_{TLH}, t_{THL}, t_W	V_{DD}	V_{SS}	PG2
$t_{PLH(R)}$, $t_{PHL(R)}$, t_W	PG3	PG1	PG2

*Includes capacitance of probes, wiring, and fixture parasitic.

NOTE: AC test waveforms for PG1, PG2, and PG3 on next page.

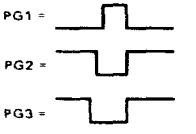


FIGURE 5 – AC TEST WAVEFORMS

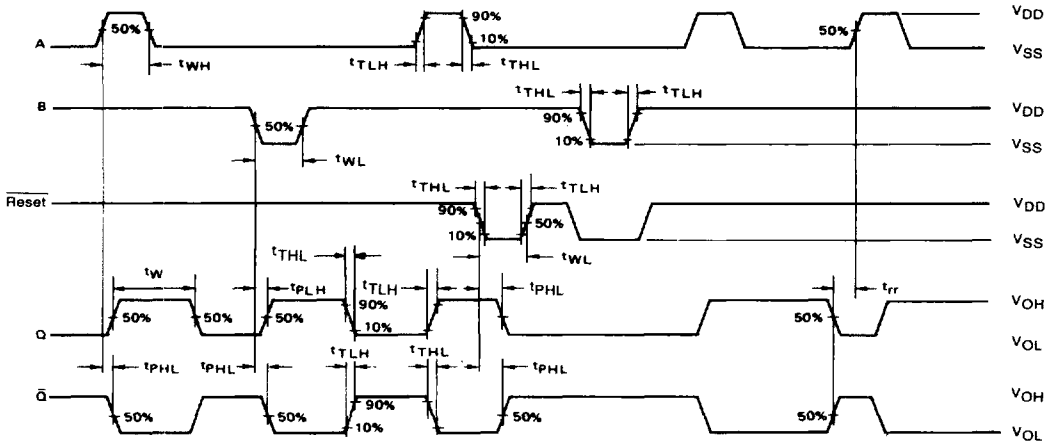
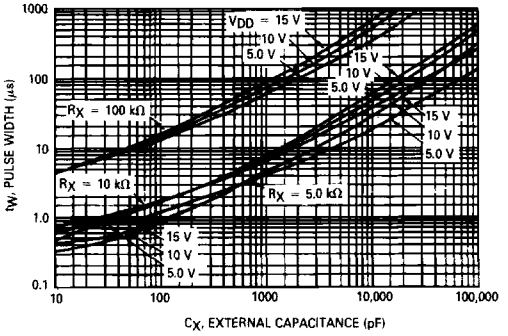


FIGURE 6 – PULSE WIDTH versus C_X



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TYPICAL APPLICATIONS

FIGURE 7 — RETRIGGERABLE MONOSTABLES CIRCUITRY

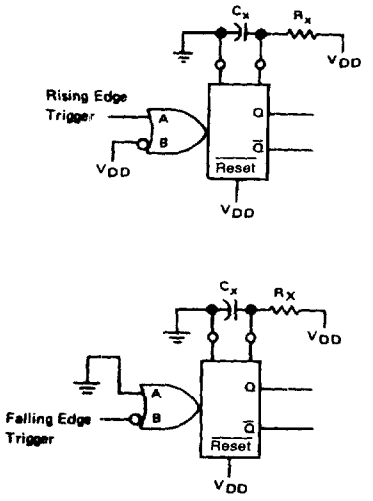


FIGURE 8 — NON-RETRIGGERABLE MONOSTABLES CIRCUITRY

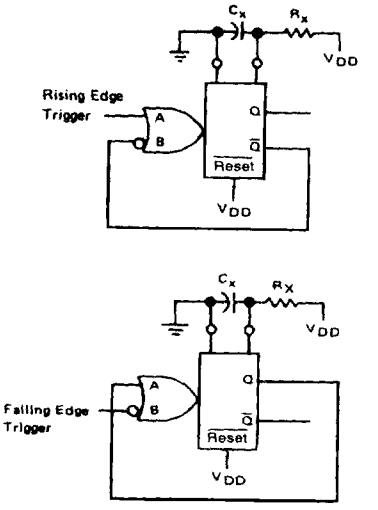


FIGURE 9 — USE OF A DIODE TO LIMIT POWER DOWN CURRENT SURGE

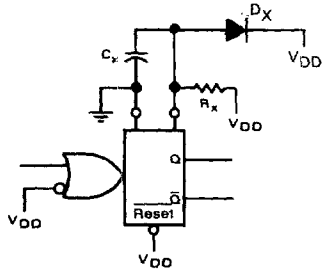
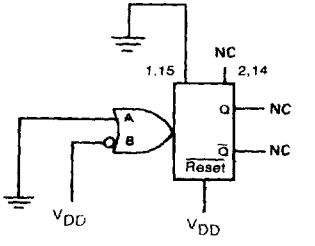


FIGURE 10 — CONNECTION OF UNUSED SECTIONS



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