OKI Semiconductor

MSM7523

Multi-Function Telecommunication LSI

GENERAL DESCRIPTION

The MSM7523 provides three kinds of functions which are often applied for telephone terminal equipment.

Those are DTMF generator, DTMF receiver and low speed 300 bps FSK modem defined as V.21 in ITU-T standard.

The different points from the family version -MSM6888B- are as follows.

* The analog input terminals are provided for each DTMF receiver and Modem.
* DTMF generator and receiver can be active at the same time.
* DTMF receiver and Modem can be active at the same time.
* The special tone (NRS) detector is not provided.

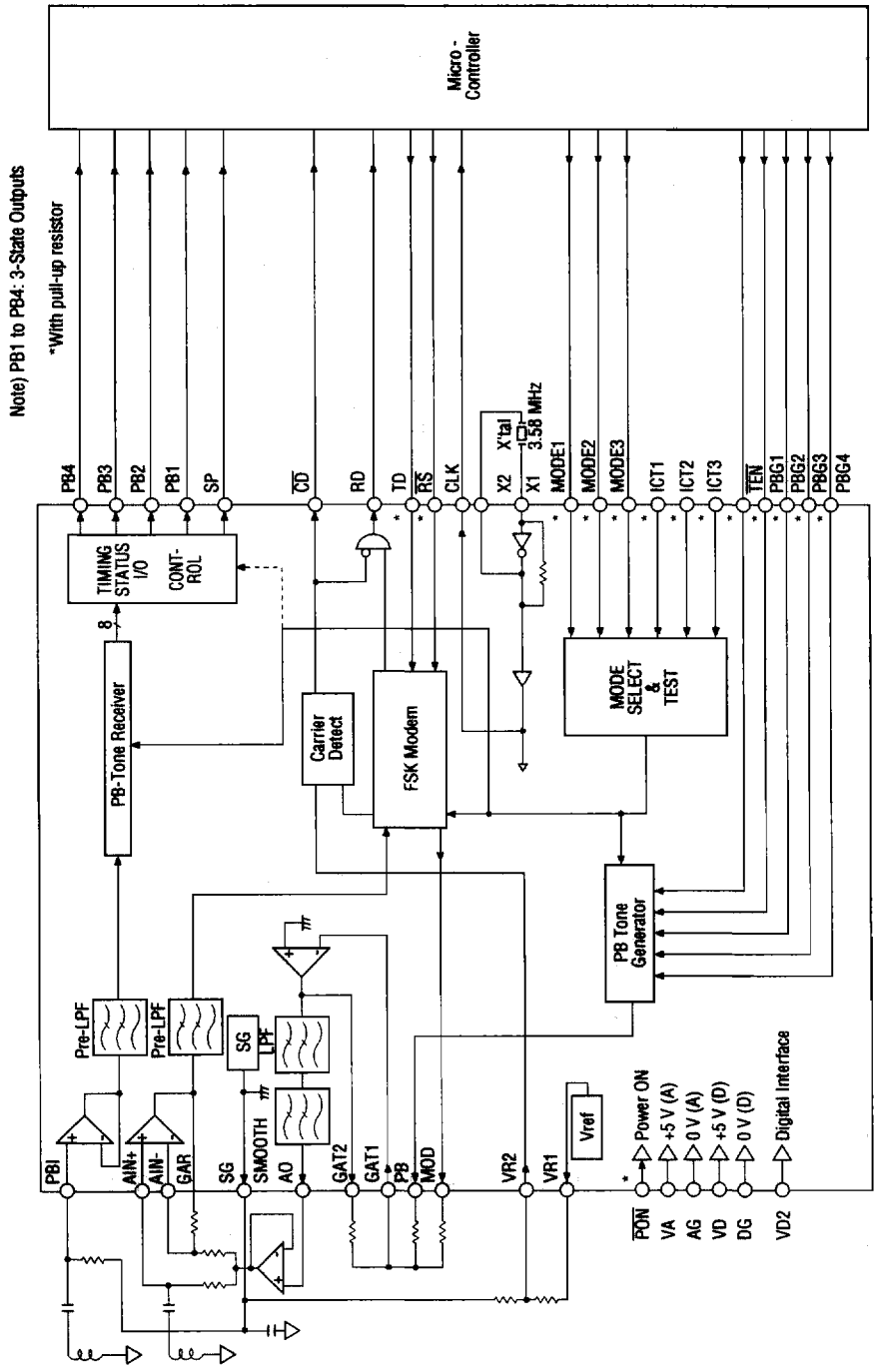
FEATURES

- +5 V Single Power Supply
  * Digital input and output terminals are capable of interfacing to the MCU when the power supply voltage is between +2.5 V to VD.
- Low Power Consumption
  Operating Mode : 9 mA Typ., 12 mA Max.
  Power Down Mode : 0.1 mA Max.
- Operating Modes;
  * DTMF Tone Generator/Receiver
  * DTMF Tone Receiver
  * 300 bps FSK Modem (Answer/Originate)/DTMF Tone Receiver
  * Modem Test
- DTMF Tone Receiver Decoded Output Terminals; 4 bit
- Modem Digital Interface Terminals; TD (Transmit Data), RS (Request to send), RD (Receive Data), CD (Receive Carrier Detect)
- On-chip Analog Pre-, Post-Low Pass Filters
- 3.579545 MHz Crystal Oscillator
- Power Down Mode
- Analog Signal Amplitude; Adjustable
- Package options:

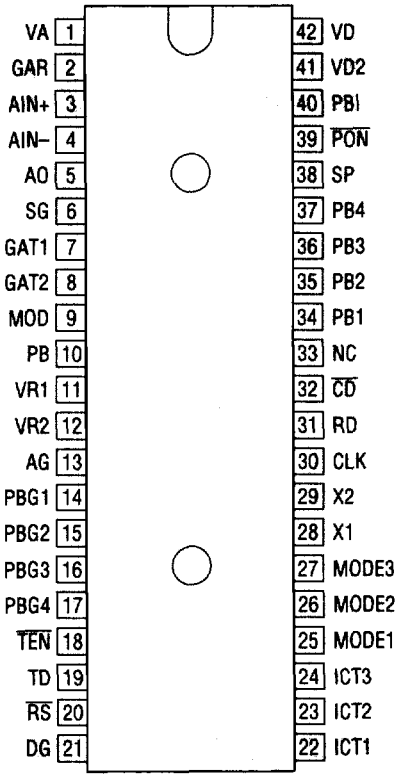
42-pin plastic DIP	(DIP42-P-600)	(Product name : MSM7523RS)
56-pin plastic QFP	(QFP56-P-1519-VK)	(Product name : MSM7523GS-VK)

Note: The MSM7523 is not pin to pin compatible to the MSM6888B.

BLOCK DIAGRAM

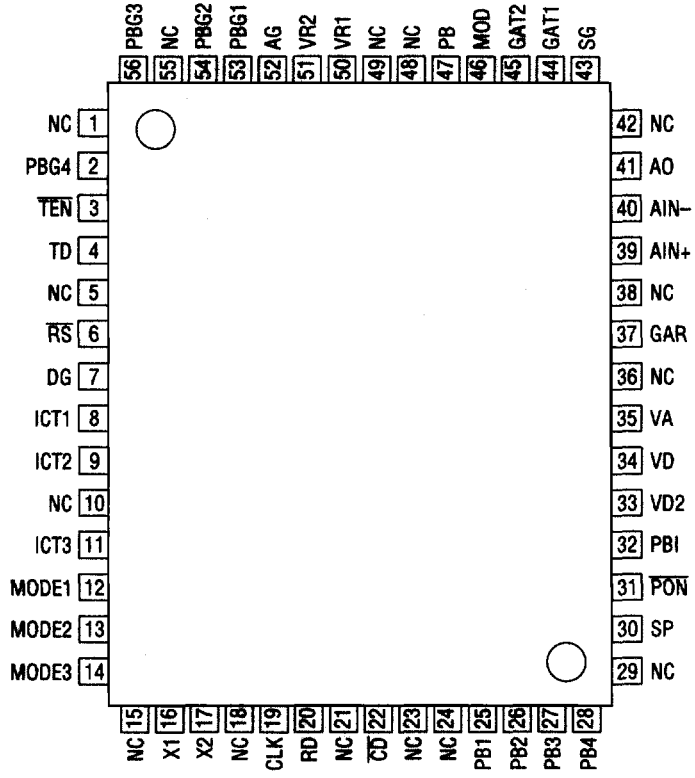


PIN CONFIGURATION (TOP VIEW)



42-Pin Plastic DIP

NC : No connect pin



56-Pin Plastic QFP

NC : No connect pin

PIN DESCRIPTION

Pin Number		Name	I/O	Description
RS	GS-VK			
1	35	VA	—	+5 V Power Supply (Analog Circuit).
2	37	GAR	O	Output, non-inverting input and inverting input pins of on-chip operational amplifier. These are used to provide the 2W/4W duplexer circuit in combination with external resistors.
3	39	AIN+	I	
4	40	AIN-	I	
5	41	AO	O	Analog signal output. DTMF tone or modem transmit signal is output from this pin.
6	43	SG	O	On-chip signal ground, and has a potential of about +2.5 V (VA/2). This pin should be bypassed to AG via 1 μF to get the better performance.
7	44	GAT1	I	MOD is the modem transmit signal output and PB is the DTMF tone output. By connecting external resistors to these pins, GAT1 and GAT2, analog signal amplitude can be set at required values for the modem signal and the DTMF tone, independently.
8	45	GAT2	O	
9	46	MOD	O	
10	47	PB	O	
11	50	VR1	O	These pins are useful to adjust the received carrier detect amplitude. The original potential of VR1 to SG is about +1.1 V and the given potential to VR2 is about +0.88 V by on-chip resistor divider between VR1 and SG. The divided potential between VR1 and SG, produced by external resistors, can be applied to VR2 to adjust the received carrier detect amplitude at the required value. The original amplitude (without external resistors) is set at –42 to –48 dBm. Please refer to Fig. 17 for the external adjustment.
12	51	VR2	I	
13	52	AG	—	Analog Ground, 0 V.
14	53	PBG1	I*	These are 4-bit control signal input pins, and DTMF tone frequency is determined by these data which are latched into the internal register at the falling edge of $\overline{TEN}$. PBG1 to 4 are pulled-up internally (*).
15	54	PBG2	I*	
16	56	PBG3	I*	
17	2	PBG4	I*	

Note: Digital input pulled up by a high resistance inside the IC.

Pin Number		Name	I/O	Description
RS	GS-VK			
18	3	$\overline{TEN}$	I*	DTMF tone transmit enable. PBG1 to PBG4 data are latched at the falling edge of $\overline{TEN}$, and DTMF tone is generated during $\overline{TEN}$ is at digital "0" level. See Fig. 6.
19	4	TD	I*	Modem transmit serial data input. Data stream less than 300 bps should be applied. Digital "1" and "0" correspond to "Mark" and "Space" respectively.
20	6	$\overline{RS}$	I*	Request to send data input . During $\overline{RS}$ is at digital "0" level, modem transmit is enabled.
21	7	DG	—	Digital Ground, 0 V.
22	8	ICT1	I*	IC test only.
23	9	ICT2	I*	Regardress of operating mode.
24	11	ICT3	I*	Should be open.
25	12	MODE1	I*	Operating mode select data. Refer to Table-1.
26	13	MODE2	I*	
27	14	MODE3	I*	
28	16	X1	I	3.579545 MHz crystal resonator should be connected to X1 and X2. When applying external clock of 3.579545 MHz to the device, it should be connected to X2 (not X1) through the AC coupling capacitor of 100 pF and X1 has to be opened.
29	17	X2	O	
30	19	CLK	O	3.579545 MHz clock output.
31	20	RD	O	Modem receive serial data output. Digital "1" and "0" correspond to "Mark" and "Space" respectively. When $\overline{CD}$ (Carrier Detect) is off (Digital "1"), RD is hold at "Mark" state.
32	22	$\overline{CD}$	O	Carrier Detect output. Digital "0" and "1" represent "Detect" and "No-detect" respectively.

Note: Digital input pulled up by a high resistance inside the IC.

Pin Number		Name	I/O	Description
RS	GS-VK			
34	25	PB1	O	4 bits decoded output data from DTMF receiver.
35	26	PB2	O	
36	27	PB3	O	
37	28	PB4	O	
38	30	SP	O	DTMF signal present. Digital "1" represents that the decoded data on PB1 to PB4 is validated. At the rising edge of SP, the decoded data should be read into the MCU chip. See Fig. 7.
39	31	$\overline{PON}$	I	Power Down mode select. Digital "1" on this pin makes the whole circuit of the device to be in the power down state.
40	32	PBI	I	DTMF signal input terminal.
41	33	VD2	—	Power supply for digital interface input and output. The supply voltage from +2.5 V to VD (Applied supply voltage to the pin VD) is possible for VD2. For example, when the chip is interfaced to the MCU working on +3 V supply, the +3 V supply has to be applied to the pin VD2. Note) This function is effective to all of digital input and output pins except X1, X2 and CLK pins. There is no limitation regarding the power supplies' (VD and VD2) applying procedure (Latch up free).
42	34	VD	—	+5 V Power Supply (Digital Circuit).

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Power Supply Voltage	VA, VD	Ta = 25°C Referred to AG or DG	−0.3 to 7	V
	VD2		−0.3 to VD	
Analog Input Voltage			−0.3 to VA + 0.3	
Digital Input Voltage			−0.3 to VD + 0.3	
Operating Temperature		—	−40 to 85	°C
Storage Temperature		—	−65 to 150	
Pin Soldering Temperature		Within 10 sec	260	

RECOMMENDED OPERATING CONDITIONS

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit
Power Supply Voltage		VA, VD	—	4.5	5.0	5.5	V
		VD2		2.5	—	VD	
Digital Input Voltage		V_{IH}	—	2.0	—	VD	V
		V_{IL}		0	—	0.8	
Digital Output Current		I_{OH}	VD2 = VD, Except X2	−0.05	—	—	mA
		I_{OL}		—	—	0.4	
Operating Temperature		T_{op}	—	−40	—	+85	°C
Input Clock Frequency		f_{CLK}	—	−0.1	—	+0.1	%
Bypass Capacitance		VA	—	0.1 + 10	—	—	µF
		VD, VD2		1	—	—	
		SG		1	—	—	
Crystal	Frequency Deviation		25°C ±5°C	−100	—	+100	ppm
	Temperature Characteristics		At −40°C to +85°C	−50	—	+50	
	Equivalent Series Resistance		—	1	—	50	Ω
	Load Capacitance		—	—	16	—	pF

ELECTRICAL CHARACTERISTICS

DC and Digital Interface Characteristics

(VA, VD, VD2 = +5 V ±10%, Ta = −40°C to +85°C)

Parameter	Symbol	Condition		Min.	Typ.	Max.	Unit
Power Supply Current	I_{AD}	$I_A + I_D + I_{D2}$ (VD2 = VD)	$\overline{PON}$ = "0"	—	9	12	mA
	I_{PD}		$\overline{PON}$ = "1"	—	0.01	0.1	mA
Digital Input Current *	I_{IH}		$V_I = V_{IH}$ Max.	−10	—	10	µA
	I_{IL}		$V_I = V_{IL}$ Min.	−100	—	10	
Digital Output Voltage	V_{OH}		$I_O = I_{OH}$ Min.	2.4	—	VD2	V
	V_{OL}		$I_O = I_{OL}$ Max.	0	—	0.4	

* Internal pull-up resistor

Analog Interface Characteristics

(VA, VD, VD2 = +5 V ±10%, Ta = −40°C to +85°C)

Parameter	Condition		Min.	Typ.	Max.	Unit
Input Impedance	PBI, AIN+, 0 to 10 kHz		20	—	—	kΩ
Output Voltage Swing	AO, $R_L \geq 20$ kΩ		2.2	3	—	V_{P-P}
Load Resistance	AO, MOD, PB, GAT2		20	—	—	kΩ
Output DC Potential	MOD, PB		$\frac{VA}{2} - 0.1$	$\frac{VA}{2}$	$\frac{VA}{2} + 0.1$	V
	AO(When GAT1 and GAT2 are shortened)					
Out-of-Band Energy (At phone line terminated point)	4 to 8 kHz	P : In band Signal Energy (0.3 to 3.4 kHz)	—	—	P−20	dB
	8 to 12 kHz		—	—	P−40	
	12 kHz to		—	—	P−60	

Modem

(VA, VD = +5 V ±10%, Ta = −40°C to +85°C)

Parameter	Condition				Min.	Typ.	Max.	Unit
Transmit signal Amplitude	MOD, At MARK and SPACE, $R_L \geq 20$ kΩ				−3 / 1.55	−1 / 1.95	+1 / 2.46	dBm / V_{P-P}
Transmit Signal Amplitude Ratio	MARK/SPACE				−2	0	2	dB
Transmit Signal Frequency	Originate Mode	MARK	TD	"1"	976	980	984	Hz
		SPACE		"0"	1176	1180	1184	
	Answer Mode	MARK		"1"	1646	1650	1654	
		SPACE		"0"	1846	1850	1854	
Receive Signal Amplitude Note)	AIN+				—	—	−6	dBm
Receive Signal Detect Amplitude($\overline{C}$) Note)	VR2; Opened		OFF → ON		—	—	−42	dBm
	Orig.; 1750 Hz Ans.; 1080 Hz		ON → OFF		−48	—	—	
Hysteresis ($\overline{CD}$)	Originate Mode; 1750 Hz Answer Mode; 1080 Hz				1	—	—	dB
$\overline{CD}$ Delay Time	−60 dBm → −20 dBm ($\overline{CD}$ = "1" → $\overline{CD}$ = "0")				10	—	40	ms
$\overline{CD}$ Hold Time	−20 dBm → −60 dBm ($\overline{CD}$ = "0" → $\overline{CD}$ = "1")				0	—	40	ms
Received Data (RD) Bias Distortion	300 bps Alternative Pattern				0	—	±10	%

Note: Receive signal amplitude is specified under the condition of +6 dB voltage gain of the on-chip pre-amplifier.

DTMF Generator

(VA, VD = +5 V ±10%, Ta = −40°C to +85°C)

Parameter	Condition		Min.	Typ.	Max.	Unit
Tone Amplitude	PB $R_L \geq 20$ kΩ	Low-Group	−8.5	−6.5	−4.5	dBm
		High-Group	−7.5	−5.5	−3.5	
Tone Amplitude Ratio	High-G. Tone/Low-G. Tone		0	1	2	dB
Tone Frequency	To nominal frequency		−1.5	—	+1.5	%
Total Harmonic Distortion	All Harmonics/ Fundamental		—	—	−23	dB
PBG1 to PBG4 Input Data Set-up Time	TPBGS, Fig. 6		250	—	—	ns
PBG1 to PBG4 Input Data Hold Time	TPBGH, Fig. 6		250	—	—	ns

DTMF Receiver

(VA, VD = +5 V ±10%, Ta = −40°C to +85°C)

Parameter	Condition		Min.	Typ.	Max.	Unit
Detect Amplitude	For each single tone		−40	—	0	dBm
Non-detect Amplitude			—	—	−60	dBm
Detect Frequency	To nominal frequency		—	—	±1.5	%
Non-detect Frequency			±3.8	—	—	%
Allowable Twist	High-G. Tone/Low-G. Tone		−6	—	+6	dB
Noise to Signal Ratio	N(0.3 to 3.4 kHz)/S_{DTMF}		—	−12	—	dB
Dial Tone Rejection Ratio	380 to 420 Hz		37	—	—	dB
Signal Repetition Time	T_C	Fig. 1	120	—	—	ms
Time to Receive	T_S		49	—	—	
Invalid Tone Duration	T_I		—	—	24	
Output Delay Time	T_G		24	39	49	
Interdigit Pause	T_P		30	—	—	
Acceptable Drop Out	T_B		—	—	2	
SP Delay Time	T_{SP}		6	8	10	
Output Trailing Edge Delay	T_D		21	28	35	

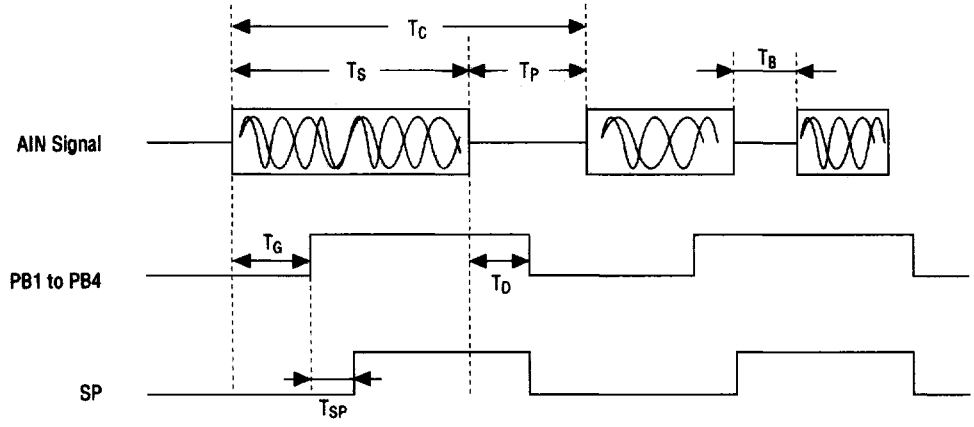


Figure 1

FUNCTIONAL DESCRIPTION AND APPLICATION

Operation Mode

Table-1

Mode Select			Operation Mode		Function Block		
MODE1	MODE2	MODE3			DTMF Gen.	DTMF Rec.	FSK (V.21) MODEM
0	0	0	DTMF Tone Transmit		*	*	
1	0	0	DTMF Tone Receive			*	
0	1	0	Originate MODEM			*	*
1	1	0	Answer MODEM			*	*
0	0	1	Analog Loop	Orig.		*	*
1	0	1	Back Test	Ans.		*	*
0	1	1	Remote Digital	Orig.		*	*
1	1	1	Loop Back Test	Ans.		*	*

Note 1 : * ; Active

Note 2 : In the loop back test modes, the originate and the answer correspond to the set mode of the transmitter.

Signal flow concept, for the modem normal operating mode and the loop back test modes, are shown in Fig. 2, Fig. 3 and Fig. 4.

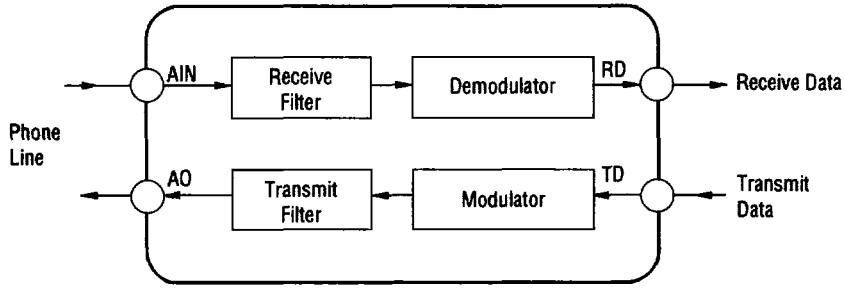


Figure 2 Normal Operation

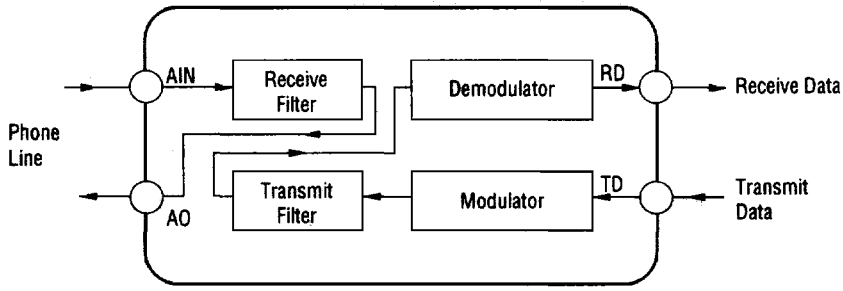


Figure 3 Analog Loop Back Test

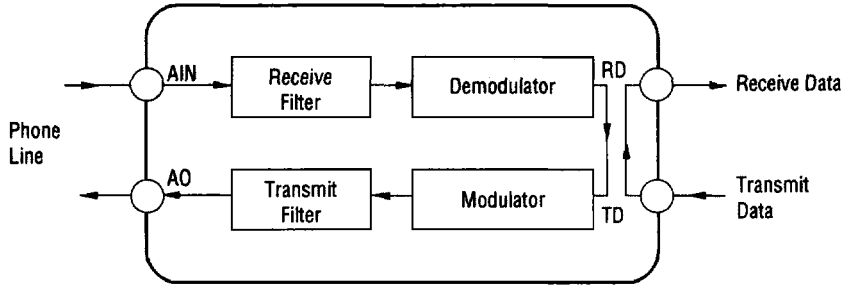


Figure 4 Remote Digital Loop Back Test

External Bus-Line Connection

Since the DTMF receiver provided on this device is always active (PB1 to PB4: Low-Output Impedance), both 4 bits PBG and PB pins can not be connected externally like I/O bus line. Therefore, differing from the other family products, the circuit wiring as shown in Fig. 5 is not possible.

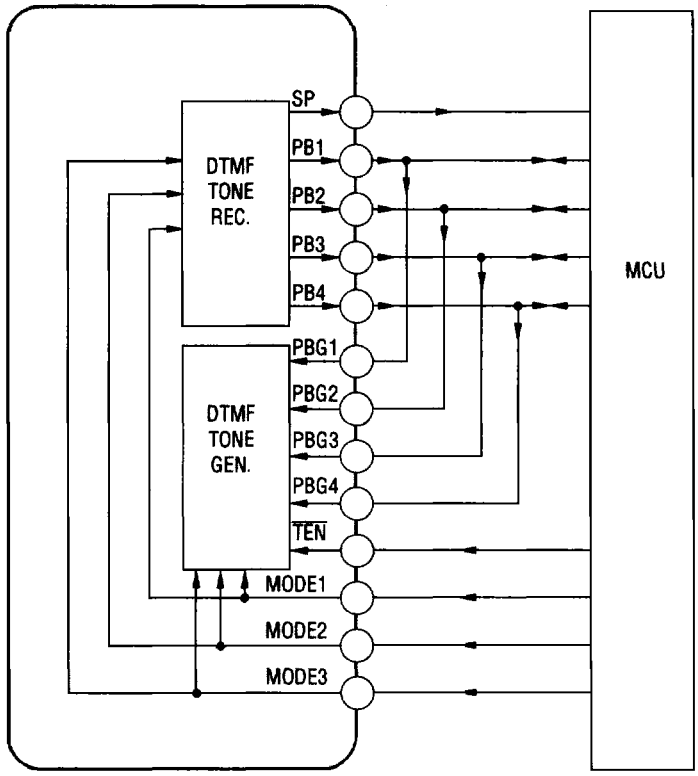


Figure 5

DTMF Tone Generator

During $\overline{TEN}$ is on digital "0" state, DTMF tone is generated according to Table-2.

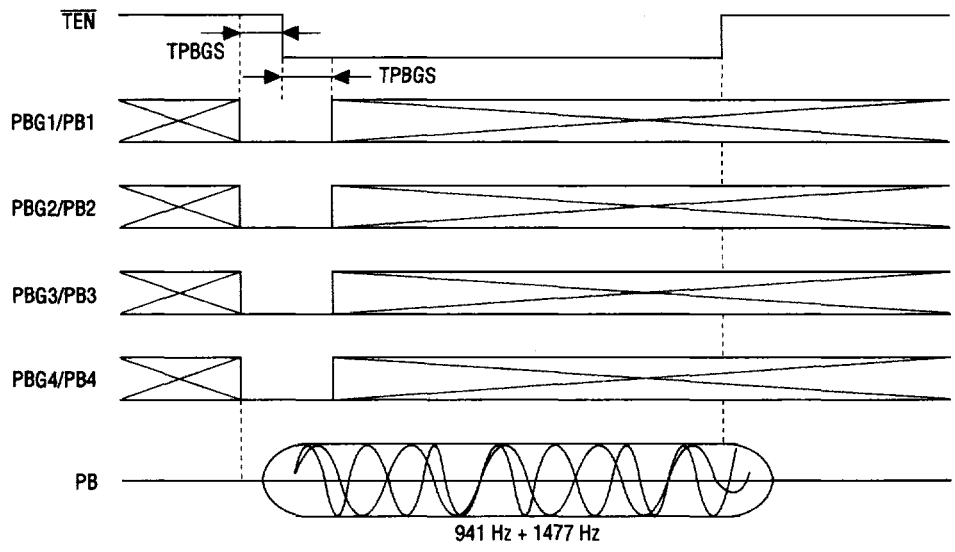


Figure 6

DTMF Tone Receiver

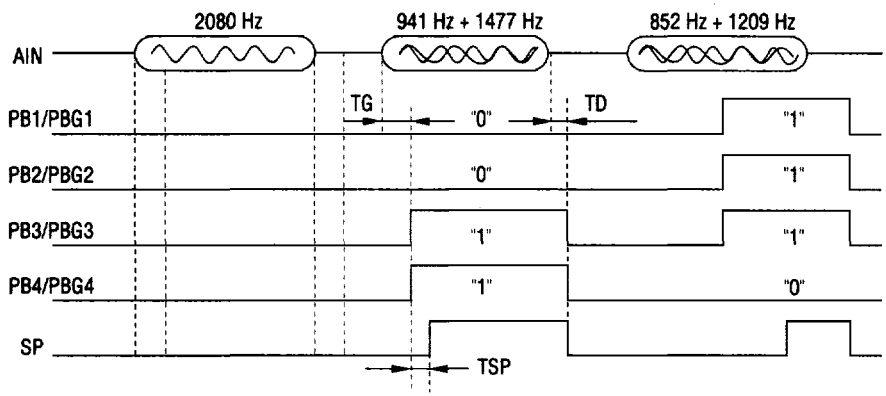


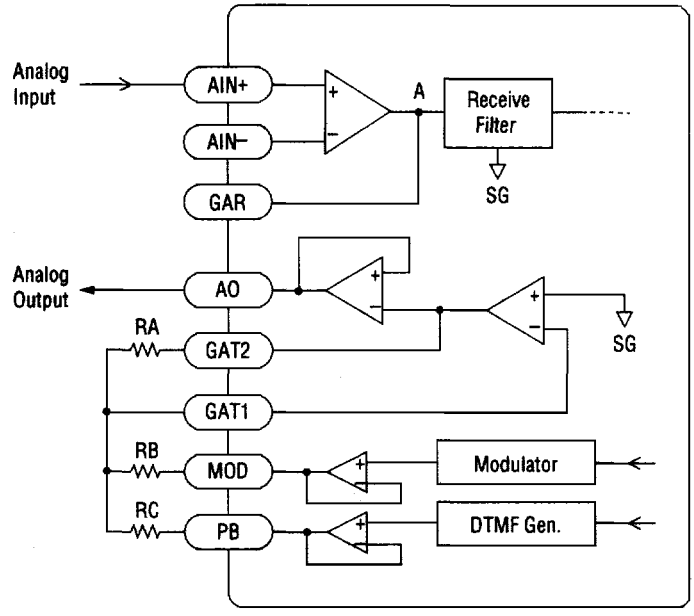
Figure 7

Table-2

Button	Low-Group Freq. (Hz)				High-Group Freq. (Hz)				PB4/	PB3/	PB2/	PB1/
	697	770	852	941	1209	1336	1477	1633	PBG4	PBG3	PBG2	PBG1
1	*				*				0	0	0	1
2	*					*			0	0	1	0
3	*						*		0	0	1	1
4		*			*				0	1	0	0
5		*				*			0	1	0	1
6		*					*		0	1	1	0
7			*		*				0	1	1	1
8			*			*			1	0	0	0
9			*				*		1	0	0	1
0				*		*			1	0	1	0
*				*	*				1	0	1	1
#				*			*		1	1	0	0
A	*							*	1	1	0	1
B		*						*	1	1	1	0
C			*					*	1	1	1	1
D				*				*	0	0	0	0

Analog Output Interface

Analog output and input circuit of the MSM7523 is described in Fig. 8.



Note: RA, RB, RC; External Resistor

Figure 8 Analog Output and INput Circuit

Since the minimum load resistance for AO is specified to be 20 kΩ, AO should be interfaced to phone line normally through an external operational amplifier as shown in Fig. 9.

If AO can directly drive the low impedance of phone line, it may be convenient for some applications. But, since the output signal amplitude (limited by the applied supply voltage, etc.) is not so high as described below, the external amplifier may be often required depending on application.

When the external amplifier is needed to amplify the output signal, the low impedance (ex. 600 Ω) driving capability is not necessary for the terminal AO and the power consumption will increase if the driving capability is implemented on the chip.

These are reasons why the low impedance driving capability has not been given to the MSM7523.

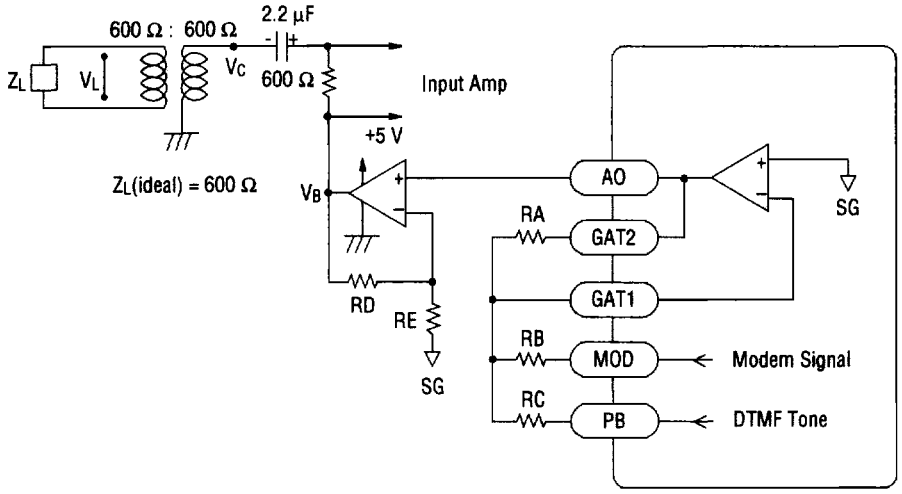
Modem output signal amplitude at MOD:	–1 dBm ±2 dB
DTMF output signal amplitude at PB:	–6.5 dBm ±2 dB (Low-G.)
	–5.5 dBm ±2 dB (High-G.)

The reason why each tone of DTMF signal is lower (to 1/2) than that of Modem signal is that DTMF signal consists of a tone-pair and FSK Modem signal is a single wave. The peak to peak analog signal voltage swing is limited by the linear range of on-chip operational amplifiers and its marginal value is 2.2 V_{p-p}.

The following describes how to design the output signal amplitude over a phone line.

(1)The relative amplitude of the Modem and the DTMF signal are determined by the ratio of RA/RB and RA/RC. The larger ratio must be equal to 1 and the smaller should be less than 1, and each resistor has to be higher than 20 kΩ.
In normal case, RC is equal to RA and RB is equal to RA or higher than RA.

(2) The absolute amplitude of the transmit signal sent over a phone line is determined by an external amplifier.
The voltage gain of the external amplifier should be given considering two factors.
The first one is the signal amplitude at AO determined by the ratio of RA/RB and RA/RC and the second one is the insertion loss of a line transformer.
The loss is ideally 6 dB, but is not equal to 6 dB in many actual cases.
Considering all of them, the voltage gain should be given by the ratio of RD and RE.



Note: Ideal condition;
$V_B = 2\,V_C = 2\,V_L$

Figure 9

For the external operational amplifier, a device with the widest possible linear voltage swing range should be chosen.
Even if such an operational amplifier is chosen, it may not be sufficient to the required transmit signal amplitude in some cases because the considerable maximum amplitude (V_L) will be as follows.

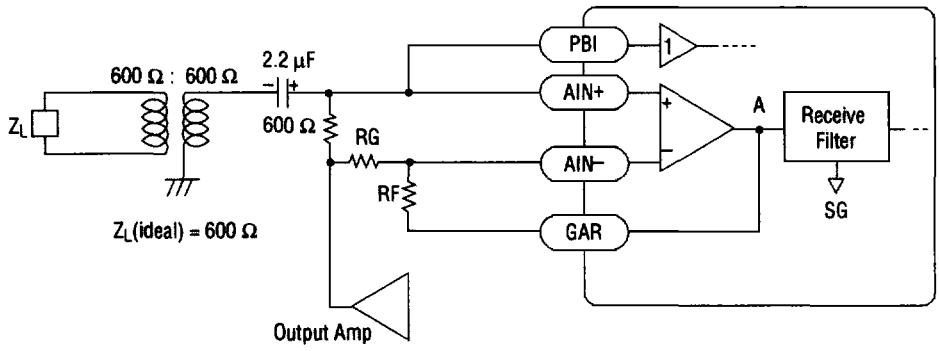
Modem transmit signal amplitude: to + 1 dBm
DTMF transmit signal amplitude: to -5 dBm/tone

(Conditions; Power Supply Voltage = +5 V ±10%
External Op. Amp = Ideal
Line Transformer = Ideal)

In actual conditions, these amplitudes are lower than the above described values.
When the required amplitude cannot be attained with +5 V single supply, it is needed to use, for example, +/-5 V or +12 V for a phone line interface circuit. In this case, AC-coupling capacitors are necessary.
Refer to Fig. 17 as an example.

Analog Input Interface

The on-chip input operational amplifiers can be applied for the 2W/4W conversion (Hybrid/ Duplexer) circuit as shown in Fig. 10.



Note: RG = RF (≥ 20 kΩ) under the ideal condition

Figure 10

The maximum input analog signal amplitude is specified with -6 dBm for both Modem signal and each DTMF tone. The specified condition is that RF is equal to RG, namely, the voltage gain of the input amplifier is 6 dB (× 2) from AIN+ to point A.

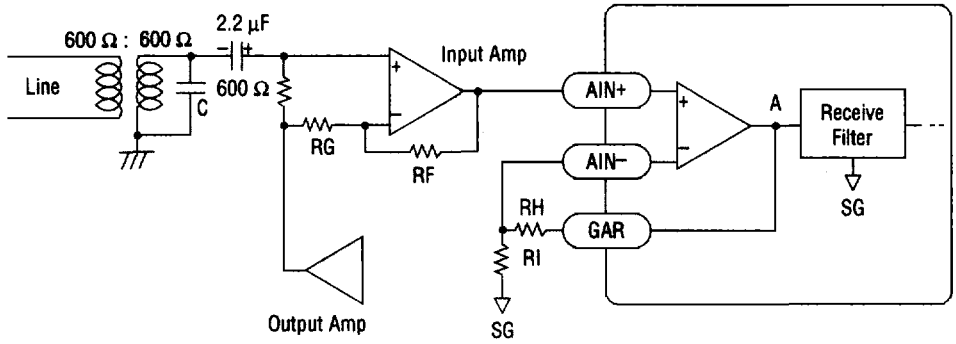
In another meaning, the Modem signal amplitude at point A will be 0 dBm (2.2 V_{p-p}) when RF is equal to RG and the specified maximum Modem signal is applied to AIN+.

Since DTMF signal is a tone-pair, the on-chip unity gain amplifier receives the DTMF tone via PBI.

To get the best performance considering S/N on the chip, it is necessary to design the signal level diagram so that the signal amplitude will be 0 dBm (2.2 V_{p-p}) on the chip when the maximum receive signal reaches to the line terminated point.

So, voltage amplifying is normally required for the input interface circuit. If modifying the ratio of RF/RG to get any voltage gain, the hybrid (Duplexer) function may become not to work well. Therefore, the external input amplifier beside the on-chip amplifier is normally needed. The application example is shown in Fig. 11. In this case, the external and the on-chip amplifiers work as the hybrid and the receive signal amplifier respectively.

Figures 12 and 13 show other applications of the on-chip amplifier.



Note 1: Ideally, RG = RF
Note 2: RH, RI ≥ 20 kΩ
Note 3: C = 0.047 µF, for out-of-band noise suppression

Figure 11

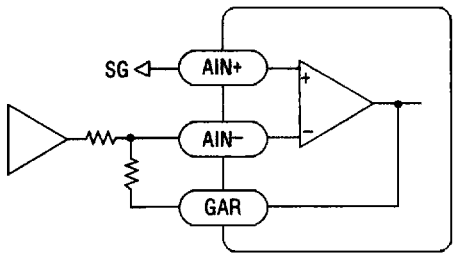


Figure 12

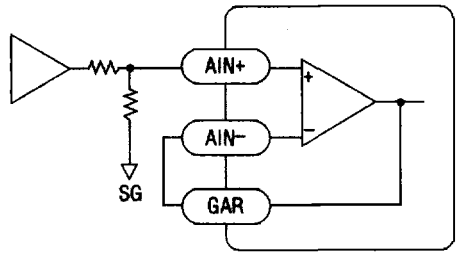
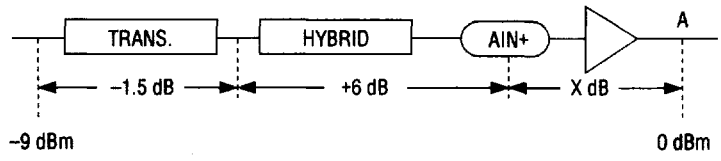


Figure 13

Design Example of Receive Signal Level Diagram

The following design procedure is considered when the receive signal amplitude range is, for example, from -9 dBm to -45.5 dBm at the line terminated point.

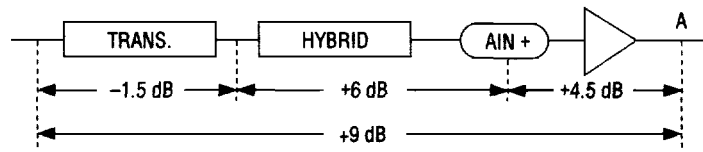
1) If the insertion loss of the line transformer is 1.5 dB, the voltage gain of the input amplifier by the on-chip operational amplifier should be 4.5 dB based on the following equation. Figure14 should be referred to this consideration.



$-9 - 1.5 + 6 + X = 0 \Rightarrow X = 4.5$ dB

Figure 14

When RH and RI (shown in Fig. 11) are 22 kΩ and 33 kΩ respectively, the voltage gain will be 4.5 dB.
When considering the carrier detect (CD) function, the carrier detect ON (CD = "0") and OFF (CD = "1") will be lower than -45 dBm and higher than -51 dBm respectively.



CD/ON :	< -45 dBm	< -36 dBm
CD/OFF:	< -51 dBm	< -42 dBm

Figure 15

Note) The carrier detect amplitude is specified with < -42 dBm for CD/ON and > -48 dBm for CD/OFF as electrical characteristics.
But, these values are based on the following conditions:

Defined Point ..... Terminal "AIN+"
Input Amp's Gain ..... +6 dB

So, CD/ON and CD/OFF amplitude at point A will be < -36 dBm and > -42 dBm, respectively.
This result (CD/ON; < -45 dBm) does not satisfy the original design goal (Receive Signal Amplitude: -9 to -45.5 dBm), slightly.

CD/ON amplitude is adjustable by trimming of the on-chip voltage reference.

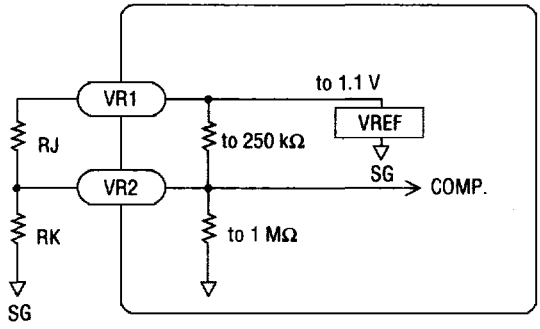


Figure 16

For the carrier detect circuit, approximate 0.9 V is used as a comparison voltage originally.

Additional external resistors, RJ and RK, can change this comparison voltage and the sensitivity for the CD/ON amplitude can be higher by 0.5 dB.

$$1.1\ V \times \frac{1\ M\Omega}{1\ M\Omega + 250\ k\Omega} = 0.88\ V \text{ (Original VR2 voltage)}$$

$$0.88\ V \times 10^{-0.5/20} = 0.83\ V$$

For example, 7.2 kΩ and 22 kΩ can be chosen for RJ and RK respectively.
RJ and RK should be much lower than on-chip resistors and (RJ + RK) should be higher than 20 kΩ.

Above mentioned procedure is just a reference for customer's design consideration, and all of described values are not guaranteed.
So, it is necessary to use the variable resistor for strict adjustment.

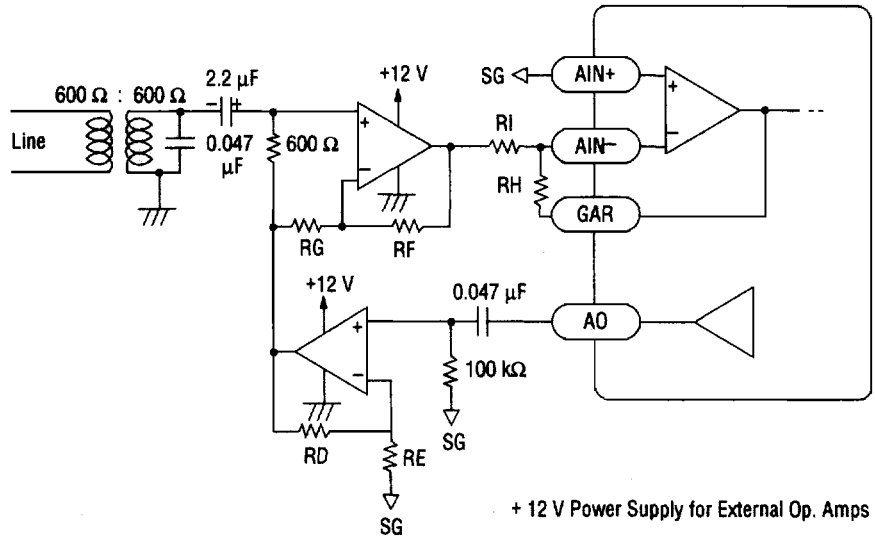
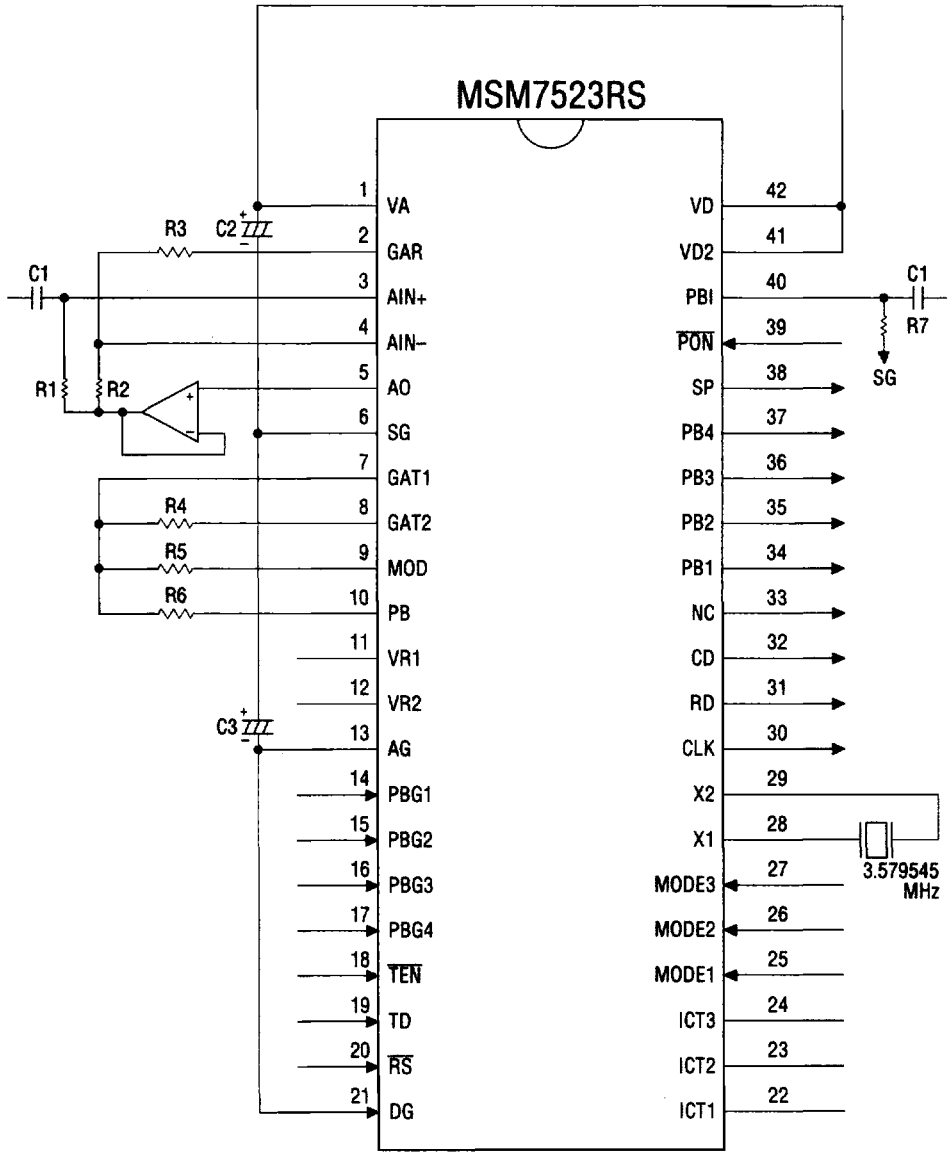

600 Ω : 600 Ω
2.2 μF
+12 V
SG
AIN+
Line
0.047 μF
600 Ω
RI
AIN−
RH
GAR
RG
RF
+12 V
0.047 μF
AO
100 kΩ
SG
RD
RE
SG
+ 12 V Power Supply for External Op. Amps

Figure 17

Application Circuit

Pin connection



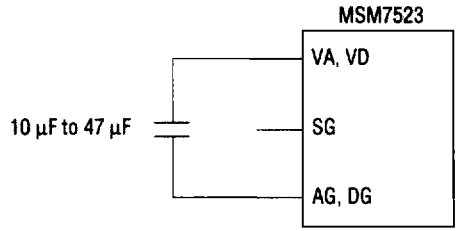
R1 = 600 Ω, R2 = R3 = R4 = R5 = R6 = 51 kΩ, R7 ≥ 200 kΩ
C1 = 2 μF, C2 = C3 = 10 μF

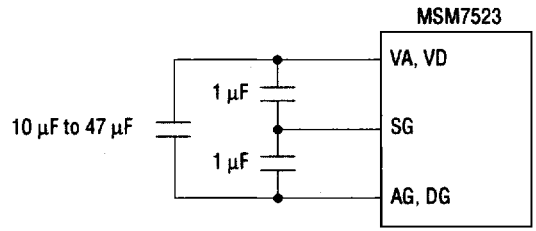
Bypass Capacitor Connections

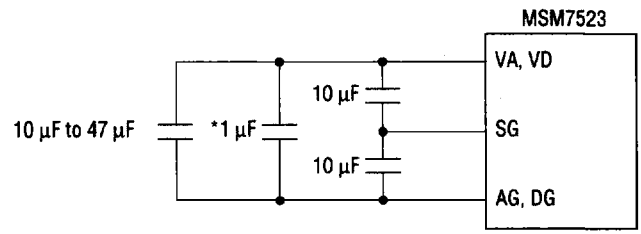
The MSM7523 contains analog circuits.

Note that noise occurred in the power supply by trouble in other circuits may cause degradation in characteristics of the device.

The examples of connected bypass capacitors of the MSM7523 are shown below.







* Laminated ceramic capacitor