Signetics

FAST 74F168, 74F169 Counters

74F168 4-Bit Up/Down Decade Synchronous Counter
74F169 4-Bit Up/Down Binary Synchronous Counter
Product Specification

FAST Products

FEATURES

- **Synchronous counting and loading**
- **Up/down counting**
- **BCD decade counter- 'F168**
- **Modular 16 binary counter- 'F169**
- **Two Count Enable inputs for n-bit cascading**
- **Positive edge-triggered clock**
- **Built-in lookahead carry capability**
- **Presettable for programmable operation**

TYPE	TYPICAL f_{MAX}	TYPICAL SUPPLY CURRENT (TOTAL)
74F168	115MHz	35mA
74F169	115MHz	35mA

ORDERING INFORMATION

PACKAGES	COMMERCIAL RANGE V_{CC} = 5V±10%; T_A = 0°C to +70°C
16-Pin Plastic Dip	N74F168N, N74F169N
16-Pin Plastic SO	N74F168D, N74F169D

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE

PINS	DESCRIPTION	74F(U.L.) HIGH/LOW	LOAD VALUE HIGH/LOW
D_0 - D_3	Parallel data inputs	1.0/1.0	20µA/0.6mA
$\overline{CEP}$	Count Enable parallel input (active Low)	1.0/1.0	20µA/0.6mA
$\overline{CET}$	Count Enable Trickle input (active Low)	1.0/2.0	20µA/1.2mA
CP	Clock input (active rising edge)	1.0/1.0	20µA/0.6mA
$\overline{PE}$	Parallel Enable input (active Low)	1.0/1.0	20µA/0.6mA
U/$\overline{D}$	Up/Down count control input	1.0/1.0	20µA/0.6mA
Q_0 -Q_3	Flip-flop outputs	50/33	1.0mA/20mA
$\overline{TC}$	Terminal count output (active Low)	50/33	1.0mA/20mA

NOTE:
One (1.0) FAST Unit Load is defined as: 20µA in the High state and 0.6mA in the Low state.

DESCRIPTION

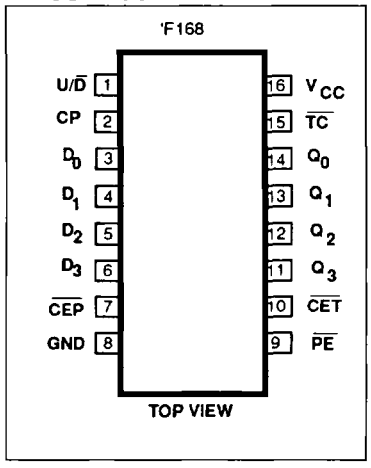
The 74F168 and 74F169 are 4-bit synchronous Up/Down Counters. The 74F168 is a synchronous, presettable BCD Decade Up/Down Counter featuring an internal carry look-ahead for applications in high speed counting designs. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the Count Enable inputs and internal gating. This mode of operation eliminates the output spikes which are normally associated with asynchronous (ripple clock) counters. A buffered clock input triggers the flip-flops on the Low-to-High transition of the clock. The counter is fully programmable; that is, the outputs may be preset to either level.

Presetting is synchronous with the clock and takes place regardless of the levels of the Count Enable inputs. A Low level on the Parallel Enable ($\overline{PE}$) input disables the counter causes the data at the D_n input to be loaded into the counter on the next Low-to-High transition of the clock.

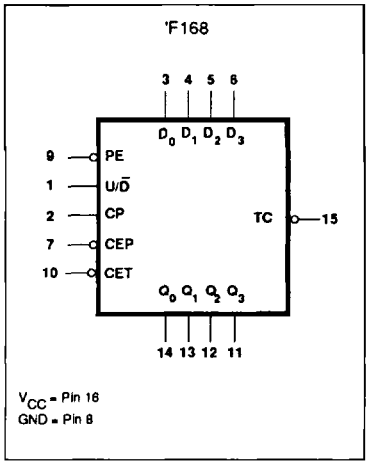
The direction of the counting is controlled by the by the Up/Down (U/$\overline{D}$) input; a High will cause the count to increase, a Low will cause the count to decrease.

The carry look ahead circuitry is provided for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two Count Enables($\overline{CEP}$, $\overline{CET}$) inputs and a Terminal Count ($\overline{TC}$) output. Both Count Enable inputs must be Low to count. The $\overline{CET}$ input is fed forward to enable the $\overline{TC}$ output. The $\overline{TC}$ output thus enabled will produce a Low output pulse with a duration approximately equal the High level portion of Q_0 output. The Low level $\overline{TC}$ pulse is used to enable successive cascaded stages. See Figure 1 for the fast synchronous multistage counting connections. The 74F169 is identical except that it is a Modula 16 counter.

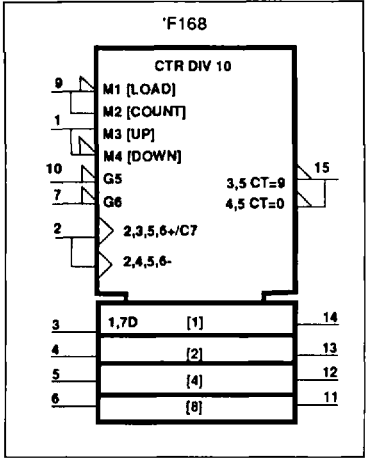
PIN CONFIGURATION



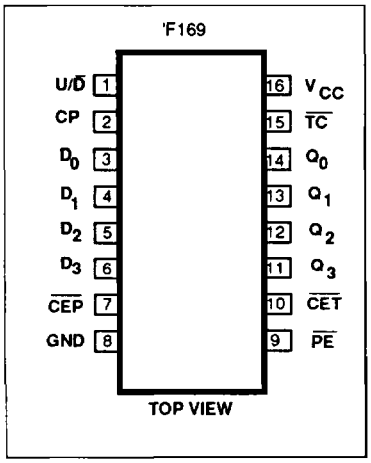
LOGIC SYMBOL



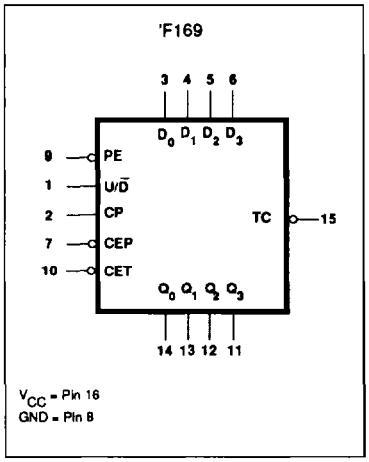
LOGIC SYMBOL(IEEE/IEC)



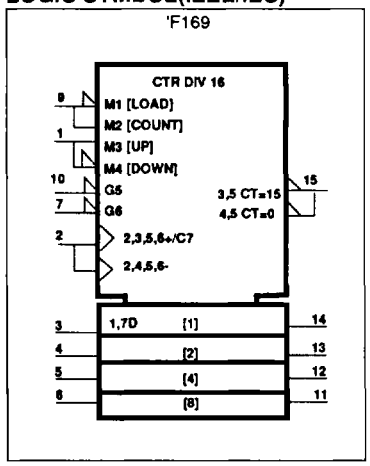
PIN CONFIGURATION



LOGIC SYMBOL



LOGIC SYMBOL(IEEE/IEC)



FUNCTIONAL DESCRIPTION

The 'F168 and 'F169 use edge triggered J-K type flip-flops and have no constraints on changing the control or data input signals in either state of the clock. The only requirement is that the various inputs attain the desired state at least a set-up time before the rising edge of the clock and remain valid for the recommended hold time thereafter. The parallel load operation takes precedance over the other operations, as indicated in the Mode Select Table. When $\overline{PE}$ is Low, the data on the D_0-D_3 inputs enter the flip-flops on the next rising edge of the clock. In order for counting to occur, both $\overline{CEP}$ and $\overline{CET}$ must be Low and $\overline{PE}$ must be High; the U/$\overline{D}$ input determines the direction of counting. The Terminal Count ($\overline{TC}$) output is normally High and goes Low, provided that $\overline{CET}$ is Low. When a counter reaches zero in the count down mode or reaches 9 (15 for 'F169) in the count up mode. The $\overline{TC}$ output state is not a function of the Count Enable Parallel($\overline{CEP}$) input level. The $\overline{TC}$ output of the 'F168 decade counter can also be Low in the illegal states 11, 13, 15, which can occur when power is turned on or via parallel loading. If an illegal state occurs, the 'F168 will return to the legitimate sequence within two counts. Since the $\overline{TC}$ signal is derived by decoding the flip-flop states, there exists the possibility of decoding spikes on $\overline{TC}$. For this reason the use of $\overline{TC}$ as a clock signal is not recommended (See logic equations below).

1) Count Enable= $\overline{CEP}\cdot\overline{CET}\cdot\overline{PE}$
2) Up: $\overline{TC}=Q_0\cdot Q_3\cdot(U/\overline{D})\cdot\overline{CET}$
3) Down: $\overline{TC}=\overline{Q_0}\cdot\overline{Q_1}\cdot\overline{Q_2}\cdot\overline{Q_3}\cdot(U/\overline{D})\cdot\overline{CET}$

MODE SELECT-FUNCTION TABLE

INPUTS						OUTPUTS		OPERATING MODE
CP	U/$\overline{D}$	$\overline{CEP}$	$\overline{CET}$	$\overline{PE}$	D_n	Q_n	$\overline{TC}$	
↑	X	X	X	l	l	L	(1)	Parallel load (Dn → Qn)
↑	X	X	X	X	X	H	(1)	
↑	h	l	l	h	X	Count up	(1)	Count up (increment)
↑	l	l	l	h	X	Count down	(1)	Count down (decrement)
↑	X	h	X	h	X	q_n	(1)	Hold (do nothing)
↑	X	X	X	h	X	q_n	H	

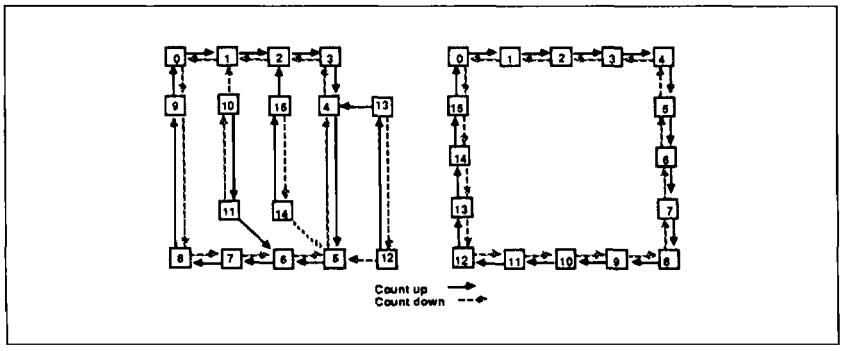
H = High voltage level
h = High voltage level one setup prior to the Low-to-High clock transition
L = Low voltage level
l = Low voltage level one setup prior to the Low-to-High clock transition
q = Lower case letters indicate the state of the referenced output prior to the Low-to-High clock transition
X = Don't care
↑ = Low-to-High clock transition
(1) = $\overline{TC}$ is Low when $\overline{CET}$ is Low and the counter is at Terminal Count.
The Terminal Count Up is (HLLH) and Terminal Count Down is (LLLL) for 'F168.
The Terminal Count Up is (HHHH) and Terminal Count Down is (LLLL) for 'F169.

MODE SELECT TABLE

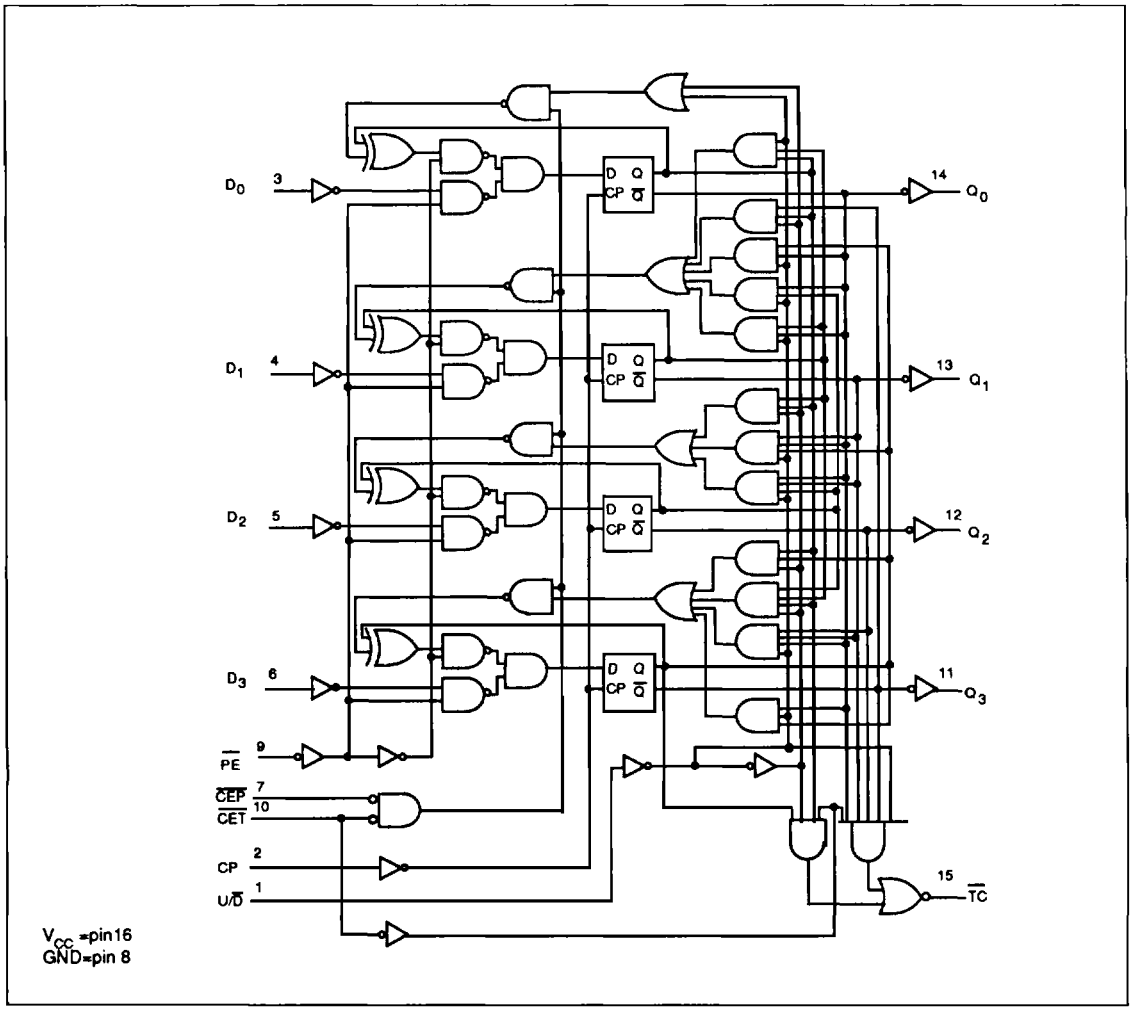
INPUTS				OPERATING MODE
$\overline{PE}$	$\overline{CEP}$	$\overline{CET}$	U/$\overline{D}$	
L	X	X	X	Load (Dn → Qn)
H	L	L	H	Count up (increment)
H	L	L	L	Count down (decrement)
H	H	X	X	No change (Hold)
H	X	H	X	No change (Hold)

H = High voltage level
L = Low voltage level
X = Don't care

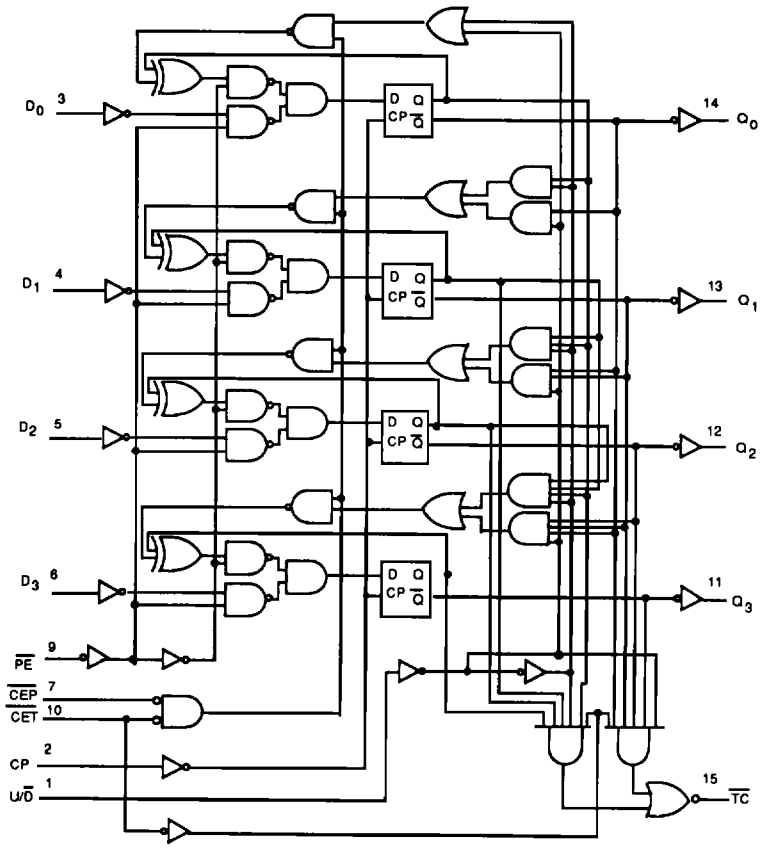
STATE DIAGRAM



LOGIC DIAGRAM for'F168



LOGIC DIAGRAM for 'F169



V_{CC} =pin16
GND=pin 8

APPLICATION

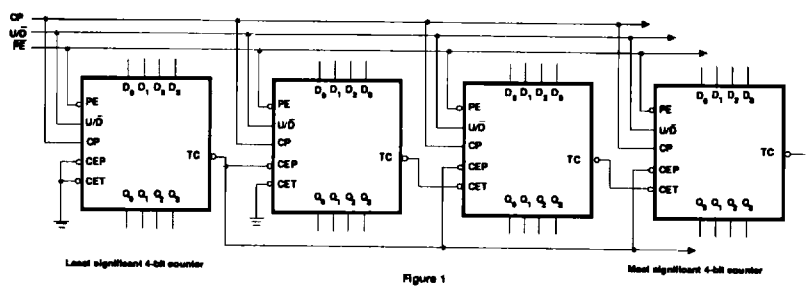


Figure 1
Synchronous multistage counting scheme

ABSOLUTE MAXIMUM RATINGS

(Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted these limits are over the operating free-air temperature range.)

SYMBOL	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	-0.5 to +7.0	V
V_{IN}	Input voltage	-0.5 to +7.0	V
I_{IN}	Input current	-30 to +5	mA
V_{OUT}	Voltage applied to output in High output state	-0.5 to +V_{CC}	V
I_{OUT}	Current applied to output in Low output state	40	mA
T_A	Operating free-air temperature range	0 to +70	°C
T_{STG}	Storage temperature	-65 to +150	°C

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS			UNIT
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5.0	5.5	V
V_{IH}	High-level input voltage	2.0			V
V_{IL}	Low-level input voltage			0.8	V
I_{IK}	Input clamp current			-18	mA
I_{OH}	High-level output current			-1	mA
I_{OL}	Low-level output current			20	mA
T_A	Operating free-air temperature range	0		70	°C

DC ELECTRICAL CHARACTERISTICS

(Over recommended operating free-air temperature range unless otherwise noted.)

SYMBOL	PARAMETER		TEST CONDITIONS[1]		LIMITS			UNIT
					Min	Typ[2]	Max	
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}	2.5			V
			V_{IH} = MIN, I_{OH} = MAX	±5%V_{CC}	2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IL} = MAX	±10%V_{CC}		0.35	0.50	V
			V_{IH} = MIN, I_{OL} = MAX	±5%V_{CC}		0.35	0.50	V
V_{IK}	Input clamp voltage		V_{CC} = MIN, I_I = I_{IK}			-0.73	-1.2	V
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7.0V				100	µA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.7V				20	µA
I_{IL}	Low-level input current	$\overline{CET}$	V_{CC} = MAX, V_I = 0.5V				-1.2	mA
		others					-0.6	mA
I_{OS}	Short circuit output current[3]		V_{CC} = MAX		-60		-150	mA
I_{CC}	Supply current (total)[4]		V_{CC} = MAX			35	52	mA

NOTES:

1. For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable type.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Not more than one output should be shorted at a time. For testing I_{OS}, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I_{OS} tests should be performed last.
4. I_{CC} is measured with after applying a momentary 4.5V, then ground to the clock input with all other inputs grounded and all outputs open.

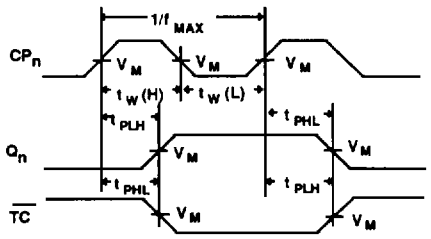
AC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
f_{MAX}	Maximum clock frequency		Waveform 1	100	115		90		MHz
t_{PLH} t_{PHL}	Propagation delay CP to Q_n ($\overline{PE}$, High or Low)		Waveform 1	3.0 4.0	6.5 9.0	8.5 11.5	3.0 4.0	9.5 13.0	ns
t_{PLH} t_{PHL}	Propagation delay CP to $\overline{TC}$		Waveform 1	5.5 4.0	12.0 8.5	15.5 11.0	5.5 4.0	17.0 12.5	ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CET}$ to $\overline{TC}$		Waveform 2	2.5 2.5	4.5 6.0	6.0 8.0	2.5 2.5	7.0 9.0	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	'F168	Waveform 3	3.5 4.0	8.5 12.5	11.0 16.0	3.5 4.0	12.5 17.5	ns
t_{PLH} t_{PHL}	Propagation delay U/$\overline{D}$ to $\overline{TC}$	'F169	Waveform 3	3.5 4.0	8.5 8.0	15.0 10.5	3.5 4.0	15.5 12.0	ns

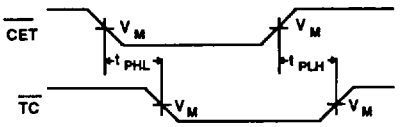
AC SETUP REQUIREMENTS

SYMBOL	PARAMETER		TEST CONDITION	LIMITS					UNIT
				T_A = +25°C, V_{CC} = 5V, C_L = 50pF, R_L = 500Ω			T_A = 0°C to +70°C, V_{CC} = 5V ±10%, C_L = 50pF, R_L = 500Ω		
				Min	Typ	Max	Min	Max	
$t_s(H)$ $t_s(L)$	Setup time, High or Low D_n to CP		Waveform 4	4.0 4.0			4.5 4.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low D_n to CP		Waveform 4	3.0 3.0			3.5 3.5		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP		Waveform 5	5.0 5.0			5.5 5.5		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{CEP}$ or $\overline{CET}$ to CP		Waveform 5	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low $\overline{PE}$ to CP		Waveform 4	8.0 8.0			9.0 9.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low $\overline{PE}$ to CP		Waveform 4	0 0			0 0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low U/$\overline{D}$ to CP	'F168	Waveform 6	11.0 16.5			12.5 18.0		ns
$t_s(H)$ $t_s(L)$	Setup time, High or Low U/$\overline{D}$ to CP	'F169	Waveform 6	11.0 7.0			12.5 8.0		ns
$t_h(H)$ $t_h(L)$	Hold time, High or Low U/$\overline{D}$ to CP		Waveform 6	0 0			0 0		ns
$t_w(H)$ $t_w(L)$	CP_U or CP_D Pulse width, High or Low		Waveform 1	5.0 5.0			5.5 5.5		ns

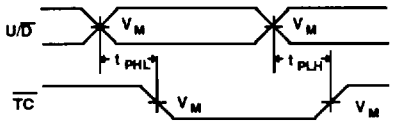
AC WAVEFORMS



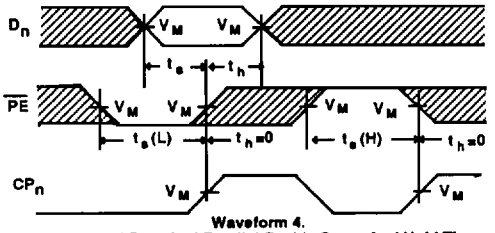
Waveform 1.
Propagation Delay, Clock Input To Output, Clock Pulse Width, and Maximum Clock Frequency



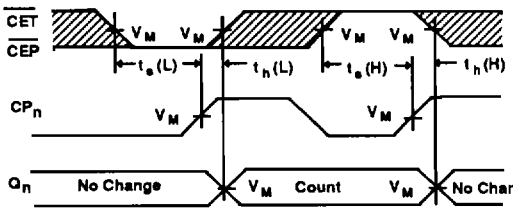
Waveform 2.
Propagation Delay, $\overline{CET}$ Input to Terminal Count Output



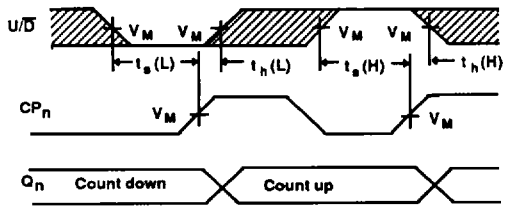
Waveform 3.
Propagation Delay, U/$\overline{D}$ Input to Terminal Count Output



Waveform 4.
Data Parallel Data And Parallel Enable Setup And Hold Times



Waveform 5.
Count Enable Data Setup And Hold Times

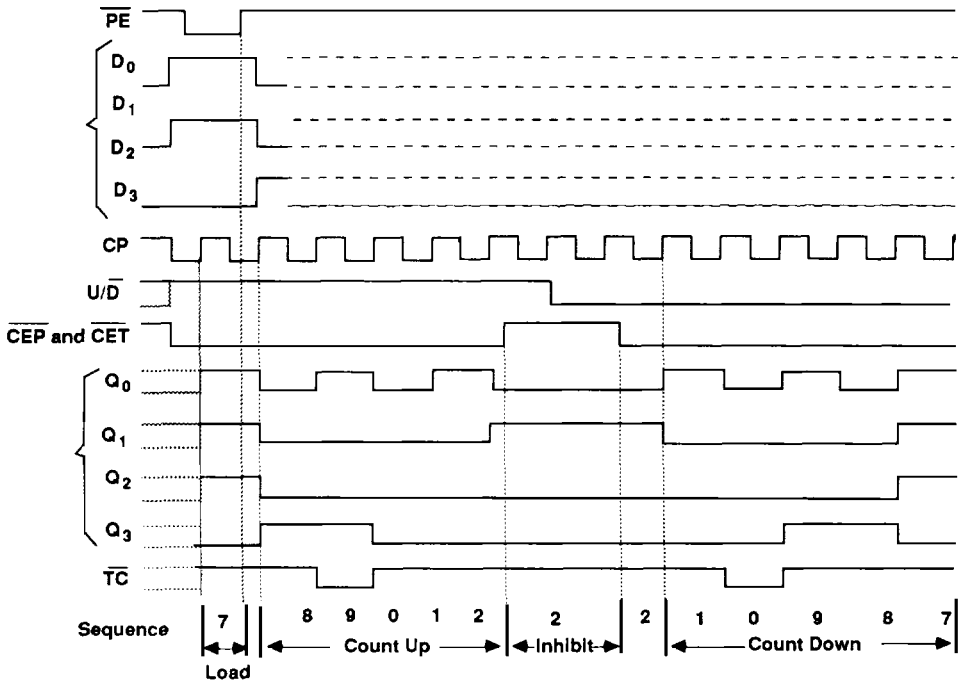


Waveform 6.
Up/Down Control Setup And Hold Times

NOTE: For all waveforms, V_M = 1.5V.

The shaded areas indicate when the input is permitted to change for predictable output performance.

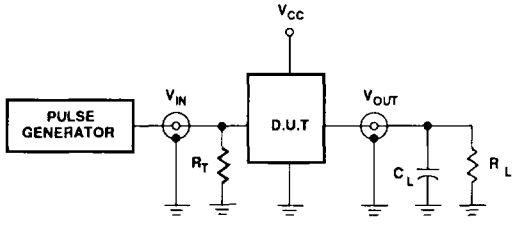
TIMING DIAGRAM (Typical clear, load, and count sequence) for 'F168



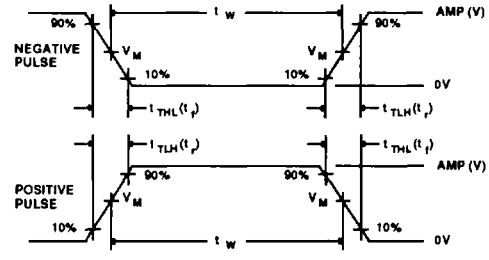
NOTES: Illustrated above is the sequence for the 'F168. The operation of the 'F169 is similar.

1. Load (preset) to BCD seven
2. Count up to eight, nine (maximum),zero, one, and two
3. Inhibit
4. Count down to one, zero (minimum), nine eightm and seven

TEST CIRCUIT AND WAVEFORMS



Test Circuit For Totem-Pole Outputs



V_M = 1.5V

Input Pulse Definition

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_{TLH}	t_{THL}
74F	3.0V	1MHz	500ns	2.5ns	2.5ns