ARINC 429 Multi-channel Buffer Receiver (RTA) (N Channel, Silicon Gate)

EF4442

Datasheet

Features

- **Four Independent Receivers**
- **OneTransmitter in A Mode**
- **Direct 6800 Microprocessor Interface**
- **8-bit Data Bus**
- **ARINC Interface: “1” and “0” Lines, RZ Code**
- **Software Label Control in A Mode**
- **Parity Control: Odd or No Parity**
- **Interrupt Capability in A Mode**
- **Test Mode Capability**

Description

The EF4442 is a reception interface for 4 ARINC 429 channels.

Two models of operation are provided:

- When in A mode, the circuit can be considered as a peripheral of an EF 6800 or EF6802 microprocessor and is totally software programmable (for example, for test purposes).
- When in B mode, the parameters are hardware programmed. Reading the registers which contain messages is only possible (max. scan frequency: 2 MHz).

Screening Quality

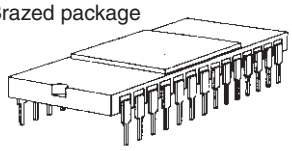
This product is manufactured in full compliance with either:

- NFC 96883 class G
- MIL-STD-883 class B
- According to e2v standards

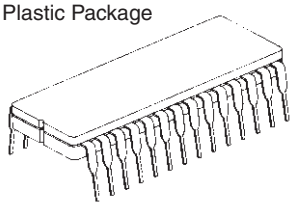
Application Note

Ask for application note: “General application principles EF4442(RTA)”

C Suffix
DIL 28
Ceramic Side Brazed package



P Suffix
DIP 28
Plastic Package



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1. Block Diagram

Figure 1-1. Block Diagram

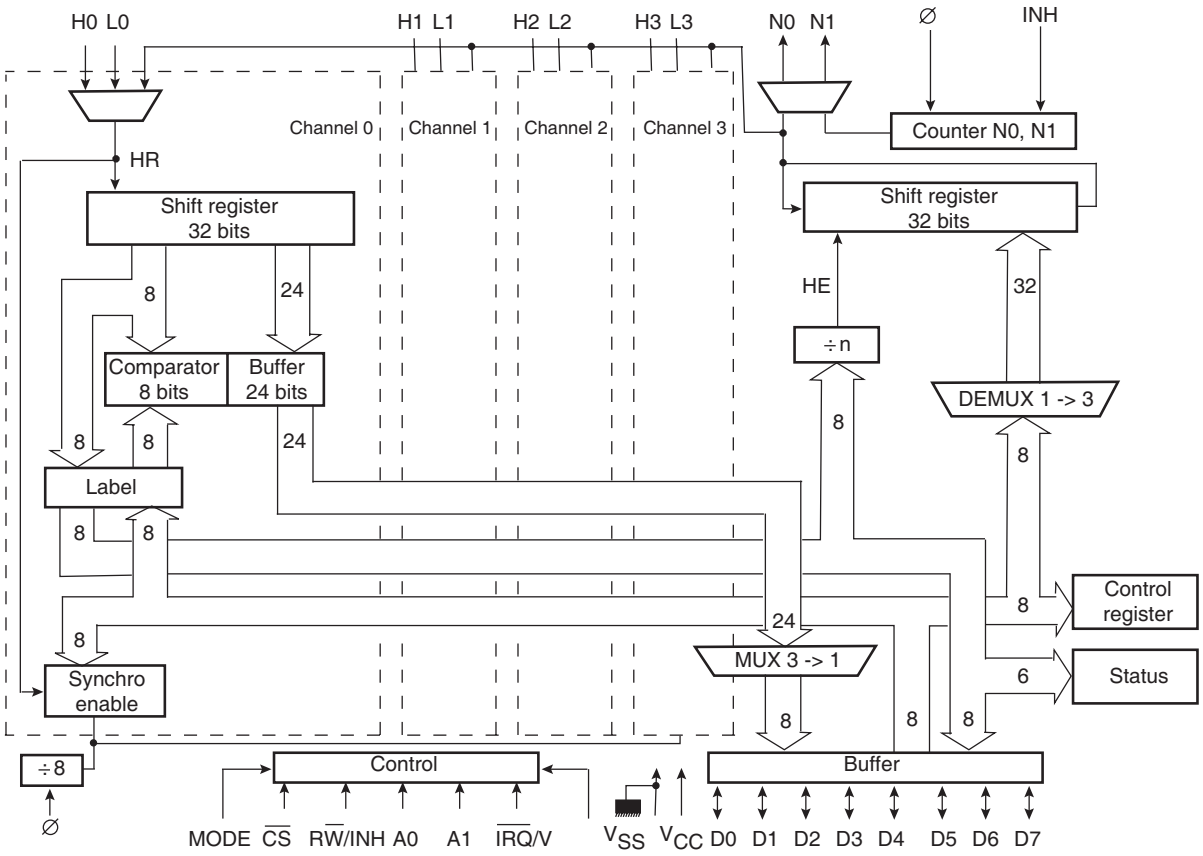


Table 1-1. Pin Description

Name Number	Description
V_{SS}	This pin is connected to the negative side of the power supply (ground).
R$\overline{W}$/INH	This input selects the direction of transfer (write or read) of data between the circuit and the microprocessor when the circuit is programmed in mode A (cf. Pin 28). In B mode, this input is used to disable the channel scanning divide by 4 counter. In A mode, this output has a transmit function. The signal corresponding to the result of ANDing.
N0	In A mode, this output has a transmit function. The signal corresponding to the result of ANDing the ARINC transmit clock and the complemented output signal of the transmit shift register (logic “0” clock output) is available on this pin. In B mode, the value of the least significant bit of the address of the scanned channel is available on this pin.
N1	In A mode, this output has a transmit function. The signal corresponding to the result of ANDing the ARINC transmit clock and the output signal of the transmit shift register (logic “1” clock available on this pin). In B mode, the value of the least significant bit of the address of the scanned channel is available on this pin.
$\overline{CS}$	In A mode, this input (active when low) selects the chip for a microprocessor access.
A0	In A mode, this input corresponds to the most significant bit of the circuit function address. In B mode, this input corresponds to the least significant bit of the address of the data byte in the message.

Table 1-1. Pin Description (Continued)

Name Number	Description
A1	In A mode, this input corresponds to the most significant bit of the circuit function address. In B mode, this input corresponds to the most significant bit of the address of the data byte in the message.
$\overline{\text{RESET}}$	This input (active when low) initializes the circuit by resetting some registers.
Ø	This input receives the clock signal from the circuit which corresponds to the phase Ø2 of the microprocessor clock.
D7	This tristate input/output is connected to the eighth line of the data bus.
D6	This tristate input/output is connected to the seventh line of the data bus.
D5	This tristate input/output is connected to the sixth line of the data bus.
D4	This tristate input/output is connected to the fifth line of the data bus.
V_{CC}	This pin is connected to the positive side of the power supply (+5V).
D3	This tristate input/output is connected to the fourth line of the data bus.
D2	This tristate input/output is connected to the third line of the data bus.
D1	This tristate input/output is connected to the second line of the data bus.
D0	This tristate input/output is connected to the first line of the data bus.
L0	This input receives the logic “0” clock from the signal shaping/separation subsystem of the first ARINC channel.
H0	This input receives the logic “1” clock from the signal shaping/separation subsystem of the first ARINC channel.
L1	This input receives the logic “0” clock from the signal shaping/separation subsystem of the second ARINC channel.
H1	This input receives the logic “1” clock from the signal shaping/separation subsystem of the second ARINC channel.
L2	This input receives the logic “0” clock from the signal shaping/separation subsystem of the third ARINC channel.
H2	This input receives the logic “1” clock from the signal shaping/separation subsystem of the third ARINC channel.
L3	This input receives the logic “0” clock from the signal shaping/separation subsystem of the fourth ARINC channel.
H3	This input receives the logic “1” clock from the signal shaping/separation subsystem of the fourth ARINC channel.
$\overline{\text{IRQ}}$/V	In A mode, this pin (active when low) constitutes an open drain output delivering the signal for interrupting the microprocessor. In B mode, this pin is an input used to program the number of high speed channels.
Mode	This input is used to program the operating mode (A or B) of the circuit and also to enable or disable this parity check.

2. Description of Registers

The EF4442 circuit features three types of internal register:

- Registers concerned with general circuit operation,
- Registers specific to the transmit channel,
- Registers specific to each receive channel.

2.1 General Registers

2.1.1 Status Register

This register is used only when the circuit is programmed in A mode. Its contents inform the microprocessor about the status of the circuit functions. Bits S0 and S4 activate output $\overline{IRQ}$ when at 1 (except S4 which is maskable - cf. description of control register).

Bits S0 and S3 at 1 indicate that the channel with the address which corresponds to the rank of the bit has received a correct message (label recognized and correct parity in the case of a circuit programmed to check the parity of messages).

Each bit is reset to 0 on reading the registers of the corresponding channel.

In transmit mode, bit S4 of the status register is set to 1 when transmission of the message is terminated.

Bit S4 is reset to 0 when control bit C4 (see below) is a 1.

Bits S5 and S6 are not used.

Bit S7 is at 1 throughout transmission.

2.1.2 Control Register

This eight-bit register (C0-C7) monitors operation of the circuit in A mode.

In receive mode, bits C0-C3 select the corresponding channels for writing or reading when set to 1 by the microprocessor.

Bit C4 at 1 enables programming of the transmit channel (data to send and transmission speed). The setting of bit C4 to 1 resets to 0 the index of the four-byte stack constituting the message to send.

Bit C5 at 1 is used to initiate transmission of the message. It is set to 0 when transmission is terminated.

Bit C6 at 1 simultaneously with bit C5 at 1 loops back the transmitted data to the input of the receive channel selected by bits C0-C3, for test purposes. It is set to 0 by any control register access.

Bit C7 at 1 masks status bit S4 and thus prevents activation of output $\overline{IRQ}$.

2.2 Transmit Channel Registers (A mode only)

2.2.1 Programmable Divider Register

This eight-bit register is programmed by the microprocessor and contains the value n of the division ratio (the least significant bit is always considered to be at 0).

The programmable divider generates a clock signal at a frequency equal to clock Ø divided by n.

2.2.2 Transmit Register

This 32-bit shift register may be programmed in four phases by the microprocessor. This writing must be effected immediately after the setting to 1 of control bit C4 (cf. description of control register). This resets to zero the index of the 4-byte stack.

The transmit register shifts the data present in it to the outputs in accordance with the states of the bits in the control register.

2.3 Receive Channel Registers

Each receive channel comprises the following registers:

2.3.1 Synchronization/Enable Register

This eight-bit register is programmable by the microprocessor.

The most significant bit (bit 7) is used, in A mode only, to disable the transfer of data at the input into the buffer register (cf. description of these two registers). The channel affected is then seen as being out of service.

The other seven bits (bits 0 - 6) select the value of the time-delay used to detect the presence of a “gap”. This is the space between two consecutive messages, the minimum duration of which is four periods of the transmit clock. This value is loaded into the register by the microprocessor, in A mode, at the same time as the enable bit.

In B mode, this value is selected from two hardwired values, according to the state on pin $\overline{IRQ}$/V.

If n is the programmed value, the gap detection time-delay will be (8n - 4) ± 4 period of clock Ø.

2.3.2 Input Register

This 32-bit shift register receives the data corresponding to the messages. The message received is transferred into the registers on its output side if:

- a gap detection signal has previously occurred,
- the registers which will receive the transferred data are not being read,
- the parity of the received message is correct if the circuit is programmed with the parity check enabled,
- the enable bit of the synchronization/enable register is set to 1 (A mode only),
- in A mode, the first eight bits received correspond to the programmed label (cf. description of label register).

2.3.3 Label Register

In A mode, this eight-bit register is programmed by the microprocessor. It contains the label to be recognized.

In B mode, this register receives the first eight bits of the received message transferred from the input register.

In this case, this register may be read by the external automatic scanning device.

2.3.4 Buffer Register

This 24-bit register receives data transferred from the input register.

It may be read by the microprocessor in A mode or by the external automatic scanning device in B mode.

3. Circuit Operation

3.1 Logic Convention

“1” (high state) = most positive level

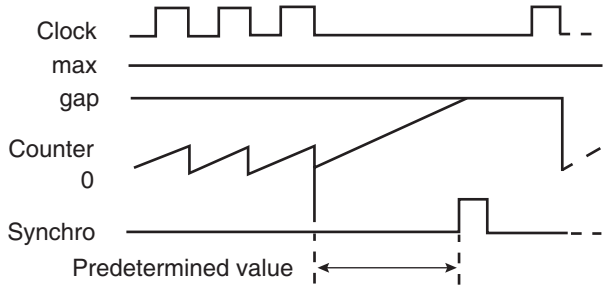
“0” (low state) = most negative level

3.2 Operation of a Receive Channel

3.2.1 Data Acquisition

Serial data is received on the “low” and the “high” lines (Hi and Li inputs). The Clock is reconstructed by OR-ing these inputs. Data is then directed towards a 32-bit shift register. Parity is computed. The reconstructed clock fall edge resets the message synchronization counter. This counter is incremented on each Ø: 8 clock period and delivers a word synchronization signal (gap) as described below (Figure 3-1) when reading a programmed value.

Figure 3-1. Gap Detection



The predetermined value together with an enable bit is loaded in the internal synchro/validation register when in A mode; it is chosen between two hardware programmed values when in B mode, according to the $\overline{IRQ}$/V pin.

Then:

- **When in A Mode**

The first 8 bits (M0-M7) that are received, are bits compared to a programmed word (label), this for each channel. If identical, the 24 other bits of the shift register are transferred in a 24-bit buffer register. The corresponding status bit is switched to 1 and the $\overline{IRQ}$ line is activated ($\overline{IRQ}$ = 0).

If the channel enable bit is in the low state, transfer is not executed and the $\overline{IRQ}$ line is not activated.

- **When in B Mode**

All the shift register bits are transferred in the label and the 24-bit buffer register.

Transfers are inhibited if the message parity is wrong in either mode (even number of bits in the high state) and if the circuit is programmed for parity check (Mode pin).

This last one generates a Ø + n frequency square wave, n being the programmed value (the least significant bit being always set to 0).

Then successively addresses the 8-bit bytes of the 24-bit buffer which are then available on the bus (D0-D7).

Reading the last byte resets the corresponding status byte to the low state.

The transfer from the receive register to the buffer register is inhibited from the “read” addressing of the channel (first or second byte) to the end of the last byte reading.

- **When in B Mode**

A divide by 4 counter is incremented on each Ø clock period and successively addresses the 4 channels. When the circuit is selected ($\overline{CS}$ = 0) and when A0 - A1 = 11, the label of the addressed channel is available on the bus (D0 - D7), as well as the channel number on the N0-N1 outputs.

Counting is inhibited when $R\overline{W}$/INH is in the high state. If the circuit is selected, the three bytes of the buffer register are then available on the bus when addressed through A0 - A1 in the same way as A mode.

The transfer from the receive register to the buffer register is done in the same way as A mode.

In order to read the message corresponding to label received, $\overline{CS}$ has to stay activated to 0 during the reading of label and message RT_1 - RT_3 (minimum $\overline{CS}$ = 0 during the reading of the label and RT_1).

However $\overline{CS}$ has to stay activated to 0 during less than 30 clock periods of PHI (Ø).

3.3 Operation of the Transmit Channel (only in A mode)

The transmit channel is composed of a 32-bit shift register and a programmable divider. The operation of this channel is controlled by the control register (C0 - C7).

C4 selects the program of the transmit channel (see “Programming In A Mode (MODE = 0)” on page 7). The 4 bytes of the shift register are loaded (including the microprocessor computed parity bit). So is the divider by n register byte.

The latter generates a divided by n frequency square wave, n being the programmed value (the least significant bit being always set to 0).

Transmission starts when C5 is set to 1. The data of the shift register is then available on the 0 and 1 lines of the channel and is clocked out at the chosen frequency.

The shift register is also feed forwarded so that data should not be lost. After the transmission of the 32nd bit, C5 is reset. The S4 bit is set to 1. It will be reset when C4 will be positioned to 1.

The S7 bit of the status register is set to 1 during the transmission time.

If C5 is set to 1 after transmission of the 32nd bit, the message is retransmitted after 4 transmit clock periods. The S4 status bit will also be reset when control bit C4 is set to 1.

C6 is used for starting the receive channel testing. This test cannot be done during the reception of a message. If C6 = 1 the transmission channel signals are switched to the inputs of the control register selected receive channel. C6 is reset by any access to the control register.

C7 is a mask bit of the S4 bit of the status register. If C7 = 0 and S4 = 1, the $\overline{IRQ}$ line will be activated. If C7 = 1, the $\overline{IRQ}$ line will not be activated by S4.

Note: C5 and C6 should be programmed at the same time in order to avoid transmission or test errors.

3.4 Programming In A Mode (MODE = 0)

When seen from the microprocessor, the circuit looks like 4 addresses (“read” or “write”).

Addressing any register of a channel is done in two steps:

- channel addressing by the control register
- byte of the selected channel addressing

Thus, programming of the synchro registers or the labels and reading of the 24-bit buffers or the status register are possible.

Loading of the transmit channel shift register is done through successive writing of the 4 bytes, the first being the label then RT_1, RT_2, RT_3. The addresses of the 4 bytes are generated by an internal modulo-4 counter which is reset by any addressing of the control register (see Table 3-1 - Addressing with $\overline{CS}$ = 0 and Table 3-2 - Addressing of the channels by the control register).

Table 3-1. Addressing with $\overline{CS}$ = 0

R$\overline{W}$/INH	A1	A0	Direct Addressing	Channel Addressing With the Control Register
Read 1	0	0	–	RT1
	0	1	–	RT2
	1	0	–	RT3
	1	1	Status	–
Write 0	0	0	–	Synchro and divider by n
	0	1	Control	–
	1	0	Not used	–
	1	1	–	Label

Table 3-2. Channel Addressing by the Control Register

C0	C1	C2	C3	Channel Number
1	x	x	x	channel 0
0	1	x	x	channel 1
0	0	1	x	channel 2
0	0	0	1	channel 3

The gap detection counters are incremented on each Ø divided by 8 clock period, if n is the synchro register value, the minimum detected gap length is (8n - 4) ± 4 Ø clock periods.

C4 to C7 bits are independently interpreted.

C4: Pile loading if A0 - A1 = 11 and divider by n if A0 - A1 = 00.

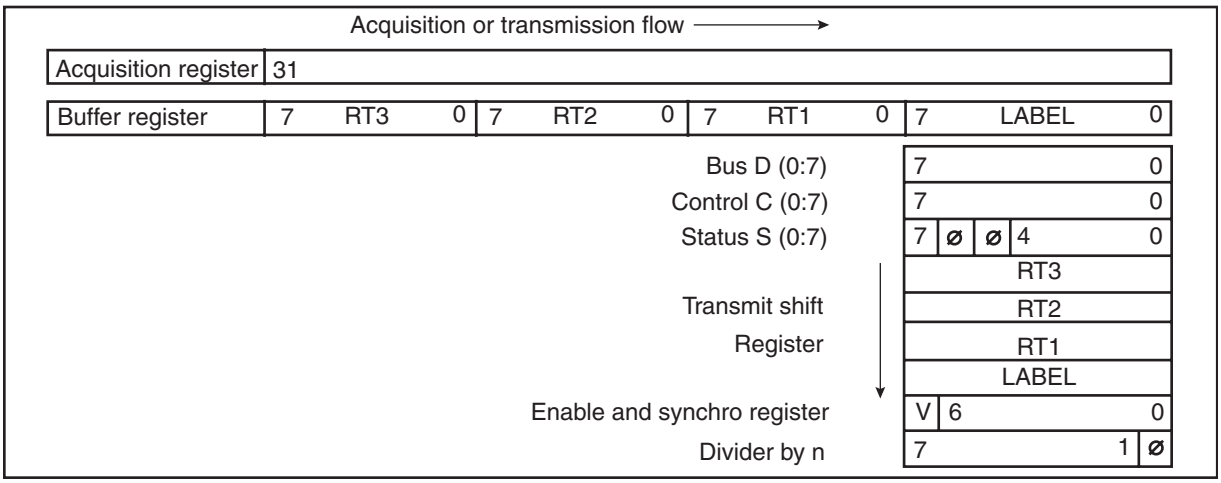
The loading of the 4 bytes to be transmitted should be done immediately after positioning C4 to 1, this operation resetting the pile index at the level of the label byte.

C5:Transmission start

C6: Test mode

C7: Transmit channel interrupt mask

Figure 3-2. Bit Correspondence



3.5 Programming in B Mode (MODE = 1)

When in B mode, programming is done by hardware. The number of high speed channels is programmed on $\overline{IRQ}$/V pin (see Table 3-3).

The synchro register is set to 5 for high speed channels and to 32 for low speed channels. This corresponds to a nominal Ø clock frequency of 2 MHz and transmission frequencies of 12 to 14.5 kHz for low speed and of 99 to 101 kHz for high speed.

Table 3-3. Programming of the $\overline{IRQ}$/Vpin

$\overline{IRQ}$/V	High Speed Channel Numbers
0: Low impedance	-
0: High impedance	0
1: Low impedance	0, 1
1: High impedance	0, 1, 2

3.6 Parity Check

If the MODE pin senses a high impedance (typ. > 10 kΩ) the circuit checks the parity of the messages for each receive channel. If the number of received 1's in a message is even, the transfer is not done and the message is discarded (odd parity).

When transmitting, the parity bit value is computed and loaded by the microprocessor or is the value of the received test message.

If the MODE pin is directly strapped to V_{CC} or $V_{SS,}$ parity check is not done.

3.6.1 Initialization

On power-on or when the $\overline{RESET}$ pin is set to 0, the following registers are reset to 0:

- control register
- status register
- the 4 label registers of the receive channels
- the 4 synchro registers.

The first gap after initialization is also ignored for each channel because acquired data could not be error-free.

4. Electrical Characteristics

Maximum Ratings

Symbol	Rating		Value	Unit
V_{CC}	Supply Voltage		-0.3 to +7	V_{dc}
V_{IN}	Input Voltage		-0.3 to +7	V_{dc}
T_C	Operating Temperature Range		TL to TH -55 to +125	°C
T_{stg}	Storage Temperature Range		-55 to +150	°C
Pd	Power Dissipation	Tc = 125°C Tc = 25°C Tc = -55°C	300 350 550	mW mW mW

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields: however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

Table 4-1. Thermal Characteristics (at 25°C)

Package	Symbol	Parameter	Value	Unit
DIL 28	θ_{J-A}	Thermal Resistance Junction-to-ambient	35,1	°C/W
	θ_{J-C}	Thermal Resistance Junction-to-case	4	°C/W
DIP28	θ_{J-A}	Thermal Resistance Junction-to-ambient	37,2	°C/W
	θ_{J-C}	Thermal Resistance Junction-to-case	18,6	°C/W

4.1 Power Considerations

The average chip-junction temperature, TJ, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad \textbf{(1)}$$

T_A = Ambient Temperature,°C
θ_{JA} = Package Thermal Resistance,
Junction-to-Ambient,°C/W
$P_D = P_{INT} + P_{I/O}$
$P_{INT} = I_{CC} \times V_{CC}$,Watts – Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins – User Determined

For most applications $P_{I/O} < P_{INT}$ and can be neglected.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K: (T_J + 273) \quad \textbf{(2)}$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273) + \theta_{JA} \cdot P_D^2 \quad \textbf{(3)}$$

where K is a constant pertaining to the particular part K can be determined from equation (3) by measuring P_D (at equilibrium) for a know T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The total thermal resistance of a package (θ_{JA}) can be separated into two components, θ_{JC} and θ_{CA}, representing the barrier to heat flow from the semiconductor junction to the package (case), surface (θ_{JC}) and from the case to the outside ambient (θ_{CA}). These terms are related by the equation:

$$\theta_{JA} = \theta_{JC} + \theta_{CA} \quad \textbf{(4)}$$

θ_{JC} is device related and cannot be influenced by the user. However, θ_{CA} is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θ_{CA} so that θ_{JA} approximately equals θ_{JC}. Substitution of θ_{JC} for θ_{JA} in equation (1) will result in a lower semiconductor junction temperature.

Table 4-2. Recommended Static Operating Conditions

Symbol	Parameter	Min	Max	Unit
V_{IH}	Input High Voltage	2.0	5.25	V
V_{IL}	Input Low Voltage	-0.3	0.8	V
V_{CC}	Supply Voltage	4.75	5.25	V

Table 4-3. Static Characteristics (V_{CC} = 5.0V ± 5%; V_{SS} = 0V; -55°C < TC < + 125°C)

Symbol	Characteristics	Min	Typ	Max	Unit
V_{IH}	Input high voltage (except MODE, $\overline{IRQ}$/V)	2.2		V_{CC}	V
V_{IL}	Input low voltage (except MODE, $\overline{IRQ}$/V)	-0.3		0.8	V
I_{in}	Input state leakage current (except MODE, $\overline{IRQ}$/V) (V_{IN} = 0.4 to 5.25V)	-10			µA
I_{TSI}	Three state leakage current N0-N1, D0-D7 (V_{IN} = 0.4 to 2.4V)	-10		10	µA
V_{OH}	Output high voltage (I_{Load} = -250 µA) N0-N1, D0-D7 (I_{Load} = +10 µA) $\overline{IRQ}$/V	 2.4 2.4		 V_{CC} V_{CC}	V
V_{OL}	Output high voltage (I_{Load} = 1.6 mA) N0-N1, D0-D7 (I_{Load} = 3.2 mA) $\overline{IRQ}$/V			0.4	V
C_{in}	Capacitance (V_{in}= 0, TC = 25°C, f = 1 MHz) (except MODE, $\overline{IRQ}$/V)			10	pF
R_H	External high programming impedance MODE, $\overline{IRQ}$/V, (C_{load} ≤ 20pF) Scan frequency = f clock: 8)	10 K			Ω

Table 4-3. Static Characteristics (V_{CC} = 5.0V ± 5%; V_{SS} = 0V; -55°C < TC < + 125°C) (Continued)

Symbol	Characteristics	Min	Typ	Max	Unit
R_L	External low programming impedance Mode, $\overline{IRQ}$/V ($C_{load} \leq 20$ pF) Scan frequency = f clock: 8)			10	Ω
P_D	Power dissipation		310	550	mW
f	Maximum operating frequency in A mode	500		2000	kHz
F	Maximum operating frequency in B mode	1000		2000	kHz

4.2 Dynamic Characteristics

Table 4-4. Bus Timing Characteristics (Load Conditions, see Figure 4-6)
(V_{CC} = 5.0V ± 5%; V_{SS} = 0V; -55°C < TC < +125°C)

Symbol	Characteristic		Min	Max	Unit
Read – A Mode (Figure 4-1)					
t_{AH}	Address Input Hold Time	A0-A1, R$\overline{W}$/INH, $\overline{CS}$	10		ns
T_{ACC}	Data Access Time(1)	D0-D7		300	ns
t_{DH}	Data Output Hold Time	D0-D7	10		ns
Write – A Mode (Figure 4-2)					
t_{AS} A0-A1ns	Address Input Setup Time	A0-A1, R$\overline{W}$/INH, $\overline{CS}$	50		ns
t_{AH}	Address Input Hold Time	A0-A1, R$\overline{W}$/INH, $\overline{CS}$	10		ns
t_{DS}	Data Set Up Time	D0-D7	100		ns
t_{DH}	Data Input Hold Time	D0-D7	50		ns
Read – B Mode (Figure 4-3)					
t_{AS}	Address Setup Time	A0-A1, R$\overline{W}$/INH, $\overline{CS}$	50		ns
t_{AH}	Address Input Hold Time	A0-A1, R$\overline{W}$/INH, $\overline{CS}$	10		ns
t_{DH}	Data Output Hold Time	0-N1, D0-D7	10		ns
t_{ACC}	Data Access Time	N0-N1, D0-D7		300	ns
t_{SI}	R$\overline{W}$/INH Setup Time		50		ns

Note: 1. See condition of validity for the access time of EF4442 status register at high temperature (Tc ≥ +85°C) in "Annexe 1: EF4442 ARINC Controller/Bug Description:" on page 19.

Table 4-5. Clock Timing Characteristics (see Figure 4-5)

Symbol	Characteristic	Min	Max	Unit
t_{CA}	A Mode Cycle Time	500	2000	ns
t_{CB}	B Mode Cycle Time	500	1000	ns
t_{WH}	Pulse Width – Low 2000	180	2000	ns
t_{WL}	Pulse Width – High	180	2000	ns
t_r, t_f	Rise Time, Fall Time		15	ns

Table 4-6. $\overline{IRQ}$/V Output Timing Characteristics (see Figure 4-4)

Symbol	Characteristic	Max	Unit
t_{PHL}	Delay Time – Low To High State	1600	ns
t_{PHL}	Delay Time – High To Low State	1000	ns

4.2.1 Timing Diagrams

Figure 4-1. Read A Mode

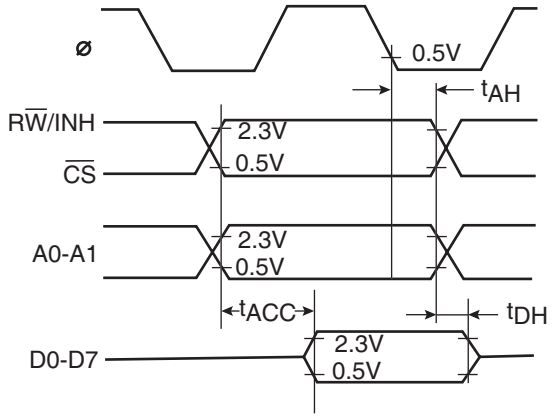


Figure 4-2. Write A Mode

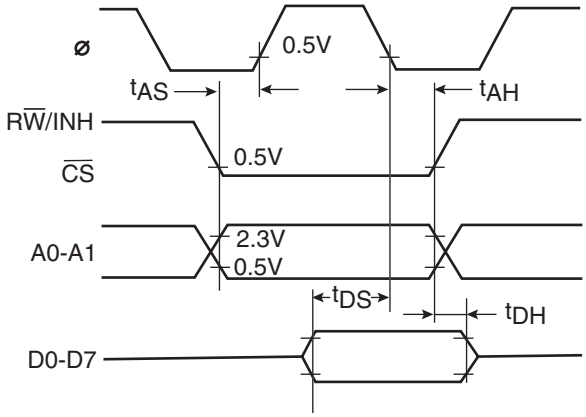


Figure 4-3. Read B Mode

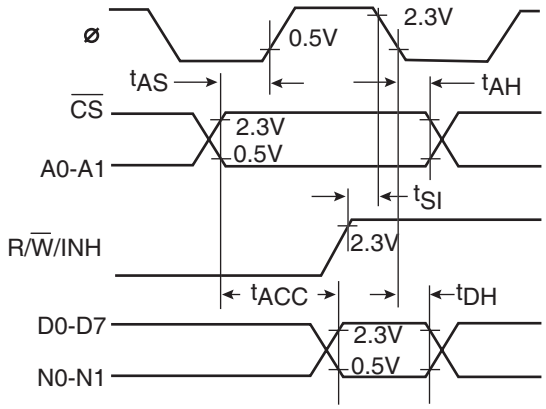


Figure 4-4. IRQ/V Output

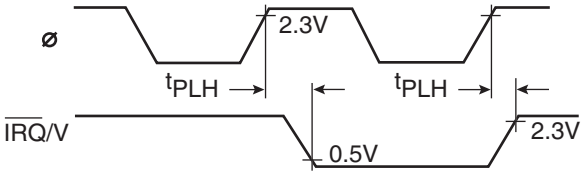


Figure 4-5. Clock

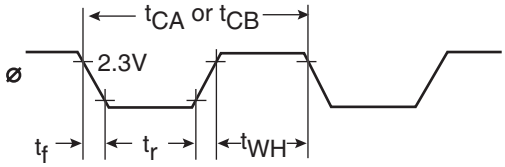
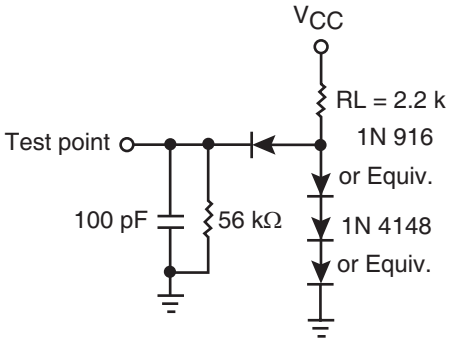


Figure 4-6. Test Load



5. Preparation For Delivery

5.1 Packaging

The microcircuits are packaged in a hermetically sealed package which is conformed to case outlines of MIL-STD-883 28 lead DIL/SB

5.2 Certificate of Compliance

e2v offers a certificate of compliance with each shipment of parts, affirming the products are in compliance either with MIL-STD-883 or e2v standard and guaranteeing the parameters are tested at extreme temperatures for the entire temperature range.

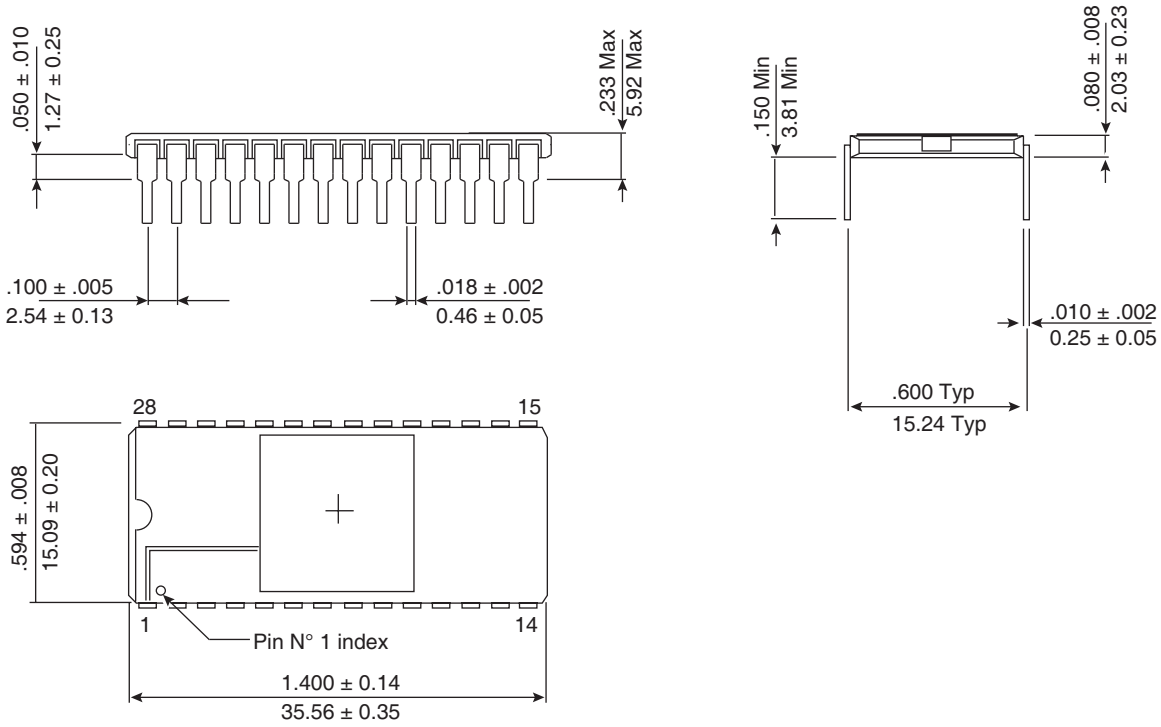
6. Handling

Devices must be handled with certain precautions to avoid damage due to accumulation of static charge. Input protection devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

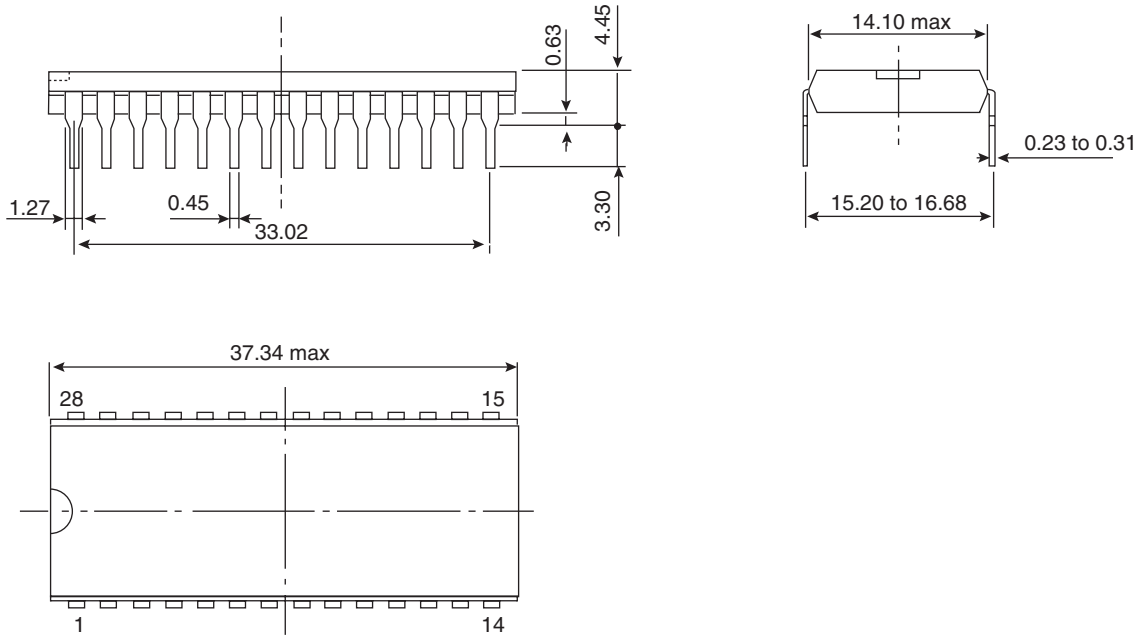
1. Device should be handled on benches with conductive and grounded surface.
2. Ground test equipment, tools and operator.
3. Do not handle devices by the leads.
4. Store devices in conductive foam or carriers.
5. Avoid use of plastic, rubber, or silk.
6. Maintain relative humidity above 50%, if practical.

7. Package Mechanical Data

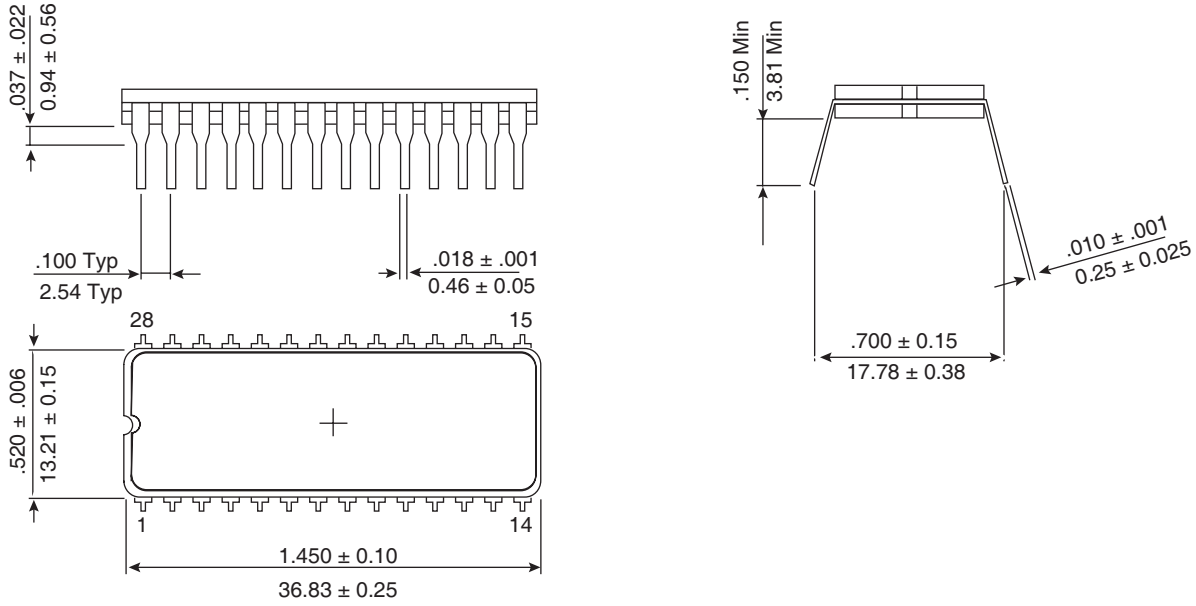
7.1 DIL 28 – Ceramic Side Brazed Package



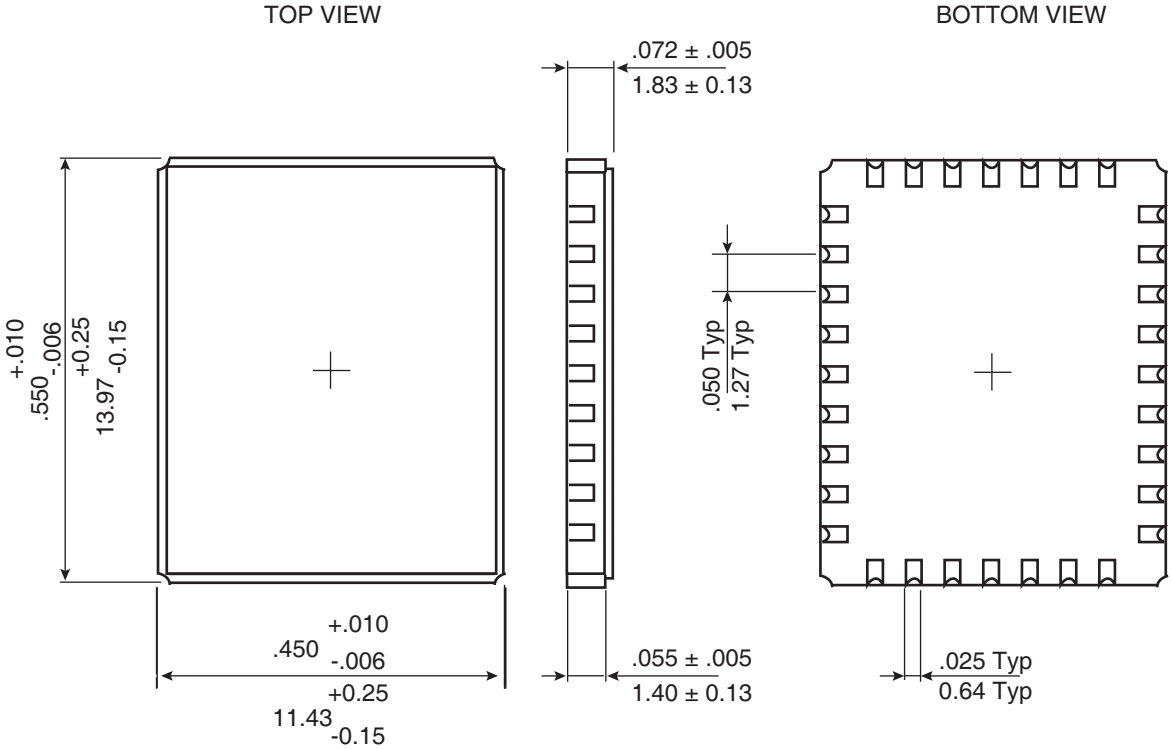
7.2 DIP 28 – Plastic Dual In Line Package



7.3 DIL 28 – Cerdip Package (Obsolete Package, for Traceability Purpose Only)



7.4 LCCC32 – Leadless Ceramic Chip Carrier package (Obsolete Package, for Traceability Purpose Only) To Be Confirmed



0859B–HIREL–06/07

7.5 Terminal Designation

Figure 7-1. DIL 28/DIP 28

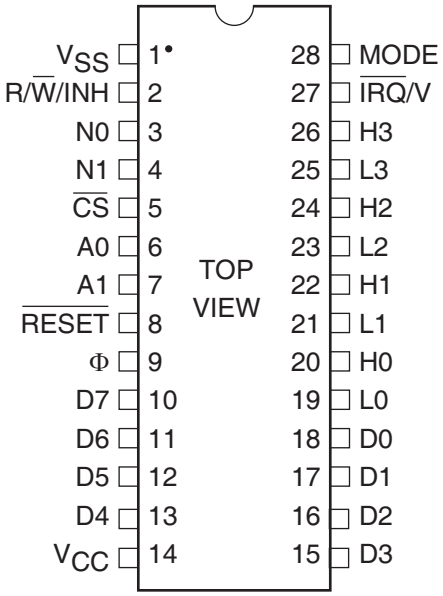
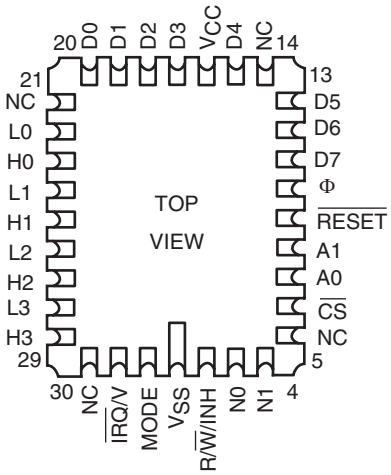


Figure 7-2. LCCC 32 (Obsolete Package)



8. Ordering Information

Table 8-1. Hi-REL Product

Commercial e2v Part-Number	Norms	Package	Temperature Range Tc (C)	Class	Drawing Number
EF4442CMG/BZ63	NFC 96883	DIL 28 Side Brazed	-55/ +125	G	Data sheet
EF4442CMB/TZ63	According to MIL-STD-883	DIL 28 Side Brazed	-55/ +125	B	Data sheet
EF4442PVZ63	e2v Standard	DIP 28	-40/ +85		Data sheet

9. Annexe 1: EF4442 ARINC Controller/Bug Description:

Condition of Validity for the Access Time in A mode (Tacc) of EF4442 Status Register at High Temperature ($T_{CASE} \geq 85°C$).

9.1 Description

In a particular condition described here after, the access time (Tacc) of EF4442 status register is above the maximum value specified in Table 4-4.

9.2 Conditions

The defect appears for high temperature 85°C and +125°C.

When the R_{TA} starts a new transmission in A mode, the S7 bit of the status register is set to 1 after 4 transmit clock periods. If this S7 bit is read before it has risen to 1 (i.e. S7 = 0), then the first access time (Tacc) for S7 = 1 will be longer than the specification:

- maximum value up to 400 ns for military range part number (M),
- maximum value up to 330 ns for industrial range part number (V).

If a second read is performed to the S7 bit, the access time (Tacc) will be compliant with the specification (max value = 300 ns).

9.3 Workaround 1

After a new transmission start in A mode (bit C5 of control register = 1), the status register does not have to be read before the S7 bit is set to 1. In that case the access time would be correct.

9.4 Workaround 2

Perform two successive read access to the Status register. The second access time would be correct.

10. Document Revision History

Table 10-1 provides a revision history for this hardware specification.

Table 10-1. Document Revision History

Revision Number	Date	Substantive Change(s)
B	05/2007	Package modification Rth (see Table 4-1 on page 10) Name change from Atmel to e2v
A	11/2002	Initial revision

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