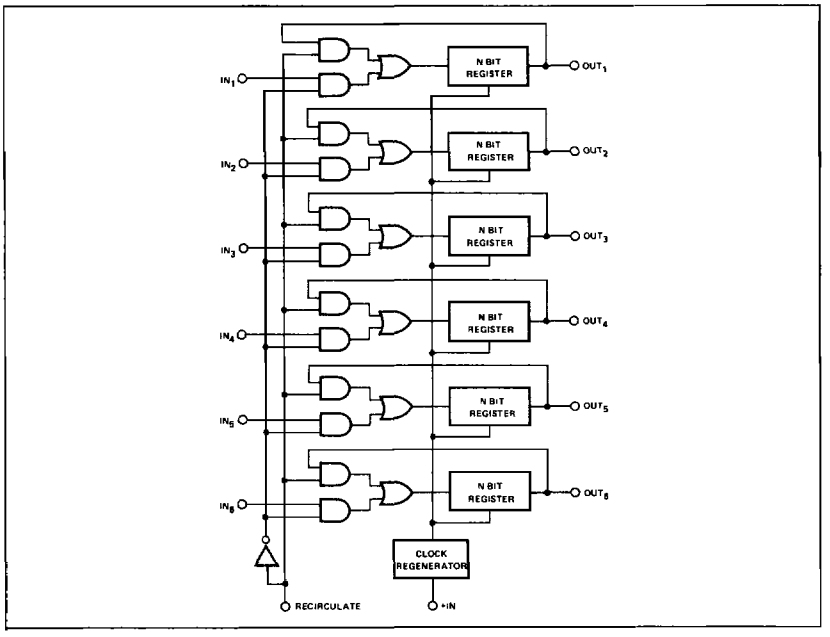
2518-B,I,F

DESCRIPTION

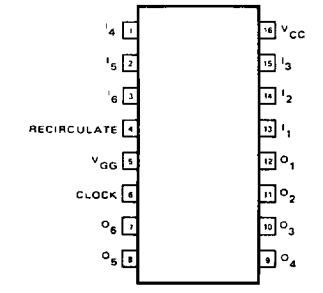
The 2518 and 32-bit recirculating static shift registers consist of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip. Internal recirculation logic plus TTL/DTL level clock signals are provided for maximum interfacing ease.

BLOCK DIAGRAM



PIN CONFIGURATION

B, I, F PACKAGE



TRUTH TABLE

RECIRCULATE	INPUT	FUNCTION
1	0	Recirculate
1	1	Recirculate
0	0	"0" is Written
0	1	"1" is Written

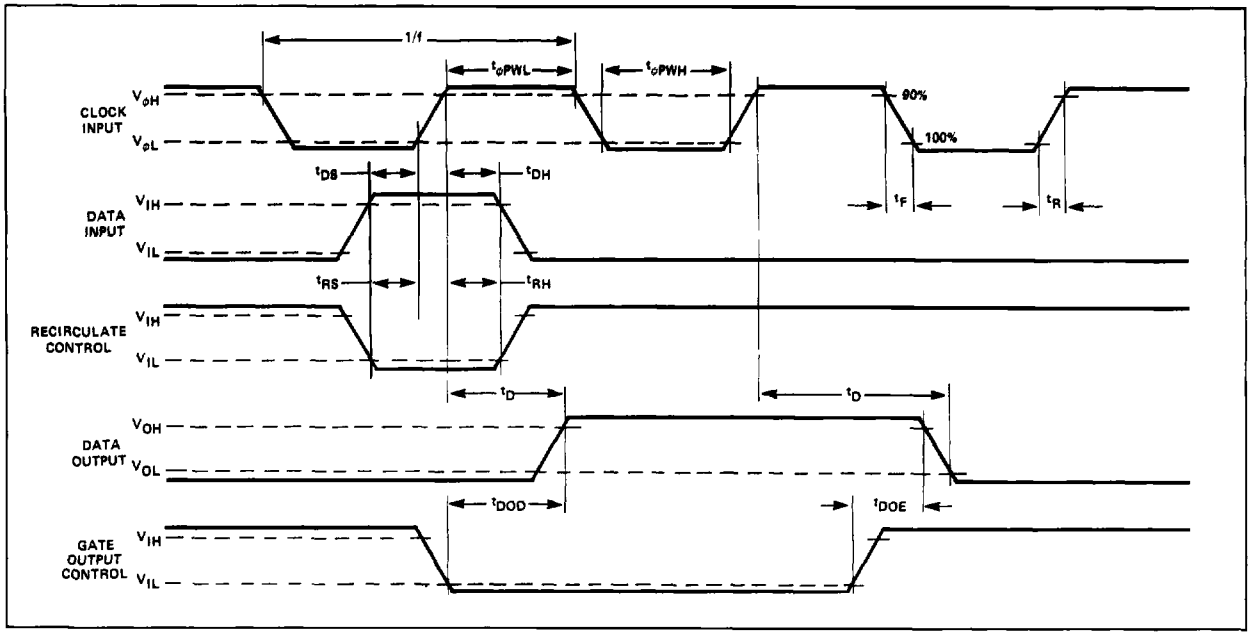
Data is Read Out when output enable is "low." Output is tri-stated when output enable is "high."

SWITCHING CHARACTERISTICS

PARAMETER	LIMITS		UNIT
	MIN	MAX	
t_{RS} Recirculate set-up time	150		ns
t_{RH} Recirculate hold time	50		ns
t_{DOE} Output enable time		100	ns
t_{DOD} Output disable time		100	ns

2518-B,I,F

TIMING DIAGRAM



2519-B,I,F

DESCRIPTION

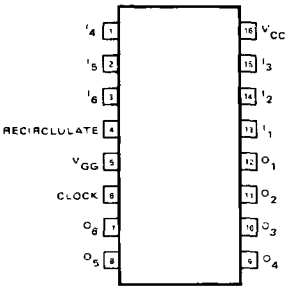
The 2519 40-bit recirculating static shift registers consist of enhancement mode P-channel silicon gate MOS devices integrated on a single monolithic chip. Internal recirculation logic plus TTL/DTL level clock signals are provided for maximum interfacing ease.

SWITCHING CHARACTERISTICS

PARAMETER	LIMITS		UNIT
	MIN	MAX	
t_{RS} Recirculate set-up time	150		ns
P_{RH} Recirculate hold time	50		ns
t_{DOE} Output enable time		100	ns
t_{DOD} Output disable time		100	ns

PIN CONFIGURATION

B, I, F PACKAGE



TRUTH TABLE

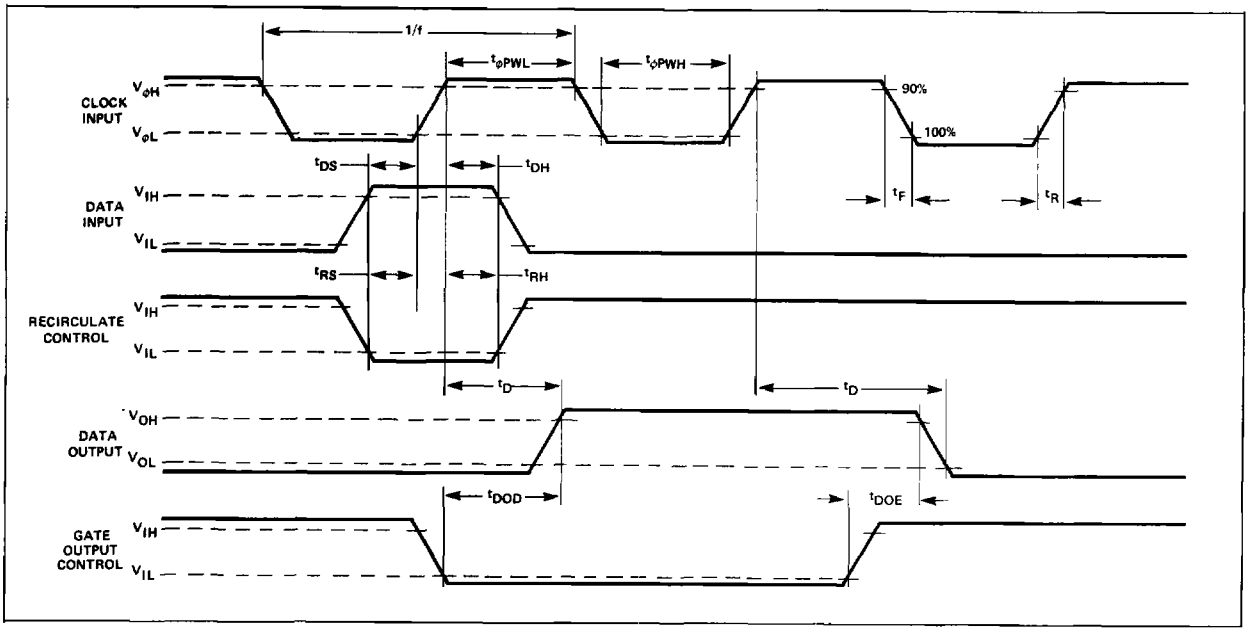
RECIRCULATE	INPUT	FUNCTION
1	0	Recirculate
1	1	Recirculate
0	0	"0" is Written
0	1	"1" is Written

Data is Read out when output enable is low. Output is tri-stated when output enable is "high."

MEMORIES

2519-B,I,F

TIMING DIAGRAM



BLOCK DIAGRAM