2N5432, 2N5433, 2N5434

N-CHANNEL SILICON JUNCTION FIELD-EFFECT TRANSISTOR

- LOW ON RESISTANCE SWITCHES
- CHOPPERS

absolute maximum ratings at 25°C free-air temperature

Drain-Gate Voltage	−25 V
Reverse Gate-Source Voltage	−25 V
Continuous Forward Gate Current	100 mA
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature	300 mW

Electrical Characteristics (25°C)

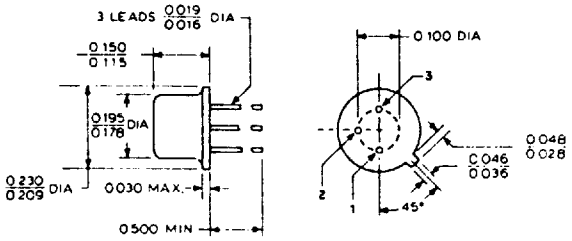
PARAMETER		2N5432		2N5433		2N5434		UNIT	TEST CONDITIONS	
		Min	Max	Min	Max	Min	Max			
I_{GSS}	Gate Reverse Current		−200		−200		−200	pA	V_{GS} = −15 V, V_{DS} = 0	
			−200		−200		−200	nA		150°C
BV_{GSS}	Gate Source Breakdown Voltage	−25		−25		−25		V	I_G = −1 uA, V_{DS} = 0	
$I_{D(off)}$	Drain Cutoff Current		200		200		200	pA	V_{DS} = 5 V, V_{GS} = −10 V	
			200		200		200	nA		150°C
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−4	−10	−3	−9	−1	−4	V	V_{DS} = 5 V, I_D = 3 nA	
I_{DSS}	Saturation Drain Current (Note 1)	150		100		30		mA	V_{DS} = 15 V, V_{GS} = 0	
$r_{DS(on)}$	Static Drain-Source ON Resistance	2	5		7		10	ohm	V_{GS} = 0, I_D = 10 mA	
$V_{DS(on)}$	Drain-Source ON Voltage		50		70		100	mV		
$r_{ds(on)}$	Drain-Source ON Resistance		5		7		10	ohm	V_{GS} = 0, I_D = 0	f = 1 kHz
C_{iss}	Common-Source Input Capacitance		30		30		30	pF	V_{DS} = 0, V_{GS} = −10 V	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		15		15		15			
$t_{d(on)}$	Turn-ON Delay Time		4		4		4	ns	V_{DD} = 1.5 V, $V_{GS(on)}$ = 0, $V_{GS(off)}$ = −12 V, $I_{D(on)}$ = 10 mA	R_L = 145 ohms (2N5432) 143 ohms (2N5433) 140 ohms (2N5434)
t_r	Rise Time		1		1		1			
$t_{d(off)}$	Turn-OFF Delay Time		6		6		6			
t_f	Fall Time		30		30		30			

NOTES:
1. Pulse test duration 300 us, duty cycle less than or equal to 3%.

PROCESS NJ450

TO-52

DIMENSIONS IN INCHES



PIN CONFIGURATION

1 - SOURCE
2 - DRAIN
3 - GATE

Surface Mount — SMP5432
SMP5433, SMP5434

InterFET
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