Chapter 1

Introduction

This user's guide discusses the TMS320C5x generation of fixed-point digital signal processors (DSPs) in the TMS320 family. The 'C5x DSP provides improved performance over earlier 'C1x and 'C2x generations while maintaining upward compatibility of source code between the devices. The 'C5x central processing unit (CPU) is based on the 'C25 CPU and incorporates additional architectural enhancements that allow the device to run twice as fast as 'C2x devices. Future expansion and enhancements are expected to heighten the performance and range of applications of the 'C5x DSPs.

The 'C5x generation of static CMOS DSPs consists of the following devices:

Device	On-Chip RAM	On-Chip ROM
TMS320C50/LC50	10K words	2K words
TMS320C51/LC51	2K words	8K words
TMS320C52/LC52	1K words	4K words
TMS320C53/LC53	4K words	16K words
TMS320C53S/LC53S	4K words	16K words
TMS320LC56	7K words	32K words
TMS320LC57	7K words	32K words
TMS320C57S/LC57S	7K words	2K words

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1.1 TMS320 Family Overview

The TMS320 family consists of two types of single-chip DSPs: 16-bit fixed-point and 32-bit floating-point. These DSPs possess the operational flexibility of high-speed controllers and the numerical capability of array processors. Combining these two qualities, the TMS320 processors are inexpensive alternatives to custom-fabricated VLSI and multichip bit-slice processors. Refer to subsection 1.1.2, *TMS320 Typical Applications*, for a detailed list of applications of the TMS320 family. The following characteristics make this family the ideal choice for a wide range of processing applications:

- ❑ Very flexible instruction set
- ❑ Inherent operational flexibility
- ❑ High-speed performance
- ❑ Innovative, parallel architectural design
- ❑ Cost-effectiveness

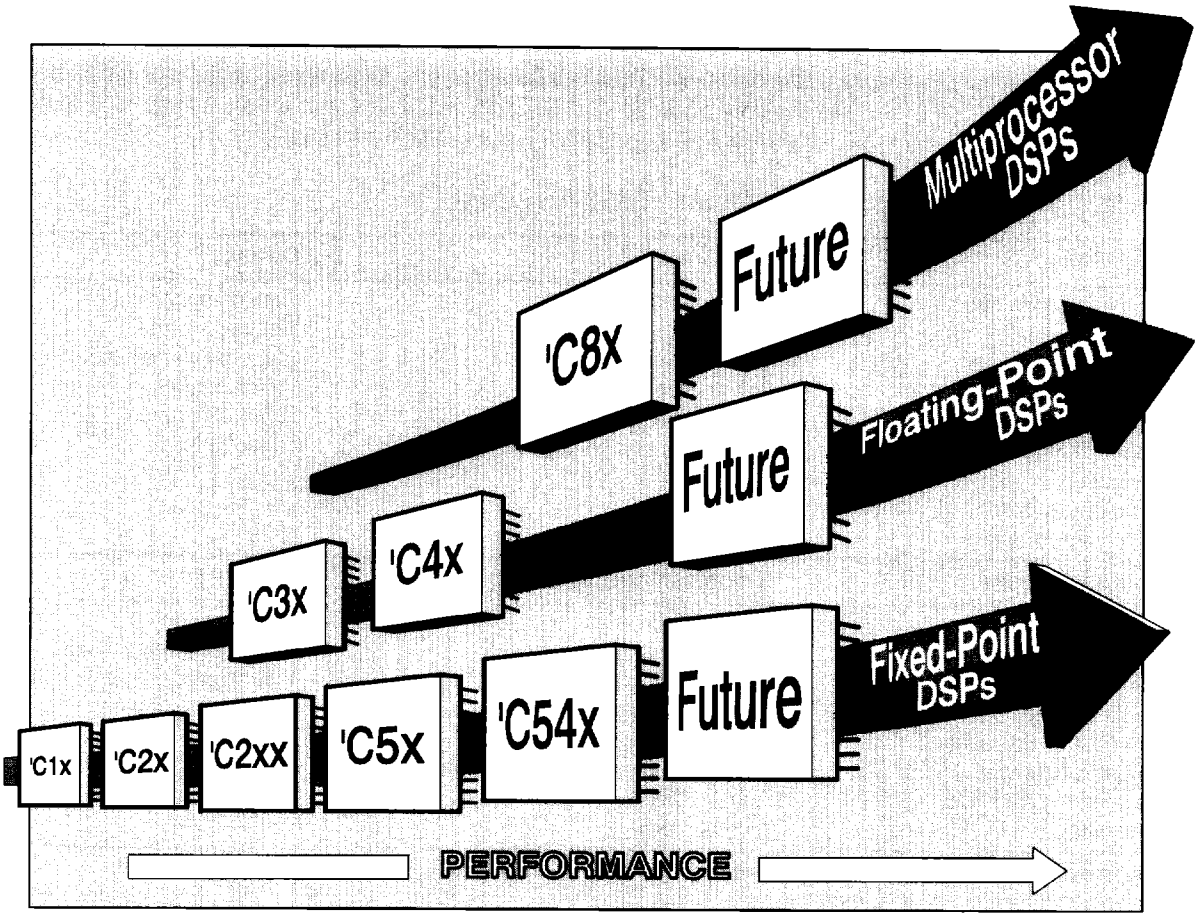
1.1.1 History, Development, and Advantages of TMS320 DSPs

In 1982, Texas Instruments introduced the TMS32010 — the first fixed-point DSP in the TMS320 family. Before the end of the year, the *Electronic Products* magazine awarded the TMS32010 the title "Product of the Year". The TMS32010 became the model for future TMS320 generations.

Today, the TMS320 family consists of eight generations: the 'C1x, 'C2x, 'C2xx, 'C5x, and 'C54x are fixed-point, the 'C3x and 'C4x are floating-point, and the 'C8x is a multiprocessor. Figure 1–1 illustrates the performance gains that the TMS320 family has made over time with successive generations. Source code is upward compatible from one fixed-point generation to the next fixed-point generation (except for the 'C54x), and from one floating-point generation to the next floating-point generation. Upward compatibility preserves the software generation of your investment, thereby providing a convenient and cost-efficient means to a higher-performance, more versatile DSP system.

Each generation of TMS320 devices has a CPU and a variety of on-chip memory and peripheral configurations for developing spin-off devices. These spin-off devices satisfy a wide range of needs in the worldwide electronics market. When memory and peripherals are integrated into one processor, the overall system cost is greatly reduced, and circuit board space is saved.

Figure 1–1. Evolution of the TMS320 Family



1.1.2 TMS320 Typical Applications

The TMS320 family of DSPs offers better, more adaptable approaches to traditional signal-processing problems, such as vocoding, filtering, and error coding. Furthermore, the TMS320 family supports complex applications that often require multiple operations to be performed simultaneously. Figure 1–2 shows many of the typical applications of the TMS320 family.

Figure 1–2. Typical Applications for the TMS320 Family

Automotive	Consumer	Control
Adaptive ride control	Digital radios/TVs	Disk drive control
Antiskid brakes	Educational toys	Engine control
Cellular telephones	Music synthesizers	Laser printer control
Digital radios	Power tools	Motor control
Engine control	Radar detectors	Robotics control
Global positioning	Solid-state answering machines	Servo control
Navigation		
Vibration analysis		
Voice commands		
General-Purpose	**Graphics/Imaging**	**Industrial**
Adaptive filtering	3-D rotation	Numeric control
Convolution	Animation/digital map	Power-line monitoring
Correlation	Homomorphic processing	Robotics
Digital filtering	Pattern recognition	Security access
Fast Fourier transforms	Image enhancement	
Hilbert transforms	Image compression/transmission	
Waveform generation	Robot vision	
Windowing	Workstations	
Instrumentation	**Medical**	**Military**
Digital filtering	Diagnostic equipment	Image processing
Function generation	Fetal monitoring	Missile guidance
Pattern matching	Hearing aids	Navigation
Phase-locked loops	Patient monitoring	Radar processing
Seismic processing	Prosthetics	Radio frequency modems
Spectrum analysis	Ultrasound equipment	Secure communications
Transient analysis		Sonar processing
Telecommunications		**Voice/Speech**
1200- to 19200-bps modems	DTMF encoding/decoding	Speech enhancement
Adaptive equalizers	Echo cancellation	Speech recognition
ADPCM transcoders	Fax	Speech synthesis
Cellular telephones	Line repeaters	Speaker verification
Channel multiplexing	Speaker phones	Speech vocoding
Data encryption	Spread spectrum communications	Voice mail
Digital PBXs	Video conferencing	Text-to-speech
Digital speech interpolation (DSI)	X.25 Packet Switching	
Personal digital assistants (PDA)	Personal communications systems (PCS)	

1.2 TMS320C5x Overview

The 'C5x generation consists of the 'C50, 'C51, 'C52, 'C53, 'C53S, 'C56, 'C57, and 'C57S DSPs, which are fabricated by CMOS integrated-circuit technology. Their architectural design is based on the 'C25. The operational flexibility and speed of the 'C5x are the result of combining an advanced Harvard architecture (which has separate buses for program memory and data memory), a CPU with application-specific hardware logic, on-chip peripherals, on-chip memory, and a highly specialized instruction set. The 'C5x is designed to execute up to 50 million instructions per second (MIPS). Spin-off devices that combine the 'C5x CPU with customized on-chip memory and peripheral configurations may be developed for special applications in the worldwide electronics market.

The 'C5x devices offer these advantages:

- Enhanced TMS320 architectural design for increased performance and versatility
- Modular architectural design for fast development of spin-off devices
- Advanced integrated-circuit processing technology for increased performance and low power consumption
- Source code compatibility with 'C1x, 'C2x, and 'C2xx DSPs for fast and easy performance upgrades
- Enhanced instruction set for faster algorithms and for optimized high-level language operation
- Reduced power consumption and increased radiation hardness because of new static design techniques

Table 1–1 lists the major characteristics of the 'C5x DSPs. The table shows the capacity of on-chip RAM and ROM, number of serial and parallel input/output (I/O) ports, power supply requirements, execution time of one machine cycle, and package types available with total pin count. Use Table 1–1 for guidance in choosing the best 'C5x DSP for your application.

Table 1–1. Characteristics of the 'C5x DSPs

TMS320 Device	ID	On-Chip Memory (16-bit words) DARAM†	SARAM‡	ROM	I/O Ports Serial	Parallel ◊	Power Supply (V)	Cycle Time (ns)	Package Type
'C50	PQ	1056	9K	2K§	2¶	64K	5	50/35/25	132 pin BQFP○
'LC50	PQ	1056	9K	2K§	2¶	64K	3.3	50/40/25	132 pin BQFP○
'C51	PQ	1056	1K	8K§	2¶	64K	5	50/35/25/20	132 pin BQFP○
'C51	PZ	1056	1K	8K§	2¶	64K	5	50/35/25/20	100 pin TQFP*
'LC51	PQ	1056	1K	8K§	2¶	64K	3.3	50/40/25	132 pin BQFP○
'LC51	PZ	1056	1K	8K§	2¶	64K	3.3	50/40/25	100 pin TQFP*
'C52	PJ	1056	—	4K§	1	64K	5	50/35/25/20	100 pin QFP□
'C52	PZ	1056	—	4K§	1	64K	5	50/35/25/20	100 pin TQFP*
'LC52	PJ	1056	—	4K§	1	64K	3.3	50/40/25	100 pin QFP□
'LC52	PZ	1056	—	4K§	1	64K	3.3	50/40/25	100 pin TQFP*
'C53	PQ	1056	3K	16K§	2¶	64K	5	50/35/25	132 pin BQFP○
'C53S	PZ	1056	3K	16K§	2	64K	5	50/35/25	100 pin TQFP*
'LC53	PQ	1056	3K	16K§	2¶	64K	3.3	50/40/25	132 pin BQFP○
'LC53S	PZ	1056	3K	16K§	2	64K	3.3	50/40/25	100 pin TQFP*
'LC56	PZ	1056	6K	32K	2#	64K	3.3	50/35/25	100 pin TQFP*
'C57S	PGE	1056	6K	2K§	2#	64K‖	5	50/35/25	144 pin TQFPΔ
'LC57	PBK	1056	6K	32K	2#	64K‖	3.3	50/35/25	128 pinTQFP*
'LC57S	PGE	1056	6K	2K§	2#	64K‖	3.3	50/35	144 pin TQFPΔ

† Dual-access RAM (DARAM)
‡ Single-access RAM (SARAM)
§ ROM bootloader available
¶ Includes time-division multiplexed (TDM) serial port
# Includes buffered serial port (BSP)
‖ Includes host port interface (HPI)
○ 20 × 20 × 3.8 mm bumpered quad flat-pack (BQFP) package
* 14 × 14 × 1.4 mm thin quad flat-pack (TQFP) package
□ 14 × 20 × 2.7 mm quad flat-pack (QFP) package
Δ 20 × 20 × 1.4 mm thin quad flat-pack (TQFP) package
◊ Sixteen of the 64K parallel I/O ports are memory mapped.

1.3 TMS320C5x Key Features

Key features of the 'C5x DSPs are listed below. Where a feature is exclusive to a particular device, the device's name is enclosed within parentheses and noted after that feature.

- Compatibility: Source-code compatible with 'C1x, 'C2x, and 'C2xx devices
- Speed: 20-/25-/35-/50-ns single-cycle fixed-point instruction execution time (50/40/28.6/20 MIPS)
- Power
  - 3.3-V and 5-V static CMOS technology with two power-down modes
  - Power consumption control with IDLE1 and IDLE2 instructions for power-down modes
- Memory
  - 224K-word × 16-bit maximum addressable external memory space (64K-word program, 64K-word data, 64K-word I/O, and 32K-word global memory)
  - 1056-word × 16-bit dual-access on-chip data RAM
  - 9K-word × 16-bit single-access on-chip program/data RAM ('C50)
  - 2K-word × 16-bit single-access on-chip boot ROM ('C50, 'C57S)
  - 1K-word × 16-bit single-access on-chip program/data RAM ('C51)
  - 8K-word × 16-bit single-access on-chip program ROM ('C51)
  - 4K-word × 16-bit single-access on-chip program ROM ('C52)
  - 3K-word × 16-bit single-access on-chip program/data RAM ('C53, 'C53S)
  - 16K-word × 16-bit single-access on-chip program ROM ('C53, 'C53S)
  - 6K-word × 16-bit single-access on-chip program/data RAM ('LC56, 'C57S, 'LC57)
  - 32K-word × 16-bit single-access on-chip program ROM ('LC56, 'LC57)

- Central processing unit (CPU)
  - Central arithmetic logic unit (CALU) consisting of the following:
    - 32-bit arithmetic logic unit (ALU), 32-bit accumulator (ACC), and 32-bit accumulator buffer (ACCB)
    - 16-bit × 16-bit parallel multiplier with a 32-bit product capability
    - 0- to 16-bit left and right data barrel-shifters and a 64-bit incremental data shifter
  - 16-bit parallel logic unit (PLU)
  - Dedicated auxiliary register arithmetic unit (ARAU) for indirect addressing
  - Eight auxiliary registers
- Program control
  - 8-level hardware stack
  - 4-deep pipelined operation for delayed branch, call, and return instructions
  - Eleven shadow registers for storing strategic CPU-controlled registers during an interrupt service routine (ISR)
  - Extended hold operation for concurrent external direct memory access (DMA) of external memory or on-chip RAM
  - Two indirectly addressed circular buffers for circular addressing
- Instruction set
  - Single-cycle multiply/accumulate instructions
  - Single-instruction repeat and block repeat operations
  - Block memory move instructions for better program and data management
  - Memory-mapped register load and store instructions
  - Conditional branch and call instructions
  - Delayed execution of branch and call instructions
  - Fast return from interrupt instructions
  - Index-addressing mode
  - Bit-reversed index-addressing mode for radix-2 fast-Fourier transforms (FFTs)

- On-chip peripherals
  - 64K parallel I/O ports (16 I/O ports are memory-mapped)
  - Sixteen software-programmable wait-state generators for program, data, and I/O memory spaces
  - Interval timer with period, control, and counter registers for software stop, start, and reset
  - Phase-locked loop (PLL) clock generator with internal oscillator or external clock source
  - Multiple PLL clocking option (x1, x2, x3, x4, x5, x9, depending on the device)
  - Full-duplex synchronous serial port interface for direct communication between the 'C5x and another serial device
  - Time-division multiplexed (TDM) serial port ('C50, 'C51, 'C53)
  - Buffered serial port (BSP) ('LC56, 'C57S, 'LC57)
  - 8-bit parallel host port interface (HPI) ('C57, 'C57S)
- Test/Emulation
  - On-chip scan-based emulation logic
  - IEEE JTAG Standard 1149.1 boundary scan logic ('C50, 'C51, 'C53, 'C57S)
- Packages
  - 100-pin quad flat-pack (QFP) package ('C52)
  - 100-pin thin quad flat-pack (TQFP) package ('C51, 'C52, 'C53S, 'LC56)
  - 128-pin TQFP package ('LC57)
  - 132-pin bumpered quad flat-pack (BQFP) package ('C50, 'C51, 'C53)
  - 144-pin TQFP package ('C57S)