SiT9501

ADVANCED

Ultra-low Jitter Differential XO for Standard Networking Frequencies

Description

The SiT9501 is a differential MEMS oscillator that is engineered for low-jitter applications requiring standard networking frequencies from 25 MHz to 644.53125 MHz.

A unique FlexSwing output-driver performs like LVPECL but provides independent control of voltage swing and DC offset to simplify interfacing with chipsets having non-standard input voltage requirements and eliminate all external source-bias resistors. The device also integrates multiple on-chip regulators to filter power supply noise, eliminating the need for an external dedicated LDO.

The SiT9501 can be factory programmed for specific combinations of frequency, stability, voltage, output signaling, and pin 1 functionality. Programmability enables designers to optimize clock configurations while eliminating long lead times and customization costs associated with quartz devices where each combination is custom built.

The wide frequency range and programmability makes this device ideal for communications, enterprise, and industrial applications that require a variety of frequencies and operate in noisy environments.

Refer to Manufacturing Notes for proper reflow profile, tape and reel dimension, and other manufacturing related information.

Features

- 14 Standard networking frequencies from 25 MHz to 644.53125 MHz
- 70 fs RMS typical phase jitter, 12 kHz to 20 MHz
- Excellent power-supply noise rejection
- LVPECL, LVDS, HCSL, Low-power HCSL, and FlexSwing signaling options
- ±20, ±25, ±30, and ±50 ppm frequency stabilities
- Wide temperature support up to -40°C to 105°C
- Factory programmable options for low lead time
- 1.8 V, 2.5 V, 3.3 V, and wide continuous range power supply voltage
- 2 x 1.6, 2.5 x 2, 3.2 x 2.5 mm x mm package (Contact SiTime for 7 x 5, and 5 x 3.2 mm x mm packages)

Applications

- 400G/800G network equipment
- Optical modules
- Coherent optics
- Network switches, routers
- Industrial networking equipment

Block Diagram

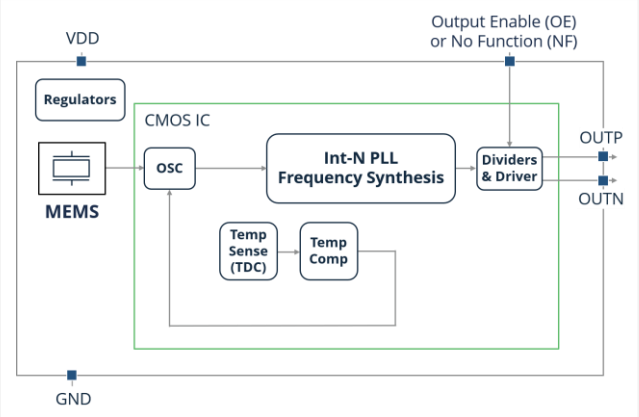


Figure 1. SiT9501 Block Diagram

Package Pinout

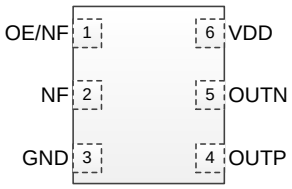


Figure 2. Pin Assignments (Top view)
(Refer to Table 17 for Pin Descriptions)

Typical Phase Jitter (70 fs RMS) and Phase Noise Data

Table 1. Phase Noise for 3.3 V 156.25 MHz LVPECL Device at 25°C

Offset Frequency (Hz)	Phase Noise (dBc/Hz)
100	-87
1k	-114
10k	-141
100k	-151
1M	-152
10M	-165
40M	-170

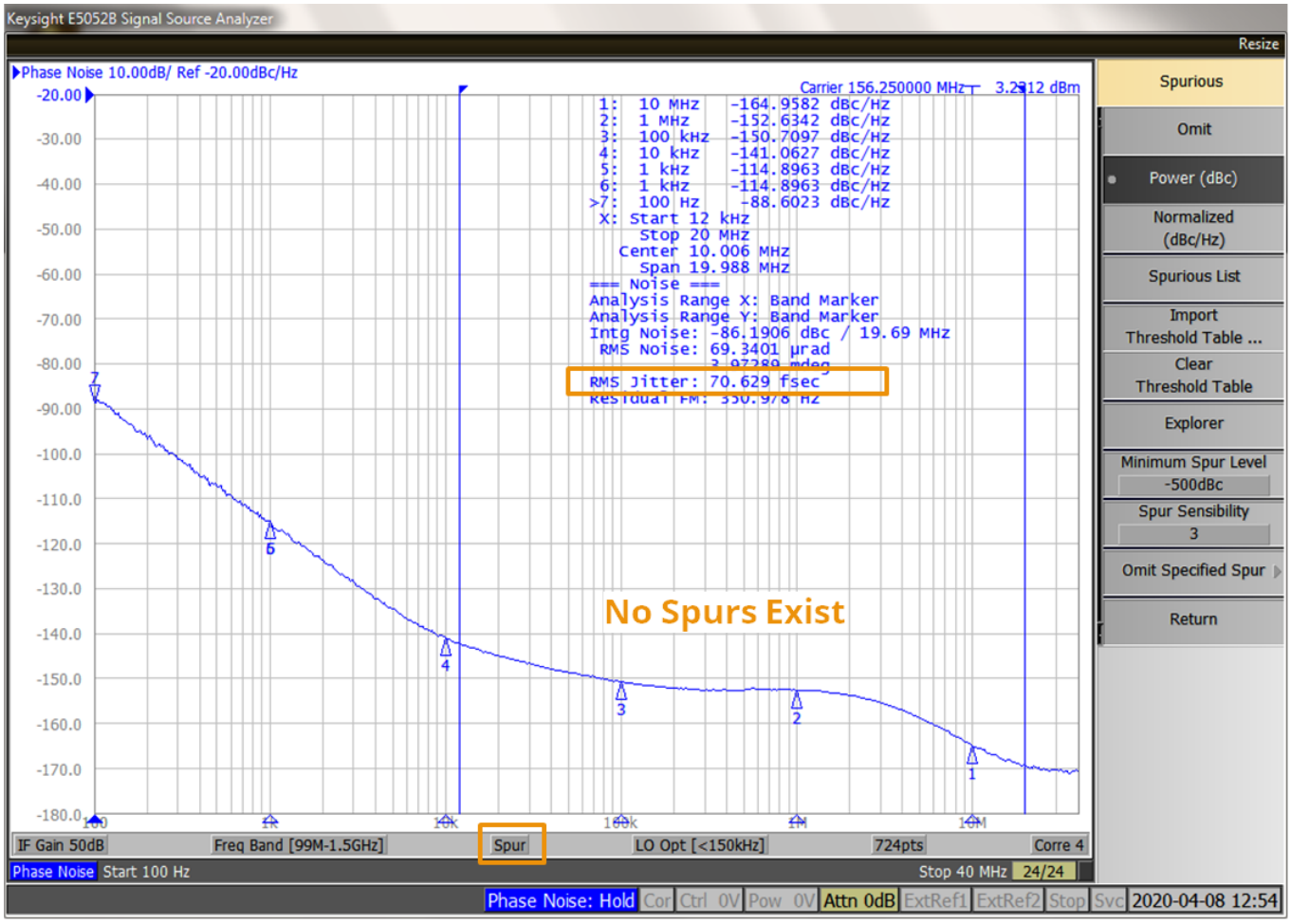


Figure 3. Phase Noise Plot of 3.3 V 156.25 MHz LVPECL Device at 25°C

Ordering Information

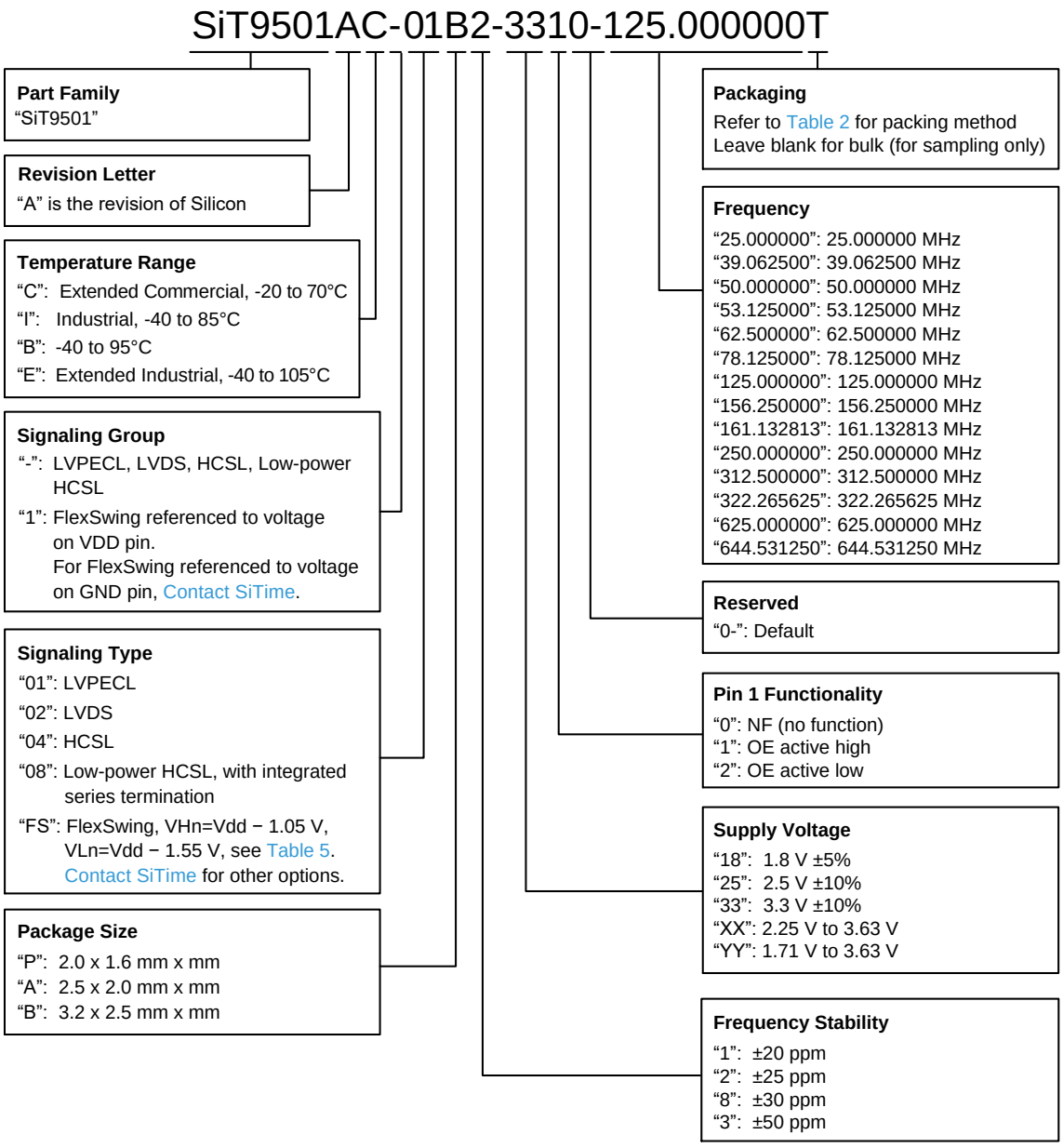


Table 2. Ordering Codes for Supported Tape & Reel Packing Method

Device Size (mm x mm)	8 mm T&R (3ku)	8 mm T&R (1ku)
2.0 x 1.6	D	E
2.5 x 2.0	D	E
3.2 x 2.5	D	E

TABLE OF CONTENTS

Description 1
Features 1
Applications 1
Block Diagram 1
Package Pinout 1
Typical Phase Jitter (70 fs RMS) and Phase Noise Data 2
Ordering Information 3
Electrical Characteristics 5
Pin Description 12
FlexSwing Configurations 13
Waveform Diagrams 15
Termination Diagrams 18
LVPECL and FlexSwing Termination 18
LVDS, Supply Voltage: 1.8 V ±5%, 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V 19
HCSL, Supply Voltage: 1.8 V ±5%, 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V 19
Low-power HCSL, Supply Voltage: 1.8 V ±5%, 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V 19
Dimensions and Patterns — 2.0 x 1.6 mm x mm 20
Dimensions and Patterns — 2.5 x 2.0 mm x mm 21
Dimensions and Patterns — 3.2 x 2.5 mm x mm 22
Additional Information 23
Revision History 23

Electrical Characteristics

All Min and Max limits in the Electrical Characteristics tables are specified over operating temperature and rated operating voltage with standard output termination shown in the termination diagrams. Typical values are at 25°C and nominal supply voltage.

Table 3. Electrical Characteristics – Common to All Output Signaling Types

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Frequency Range						
Output Frequency Range	f	Standard frequencies			MHz	Refer to frequencies listed in Ordering Information section.
Frequency Stability						
Frequency Stability	F_stab	–	–	±20	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage, load variation of 15 pF ± 10%, and 10 years aging at 25°C
		–	–	±25	ppm	Inclusive of initial tolerance, operating temperature, rated power supply voltage, load variation of 15 pF ± 10%, and first year aging at 25°C
		–	–	±30	ppm	
		–	–	±50	ppm	
10 Year Aging	F_10y	–	±1	–	ppm	Ambient temperature of 25°C
Temperature Range						
Operating Temperature Range	T_use	-20	–	+70	°C	Extended commercial, ambient temperature
		-40	–	+85	°C	Industrial, ambient temperature
		-40	–	+95	°C	Ambient temperature
		-40	–	+105	°C	Extended industrial, ambient temperature
Supply Voltage						
Supply Voltage	Vdd	1.71	–	3.63	V	Voltage-supply order code “YY”
		2.25	–	3.63	V	Voltage-supply order code “XX”
		1.71	1.80	1.89	V	Voltage-supply order code “18”. Contact SiTime for 1.5 V
		2.25	2.50	2.75	V	Voltage-supply order code “25”
		2.97	3.30	3.63	V	Voltage-supply order code “33”
Input Characteristics						
Input Voltage High	VIH	70%	–	–	Vdd	Pins 1 and 2 for OE and SE, respectively
Input Voltage Low	VIL	–	–	30%	Vdd	Pins 1 and 2 for OE and SE, respectively
Input Pull-up Impedance	Z_in	–	100	–	kΩ	Pins 1 and 2 for OE and SE, respectively
Output Characteristics						
Duty Cycle	DC	45	–	55	%	See Figure 6 and Figure 8
Startup, OE and SE Timing						
Startup Time	T_start	–	1	5	ms	Measured from the time Vdd reaches its rated minimum value
Output Enable Time	T_oe	–	–	100+3 clock cycles	ns	Measured from the time OE pin toggles to enable logic level to the time clock pins reach 90% of swing. See Figure 13
Output Disable Time	T_od	–	–	100+3 clock cycles	ns	Measured from the time OE pin toggles to disable logic level to the last clock edge. See Figure 14
Jitter and Phase Noise, f = 156.25 MHz						
RMS Phase Jitter (random)	T_phj	–	70	100	fs	12 kHz to 20 MHz offset frequency integration bandwidth
Spurious Phase Noise	T_spn	–	-110	–	dBc	12 kHz to 20 MHz offset frequency range
RMS Period Jitter[1]	T_jitt_per	–	1	–	ps	
Peak Cycle-to-cycle Jitter[1]	T_jitt_cc	–	6	–	ps	

Note:

1. Measured according to JESD65B.

Table 4. Electrical Characteristics – LVPECL | Supply voltages: 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	34	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination 1	Idd_oe_wt1	–	43	–	mA	Including load termination current. See Figure 16 for termination
Current Consumption, Output Enabled with Termination 2	Idd_oe_wt2	–	62	–	mA	Including load termination current. See Figure 19 for termination
Current Consumption, Output Disabled without Termination	Idd_od_nt	–	49	–	mA	Excluding load termination current
Current Consumption Output Disabled with Termination 1	Idd_od_wt1	–	49	–	mA	Including load termination current. See Figure 16 for termination
Current Consumption, Output Disabled with Termination 2	Idd_od_wt2	–	77	–	mA	Including load termination current. See Figure 19 for termination
OE Leakage Current	I_leak	–	28	–	mA	OE = disable logic, DC termination, OUTP and OUTN held at constant voltage, see Figure 14. Use AC termination to reduce I_leak to 0 mA.
Output Characteristics						
Output High Voltage	VOH	Vdd-1.025	Vdd-0.95	Vdd-0.88	V	See Figure 5
Output Low Voltage	VOL	Vdd-1.81	Vdd-1.7	Vdd-1.62	V	See Figure 5
Output Differential Voltage Swing	V_Swing	1.2	1.5	1.9	V	See Figure 6
Rise/Fall Time	Tr, Tf	–	170	–	ps	20% to 80%. See Figure 6
Differential Asymmetry, peak-peak	V_da	–	100	–	mV	See Figure 9
Differential Skew, peak	V_ds	–	±40	–	ps	See Figure 10
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of V_Swing; see Figure 11
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 5. Electrical Characteristics – FlexSwing | Supply voltage: 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	34	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	43	–	mA	Including load termination current. See Figure 16 for termination
Current Consumption, Output Disabled without Termination	Idd_od_nt	–	49	–	mA	Excluding load termination current
Current Consumption Output Disabled with Termination	Idd_od_wt	–	49	–	mA	Including load termination current. See Figure 16 for termination
OE Leakage Current	I_leak	–	28	–	mA	OE = disable logic, DC termination, OUTP and OUTN held at constant voltage, see Figure 14. Use AC termination to reduce I_leak to 0 mA.
Output Characteristics						
Output High Voltage	VOH	VHn - 0.1	VHn	VHn + 0.1	V	See Figure 5, Refer to Table 18 or Table 19 order codes for nominal VOH (i.e. VHn) values.
Output Low Voltage	VOL	VLn - 0.1	VLn	VLn + 0.1	V	See Figure 5, Refer to Table 18 or Table 19 order codes for nominal VOL (i.e. VLn) values
Output Differential Voltage Swing	V_Swing	VOH - VOL			V	See Figure 6
Rise/Fall Time	Tr, Tf	–	170	–	ps	20% to 80%. See Figure 6
Differential Asymmetry, peak-peak	V_da	–	100	–	mV	See Figure 9
Differential Skew, peak	V_ds	–	±40	–	ps	See Figure 10
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of V_Swing; see Figure 11
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 6. Electrical Characteristics – FlexSwing | Supply voltage referred to GND, only: 1.8 V ±5%, 1.71 V to 3.63 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	34	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	43	–	mA	Including load termination current. See Figure 16 for termination
Current Consumption, Output Disabled without Termination	Idd_od_nt	–	49	–	mA	Excluding load termination current
Current Consumption Output Disabled with Termination	Idd_od_wt	–	49	–	mA	Including load termination current. See Figure 16 for termination
OE Leakage Current	I_leak	–	28	–	mA	OE = disable logic, DC termination, OUTP and OUTN held at constant voltage, see Figure 14. Use AC termination to reduce I_leak to 0 mA.
Output Characteristics						
Output High Voltage	VOH	VHn - 0.1	VHn	VHn + 0.1	V	See Figure 5, Refer to Table 18 or Table 19 order codes for nominal VOH (i.e. VHn) values
Output Low Voltage	VOL	VLn - 0.1	VLn	VLn + 0.1	V	See Figure 5, Refer to Table 18 or Table 19 order codes for nominal VOL (i.e. VLn) values
Output Differential Voltage Swing	V_Swing	VOH - VOL			V	See Figure 6
Rise/Fall Time	Tr, Tf	–	170	–	ps	20% to 80%. See Figure 6
Differential Asymmetry, peak-peak	V_da	–	100	–	mV	See Figure 9
Differential Skew, peak	V_ds	–	±40	–	ps	See Figure 10
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of V_Swing; see Figure 11
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 7. Electrical Characteristics – LVDS | Supply voltage: 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	36	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	40	–	mA	Including load termination current. See Figure 22 (a) and Figure 22 (b) for termination.
Current Consumption, Output Disabled without Termination	Idd_od_nt	–	45	–	mA	Excluding load termination current
Current Consumption Output Disabled with Termination	Idd_od_wt	–	48	–	mA	Including load termination current. See Figure 22 (a) and Figure 22 (b) for termination.
OE Leakage Current	I_leak	–	3.5	–	mA	OE = disable logic, DC termination, OUTP and OUTN held at constant voltage, see Figure 14. Use AC termination to reduce I_leak to 0 mA.
Output Characteristics						
Differential Output Voltage	VOD	250	350	450	mV	See Figure 7
Delta VOD	ΔVOD	–	–	50	mV	See Figure 7
Offset Voltage	VOS	1.125	1.2	1.375	V	See Figure 7
Delta VOS	ΔVOS	–	–	50	mV	See Figure 7
Rise/Fall Time	Tr, Tf	–	290	–	ps	Measured 20% to 80% using Figure 22 (b) for termination. See Figure 8
Differential Asymmetry, peak-peak	V_da	–	50	–	mV	See Figure 9
Differential Skew, peak	V_ds	–	±40	–	ps	See Figure 10
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of VOD; see Figure 12
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 8. Electrical Characteristics – LVDS | Supply voltage: 1.8 V ±5%, 1.71 V to 3.63 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	36	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	40	–	mA	Including load termination current. See Figure 22 (a) and Figure 22 (b) for termination.
Current Consumption, Output Disabled without Termination	Idd_od_nt	–	45	–	mA	Excluding load termination current
Current Consumption Output Disabled with Termination	Idd_od_wt	–	48	–	mA	Including load termination current. See Figure 22 (a) and Figure 22 (b) for termination.
OE Leakage Current	I_leak	–	3.5	–	mA	OE = disable logic, DC termination, OUTP and OUTN held at constant voltage, see Figure 14. Use AC termination to reduce I_leak to 0 mA.
Output Characteristics						
Differential Output Voltage	VOD	250	350	450	mV	See Figure 7
Delta VOD	ΔVOD	–	–	50	mV	See Figure 7
Offset Voltage	VOS	1.125	1.2	1.375	V	See Figure 7
Delta VOS	ΔVOS	–	–	50	mV	See Figure 7
Rise/Fall Time	Tr, Tf	–	290	–	ps	Measured 20% to 80% using Figure 22 (b) for termination. See Figure 8
Differential Asymmetry, peak-peak	V_da	–	50	–	mV	See Figure 9
Differential Skew, peak	V_ds	–	±40	–	ps	See Figure 10
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of VOD; see Figure 12
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 9. Electrical Characteristics – HCSL | Supply voltage: 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	32	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	47	–	mA	Including load termination current. See Figure 23 for termination
Current Consumption, Output Disabled without Termination	Idd_od_nt	–	40	–	mA	Excluding load termination current
Current Consumption, Output Disabled with Termination	Idd_od_wt	–	55	–	mA	Including load termination current. See Figure 23 for termination
OE Leakage Current	I_leak	–	15	–	mA	OE = disable logic, DC termination, OUTP and OUTN held at constant voltage, see Figure 14
Output Characteristics						
Output High Voltage	VOH	0.60	0.7	0.95	V	See Figure 5
Output Low Voltage	VOL	-0.1	0	0.1	V	See Figure 5
Output Differential Voltage Swing	V_Swing	1	1.4	1.6	V	See Figure 6
Rise/Fall Time	Tr, Tf	–	400	–	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%. See Figure 6
Differential Asymmetry, peak-peak	V_da	–	100	–	mV	See Figure 9
Differential Skew, peak	V_ds	–	±40	–	ps	See Figure 10
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of V_Swing; see Figure 11
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 10. Electrical Characteristics – HCSL | Supply voltage: 1.8 V ±5%, 1.71 V to 3.63 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	32	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	47	–	mA	Including load termination current. See Figure 23 for termination
Current Consumption, Output Disabled without Termination	Idd_od_nt	–	40	–	mA	Excluding load termination current
Current Consumption, Output Disabled with Termination	Idd_od_wt	–	55	–	mA	Including load termination current. See Figure 23 for termination
OE Leakage Current	I_leak	–	15	–	mA	OE = disable logic, DC termination, OUTP and OUTN held at constant voltage, see Figure 14
Output Characteristics						
Output High Voltage	VOH	0.60	0.7	0.95	V	See Figure 5
Output Low Voltage	VOL	-0.1	0	0.1	V	See Figure 5
Output Differential Voltage Swing	V_Swing	1	1.4	1.6	V	See Figure 6
Rise/Fall Time	Tr, Tf	–	400	–	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%. See Figure 6
Differential Asymmetry, peak-peak	V_da	–	100	–	mV	See Figure 9
Differential Skew, peak	V_ds	–	±40	–	ps	See Figure 10
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of V_Swing; see Figure 11
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 11. Electrical Characteristics – Low Power HCSL | Supply voltage: 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	35	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	37	–	mA	Including load termination current for 5pF loading at 156.25 MHz. See Figure 24 for termination
Current Consumption, Output Disabled without Termination	Idd_od_nt	–	39	–	mA	Excluding load termination current
Current Consumption, Output Disabled with Termination	Idd_od_wt	–	39	–	mA	Including load termination current for 5pF loading at 156.25 MHz. See Figure 24 for termination
OE Leakage Current	I_leak	–	0	–	mA	OE = disable logic, AC termination, OUTP and OUTN held at constant voltage, see Figure 14
Output Characteristics						
Output High Voltage	VOH	0.8	0.9	1.15	V	See Figure 5
Output Low Voltage	VOL	-0.3	0	0.1	V	See Figure 5
Output Differential Voltage Swing	V_Swing	1.55	1.65	1.9	V	See Figure 6
Rise/Fall Time	Tr, Tf	–	520	–	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%. See Figure 6
Differential Asymmetry, peak-peak	V_da	–	550	–	mV	See Figure 9
Differential Skew, peak	V_ds	–	±30	–	ps	See Figure 10
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of V_Swing; see Figure 11
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Table 12. Electrical Characteristics – Low Power HCSL | Supply voltage: 1.8 V ±5%, 1.71 V to 3.63 V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Condition
Current Consumption, f = 156.25 MHz						
Current Consumption, Output Enabled without Termination	Idd_oe_nt	–	35	–	mA	Excluding load termination current
Current Consumption, Output Enabled with Termination	Idd_oe_wt	–	37	–	mA	Including load termination current for 5 pF loading at 156.25 MHz. See Figure 24 for termination
Current Consumption, Output Disabled without Termination	Idd_od_nt	–	39	–	mA	Excluding load termination current
Current Consumption, Output Disabled with Termination	Idd_od_wt	–	39	–	mA	Including load termination current for 5 pF loading at 156.25 MHz. See Figure 24 for termination
OE Leakage Current	I_leak	–	0	–	mA	OE = disable logic, AC termination, OUTP and OUTN held at constant voltage, see Figure 14
Output Characteristics						
Output High Voltage	VOH	0.8	0.9	1.15	V	See Figure 5
Output Low Voltage	VOL	-0.3	0	0.1	V	See Figure 5
Output Differential Voltage Swing	V_Swing	1.55	1.65	1.9	V	See Figure 6
Rise/Fall Time	Tr, Tf	–	520	–	ps	Measured with 2 pF capacitive loading to GND, 20% to 80%. See Figure 6
Differential Asymmetry, peak-peak	V_da	–	550	–	mV	See Figure 9
Differential Skew, peak	V_ds	–	±30	–	ps	See Figure 10
Overshoot Voltage, peak	V_ov	–	10	–	%	Measured as percent of V_Swing; see Figure 11
Power Supply Noise Immunity						
Power Supply-Induced Jitter Sensitivity[2]	PSJS	–	0.01	–	ps/mV	Power supply ripple from 1 kHz to 20 MHz
Power Supply-Induced Phase Noise	PSPN	–	-80	–	dBc	156.25 MHz, 50 mV peak-peak ripple on VDD

Note:

2. Terminology chosen for clarity; referred to historically as power-supply noise rejection (PSNR).

Table 13. Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings may cause permanent damage to the part.
Actual performance of the IC is only guaranteed within the operational specifications, not at absolute maximum ratings.

Parameter	Test Conditions	Min.	Max.	Unit
Continuous Power Supply Voltage Range (Vdd)		-0.5	4.0	V
Input Voltage, Maximum	Any input pin	–	Vdd + 0.3	V
Input Voltage, Minimum	Any input pin	-0.3	–	V
Storage Temperature		-65	150	°C
Maximum Junction Temperature		–	130	°C
Soldering Temperature (follow standard Pb-free soldering guidelines)		–	260	°C

Table 14. Thermal Considerations[3]

Package	θ_{JA}, 4 Layer Board (°C/W)	θ_{JC}, Bottom (°C/W)
3225, 6-pin	TBD	TBD

Notes:
3. Refer to JESD51 for θ_{JA} and θ_{JC} definitions, and reference layout used to determine the θ_{JA} and θ_{JC} values in the above table.

Table 15. Maximum Operating Junction Temperature[4]

Max Operating Temperature (ambient)	Maximum Operating Junction Temperature
70°C	TBD
85°C	TBD
95°C	TBD
105°C	TBD

Notes:
4. Datasheet specifications are not guaranteed if junction temperature exceeds the maximum operating junction temperature.

Table 16. Environmental Compliance

Parameter	Test Conditions	Value	Unit
Mechanical Shock Resistance	MIL-STD-883F, Method 2002	10,000	*g*
Mechanical Vibration Resistance	MIL-STD-883F, Method 2007	70	*g*
Soldering Temperature (follow standard Pb free soldering guidelines)	MIL-STD-883F, Method 2003	260	°C
Moisture Sensitivity Level	MSL1 @ 260°C		
Electrostatic Discharge (HBM)	HBM, JESD22-A114	2,000	V
Charge-Device Model ESD Protection	JESD220C101	750	V
Latch-up Tolerance	JESD78 Compliant		

Pin Description

Table 17. Pin Description

Pin	Map	Functionality	
1	OE/NF	Output Enable (OE)	H[5] Specified frequency output L: OUTP (OUTN) held at logic high (low)
		No Function (NF)	H or L or Open: No effect on output frequency or other device functions.
2	NF	No Function	H or L or Open: No effect on output frequency or other device functions
3	GND	Power	VDD Power Supply Ground
4	OUTP	Output	Oscillator output
5	OUTN	Output	Complementary oscillator output
6	VDD	Power	Power supply voltage[6]

Top View

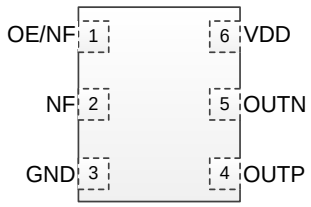


Figure 4. Pin Assignments

Notes:

5. OE pin includes a 120 kΩ internal pull-up resistor to VDD when active high, and a 120 kΩ internal pull-down resistor to GND when active low. In noisy environments, OE pin that is active high or active low are recommended to include an external pull-up or pull-down resistor, respectively, of 10 kΩ when the pin is not externally driven.
6. A capacitor of value 0.1 µF or higher between VDD and GND pins is required.

FlexSwing Configurations

A FlexSwing output-driver performs like LVPECL but provides independent control of voltage swing and DC offset voltage levels. This simplifies interfacing with chipsets having non-standard input voltage requirements and can eliminate all external source-bias resistors. FlexSwing supports power supply voltages from 1.71 V to 3.63 V, and the programmable VOH and VOL levels may be referenced to the voltage on either VDD or GND pins.

Table 18. FlexSwing 2-digit Order Codes specifying VHn and VLn referenced to voltage on VDD pin

Order Code V_Swing (V)			VLn																					
			A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V	W	X
			Vdd-2.35V	Vdd-2.30V	Vdd-2.25V	Vdd-2.20V	Vdd-2.15V	Vdd-2.10V	Vdd-2.05V	Vdd-2.00V	Vdd-1.95V	Vdd-1.90V	Vdd-1.85V	Vdd-1.80V	Vdd-1.75V	Vdd-1.70V	Vdd-1.65V	Vdd-1.60V	Vdd-1.55V	Vdd-1.50V	Vdd-1.45V	Vdd-1.40V	Vdd-1.35V	Vdd-1.30V
VHn	A	Vdd-0.80V														AP 1.8	AQ 1.7	AR 1.6	AS 1.5	AT 1.4	AU 1.3	AV 1.2	AW 1.1	AX 1
	B	Vdd-0.85V													BN 1.8	BP 1.7	BQ 1.6	BR 1.5	BS 1.4	BT 1.3	BU 1.2	BV 1.1	BW 1	BX 0.9
	C	Vdd-0.90V												CM 1.8	CN 1.7	CP 1.6	CQ 1.5	CR 1.4	CS 1.3	CT 1.2	CU 1.1	CV 1	CW 0.9	CX 0.8
	D	Vdd-0.95V											DL 1.8	DM 1.7	DN 1.6	DP 1.5	DQ 1.4	DR 1.3	DS 1.2	DT 1.1	DU 1	DV 0.9	DW 0.8	DX 0.7
	E	Vdd-1.00V										EK 1.8	EL 1.7	EM 1.6	EN 1.5	EP 1.4	EQ 1.3	ER 1.2	ES 1.1	ET 1	EU 0.9	EV 0.8	EW 0.7	EX 0.6
	F	Vdd-1.05V									FJ 1.8	FK 1.7	FL 1.6	FM 1.5	FN 1.4	FP 1.3	FQ 1.2	FR 1.1	FS 1	FT 0.9	FU 0.8	FV 0.7	FW 0.6	FX 0.5
	G	Vdd-1.10V								GH 1.8	GJ 1.7	GK 1.6	GL 1.5	GM 1.4	GN 1.3	GP 1.2	GQ 1.1	GR 1	GS 0.9	GT 0.8	GU 0.7	GV 0.6	GW 0.5	GX 0.4
	H	Vdd-1.15V							HG 1.8	HH 1.7	HJ 1.6	HK 1.5	HL 1.4	HM 1.3	HN 1.2	HP 1.1	HQ 1	HR 0.9	HS 0.8	HT 0.7	HU 0.6	HV 0.5	HW 0.4	HX 0.3
	J	Vdd-1.20V						JF 1.8	JG 1.7	JH 1.6	JJ 1.5	JK 1.4	JL 1.3	JM 1.2	JN 1.1	JP 1	JQ 0.9	JR 0.8	JS 0.7	JT 0.6	JU 0.5	JV 0.4	JW 0.3	JX 0.2
	K	Vdd-1.25V					KE 1.8	KF 1.7	KG 1.6	KH 1.5	KJ 1.4	KK 1.3	KL 1.2	KM 1.1	KN 1	KP 0.9	KQ 0.8	KR 0.7	KS 0.6	KT 0.5	KU 0.4	KV 0.3	KW 0.2	
	L	Vdd-1.30V				LD 1.8	LE 1.7	LF 1.6	LG 1.5	LH 1.4	LJ 1.3	LK 1.2	LL 1.1	LM 1	LN 0.9	LP 0.8	LQ 0.7	LR 0.6	LS 0.5	LT 0.4	LU 0.3	LV 0.2		
	M	Vdd-1.35V			MC 1.8	MD 1.7	ME 1.6	MF 1.5	MG 1.4	MH 1.3	MJ 1.2	MK 1.1	ML 1	MM 0.9	MN 0.8	MP 0.7	MQ 0.6	MR 0.5	MS 0.4	MT 0.3	MU 0.2			
	N	Vdd-1.40V		NB 1.8	NC 1.7	ND 1.6	NE 1.5	NF 1.4	NG 1.3	NH 1.2	NJ 1.1	NK 1	NL 0.9	NM 0.8	NN 0.7	NP 0.6	NQ 0.5	NR 0.4	NS 0.3	NT 0.2				
	P	Vdd-1.45V	PA 1.8	PB 1.7	PC 1.6	PD 1.5	PE 1.4	PF 1.3	PG 1.2	PH 1.1	PJ 1	PK 0.9	PL 0.8	PM 0.7	PN 0.6	PP 0.5	PQ 0.4	PR 0.3	PS 0.2					
	Q	Vdd-1.50V	QA 1.7	QB 1.6	QC 1.5	QD 1.4	QE 1.3	QF 1.2	QG 1.1	QH 1	QJ 0.9	QK 0.8	QL 0.7	QM 0.6	QN 0.5	QP 0.4	QQ 0.3	QR 0.2						
	R	Vdd-1.55V	RA 1.6	RB 1.5	RC 1.4	RD 1.3	RE 1.2	RF 1.1	RG 1	RH 0.9	RJ 0.8	RK 0.7	RL 0.6	RM 0.5	RN 0.4	RP 0.3	RQ 0.2							
	S	Vdd-1.60V	SA 1.5	SB 1.4	SC 1.3	SD 1.2	SE 1.1	SF 1	SG 0.9	SH 0.8	SJ 0.7	SK 0.6	SL 0.5	SM 0.4	SN 0.3	SP 0.2								
	T	Vdd-1.65V	TA 1.4	TB 1.3	TC 1.2	TD 1.1	TE 1	TF 0.9	TG 0.8	TH 0.7	TJ 0.6	TK 0.5	TL 0.4	TM 0.3	TN 0.2									
	U	Vdd-1.70V	UA 1.3	UB 1.2	UC 1.1	UD 1	UE 0.9	UF 0.8	UG 0.7	UH 0.6	UJ 0.5	UK 0.4	UL 0.3	UM 0.2										
	V	Vdd-1.75V	VA 1.2	VB 1.1	VC 1	VD 0.9	VE 0.8	VF 0.7	VG 0.6	VH 0.5	VJ 0.4	VK 0.3	VL 0.2											
	W	Vdd-1.80V	WA 1.1	WB 1	WC 0.9	WD 0.8	WE 0.7	WF 0.6	WG 0.5	WH 0.4	WJ 0.3	WK 0.2												

Supply Voltage	Available Colors
1.8V±5%	Not Supported
1.71V to 3.63V	Not Supported
2.5V±10%	Blue
3.3V±10%	Blue / Red
2.25V to 3.63V	Blue

The above table identifies supported combinations of nominal VOH (i.e. VHn) and nominal VOL (i.e. VLn) in colored boxes. The two-character code in each box corresponds to the VHn and VLn codes specified in the 2nd column and 2nd row in the table, respectively. The number in each box indicates the nominal differential swing (i.e. VHn – VLn).

For example, order code “FS” selects VHn code “F” (i.e. Vdd-1.05 V) and VLn code “S” (i.e. Vdd-1.55 V) corresponding to a V_Swing of 1 V peak-peak, which may be used for supply voltages of 2.5 V ±10%, 3.3 V ±10% or (2.25 V to 3.63 V). Alternatively, an order code of “GS” corresponds to a VHn code “G” (i.e. Vdd-1.10 V) and a VLn order code “S” (e.g. Vdd-1.55 V) corresponding to a V_Swing of 0.9 V peak-peak, which may be used for a supply voltage of 3.3 V ±10%.

Table 19. FlexSwing 2-digit Order Codes specifying VHn and VLn referenced to voltage on GND pin

Supply Voltage	Available Colors
1.8V±5%	Green
1.71V to 3.63V	Green
2.5V±10%	Green, Blue
3.3V±10%	Green, Blue, Red
2.25V to 3.63V	Green, Blue

Order Code V_Swing (V)			VLn																												
			A	B	C	D	E	F	G	H	J	K	L	M	N	P	Q	R	S	T	U	V	W	X	Y	Z	1	2	3	4	5
			0.30V	0.35V	0.40V	0.45V	0.50V	0.55V	0.60V	0.65V	0.70V	0.75V	0.80V	0.85V	0.90V	0.95V	1.00V	1.05V	1.10V	1.15V	1.20V	1.25V	1.30V	1.35V	1.40V	1.45V	1.50V	1.55V	1.60V	1.65V	1.70V
VHn	A	2.50V																											A3 1.8	A4 1.7	A5 1.6
	B	2.45V																										B2 1.8	B3 1.7	B4 1.6	B5 1.5
	C	2.40V																									C1 1.8	C2 1.7	C3 1.6	C4 1.5	C5 1.4
	D	2.35V																								DZ 1.8	D1 1.7	D2 1.6	D3 1.5	D4 1.4	D5 1.3
	E	2.30V																							EY 1.8	EZ 1.7	E1 1.6	E2 1.5	E3 1.4	E4 1.3	E5 1.2
	F	2.25V																						FX 1.8	FY 1.7	FZ 1.6	F1 1.5	F2 1.4	F3 1.3	F4 1.2	F5 1.1
	G	2.20V																					GW 1.8	GX 1.7	GY 1.6	GZ 1.5	G1 1.4	G2 1.3	G3 1.2	G4 1.1	G5 1
	H	2.15V																				HV 1.8	HW 1.7	HX 1.6	HY 1.5	HZ 1.4	H1 1.3	H2 1.2	H3 1.1	H4 1	H5 0.9
	J	2.10V																			JU 1.8	JV 1.7	JW 1.6	JX 1.5	JY 1.4	JZ 1.3	J1 1.2	J2 1.1	J3 1	J4 0.9	J5 0.8
	K	2.05V																		KT 1.8	KU 1.7	KV 1.6	KW 1.5	KX 1.4	KY 1.3	KZ 1.2	K1 1.1	K2 1	K3 0.9	K4 0.8	K5 0.7
	L	2.00V																	LS 1.8	LT 1.7	LU 1.6	LV 1.5	LW 1.4	LX 1.3	LY 1.2	LZ 1.1	L1 1	L2 0.9	L3 0.8	L4 0.7	L5 0.6
	M	1.95V																MR 1.8	MS 1.7	MT 1.6	MU 1.5	MV 1.4	MW 1.3	MX 1.2	MY 1.1	MZ 1	M1 0.9	M2 0.8	M3 0.7	M4 0.6	M5 0.5
	N	1.90V															NQ 1.8	NR 1.7	NS 1.6	NT 1.5	NU 1.4	NV 1.3	NW 1.2	NX 1.1	NY 1	NZ 0.9	N1 0.8	N2 0.7	N3 0.6	N4 0.5	N5 0.4
	P	1.85V														PP 1.8	PQ 1.7	PR 1.6	PS 1.5	PT 1.4	PU 1.3	PV 1.2	PW 1.1	PX 1	PY 0.9	PZ 0.8	P1 0.7	P2 0.6	P3 0.5	P4 0.4	P5 0.3
	Q	1.80V													QN 1.8	QP 1.7	QQ 1.6	QR 1.5	QS 1.4	QT 1.3	QU 1.2	QV 1.1	QW 1	QX 0.9	QY 0.8	QZ 0.7	Q1 0.6	Q2 0.5	Q3 0.4	Q4 0.3	Q5 0.2
	R	1.75V												RM 1.8	RN 1.7	RP 1.6	RQ 1.5	RR 1.4	RS 1.3	RT 1.2	RU 1.1	RV 1	RW 0.9	RX 0.8	RY 0.7	RZ 0.6	R1 0.5	R2 0.4	R3 0.3	R4 0.2	
	S	1.70V											SL 1.8	SM 1.7	SN 1.6	SP 1.5	SQ 1.4	SR 1.3	SS 1.2	ST 1.1	SU 1	SV 0.9	SW 0.8	SX 0.7	SY 0.6	SZ 0.5	S1 0.4	S2 0.3	S3 0.2		
	T	1.65V										TK 1.8	TL 1.7	TM 1.6	TN 1.5	TP 1.4	TQ 1.3	TR 1.2	TS 1.1	TT 1	TU 0.9	TV 0.8	TW 0.7	TX 0.6	TY 0.5	TZ 0.4	T1 0.3	T2 0.2			
	U	1.60V									UJ 1.8	UK 1.7	UL 1.6	UM 1.5	UN 1.4	UP 1.3	UQ 1.2	UR 1.1	US 1	UT 0.9	UU 0.8	UV 0.7	UW 0.6	UX 0.5	UY 0.4	UZ 0.3	U1 0.2				
	V	1.55V								VH 1.8	VJ 1.7	VK 1.6	VL 1.5	VM 1.4	VN 1.3	VP 1.2	VQ 1.1	VR 1	VS 0.9	VT 0.8	VU 0.7	VV 0.6	VW 0.5	VX 0.4	VY 0.3	VZ 0.2					
	W	1.50V							WG 1.8	WH 1.7	WJ 1.6	WK 1.5	WL 1.4	WM 1.3	WN 1.2	WP 1.1	WQ 1	WR 0.9	WS 0.8	WT 0.7	WU 0.6	WV 0.5	WW 0.4	WX 0.3	WY 0.2						
	X	1.45V						XF 1.8	XG 1.7	XH 1.6	XJ 1.5	XK 1.4	XL 1.3	XM 1.2	XN 1.1	XP 1	XQ 0.9	XR 0.8	XS 0.7	XT 0.6	XU 0.5	XV 0.4	XW 0.3	XX 0.2							
	Y	1.40V					YE 1.8	YF 1.7	YG 1.6	YH 1.5	YJ 1.4	YK 1.3	YL 1.2	YM 1.1	YN 1	YP 0.9	YQ 0.8	YR 0.7	YS 0.6	YT 0.5	YU 0.4	YV 0.3	YW 0.2								
	Z	1.35V				ZD 1.8	ZE 1.7	ZF 1.6	ZG 1.5	ZH 1.4	ZJ 1.3	ZK 1.2	ZL 1.1	ZM 1	ZN 0.9	ZP 0.8	ZQ 0.7	ZR 0.6	ZS 0.5	ZT 0.4	ZU 0.3	ZV 0.2									
	1	1.30V			1C 1.8	1D 1.7	1E 1.6	1F 1.5	1G 1.4	1H 1.3	1J 1.2	1K 1.1	1L 1	1M 0.9	1N 0.8	1P 0.7	1Q 0.6	1R 0.5	1S 0.4	1T 0.3	1U 0.2										
	2	1.25V		2B 1.8	2C 1.7	2D 1.6	2E 1.5	2F 1.4	2G 1.3	2H 1.2	2J 1.1	2K 1	2L 0.9	2M 0.8	2N 0.7	2P 0.6	2Q 0.5	2R 0.4	2S 0.3	2T 0.2											
	3	1.20V	3A 1.8	3B 1.7	3C 1.6	3D 1.5	3E 1.4	3F 1.3	3G 1.2	3H 1.1	3J 1	3K 0.9	3L 0.8	3M 0.7	3N 0.6	3P 0.5	3Q 0.4	3R 0.3	3S 0.2												

Waveform Diagrams

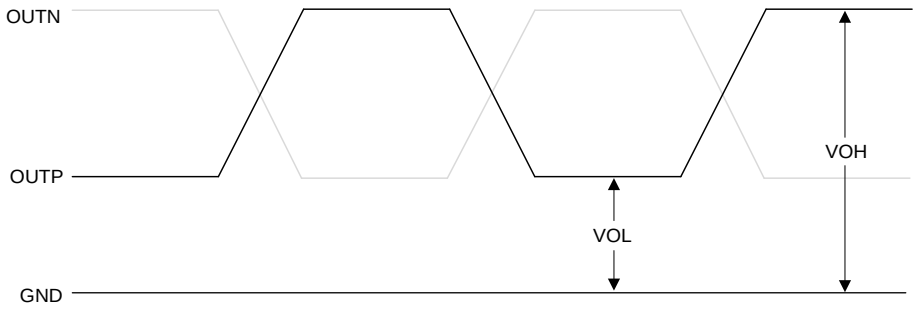


Figure 5. LVPECL, HCSL, Low-Power HCSL, and FlexSwing Voltage Levels per Differential Pin

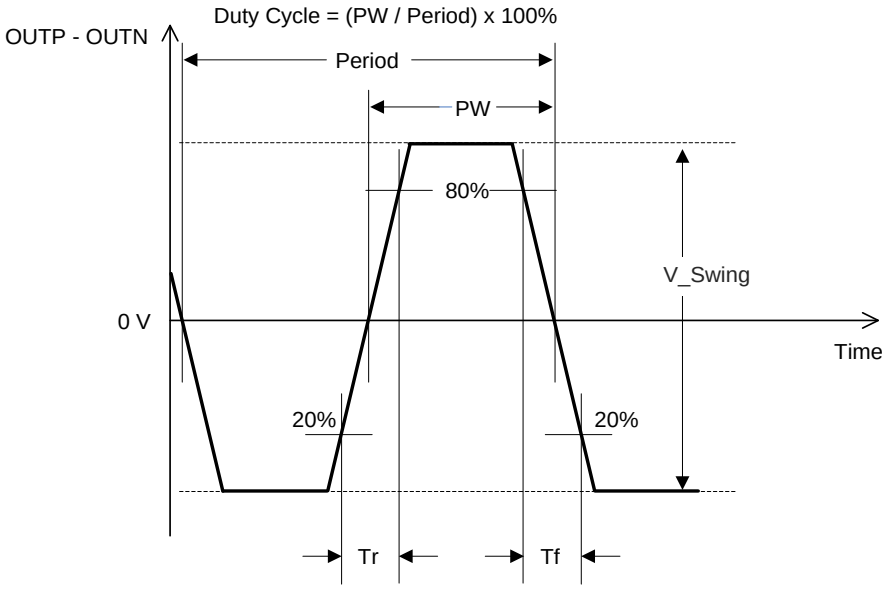


Figure 6. LVPECL, HCSL, Low-Power HCSL, and FlexSwing Voltage Levels Across Differential Pair

Waveform Diagrams (continued)

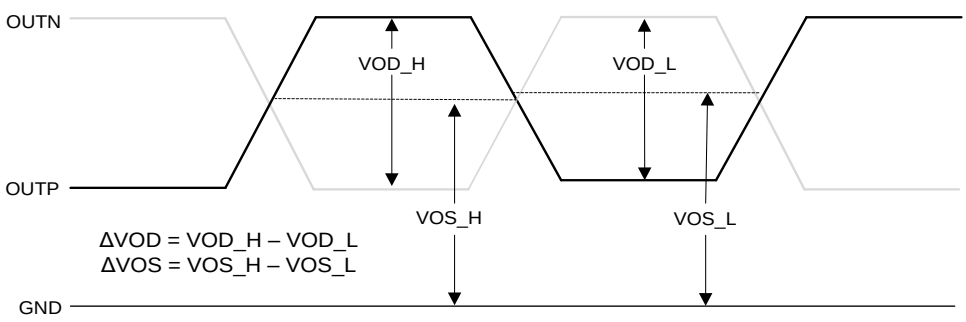


Figure 7. LVDS Voltage Levels per Differential Pin

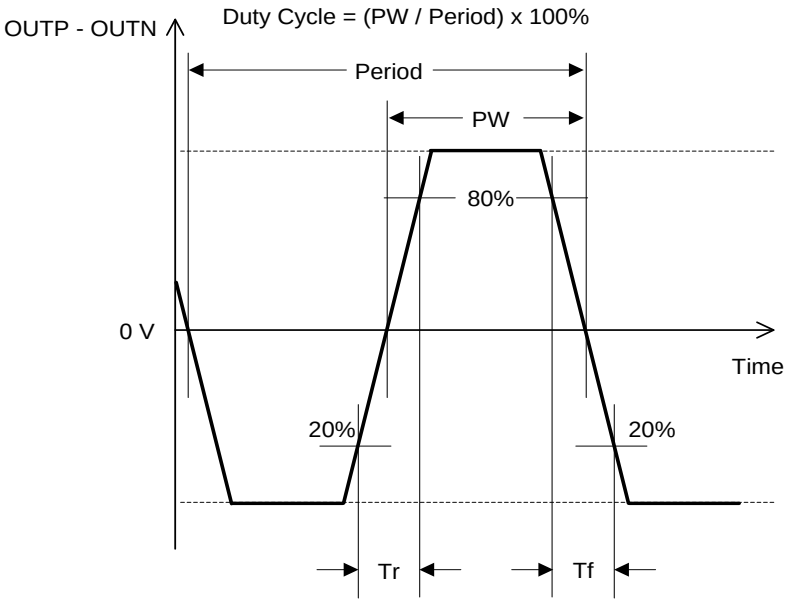


Figure 8. LVDS Differential Waveform

Waveform Diagrams (continued)

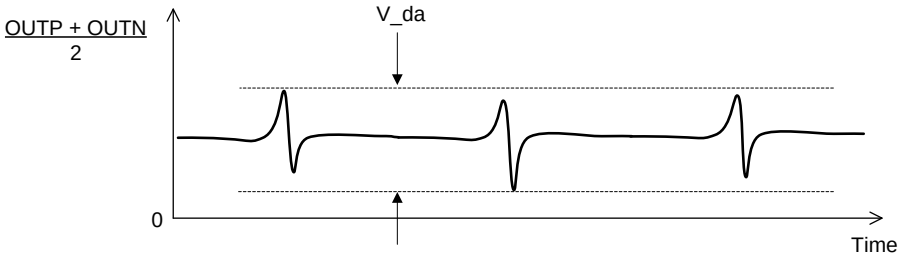


Figure 9. Differential Asymmetry (V_da)

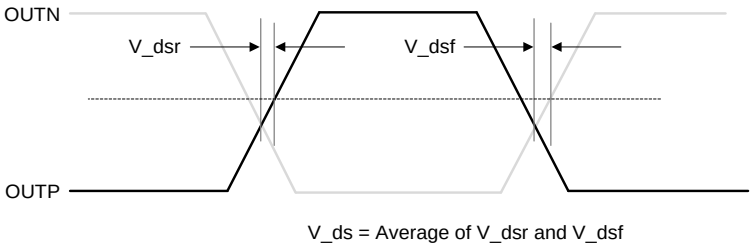


Figure 10. Differential Skew (V_ds) is measured as the Time between the Average Voltage Level and Crossing Voltage

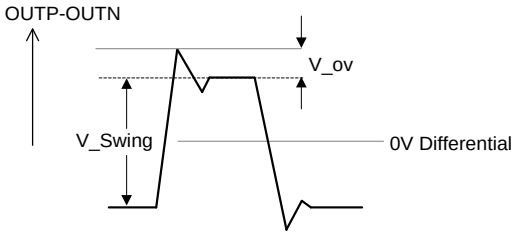


Figure 11. Overshoot Voltage (V_ov) for LVPECL, FlexSwing, HCSL, Low-power HCSL

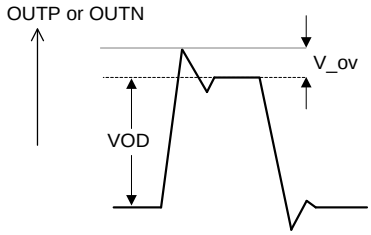


Figure 12. Overshoot Voltage (V_ov) for LVDS Output

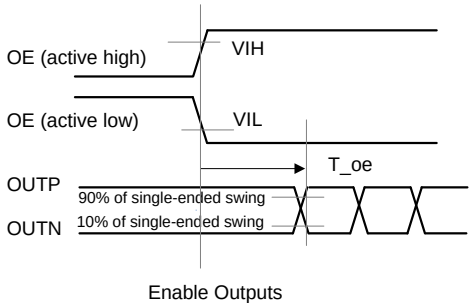


Figure 13. OE Pin Enable Timing (T_oe)

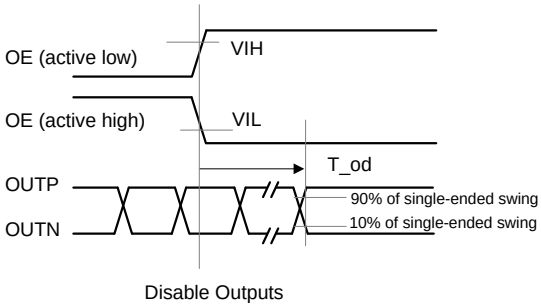


Figure 14. OE Pin Disable Timing (T_od)

Termination Diagrams

LVPECL and FlexSwing Termination

The SiT9501 output drivers include special features for supporting low-load current without sacrificing signal integrity via simple terminations as shown in Figure 16 and Figure 18. This allows very low power consumption compared to traditional LVPECL drivers. The FlexSwing and LVPECL outputs are voltage-mode drivers. Use the table and figures below to select a termination circuit for the desired supply voltage. The table also provides LVPECL current consumption (I_load) into the load termination.

Table 20. Termination Options for LVPECL and FlexSwing Signaling

Signaling	Supply Voltage, Vdd	Termination Options					
		Figure 15	Figure 16	Figure 17	Figure 18	Figure 19	Figure 20
LVPECL referenced to Vdd	2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V	OK to use I_load = 40 mA with 100 Ω near-end bias resistor	**Do Not Use**	OK to use I_load = 28 mA	OK to use	OK to use I_load = 28 mA	**Do Not Use**
FlexSwing referenced to Vdd		OK to use[7]	OK to use (see Figure 16 for frequency ranges and voltage swings)	OK to use[7]	OK to use	OK to use	**Do Not Use**
FlexSwing referenced to Gnd	1.71 V to 3.63 V			**Do Not Use**	OK to use	**Do Not Use**	**Do Not Use**
	1.8 V ±5%			**Do Not Use**	OK to use	**Do Not Use**	OK to use

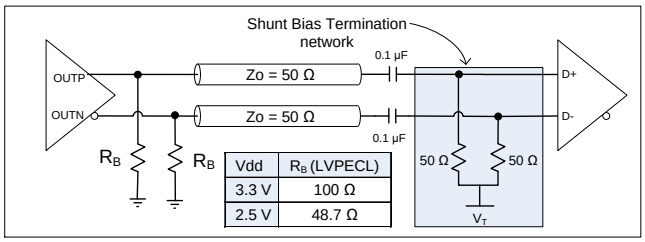


Figure 15. Recommended LVPECL and FlexSwing[8] Termination when AC-coupled

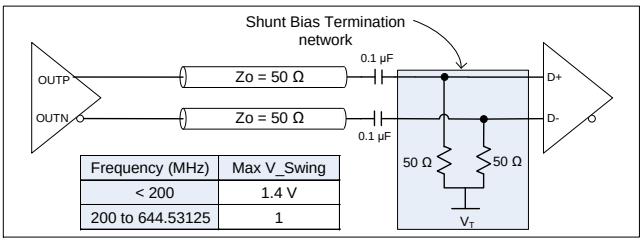


Figure 16. Recommended FlexSwing Termination when AC-coupled

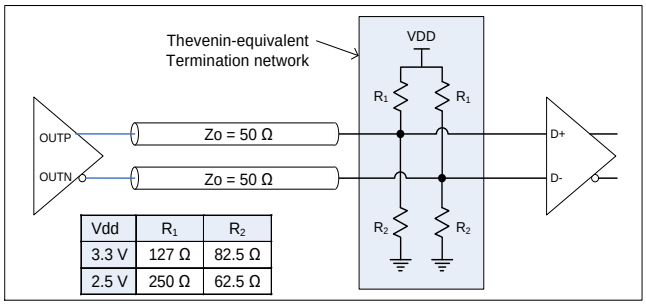


Figure 17. LVPECL and FlexSwing DC-coupled Load Termination with Thevenin Equivalent Network

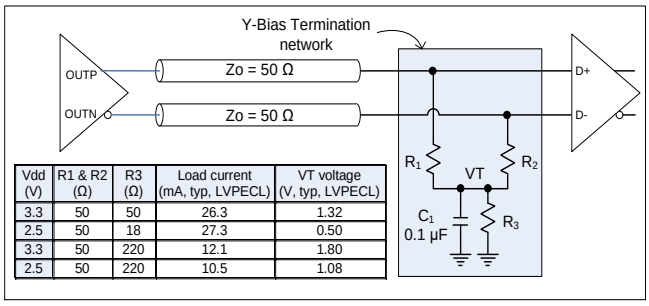


Figure 18. LVPECL and FlexSwing with DC-coupled Parallel Shunt Load Termination

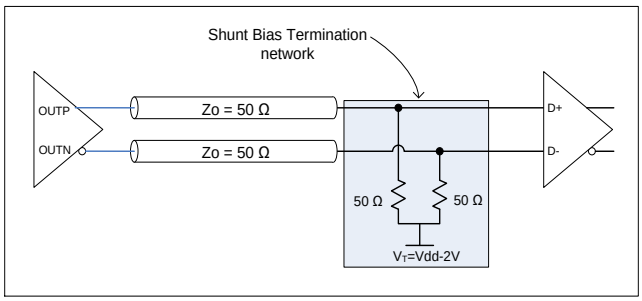


Figure 19. LVPECL and FlexSwing with Y-Bias Termination

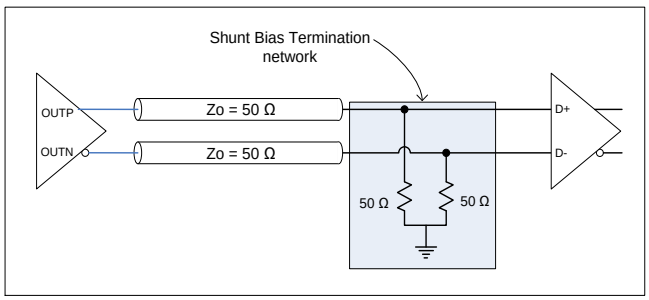


Figure 20. FlexSwing Termination – Only for use with Supply Voltage Order Code "18"

Termination Diagrams (continued)

LVDS, Supply Voltage: 1.8 V ±5%, 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

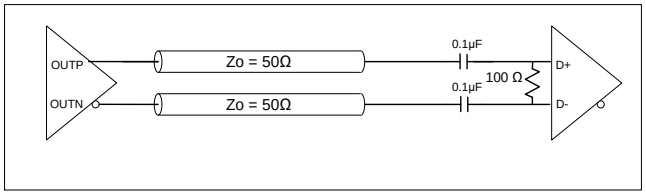


Figure 21. LVDS AC Termination

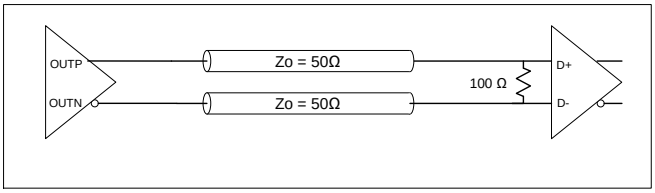


Figure 22. LVDS DC Termination at the Load

HCSL, Supply Voltage: 1.8 V ±5%, 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

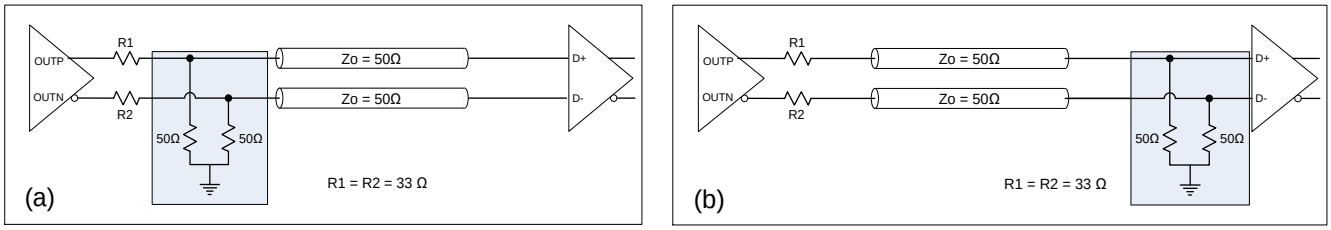


Figure 23. (a) HCSL Source Termination and (b) HCSL Load Termination

Low-power HCSL, Supply Voltage: 1.8 V ±5%, 2.5 V ±10%, 3.3 V ±10%, 2.25 V to 3.63 V, 1.71 V to 3.63 V

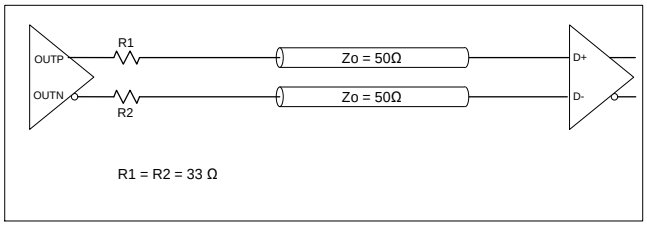


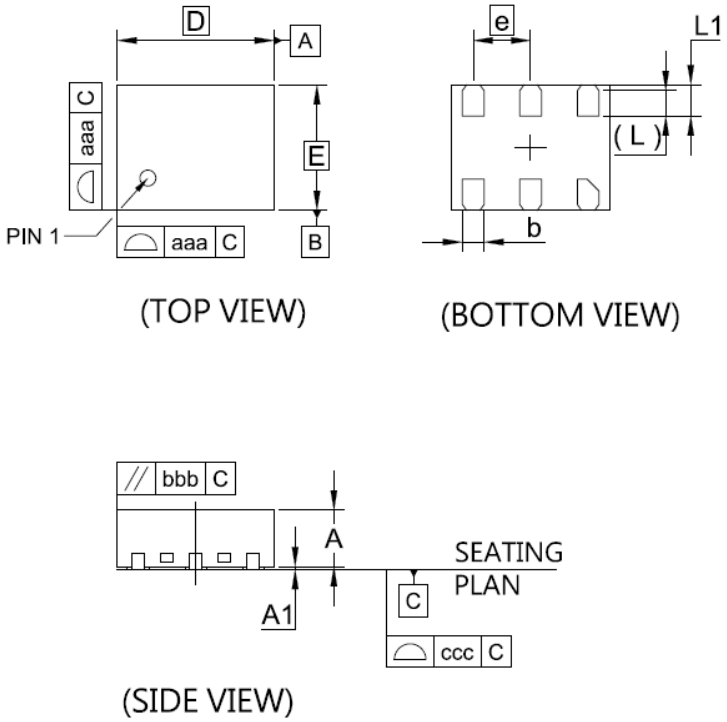
Figure 24. Low-power HCSL Termination

Notes:

7. Contact SiTime for optimum R1 and R2 values for FlexSwing options.
8. Contact SiTime for optimum Rs values for FlexSwing options.

Dimensions and Patterns — 2.0 x 1.6 mm x mm

Package Size – Dimensions (Unit: mm)[9]



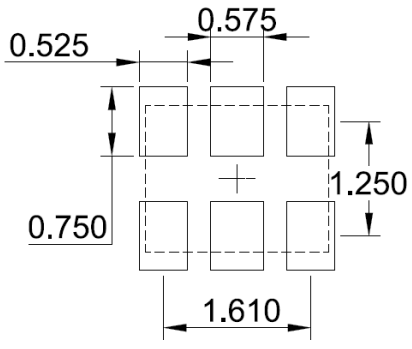
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.700	0.750	0.800
STAND OFF		A1	0.000	0.035	0.050
BODY SIZE	X	D		2.000 BSC	
	Y	E		1.600 BSC	
LEAD WIDTH		b	0.225	0.275	0.325
LEAD LENGTH		L		0.324 REF	
		L1	0.300	0.400	0.500
LEAD PITCH		e		0.730 BSC	
PACKAGE TOLERNCE		aaa		0.100	
MOLD FLATNESS		bbb		0.100	
COPLANARITY		ccc		0.080	

NOTE

1. ALL DIMENSION IN MM

SiTime			
PKG INFO		DRAWING NO.	
6L PQFD 2.000x1.600X0.750 mm		POD-077-PQFN-006-C02016	
		REV	SHEET
DATE	2020/6/1	A01	01

Recommended Land Pattern (Unit: mm)[10]



Note : All units in mm.

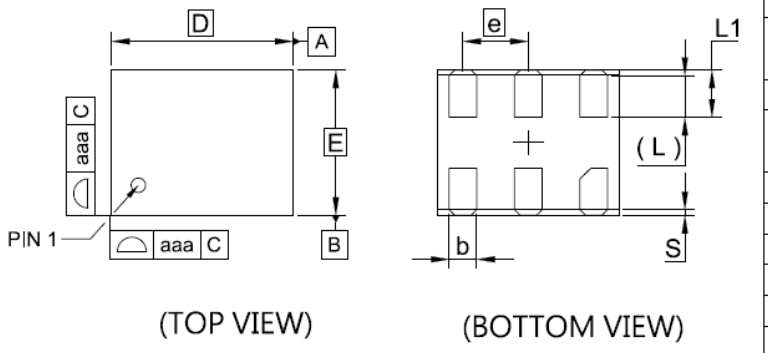
SiTime	PKG INFO	SPL DRAWING NO.	
	6L PQFN 2.000x1.600 mm	SPL-077-PQFN-006-C02016	
DATE		REV	SHEET
2020/04/20		A00	01

Notes:

9. Top Marking: Y denotes manufacturing origin and XXXX denotes manufacturing lot number. The value of “Y” will depend on the assembly location of the device.
10. A capacitor of value 0.1 µF or higher between VDD and GND is required. An additional 10 µF capacitor between VDD and GND is required for the best phase jitter performance.

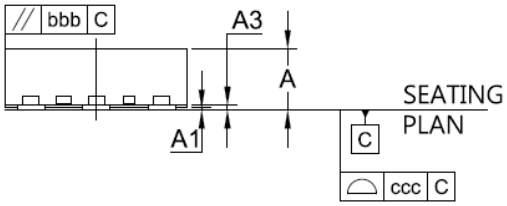
Dimensions and Patterns — 2.5 x 2.0 mm x mm

Package Size – Dimensions (Unit: mm)[9]



(TOP VIEW)

(BOTTOM VIEW)



(SIDE VIEW)

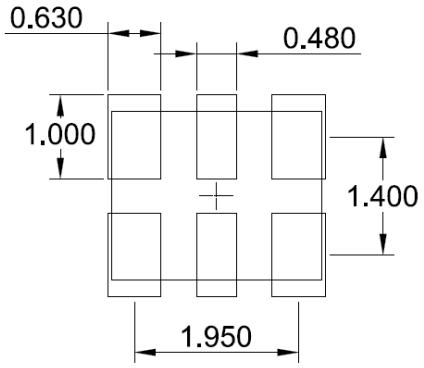
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.800	0.850	0.900
STAND OFF		A1	0.000	0.035	0.050
BODY SIZE	X	D		2.500 BSC	
	Y	E		2.000 BSC	
LEAD WIDTH		b	0.330	0.380	0.430
LEAD LENGTH		L		0.572 REF	
		L1	0.550	0.650	0.750
LEAD PITCH		e		0.900 BSC	
PACKAGE TOLERNCE		aaa		0.100	
MOLD FLATNESS		bbb		0.100	
COPLANARITY		ccc		0.080	
HALF CUT WIDTH		R	0.075	---	---
HALF CUT DEPTH		A3	---	---	0.075

NOTE

1. ALL DIMENSION IN MM

SiTime			
PKG INFO		DRAWING NO.	
6L PQFD 2.500x2.000X0.850 mm		POD-078-PQFW-006-C02520	
		REV	SHEET
DATE	2020/6/1	A01	01

Recommended Land Pattern (Unit: mm)[10]

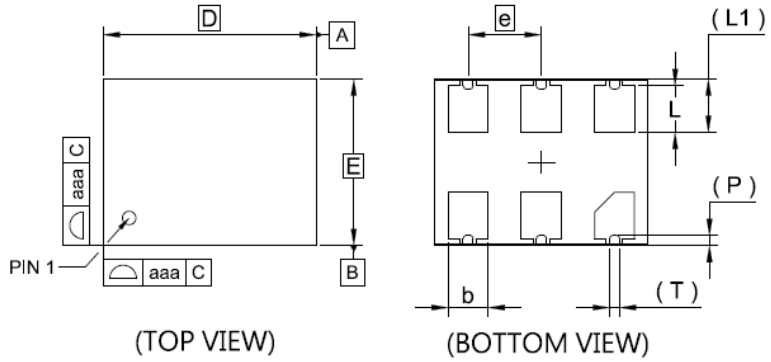


Note : All units in mm.

SiTime	PKG INFO	SPL DRAWING NO.	
	6L PQFW 2.500x2.000 mm	SPL-078-PQFW-006-C02520	
DATE		REV	SHEET
2020/04/20		A00	01

Dimensions and Patterns — 3.2 x 2.5 mm x mm

Package Size – Dimensions (Unit: mm)[9]



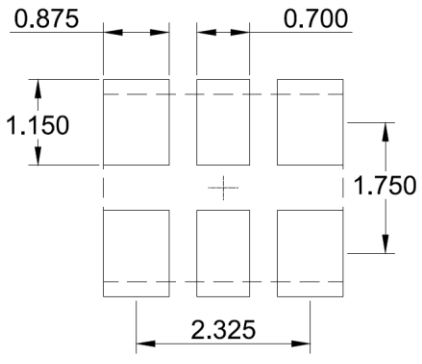
		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.800	0.850	0.900
STAND OFF		A1	0.000	0.035	0.050
BODY SIZE	X	D		3.200 BSC	
	Y	E		2.500 BSC	
LEAD WIDTH		b	0.550	0.600	0.650
LEAD LENGTH		L	0.650	0.700	0.750
		L1		0.800 REF	
LEAD PITCH		e		1.100 BSC	
PACKAGE TOLERNCE		aaa		0.100	
MOLD FLATNESS		bbb		0.100	
COPLANARITY		ccc		0.080	
DIMPLE WIDTH		T		0.150 REF	
DIMPLE LENGTH		P		0.150 REF	
DIMPLE DEPTH		A2		0.100 REF	

NOTE

1. ALL DIMENSION IN MM

SiTime			
PKG INFO		DRAWING NO.	
6L PQFD 3.200x2.500X0.850 mm		POD-076-PQFD-006-C03225	
		REV	SHEET
DATE	2020/6/1	A02	01

Recommended Land Pattern (Unit: mm)[10]



Note : All units in mm.

SiTime	PKG INFO	SPL DRAWING NO.	
	6L PQFD 3.200x2.500 mm	SPL-076-PQFD-006-C03225	
DATE		REV	SHEET
2020/04/20		A01	01

Additional Information

Table 21. Additional Information

Document	Description	Download Link
ECCN #: EAR99	Five character designation used on the commerce Control List (CCL) to identify dual use items for export control purposes.	—
HTS Classification Code: 8542.39.0000	A Harmonized Tariff Schedule (HTS) code developed by the World Customs Organization to classify/define internationally traded goods.	—
Manufacturing Notes	Tape & Reel dimension, reflow profile and other manufacturing related info	https://www.sitime.com/support/resource-library?filter=531
Termination Techniques	Termination design recommendations	http://www.sitime.com/support/application-notes
Layout Techniques	Layout recommendations	http://www.sitime.com/support/application-notes
Evaluation Boards	SiT6760EB	TBD

Revision History

Table 22. Revision History

Revision	Release Date	Change Summary
0.5	04/27/2020	Advanced datasheet
0.51	05/18/2020	Formatting changes Fixed typos Added 2016 and 2520 packages
0.52	06/01/2020	Formatting changes Updated package drawings
0.53	08/02/2020	Modified Termination Diagrams section

SiTime Corporation, 5451 Patrick Henry Drive, Santa Clara, CA 95054, USA | **Phone:** +1-408-328-4400 | **Fax:** +1-408-328-4439