PWR-INT300

Low-side Driver IC

Logic-level Input
Low-side Drive and High-side Control

Product Highlights

5 V CMOS Compatible Control Inputs
- Combines logic inputs for low and high-side drives

Built-in High-voltage Level Shifters
- Integrated level shifters simplify high-side interface
- Can withstand > 800 V for direct interface to the PWR-INT301 high-side driver
- Pulsed outputs reduce power consumption

Gate Drive Output for an External MOSFET or IGBT
- Provides 1 A sink/500 mA source current
- Can drive MOSFET or IGBT gate at up to 20 V
- External MOSFET or IGBT allows flexibility in design
- Can operate at switching rates of up to 2 MHz

Built-in Protection Features
- UV lockout

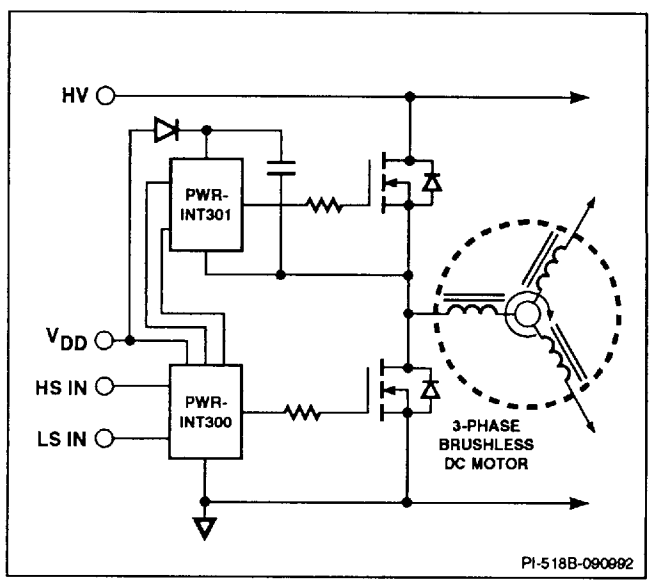


Figure 1. Typical Application

Description

The PWR-INT300 Low-side driver IC provides gate drive for an external low-side MOSFET or IGBT switch and high-side level shifting. When used in conjunction with the PWR-INT301 high-side driver, the PWR-INT300 provides a simple, cost-effective interface between low-voltage control logic and high-voltage MOSFET or IGBT switches. The PWR-INT300 is designed to be used across rectified 110 V or 220 V supplies. Both high side and low side switches can be controlled independently from ground-referenced 5 V logic inputs on the low side driver.

Simultaneous conduction is allowed by the PWR-INT300 for use with Two Transistor Forward Converters. To save power, the level shifting is done by pulsing a flip-flop in the high side driver through a high-voltage interface from the low side driver. The chips are powered from a nominal supply of 20 V to provide adequate gate drive for external MOSFETs or IGBTs. The logic inputs of the PWR-INT300 are 5 V CMOS logic compatible.

Applications include motor drives and half and full bridge power supplies.

The PWR-INT300 is available in an 8-pin plastic DIP package.

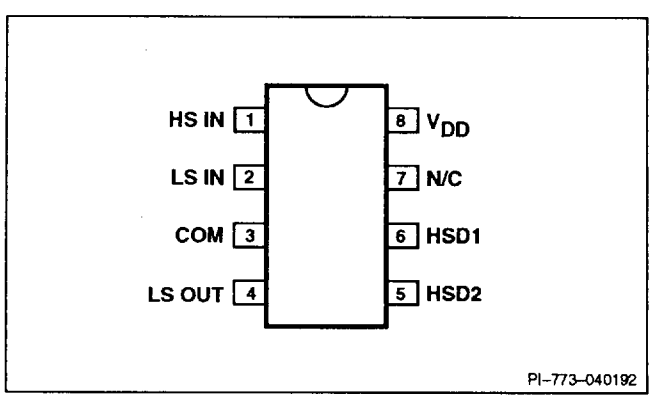


Figure 2. Pin Configuration.

ORDERING INFORMATION		
PART NUMBER	PACKAGE	TEMP RANGE
PWR-INT300PFI	8-pin PDIP	-40 to 85°C

411 Clyde Avenue
Mountain View, California, 94043
Business Phone: (415) 960-3572
Applications Hotline: (800) 552-3155
FAX: (800) 468-0809 In CA: (415) 940-1541

PRELIMINARY

November 1993

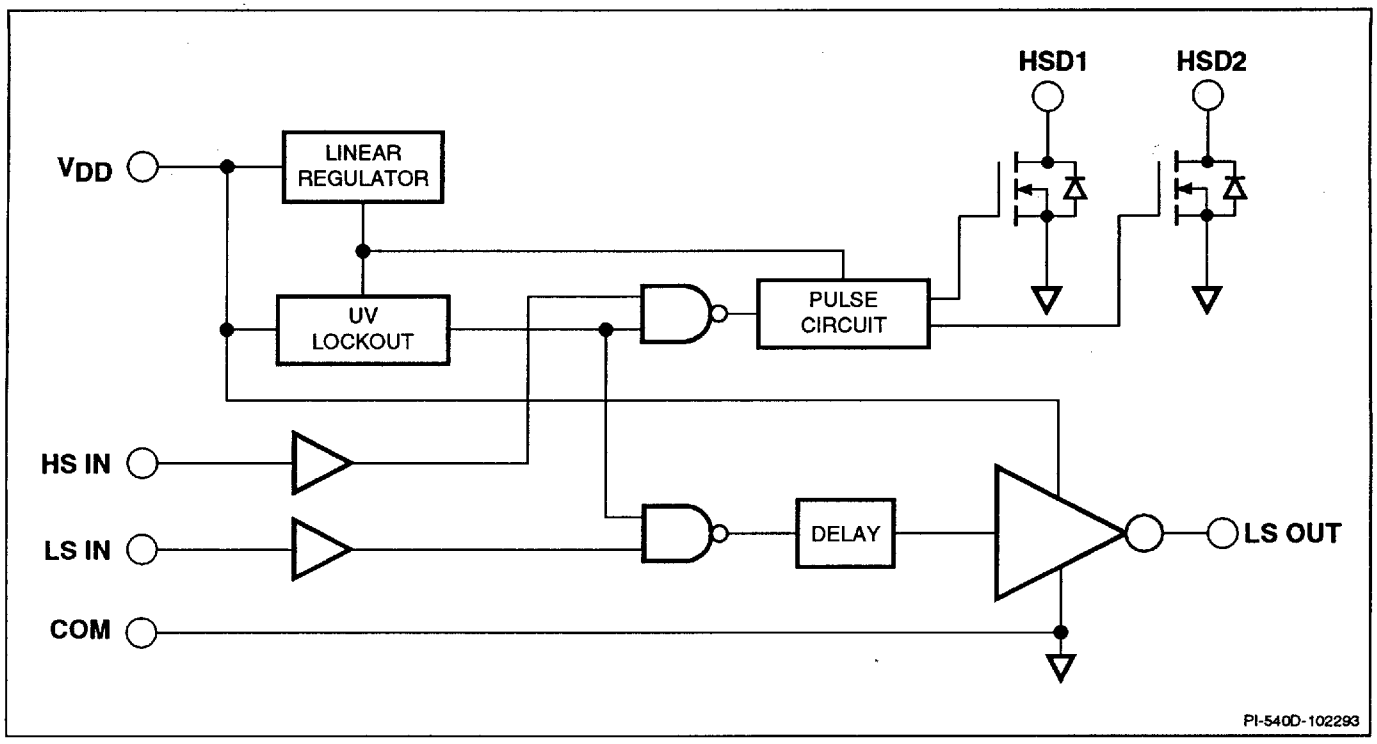


Figure 3. Functional Block Diagram of the PWR-INT300

PWR-INT300 Functional Description

5V Regulator
The 5V linear regulator circuit provides the supply voltage for the control logic and high-voltage level shift circuit. This allows the logic section to utilize separate supply voltages without the need of two external supplies.

Undervoltage Lockout
The undervoltage lockout circuit disables the LS OUT pin until the V_{DD} power supply has exceeded 9.25 V (typical), guaranteeing that the low side MOSFET OR IGBT will be off during power-up.

Pulse Circuit
The pulse circuit provides the two high-voltage level shifters with a sequence of signals allowing the part to have maximum noise immunity.

Driver
The CMOS drive circuit provides drive power to the gate of the MOSFET or IGBT. The driver consists of a CMOS buffer capable of driving external transistors at up to 20 V.

Pin Functional Description

Pin 1:
Active-high logic level input **HS IN** for turn on of the pulse circuit which signals the high side chip.

Pin 2:
Active-high logic level input **LS IN** for turn on of the low side driver.

Pin 3:
COM connection; analog reference point for the circuit.

Pin 4:
LS OUT is the output of the FET driver for the LS OUT output.

Pin 5:
Level shift output **HSD 2** is used in conjunction with HSD1 to provide a noise immune interface to the high side driver.

Pin 6:
Level shift output **HSD 1** is used in conjunction with HSD 2 to provide a noise immune interface to the high side driver.

Pin 7:
N/C.

Pin 8:
V_{DD} supplies power to the logic and drivers.

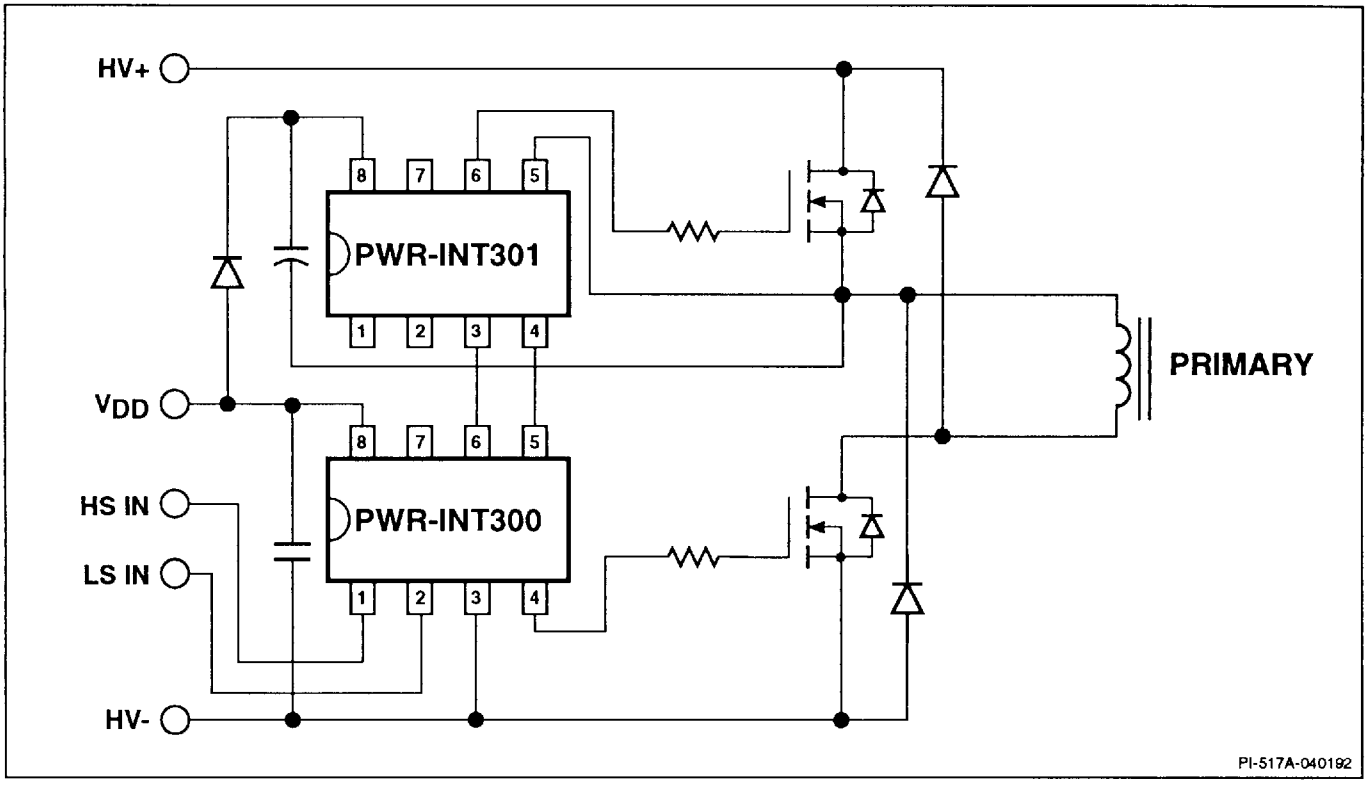


Figure 4. PWR-INT300 and PWR-INT301 driving a Two Transistor Forward Converter

ABSOLUTE MAXIMUM RATINGS[1]

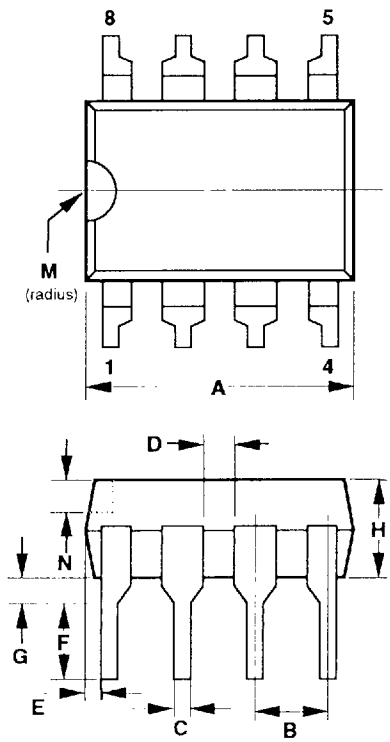
HSD1/HSD2 Voltage	800 V
HSD1/HSD2 Slew Rate	10 V/ns
V_{DD} Voltage	22 V
Logic Input Voltage	-0.3V to 5.5 V
Storage Temperature	–65 to 165°C
Ambient Temperature	-40 to 85°C
Junction Temperature	150°C
Lead Temperature[2]	260°C
Power Dissipation	1.0 W
Thermal Impedance (θ_{JA})	100°C/W

1. Unless noted, all voltages referenced to COM, T_A = 25°C
2. 1/16" from case for 5 seconds.

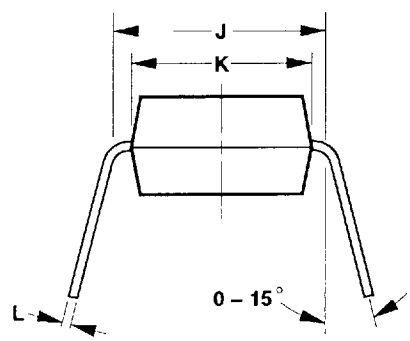
Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{DD} = 20 V, COM = 0V, T_A = -40 to 85°C	Limits			Units
			MIN	TYP	MAX	
LOGIC						
Input Current, High or Low	I_{IH}, I_{IL}		-20		20	µA
Input Voltage High	V_{IH}		3.5			V
Input Voltage Low	V_{IL}				1.5	V
HSD OUTPUTS						
Breakdown Voltage	BV_{DSS}		800			V
Off-State Output Current	I_{DSS}	V_{HSD1}, V_{HSD2} = 500 V		1		µA
On-State Output Current	$I_{D(ON)}$	V_{HSD1}, V_{HSD2} = 10 V	5			mA
Output Capacitance	C_{OSS}	V_{HSD1}, V_{HSD2} = 25 V		10		pF
Slew Rate	dV/dt			10		V/ns
LS OUT						
Output Voltage, High	V_{OH}	I_o = -65 mA	V_{DD}-1.0			V
Output Voltage, Low	V_{OL}	I_o = 130 mA			1.0	V
Output Short Circuit Current	I_{OS}	V_o = 0V			-0.5	A
		V_o = V_{DD}	1			
Propagation Delay Time	t_{PLH}, t_{PHL}				200	ns
Rise Time	t_r	C_L = 1000 pF		50		ns
Fall Time	t_f	C_L = 1000 pF		25		ns

Specification	Symbol	Test Conditions, Unless Otherwise Specified: V_{DD} = 20 V, COM = 0V, T_A = -40 to 85°C	Limits			Units
			MIN	TYP	MAX	
SYSTEM RESPONSE						
Matching (Low On to High On)	Mt_{P+}	High t_{PHL} - Low t_{PHL}			50	ns
Matching (Low Off to High Off)	Mt_{P-}	High t_{PLH} - Low t_{PLH}			50	ns
UNDERVOLTAGE LOCKOUT						
Undervoltage Threshold	V_{UV}		8.5	9.25	10	V
Undervoltage Hysterisis	V_{UH}		0.75		1.55	V
SUPPLY						
Supply Current	I_{DD}	V_{DD} = 20V		1.1		mA
Supply Voltage	V_{DD}		10		20	V

DIM	inches	mm
A	.395 MAX	10.033 MAX
B	.090-.110	2.286-2.794
C	.015-.021	.381-.533
D	.040 TYP	1.016 TYP
E	.010-.040	.254-1.016
F	.125 MIN	3.175 MIN
G	.020 MIN	.508 MIN
H	.125-.135	3.175-3.429
J	.300-.320	7.620-8.128
K	.245-.255	6.223-6.477
L	.009-.015	.229-.381
M	.030-.110	.762-2.794
N	.020 TYP	.508 TYP



8-Pin Plastic DIP
PF Suffix



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