MN373

LOW-COST
HIGH-RESOLUTION
TRACK-HOLD AMPLIFIER

MICRO NETWORKS

FEATURES

- **Low Cost**
- **Compatible with All DIP Packaged 14-16 Bit A/D's**
- **10μsec Max Acquisition Time (10V Step to ±0.003%)**
- **1nsec Aperture Jitter**
- **±0.25μV/μsec Max Droop**
- **±1mV Max Offset Error**
- **84dB Feedthrough Attenuation**
- **Full Mil Operation −55°C to +125°C**
- **MIL-H-38534 Screening Optional. MIL-STD-1772 Qualified Facility**

DESCRIPTION

MN373 is a high-resolution, moderately high-speed, track-hold (T/H) amplifier designed to be compatible with all DIP packaged 14-16 bit A/D converters available today. Some of the performance specifications that make MN373 ideal for high-resolution applications are summarized below:

Specification	Typ.	Max.	Units
Gain Linearity Error	±0.001	±0.003	%FSR
Gain Accuracy	±0.003	±0.01	%
Gain Drift	±0.25	±1	ppm/°C
Offset Voltage	±0.25	±1	mV
Offset Drift	±3	±20	μV/°C
Output Droop Rate	±0.05	±0.25	μV/μsec
Feedthrough Attenuation	84		dB

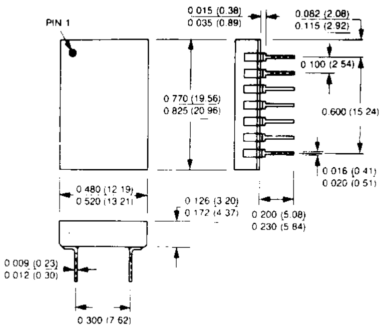
Dynamic specifications include 10μsec maximum acquisition time (for a 10V step acquired to ±0.003%), 1nsec aperture jitter and 400kHz small signal bandwidth. MN373's outstanding ±0.25μV/μsec maximum output droop rate enables the device to hold signals to the 14-bit level for up to 2.4msec and to the 16-bit level for up to 600μsec. This makes MN373 ideal for high-resolution simultaneous-sampling applications.

MN373 is packaged in a standard, 14-pin, ceramic dual-in-line and is TTL compatible. The device contains an uncommitted, high-impedance (5MΩ), input buffer amplifier that enables it to be used in numerous inverting and noninverting configurations with and without gain. The input stage has a CMV of ±10V; a CMRR of 72dB minimum; and an input bias current guaranteed not to exceed ±300nA. Required power supplies are ±15V, and maximum power consumption is 390mW.

The standard MN373 is fully specified for 0°C to +70°C (ambient) operation; with MN373H fully specified for −55°C to +125°C (ambient) operation. MN373H/B CH includes 100% screening to MIL-H-38534.

MN373 mates directly with Micro Networks MN5280/82, MN5290/91 and MN5295/96 16-bit A/D converters. For military/aerospace applications, MN373H/B can be mated with MN5290H/B to configure a full 16-bit digitizer with a 20kHz sampling rate, a 10kHz analog bandwidth, and guaranteed 14-bit no missing codes from −55°C to +125°C. With MN5295, it forms a 33kHz digitizer.

14 PIN DIP



Dimensions in Inches (millimeters)

MN373

MICRO NETWORKS
324 Clark St., Worcester, MA 01606 (508) 852-5400

May 1988

MN373 LOW-COST HIGH-RESOLUTION T/H AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

Operating Temperature Range	−55°C to +125°C
Specified Temperature Range:	
MN373	0°C to +70°C
MN373H, MN373H/B	−55°C to +125°C
Storage Temperature Range	−65°C to +150°C
+15V Supply (+V_{CC}, Pin 9)	−0.5 to +18 Volts
−15V Supply (−V_{CC}, Pin 5)	+0.5 to −18 Volts
Analog Input Voltage (Pins 1 and 2)	±15 Volts
Differential Input Voltage (Pin 1 to Pin 2)	±20 Volts
Digital Input (Pin 14)	−0.5 to +7 Volts
Output Current (Note 1)	±20mA

ORDERING INFORMATION

PART NUMBER — **MN373H/B CH**

Standard part is specified for 0°C to +70°C operation.

Add "H" for specified −55°C to +125°C operation.

Add "/B" to "H" models for Environmental Stress Screening.

Add "CH" to "/B" models for 100% screening according to MIL-H-38534.

SPECIFICATIONS (T_A = +25°C, Supply Voltages = ±15V, C_H = Internal, Load = 1kΩ//50pF unless otherwise indicated)

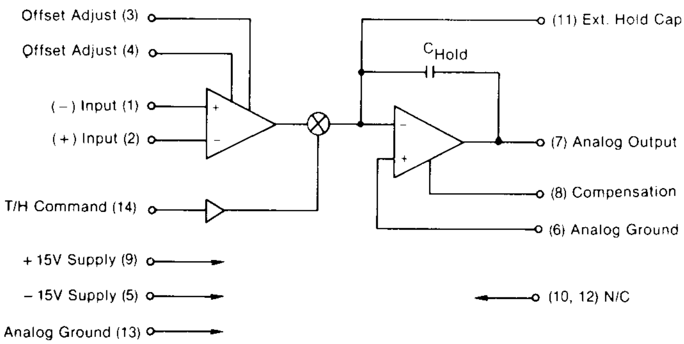
ANALOG INPUT/OUTPUT	MIN.	TYP.	MAX.	UNITS
Input/Output Voltage Range	±10	±11		Volts
Input Resistance		5		MΩ
Input Capacitance		3		pF
Input Bias Current: Initial (+25°C)		±100	±300	nA
Over Temperature		±200	±500	nA
Input Offset Current: Initial (+25°C)		±30	±300	nA
Over Temperature		±60	±500	nA
Common Mode Voltage Range	±10			Volts
CMRR	72	90		dB
Output Current (Note 1)	±10			mA
Output Resistance (Hold Mode)		1		Ω
Maximum Capacitive Load		250		pF
Output Noise (d.c. to 10MHz): Track Mode		150		μV(rms)
Hold Mode		150		μV(rms)
DIGITAL INPUTS				
Logic Levels: Logic "1" (Hold Mode)	+2			Volts
Logic "0" (Track Mode)			+0.8	Volts
Loading: Logic "1"			+10	μA
Logic "0"			−10	μA
TRANSFER CHARACTERISTICS (Note 4)				
Open Loop Gain (d.c.)	10^6	2×10^6		V/V
Gain Accuracy (G = +1)		±0.003	±0.01	%
Gain Linearity Error (Note 2)		±0.001	±0.003	%FSR
Offset Voltage (Track Mode)		±0.25	±1	mV
Pedestal (Note 3)		±0.5	±2	mV
Stability: Gain Drift		±0.25	±1	ppm/°C
Offset Drift (Track Mode)		±3	±20	μV/°C
Pedestal Drift		±10		μV/°C
DYNAMIC CHARACTERISTICS				
Acquisition Time:				
10V Step to ±0.003% (±0.3mV)		8.5	10	μsec
10V Step to ±0.006% (±0.6mV)		8	9.5	μsec
10V Step to ±0.01% (±1mV)		7.5	9	μsec
Track-to-Hold Transient Settling Time:				
to ±0.003%FS (±0.3mV)		250		nsec
to ±0.006%FS (±0.6mV)		225		nsec
to ±0.01%FS (±1mV)		200		nsec
Track-to-Hold Transient		25		mVp-p
Aperture Delay Time		30		nsec
Aperture Jitter		1		nsec
Output Slew Rate		±10		V/μsec
Small Signal Bandwidth (−3dB, G = +1)		400		kHz
Output Droop Rate: +25°C		±0.05	±0.25	μV/μsec
0°C to +70°C		±3	±7.5	μV/μsec
−55°C to +125°C ("H" Models)		±10	±20	μV/μsec
Feedthrough Attenuation (10kHz, 10Vp-p input)		84		dB

POWER SUPPLIES	MIN.	TYP.	MAX.	UNITS
Voltage Range (Note 5)	± 14.5	± 15	± 16	Volts
Power Supply Rejection: + 15V Supply − 15V Supply		± 0.1 ± 0.4		mV/V mV/V
Current Drain: + 15V Supply − 15V Supply		10 − 10	13 − 13	mA mA
Power Consumption		300	390	mW

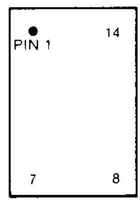
SPECIFICATION NOTES

1. The MN373's output is not short-circuit protected, and shorts to ground or either supply will result in destruction. In normal operation, continuous output current should not exceed ± 10mA.
2. FSR stands for Full Scale Range and is equal to 20 volts for the MN373. ± 0.003%FSR is equivalent to ± ½ LSB for a 14-bit system.
3. Pedestal refers to the unwanted step in output voltage that occurs as a T/H is switched from the track to the hold mode. For many T/H's pedestal amplitude is a function of input/output voltage level. For the MN373, pedestal is constant regardless of input/output level. It will vary as a function of the user-optional external hold capacitor, however.
4. Gain Accuracy, Gain Linearity, Offset Voltage, Pedestal and their respective drifts are specified for the MN373 in the follower (G = + 1) configuration.
5. MN373 will operate with ± V_{CC} supplies down to ± 10.5V if input/output voltage is kept below ± 7.5V.

BLOCK DIAGRAM



PIN DESIGNATIONS



1 (−) Input	14 T/H Command
2 (+) Input	13 Ground
3 Offset Adjust	12 N/C
4 Offset Adjust	11 External Hold Cap
5 − 15V Supply	10 N/C
6 Ground	9 + 15V Supply
7 Analog Output	8 Compensation

APPLICATIONS INFORMATION

LAYOUT CONSIDERATIONS—Proper attention to layout and decoupling is necessary to obtain specified accuracy and speed performance from the MN373. The unit's two Ground pins (pins 6 and 13) are not connected to each other internally. They should be tied together as close to the unit as possible and both connected to system analog ground, preferably through a large analog ground plane underneath the package. If p.c. card ground lines must be run separately, wide conductor runs should be used with 0.01μF ceramic capacitors interconnecting them as close to the package as possible. If your system distinguishes between analog signal and analog power gounds, pin 6 may be connected to system signal ground and pin 13 to system power ground.

Coupling between analog inputs and digital signals should be minimized to avoid noise pick-up. Care should be taken to avoid long runs or analog runs close to digital lines.

Power supply connections should be short and direct, and all power supplies should be decoupled with high-frequency bypass capacitors to ground. 1μF tantalum capacitors in parallel with 0.01μF ceramic capacitors are the most effective combination. Single 1μF ceramic capacitors can be used if necessary to save board space.

If external hold and compensation capacitors are used, they should be located as close to the MN373 as possible. If these capacitors are not used, pins 8 and 11 should be left open.

DESCRIPTION OF OPERATION—MN373 consists of a high-speed transconductance amplifier, an analog switch, a hold capacitor and a high-speed output integrating amplifier. With uncommitted inverting input, noninverting input and analog output terminals, MN373 operates as an uncommitted op amp whose output level can be held constant with the application of a digital control signal. The use of external resistors enables one to configure the MN373 in any number of inverting and noninverting configurations with and without gain.

The most popular use of the MN373 is as a noninverting, unity-gain track-hold amplifier. This is achieved by connecting pin 1 (Inverting Analog Input) to pin 7 (Analog Output) and applying the analog input signal to pin 2 (Noninverting Analog Input). In this configuration, with a logic "0" applied to pin 14 (T/H Command), the MN373's output will track its input. When a logic "1" is applied to pin 14, the

MN373 is driven into the hold mode holding its output constant at the value that appeared when the hold command was given.

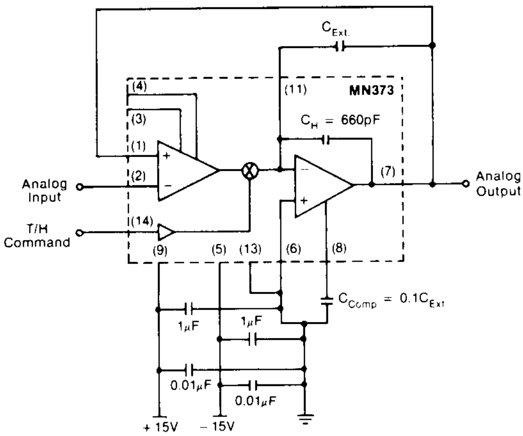


Figure 1. MN373 configured as a follower (G = +1) with additional hold capacitance.

MN373 was specifically designed for use with Micro Networks MN5290, MN5291 and MN5282 16-bit, DIP packaged, A/D converters, and its output droop rate is slow enough to hold a given analog sample to required accuracy while those devices perform a conversion. If slower droop rates are required, the MN373 can accept additional hold capacitance applied to pin 11. A later section describes this operation in detail.

MN373 can have its track mode offset error or the effect of its pedestal reduced to zero with the use of an external potentiometer. This is also described in detail in a later section.

ADDITIONAL HOLD CAPACITANCE—MN373 has an internal 660pF hold capacitor and published performance specifications are based on this capacitor. If one wishes to reduce droop rate or pedestal amplitude while trading off acquisition time, additional hold capacitance may be added between pins 11 (External Hold Cap) and 7 (Analog Output). The hold capacitor should have high insulation resistance and low dielectric absorption, to minimize droop errors. Polystyrene dielectric is a good choice for operating temperatures up to +85°C. Teflon and glass dielectrics offer good performance to +125°C and above. Whenever additional hold capacitance is used, additional compensation capacitance equal to one-tenth the additional hold capacitance must be connected between pin 8 (Compensation) and ground. Exact value and type for this capacitor are not critical.

OFFSET ADJUSTMENT—MN373's track-mode offset error can be reduced to zero using a 20kΩ potentiometer connected between pins 3 and 4 with its wiper connected to −15V. With the analog signal path grounded, the pot should be adjusted until the output equals zero volts. The pot can also be used to compensate for the effects of pedestal by performing the adjustment in the hold mode. This adjustment is normally made while continually switching from track to hold and observing the T/H output on a scope. This procedure will eliminate adjustment ambiguities resulting from output droop.

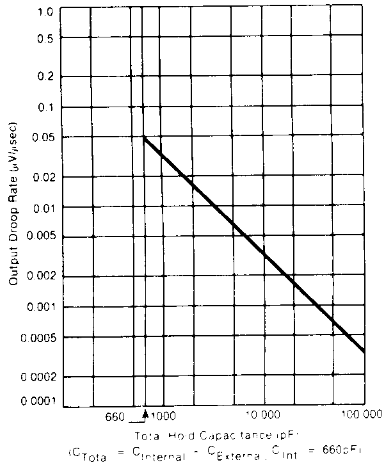


Figure 2. Output Droop Rate v.s. Hold Capacitance

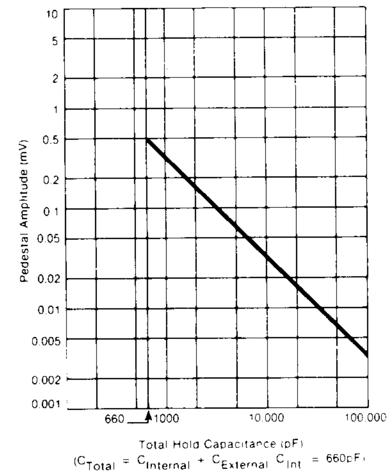


Figure 3. Pedestal Amplitude v.s. Hold Capacitance

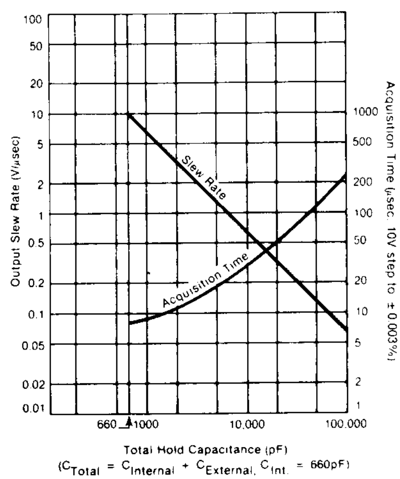


Figure 4. Slew Rate and Acquisition Time v.s. Hold Capacitance

USING MN373 WITH SUCCESSIVE APPROXIMATION A/D CONVERTERS— Successive approximation (SA) type A/D converters are oftentimes severely analog-input-signal slew-rate and bandwidth limited and can easily produce errors when used to digitize dynamically changing signals. The input-signal bandwidth limitations arise from the fact that successive approximation type A/D's sequentially determine output-bit values (from MSB to LSB) by comparing the analog equivalent of output bits already determined to the instantaneous analog input signal. The conversion process assumes the analog input signal remains "constant", and analog-input slew-rate and bandwidth limitations derive from the requirement that input signals not change more than ± ½LSB (for the appropriate resolution) during the conversion period.

$$\text{Input Slew Rate Limit} = \frac{\pm \frac{1}{2}\text{LSB}}{\text{Conversion Time}}$$

$$\text{Input Bandwidth}^{*} = \frac{\pm \frac{1}{2}\text{LSB}}{(\text{Conv. Time})\,(2\pi)\,(\text{FSR}/2)}$$

$$\text{Input Bandwidth}^{*} = \frac{(\text{FSR}/2^{n+1})}{(\text{Conv. Time})\,(2\pi)\,(\text{FSR}/2)}$$

*For full scale sine waves

FSR = A/D converter full scale range

n = resolution in bits

These A/D converter input-bandwidth limitations can be greatly overcome by using track-hold (T/H) amplifiers to track and subsequently "freeze" (hold) analog input signals that are changing too rapidly for the A/D alone to accurately digitize. If other parameters are appropriate, the slew-rate and bandwidth limiting factor of the T/H-A/D combination will be the T/H's aperture jitter (aperture uncertainty) specification, and the T/H-A/D combination will now be able to accurately sample and digitize signals slewing as much as ± ½LSB during the T/H's aperture jitter time. The formulas for determining how fast a signal a given T/H can accurately capture when used in conjunction with a given A/D converter are the same as those stated above with ± ½LSB defined for the A/D converter and with the variable (conversion time) replaced by (aperture jitter). Needless to say, aperture jitter is a significantly smaller number than conversion time, and the bandwidth improvement when using the T/H v.s. not using the T/H will equal the ratio of A/D conversion time to T/H aperture jitter.

As an example, consider Micro Networks MN5290 16-bit A/D converter. This device guarantees "no missing codes" to the 14-bit level, and it performs a 14-bit conversion in 40μsec (maximum). For this device operating on its full ±10V input voltage range, ± ½LSB (for 14 bits) is equivalent to ±0.61mV, and the analog input slew-rate limitation is equal to ± ½LSB/conversion time = ±0.61mV/40μsec = ±0.015mV/μsec. This is equivalent to the highest slew rate encountered in a full-scale (±10V) sine wave with a frequency of 0.24Hz. When used in conjunction with MN5290, MN373, with its 1nsec aperture jitter, is capable of capturing signals (to 14-bit accuracy) with slew rates up to ± ½LSB/aperture jitter = ±0.61mV/nsec = 610mV/μsec. This is the highest slew rate one would encounter in a full-scale sine wave with a frequency of 9.7kHz. As expected, the improvement ratio of 9.7kHz to 0.24Hz is equal to the ratio of 40μsec to 1nsec.

Using T/H's in conjunction with A/D's to increase analog bandwidth will reduce throughout (conversion rate) in that new digital output data cannot be realized until after the T/H has acquired a new signal (acquisition time) and the A/D has converted it (conversion time). Another consideration when calculating T/H-A/D throughput is the T/H's Track-To-Hold Transient Settling Time. If the same timing pulse is used to put the T/H into the hold mode and initiate the A/D conversion, the transient settling time has to be short enough to ensure that the A/D has a stable, accurate input when it makes the final decision on whether its MSB output should be a "I" or "0". This decision normally takes place one clock period after a conversion has begun.

In the case of using MN373 with MN5290, the A/D's MSB is not set to its final value until approximately 2.5μsec after a conversion has begun, and MN373's track-to-hold transient has long since died away. When using faster A/D's, a delay may have to be added between the time the T/H goes into hold and the A/D begins converting with the consequence that throughput suffers.

Returning to the MN373-MN5290 combination, the throughput time will be 50μsec (10μsec acquistion time plus 40μsec conversion time), and the conversion rate will be 20kHz. Comparing this to the 9.7kHz analog bandwidth leads one to conclude that the MN373-MN5290 pair is capable of "Nyquist digitizing" 9.7kHz sine waves at a 19.4kHz rate while guaranteeing true 14-bit resolution.

Other considerations when using T/H's with successive approximation A/D's involve the T/H's output stage. In the hold mode, it should exhibit a very low output impedance compared to the A/D's input impedance (usually 1 to 10kΩ) at frequencies up to five times the A/D's clock frequency. Also, the T/H should be able to fully recover (to ± ½LSB) from current transients in a time interval smaller than the A/D's clock period. These requirements are based on the fact that as a successive approximation A/D's internal D/A converter changes its output current just prior to the determination of each output bit, the T/H will be required to sink or source high frequency current transients and recover within one clock period. The MN373's output is not current limited, and in the hold mode, output impedance is typically below 1Ω. It recovers from output current transients (to ±0.003%FS) in less than 1μsec.

In most applications using MN373 in front of a successive approximation A/D converter, MN373's T/H Command pin can be driven directly (or inverted if necessary) from the converter's status output. The status output changes state when the converter receives a convert command, and this change can drive the T/H from the track to the hold mode. The change in state of the A/D's status output at the end of the conversion can put the T/H back into the track mode. The diagram below illustrates an MN373 mated with an MN5290 in this manner. Since MN5290's MSB output is not set to its final value until one clock period (approximately 2.8μsec) after a conversion begins, MN373's track-to-hold transient will be completely settled, and no extra timing precautions are necessary.

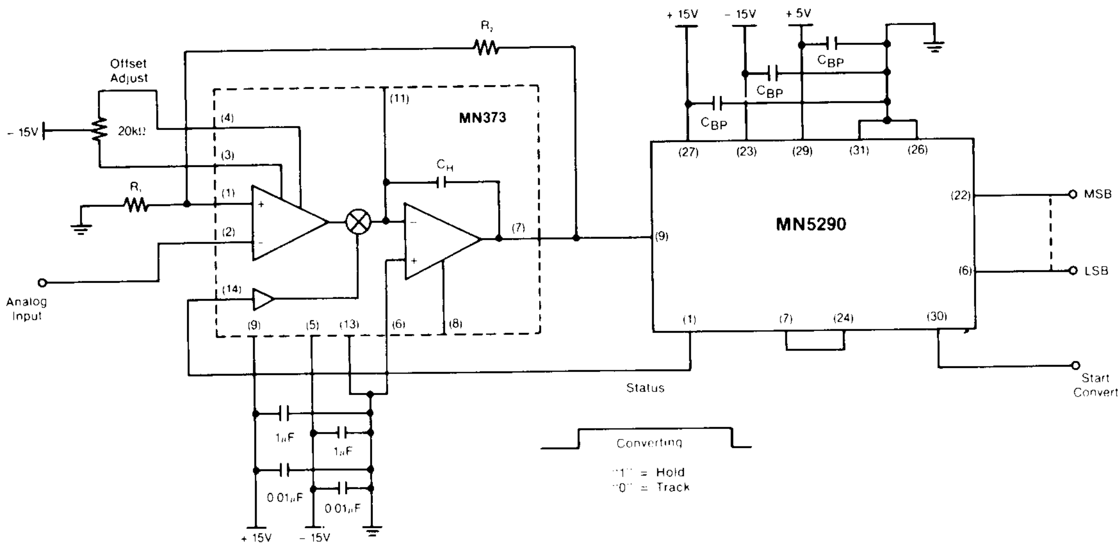


Figure 5. Combine MN373 with MN5290 to make a 14-bit digitizer with a 20kHz update rate, a 10kHz analog-signal bandwidth, and 14-bit no missing codes guaranteed over temperature.

USING MN373 TO DEGLITCH HIGH-RESOLUTION CURRENT-OUTPUT D/A CONVERTERS—Virtually all digital-to-analog (D/A) converters exhibit output transients, affectionately know as glitches, when changing output levels in response to digital-input code changes. The primary causes of glitches are unequal digital-data arrival and delay times, know as data skew, and asymmetrical switch turn-on and turn-off times. The largest glitches occur when major-carry code changes are made. In particular, the worst-case glitch occurs at half scale when the input-code change is from 0111...1 to 1000...0 or vice versa. Asymmetrical switch turn-on and turn-off delays may result in momentary slewing to the 0000...0 or 1111...1 output level until all switches achieve their final state. The binarily-weighted nature of the current switches internal to most D/A converters makes glitch slew rate and amplitude vary from transition to transition, and consequently makes glitches extremely difficult to remove with filtering. D/A converter output glitches may or may not be a problem depending upon application. In long time-constant servo applications, they will not be a problem. In high-speed, high-resolution waveform generators, they can cause severe harmonic distortions.

A deglitcher is a specially designed T/H amplifier capable of considerably reducing D/A glitch amplitude and, perhaps more importantly, making all glitches the same regardless of digital-code change. MN373 works well as a deglitcher because it has a small 25mV switching transient, and if it used to deglitch a current-output D/A, it can also act as an output amplifier supplying current-to-voltage conversion.

A T/H amplifier used as a deglitcher is connected to the output of the D/A and is kept in the track mode whenever the D/A output is stable. Just prior to the arrival of new digital data, the T/H is commanded to the hold mode to hold its output constant while the D/A's output (the T/H's input) is changing levels and experiencing its glitches. The T/H is then put back into the track mode to acquire and track the new D/A output.

The diagram on the next page illustrates MN373 performing both deglitching and current-to-voltage conversion for a current-output, 16-bit D/A converter (MNDAC71-COB-I). MN373's high-impedance input buffer allows the current-output D/A to work into a virtual ground, and the D/A's internal feedback resistor is put into MN373's feedback loop. The 16-bit D/A guarantees ±0.003%FSR maximum linearity error, and MN373's linearity error is commensurate. MN373's ±10mA minimum output current is enough to drive the feedback resistor and the load. MN373's acquisition time is equal to the D/A's settling time when used without a deglitcher so update rate is not compromised. MN373's outstanding feedthrough attenuation ensures that very little of the actual D/A glitch feeds through to the T/H output, and the unit's low output droop rate ensures that output change will be less than ±2.5μV during the approximately 10μsec that MN373 is in the hold mode.

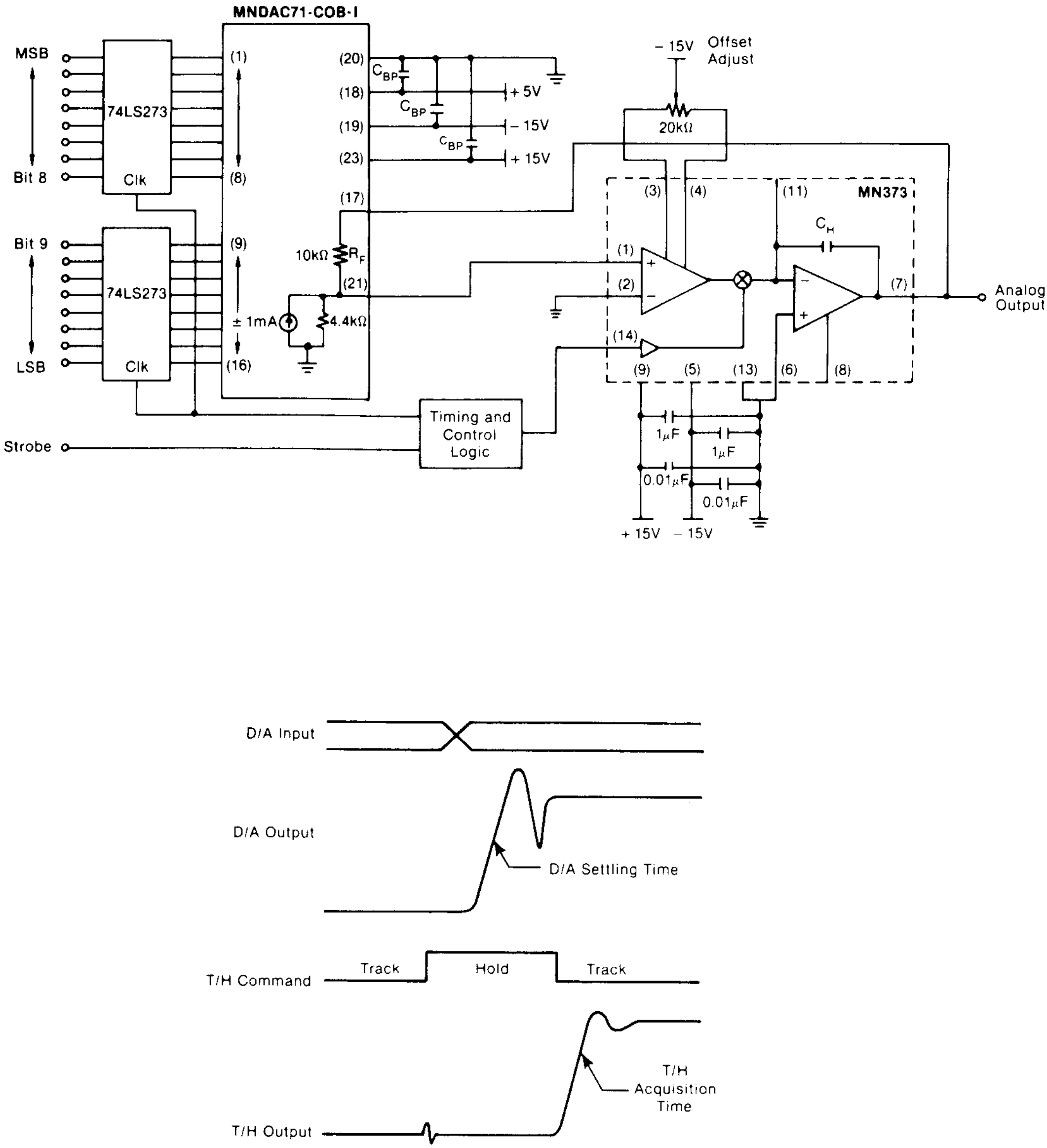
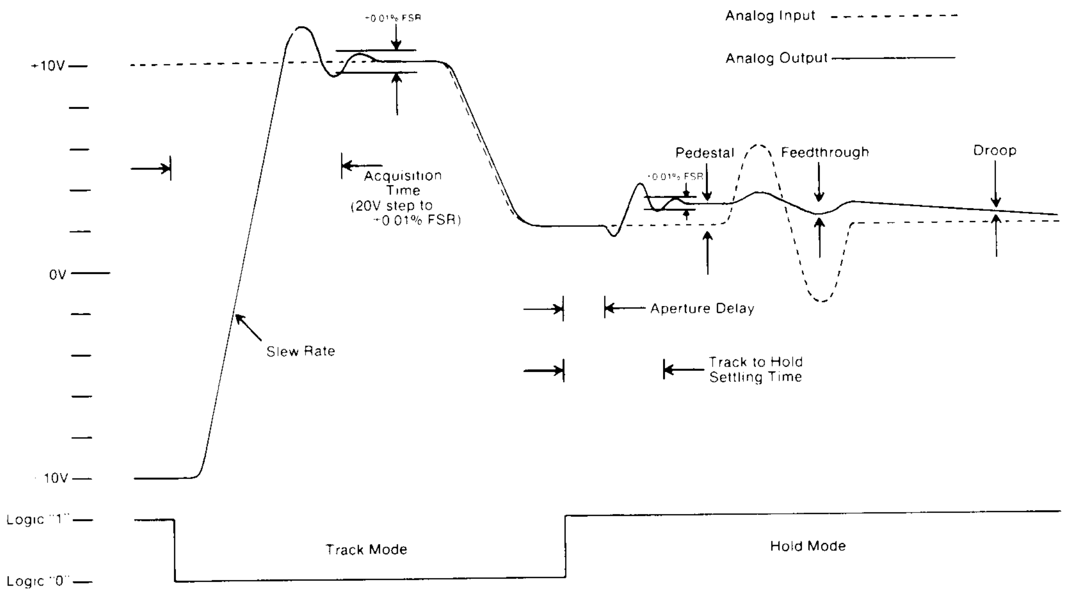


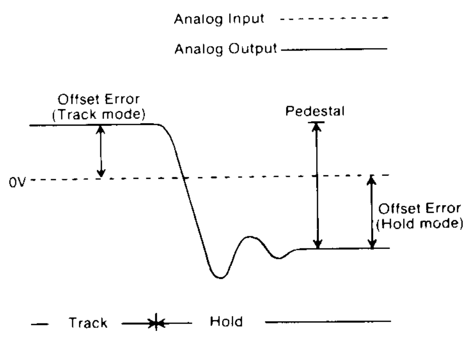
Figure 6. Use MN373 with high-resolution current-output D/A converters to perform both current-to-voltage conversion and output deglitching.

MN373

SUMMARY OF TRACK·HOLD PERFORMANCE PARAMETERS



Summary of T/H specifications. The broken line is the T/H's analog input. The solid line shows its analog output. The T/H has a ± 10V analog input range. The lower trace is the digital T/H command signal. A logic "0" puts the T/H into the track mode. A logic "1" puts it into the hold mode. See the tutorial section of the Micro Networks catalog for a detailed discussion of T/H performance specifications.



Summary of Offset (Track Mode), Offset (Hold Mode) and Pedestal Errors. Broken line is T/H analog input. Solid line is analog output. Analog input level equals zero volts.

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