Data Sheet
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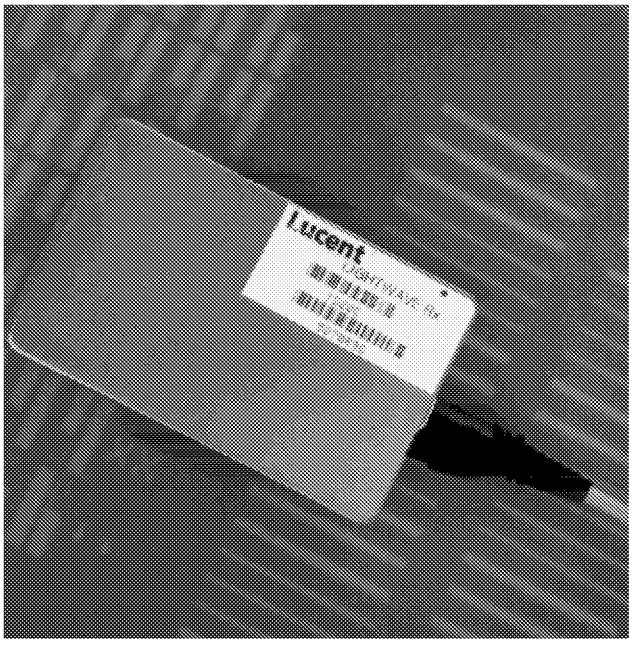
microelectronics group

Lucent Technologies
Bell Labs Innovations

1320-Type Lightwave Receiver with Clock Recovery and Data Retiming for 2488.32 Mbits/s Applications



Features

- Differential ECL-compatible data and clock outputs
- Low power dissipation
- APD and PIN versions available
  — Typical sensitivity: –32 dBm with APD
  –23 dBm with PIN
- >25 dB typical dynamic range
- Operation at 1.3 µm or 1.55 µm wavelength
- TTL link status flag
- 0 °C to 65 °C operating case temperature range
- Space-saving, self-contained, 24-pin DIP
- Lucent Technologies Microelectronics Group's Reliability and Qualification Program for built-in quality
- SONET/SDH compatible for OC-48/STM-16 data rate and ATM

Applications

- Telecommunications
  — Inter- and intraoffice SONET/SDH and ATM
  — Subscriber loop
  — Metropolitan area networks
- High-speed data communications

Description

The 1320-Type 2.5 Gbits/s Lightwave Receiver is designed for use in SONET OC-48 and synchronous digital hierarchy (SDH) STM-16 telecommunications applications and high-speed data communications applications. The receiver converts received optical signals in the range of 1.2 µm to 1.6 µm wavelength into differential ECL-compatible data and clock outputs. The receiver consists of either an InGaAs APD or PIN photodetector (depending on model selected), a GaAs preamplifier, and a silicon bipolar clock and data recovery IC (CDR). The CDR uses PLL technology to extract the clock signal from the converted optical signal. A TTL compatible link status flag signal indicates when there is a loss of optical signal.

The receiver is manufactured in a low-profile, pigtailed, 24-pin DIP package. It requires +5.0 V and –5.2 V power supplies. The APD version also requires a positive, temperature-compensated, high-voltage (~60 V) bias supply for biasing the APD.

Flag Output

When the incoming optical signal falls below the link status switching threshold, the FLAG output is asserted and the FLAG output logic level changes from a TTL low to a TTL high.

Pin Information

Pin	Name	Pin	Name
1	V_{PD}	24	Thermistor‡
2	No connect*	23	No connect*
3	FLAG†	22	V_{CC}
4	Ground	21	No connect*
5	$\overline{\text{CLOCK}}$	20	Ground
6	CLOCK	19	Ground
7	Ground	18	V_{EE}
8	Ground	17	Ground
9	Ground	16	Ground
10	DATA	15	Ground
11	$\overline{\text{DATA}}$	14	Ground
12	Ground	13	Ground

* Pins designated as no connect are connected internally. The user should not make any connections to these pins!

† The FLAG output is a logic level that indicates the presence or absence of a minimum acceptable level of optical input. A TTL logic HIGH indicates the absence of a valid optical input signal.

‡ The thermistor is not available on the PIN version of the receiver.

Handling Precautions

The 1320 receiver is manufactured with a 39 in. ± 4 in. (100 cm ± 10 cm) single-mode fiber pigtail with a 1.6 mm OD PVC outer jacket. The standard optical connector is an ultrapolished FC-PC connector. Other optical connector options are available on special order. Please contact a Microelectronics Group Account Manager for availability and ordering information.

The minimum fiber bending radius is 1.5 in. (38 mm).

Electrostatic Discharge

CAUTION: This device is susceptible to damage as a result of electrostatic discharge (ESD). Take proper precautions during both handling and testing. Follow guidelines such as JEDEC Publication No. 108-A (Dec. 1988).

Although protection circuitry is designed into the device, take proper precautions to avoid exposure to ESD.

Lucent Technologies employs a human-body model (HBM) for ESD-susceptibility testing and protection design evaluation. ESD voltage thresholds are dependent on the critical parameters used to define the model. A standard HBM (resistance = 1.5 kΩ, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes.

Receiver Processing

The 1320-Type receiver devices can withstand normal wave soldering processes. The complete receiver module is not hermetically sealed; therefore, it should not be immersed in or sprayed with any solutions. The optical connector process cap deformation temperature is 85 °C. The receiver pins can be wave soldered at 250 °C for 10 seconds.

Installation Considerations

Although the receiver has been designed with ruggedness in mind, care should be used during handling. The optical connector should be kept free from dust. The optical connector process cap should be kept in place as a dust cover when the device is not connected to a cable. If contamination is present on the optical connector, the use of canned air with an extension tube should remove any loose debris. Other cleaning procedures are outlined in the *Cleaning Fiber-Optic Assemblies* Technical Note (TN95-010LWP).

The 1320 receiver has been subjected to a fiber pull mechanical strength test as part of device qualification (see Qualification Testing Section). However, the cable should be handled conservatively with no excessive axial pulling or lateral tugging.

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability

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Parameter	Symbol	Min	Max	Unit
Operating Case Temperature	T_C	0	65	°C
Storage Temperature	T_{stg}	–40	85	°C
Optical Input Power*:				
APD	P_{IN}	—	3	dBm
PIN	P_{IN}	—	8	dBm
Supply Voltages	V_{EE}	–6.5	0	V
	V_{PIN}	0	10	V
	V_{APD}	0	V_{BR}	V
	V_{CC}	0	6.5	V
Lead Soldering Temperature/Time	—	—	250/10	°C/s

* Under biased conditions. Unbiased, the maximum input power for both devices is 6 dBm.

Characteristics

Table 1. Optical Characteristics

At 1.3 µm wavelength and 1 x 10^{-10} BER with $2^{23} – 1$ NRZ pseudorandom data.

Parameter	Symbol	Min*	Typ†	Max*	Unit
Measured Average Sensitivity:					
APD	P_{INMIN}	—	–32	–30	dBm
PIN	P_{INMIN}	—	–23	–21	dBm
Maximum Input Power:					
APD	P_{INMAX}	–9	–8	—	dBm
PIN	P_{INMAX}	0	1	—	dBm
Link Status Switching Threshold‡ Decreasing Light Input:					
APD	LSTD	–45	–40	–35	dBm
PIN	LSTD	–35	–30	–25	dBm
Flag Response Time	—	3	—	1000	µs

* Over operating temperature range and at end of life.
† Typical values at room temperature and beginning of life.
‡ The received data BER will exceed 1 x 10^{-3} when the flag switches. There is less than 0.2 dB of hysteresis in the switching level. However, due to the design of the receiver circuitry, the flag output is guaranteed not to chatter.

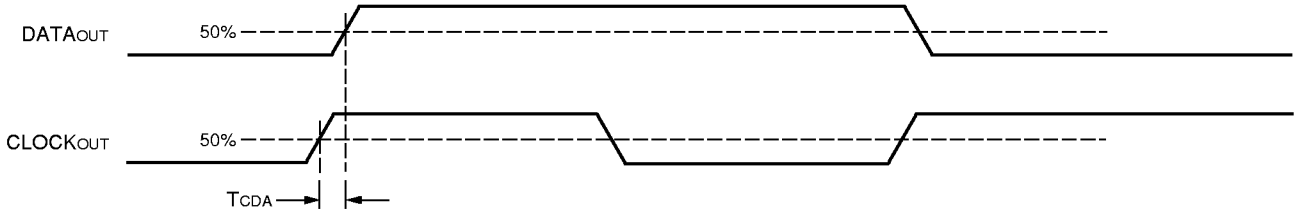

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Figure 1. Clock/Data Alignment

Characteristics (continued)

Table 2. Electrical Characteristics

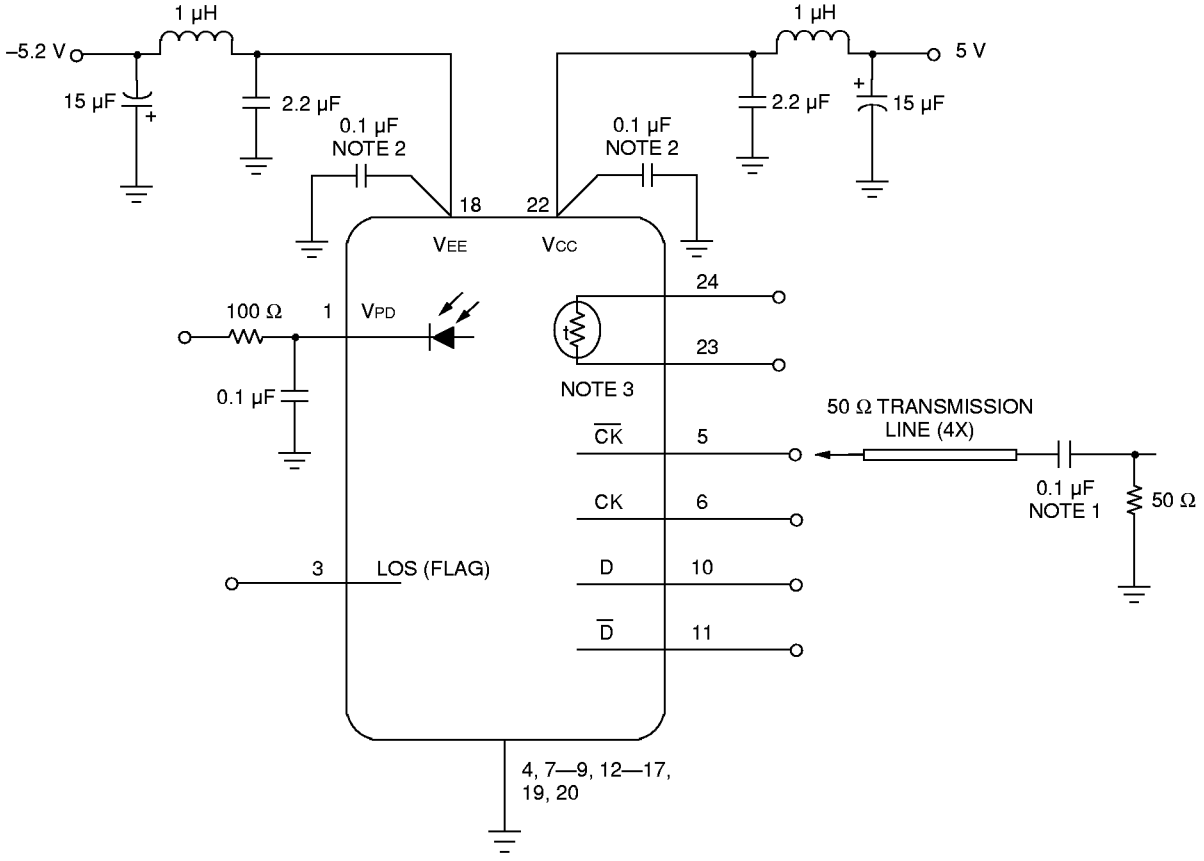
Parameter	Symbol	Min	Typ[1]	Max	Unit
Bit Rate	—	2488.07	2488.32	2488.57	Mbits/s
dc Power Supply Voltages:					
Receiver Bias	V_{CC}	4.75	5.0	5.25	V
Receiver Bias	V_{EE}	–4.94	–5.2	–5.46	V
APD Bias (1320M Types)[2]	V_{APD}	—	—	65	V
PIN Bias (1320P Types)[3]	V_{PIN}	0	5	10	V
dc Power Supply Currents	I_{CC}	—	200	275	mA
	I_{EE}	—	240	290	mA
	I_{APD}	—	—	4	mA
	I_{PIN}	—	—	4	mA
Data/Clock Rise and Fall Time	t_R/t_F	—	—	200	ps
Data/Clock Return Loss[4]	S_{22}	—	—	–8	dB
Output Data/Clock Voltage:[5]	V_O	600	700	800	mVp-p
Output Flag Voltage:[6]					
High	V_{FOH}	4.0	4.5	Vcc	V
Low	V_{FOL}	0	0.5	1.0	V
Clock/Data Alignment[7]	t_{CDA}	—	0	±40	ps
Clock Duty Cycle	—	45	50	55	%
Clock Output Random Jitter @ 2.5 Gbits/s[8]	J_C	—	—	3.6	° rms
Output Clock Jitter Transfer Peaking[9]	J_P	—	—	<0.1	dB
Jitter Tolerance	Bellcore GR-253-CORE and ITU-T G.958 Compliant				

1. Typical values measured at room temperature and beginning of life.
2. The gain = 12 APD bias voltage at 25 °C is supplied with each device. For optimum performance, V_{APD} must be set to within 100 mV of the specified value. V_{APD} needs to be temperature compensated to maintain constant gain over the operating temperature range. The nominal compensation is 0.18%/°C.
3. To obtain maximum overload input power, V_{PIN} must be biased to a positive voltage (5 V nominal). If a lower overload input power can be tolerated (≈4 dB lower), V_{PIN} can be grounded.
4. Clock S22 is for ±1 GHz around 2.488 GHz.
5. Measured with a 50 Ω to ground. Outputs must be ac-coupled into 50 Ω (see Figure 2).
6. TTL output.
7. Measured as shown in Figure 1.
8. Measured with a $2^{23} – 1$ pseudorandom word input data pattern and an optical input in the range of –29 dBm to –8 dBm.
9. The 1320 2.5 Gbits/s receiver uses a nonlinear phase detector. Therefore, the jitter transfer bandwidth is undefined. This receiver was designed with the assumption that additional clock filtering will be done at lower data rates as is done in standard SONET/SDH network elements. This subsequent clock filtering will define the jitter transfer BW. Jitter transfer is normally a requirement for the whole network element and not for just the receiver element; thus the use of the 1320 2.5 Gbits/s receiver in a standard SONET network element environment would result in a regenerator compliant to all SONET and SDH requirements.

PWB Layout Guidelines

- The DATA and CLOCK outputs are designed to drive ac-coupled 50 Ω loads. However, other impedances can be used.
- CLOCK and DATA output traces must be controlled-impedance lines and the termination impedance must match the line impedance. Avoid 90° bends in the traces. Paired lines (i.e., DATA and $\overline{\text{DATA}}$) must be equal in length.
- Data and clock output lines should be as short and straight as possible and should be shielded from noise sources to prevent noise from feeding back into the receiver.
- Use high-quality multilayer printed-wiring boards. A ground plane should occupy the area directly beneath the receiver.
- For additional information on PWB layout and biasing and interfacing to the 1320 2.5 Gbits/s receiver, please see *Biasing and Interfacing to the 1320 2.5 Gbits/s Receiver* Technical Note.

Recommended User Interfaces



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* 2 kΩ for APD; 100 Ω for PIN.

Note 1: Data and clock outputs must be ac-coupled on customer use board. Use a 0.1 µF chip capacitor with a low ESR. For optimum receiver performance, all four outputs must be terminated in equivalent loads, even if some of the outputs are not being used.

Note 2: The 0.1 µF VCC/VEE power supply bypass capacitors should be high-quality, low-ESR chip capacitors that are located as close as possible to the appropriate power supply leads and should provide a low-inductance path to the ground plane.

Note 3: These pins are open circuits on the PIN version of the 1320 that does not include the thermistor.

Figure 2. Biasing and Interfacing to the 1320-Type 2.5 Gbits/s Receiver

Qualification Testing

To help ensure high product reliability and customer satisfaction, Lucent is committed to an intensive quality program that starts in the design phase and proceeds through the manufacturing and shipping processes. Optoelectronic modules are qualified to Lucent internal standards using MIL-STD-883 test methods and procedures and sampling techniques consistent with Bellcore requirements. The receiver will meet the specifications of Bellcore TR-NWT-00468 and TA-TSY-000983.

The 1320-Type receiver has been subjected to the following qualifications and meets the specifications of Bellcore TR-NWT-000468 and TA-TSY-000983.

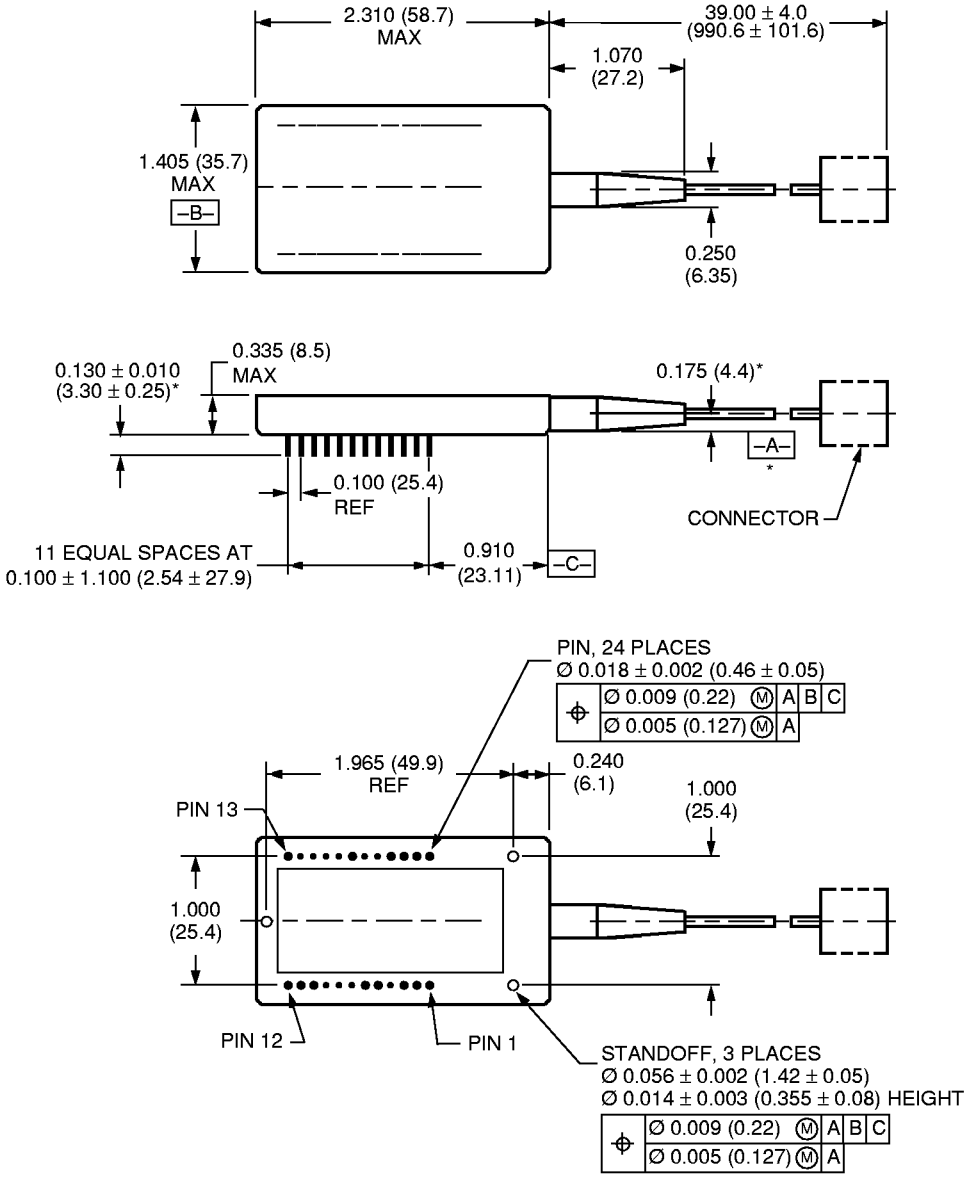
Test	Conditions	Sample Size	Failure Criteria
Physical Dimensions	MIL-STD-883C-2016	90	Visual
External Visual	MIL-STD-883C-2009.8	90	Visual
Impact Shock	1500G, 5 hits, 6 dir., MIL-STD-883C-2002, Condition B	11	Electrical/Optical
Variable Frequency Vibration	20G, 20 Hz to 2 kHz, 4 cycles, 3 directions, 4 min./cycle, MIL-STD-883C-2007.1	11	Electrical/Optical
Solderability	MIL-STD-883C-2003.6	5	Visual
Lead Integrity	MIL-STD-883C-2004.5	5	Visual
Solvent Resistance	MIL-STD-883C-2015.7	5	Visual
Temperature Cycle	–40 °C to +85 °C, 500 cycles, MIL-STD-883C-1010.7	11	Electrical/Optical
High Temperature, High Humidity, with Bias	85 °C, 85% relative humidity, rated bias, 2000 hours	11	Electrical/Optical
High Temperature with Bias	85 °C ambient, rated bias, 5000 hours, MIL-STD-883C-1005.5	11	Electrical/Optical
Internal Visual	MIL-STD-883C-2014	10	Visual
Electrostatic Discharge	Human-body model (to determine class)	5	Electrical/Optical
Fiber Pull	1 kg	11	Electrical/Optical
Low-temperature Storage	–40 °C, 2000 hours	11	Electrical/Optical
Voltage Stress	Maximum rated voltage	10	Electrical/Optical
Power Cycling	MIL-STD-1006	5	Electrical/Optical
Flammability	Fiber cable meets *UL**-listed OFN	—	—

* *UL* is a registered trademark of Underwriters Laboratories, Inc.

Outline Diagram

Dimensions are in inches and (millimeters).

Tolerances are ±0.005 in. (±0.127 mm).



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* Reference surface is to bottom of housing, not to bottom of standoffs.

Ordering Information

Table 3. Ordering Information for the 2.5 Gbits/s 1320-Type Receiver

Product Code	Photodiode	Connector	Comcode
1320PA	PIN	FC/PC	108063389
1320PC	PIN	SC	108063405
1320PD	PIN	*ST*®	108063413
1320MA	APD	FC/PC	108080540
1320MC	APD	SC	108080565
1320MD	APD	*ST*	108080573

Table 4. Related Product Information

Product Code	Description	Document Number
700B Power Module	Power Module (High-Voltage Output dc-dc Converter)	DS95-182EPS
1320 2.5 Gbits/s Receiver	Biasing and Interfacing to the 1320 2.5 Gbits/s Receiver	AP98-052LWP
T48 Transmitter	2.5 Gbits/s Uncooled Laser Transmitter	DS98-429LWP

For additional information, contact your Microelectronics Group Account Manager or the following:

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