

1M x 32 FLASH FLASH MEMORY MODULE

AVAILABLE AS MILITARY SPECIFICATIONS

- Military Processing (MIL-PRF-38534, para 1.2)
- Temperature Range -55°C to 125°C

FEATURES

- Fast access times of 90ns, 120ns, and 150ns
- 5.0V $\pm 10\%$, single power supply operation
- Low power consumption typical: 4 μ A typical CMOS stand-by
 - * ICC(active) <120mA for READ/WRITE
- 20 year DATA RETENTION at 125°C
- 1,000,000 program/erase cycles
- 16 equal sectors of 64 Kbytes each
- Any combination of sectors can be erased
- Group sector protection
- Supports FULL chip erase
- Compatible with JEDEC standards
- Embedded erase and program algorithms
- Data\ polling and toggle bits for detection of program or erase cycle completion.
- Erase suspend/resume
- Hardware reset pin (RESET\)
- Built in decoupling caps and multiple ground pins for low noise operation
- Separate power and ground planes to improve noise immunity

OPTION

• Timing

90ns

120ns

150ns

MARKING

-90

-120

-150

• Packages

Ceramic Quad Flat Pack (0.88" sq)

- MAX height .140"

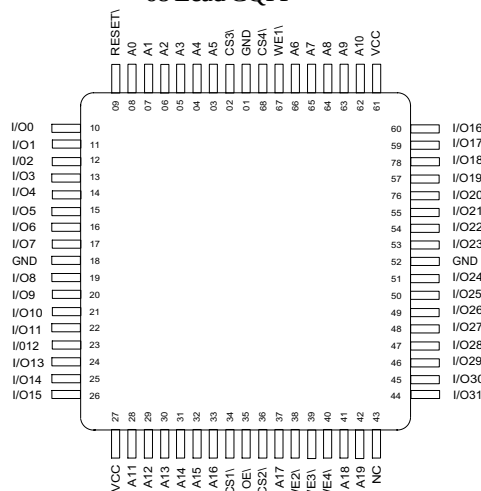
- Stand-off Height .035" min

QT

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**FIGURE 1: PIN ASSIGNMENT
(Top View)**

68 Lead CQFP



GENERAL DESCRIPTION

The Austin Semiconductor, Inc. AS8F1M32 is a 32 Mbit, 5.0 volt-only Flash memory. This device is designed to be programmed in-system with the standard system 5.0 volt VCC supply. The AS8F1M32 offers an access time of 90ns, allowing high-speed microprocessors to operate without wait states. To eliminate bus contention, the device has separate chip enable (CE\), write enable (WE\), and output enable (OE\), controls.

The device requires only a single 5.0 volt power supply for both read and write functions. Internally generated and regulated voltages are provided for the program and erase operations.

The device is entirely command set compatible with the JEDEC single-power-supply FLASH standard. Commands are written to the command register using standard microprocessor write timings. Register contents serve as input to an internal state-matching that controls the erase and programming circuitry. Write cycles also internally latch addresses and data needed for the programming and erase operations. Reading data out of the device is similar to reading from other FLASH or EPROM devices.

Device programming occurs by executing the program command sequence. This initiates the Embedded Program algorithm - an internal algorithm that automatically times the program pulse widths and verifies proper cell margin.

Device erasure occurs by executing the erase command sequence. This initiates the Embedded Erase algorithm - an internal algorithm that automatically preprograms the array (if it is not already programmed) before executing the erase operation. During erase, the device automatically times the erase pulse widths and verifies proper cell margin.

The host system can detect whether a program or erase operation is complete by observing the DQ7 (DATA\ Polling) and DQ6 (toggle) status bits. After a program or erase cycle has been completed, the device is ready to read array data or accept another command.

(continued on page 2)

GENERAL DESCRIPTION (cont.)

The Sector Erase Architecture allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

Hardware Data Protection measures include a low VCC detector that automatically inhibits write operations during power transitions. The Hardware Sector Protection feature disables both program and erase operations in any combinations of the sectors of memory. This can be achieved via programming equipment.

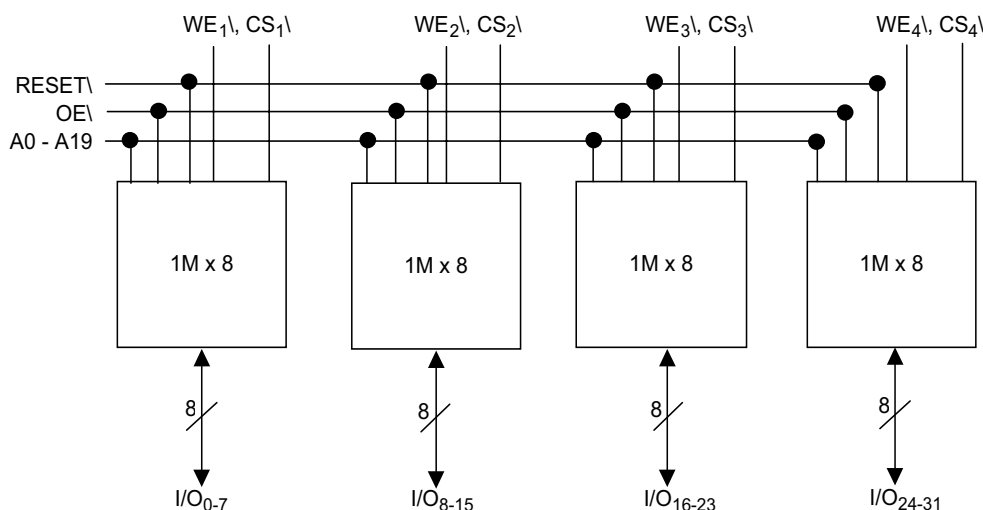
The Erase Suspend feature enables the user to put erase on hold for

any period of time to read data from, or program data to, any sector that is not selected for erasure. True background erase can thus be achieved.

The Hardware RESET pin terminates any operation in progress and resets the internal state machine to reading array data. The RESET pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the system microprocessor to read the boot-up firmware from the FLASH memory.

The system can place the device into the standby mode. Power consumption is greatly reduced in this mode.

FIGURE 2: FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTION

PIN	DESCRIPTION
I/O ₀₋₃₁	Data Inputs/Outputs
A ₀₋₁₉	Address Inputs
WE ₁₋₄	Write Enables
CS ₁₋₄	Chip Selects
OE	Output Enable
V _{CC}	Power Supply
GND	Ground
RESET	Reset

**ABSOLUTE MAXIMUM RATINGS***

Voltage on any pin relative to V_{SS}-2.0V to +7.0V
 Power Dissipation, P_T4W
 Storage Temperature, T_{stg}-65°C to +125°C
 Operating Temperature.....-55°C to +125°C
 Short Circuit Output Current, I_{OS} (1 output at a time).....100mA
 Endurance - Write/Erase Cycles1,000,000 min cycles
 Data Retention.....20 years

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

**Junction temperature depends upon package type, cycle time, loading, ambient temperature and airflow, and humidity (plastics).

ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

(4.5V $\leq$ VCC $\leq$ 5.5V , -55°C $\leq$ T_A $\leq$ +125°C)

DESCRIPTION	CONDITIONS	SYMBOL	MIN	MAX	UNITS
Input Leakage Current	V _{CC} = 5.5, V _{IN} = GND to V _{CC}	I _{LI}	-10	10	μA
Output Leakage Current	V _{CC} = 5.5, V _{IN} = GND to V _{CC}	I _{LO}	-10	10	μA
V _{CC} Active Current for Read	CS\ = V _{IL} , OE\ = V _{IH}	I _{CC1}		160	mA
V _{CC} Active Current for Program or Erase	CS\ = V _{IL} , OE\ = V _{IH}	I _{CC2}		160	mA
V _{CC} CMOS Standby	V _{CC} = 5.5V, All Inputs @ V _{CC} - 0.2V or V _{SS} + 0.2V, RESET\ = CS\ ₁₋₄ = V _{CC} - 0.2V	I _{SB}		4	mA
V _{CC} Standby Current	V _{CC} = 5.5, CS\ = V _{IH} , RESET\ = V _{CC} $\pm$ 0.3V, f=0	I _{CC3}		8	mA
Output Low Voltage	I _{OL} = 12.0 mA, V _{CC} = 4.5	V _{OL}		0.45	V
Output High Voltage	I _{OH} = -2.5 mA, V _{CC} = 4.5	V _{OH}	0.85 x V _{CC}		V
Low V _{CC} Lock-Out Voltage		V _{LKO}	3.2	4.2	V

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Supply Voltage	V _{CC}	4.5	5.0	5.5	V
Ground	V _{SS}	0	0	0	V
Input High Voltage	V _{IH}	2.2	---	V _{CC} + 0.5	V
Input Low Voltage	V _{IL}	-0.5	---	+0.8	V

CAPACITANCE (T_A = +25°C)*

PARAMETER	SYM	CONDITIONS	MAX	UNITS
OE\	C _{OE}	V _{IN} = 0V, f = 1.0 MHz	50	pF
WE\ ₁₋₄	C _{WE}		20	pF
CS\ ₁₋₄	C _{CS}		20	pF
Data I/O	C _{I/O}		50	pF
Address input	C _{AD}		50	pF

*Parameter is guaranteed, but not tested.



Austin Semiconductor, Inc.

FLASH AS8F1M32

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($V_{CC} = 5.0V$, $-55^{\circ}C \leq T_A \leq +125^{\circ}C$)

PARAMETER	SYM	-90		-120		-150		UNITS	
		MIN	MAX	MIN	MAX	MIN	MAX		
WE\ CONTROLLED (WRITE/ERASE/PROGRAM OPERATIONS)									
Write Cycle Time	t _{AVAV}	t _{WC}	90		120		150		ns
Chip Select Setup Time	t _{ELWL}	t _{CS}	0		0		0		ns
Write Enable Pulse Width	t _{WLWH}	t _{WP}	45		50		50		ns
Address Setup Time	t _{AVWL}	t _{AS}	0		0		0		ns
Data Setup Time	t _{DVWH}	t _{DS}	45		50		50		ns
Data Hold Time	t _{WHDX}	t _{DH}	0		0		0		ns
Address Hold Time	t _{WLAX}	t _{AH}	45		50		50		ns
Write Enable Pulse Width High	t _{WHWL}	t _{WPH}	20		20		20		ns
Duration of Byte Progreamming Operation ¹	t _{WHWH1}			300		300		300	μs
Sector Erase ²	t _{WHWH2}			8		8		8	sec
Read Recovery Time before Write	t _{GHWL}		0		0		0		μs
V _{CC} Setup Time	t _{VCS}		50		50		50		μs
Chip Programming Time ³				44		44		44	sec
Chip Erase Time ⁴				256		256		256	sec
Output Enable Hold Time ⁵		t _{OEHL}	10		10		10		ns
RESET\ Pulse Width		t _{RP}	500		500		500		ns
READ-ONLY OPERATIONS									
Read Cycle Time	t _{AVAV}	t _{RC}	90		120		150		ns
Address Access Time	t _{AVQV}	t _{ACC}		90		120		150	ns
Chip Select Access Time	t _{ELQV}	t _{CE}		90		120		150	ns
Output Enable to Output Valid	t _{GLQV}	t _{OE}		40		50		55	ns
Chip Select High to Output High ⁶	t _{EHQZ}	t _{DF}		20		30		35	ns
Output Enable High to Output High ⁶	t _{GHQZ}	t _{DF}		20		30		35	ns
Output Hold from Adresses, CS\ or OE\ Change, whichever is First	t _{AXQX}	t _{OH}	0		0		0		ns
RST Low to Read Mode ⁶		t _{Ready}		20		20		20	μs
CS\ CONTROLLED (WRITE/ERASE/PROGRAM OPERATIONS)									
Write Cycle Time	t _{AVAV}	t _{WC}	90		120		150		ns
Write Enable Setup Time	t _{WLEL}	t _{WS}	0		0		0		ns
Chip Select Pulse Width	t _{ELEH}	t _{CP}	45		50		50		ns
Address Setup Time	t _{AVEL}	t _{AS}	0		0		0		ns
Data Setup Time	t _{DVEH}	t _{DS}	45		50		50		ns
Data Hold Time	t _{EHDH}	t _{DH}	0		0		0		ns
Address Hold Time	t _{ELAX}	t _{AH}	45		50		50		ns
Chip Select Pulse Width High	t _{EHEL}	t _{CPH}	20		20		20		ns
Duration of Byte Progreamming Operation ¹	t _{WHWH1}			300		300		300	μs
Sector Erase Time ²	t _{WHWH2}			8		8		8	sec
Read Recovery Time	t _{GHEL}		0		0		0		μs
Chip Programming Time				44		44		44	sec
Chip Erase Time ⁴				256		256		256	sec
Output Enable Hold Time ⁵		t _{OEHL}	10		10		10		ns

NOTES:

1. Typical value for t_{WHWH1} is 7 μ s.
2. Typical value for t_{WHWH2} is 1 sec.
3. Typical value for Chip Programming is 14 sec.
4. Typical value for Chip Erase Time is 32 sec.
5. For Toggle and Data Polling.
6. This parameter is guaranteed, but not tested.

AC TEST CONDITIONS

PARAMETER	TYP	UNIT
Input Pulse Levels	$V_{IL} = 0, V_{IH} = 3.0$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

FIGURE 3: AC TEST CURRENT

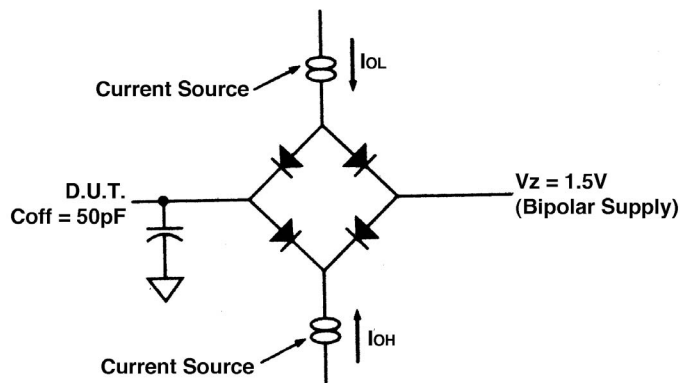


FIGURE 4: RESET Timing Diagram

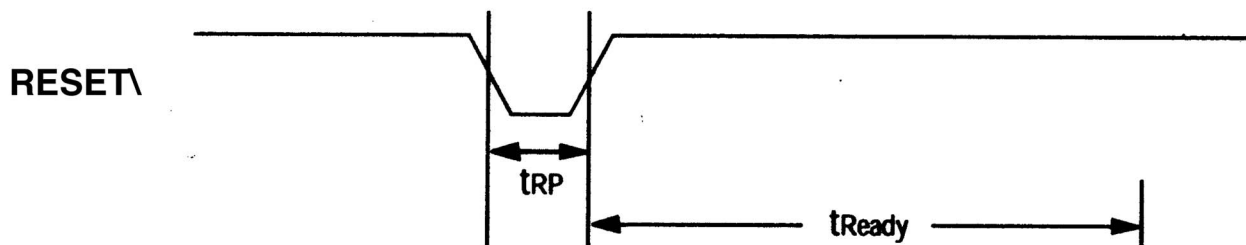


Figure 5: AC Waveforms for READ Operations

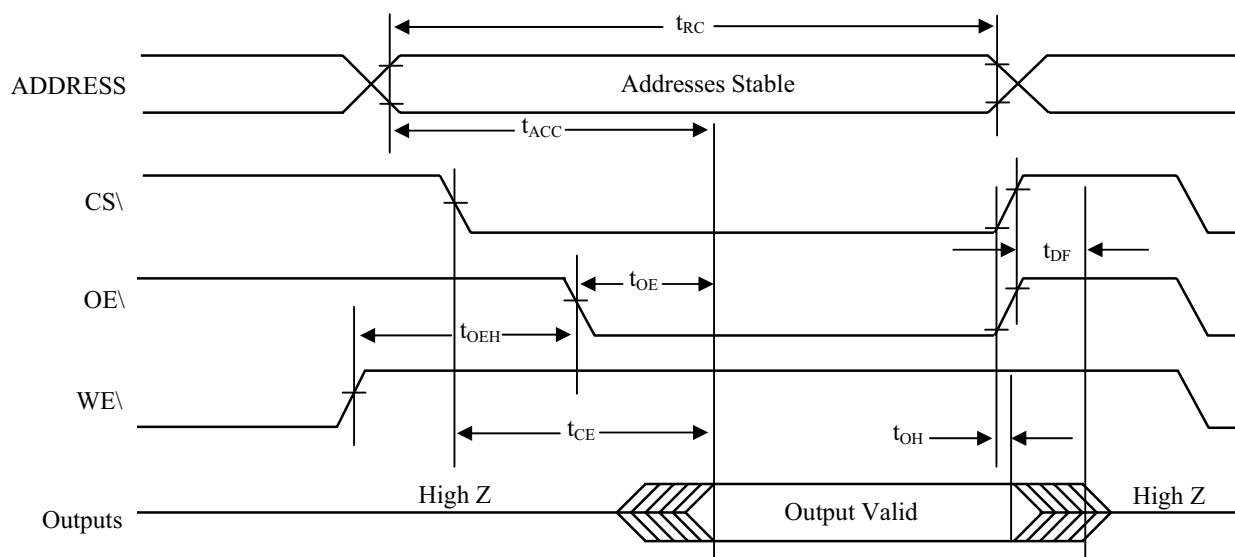
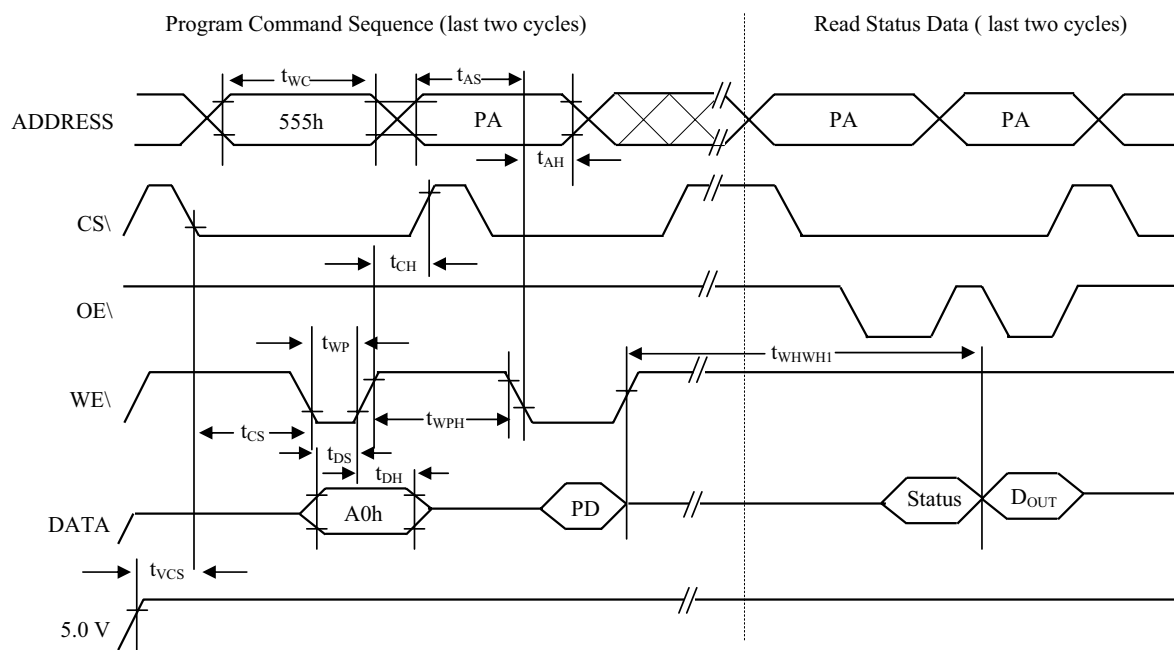


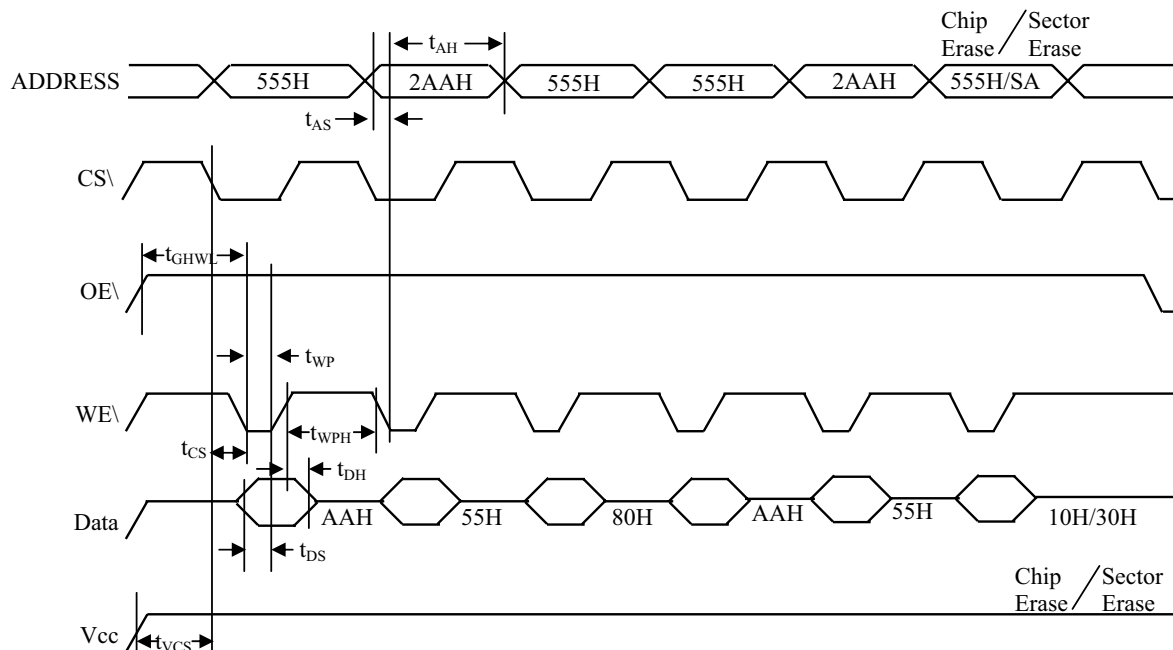
FIGURE 6: WE\ Controlled, WRITE/ERASE/PROGRAM Operation



NOTES:

1. PA is the address of the memory location to be programmed.
2. PD is the data to be programmed at byte address.
3. D_7 is the output of the complement of the data written to each chip.
4. D_{OUT} is the output of the data written to the device.
5. Figure indicates last two bus cycles of four bus cycle sequence.

Figure 7: AC Waveforms Chip/Sector Erase Operations



NOTES:

1. SA is the sector address for Sector ERASE.

Figure 8: AC Waveforms for DATA\ Polling During Embedded Algorithm Operations

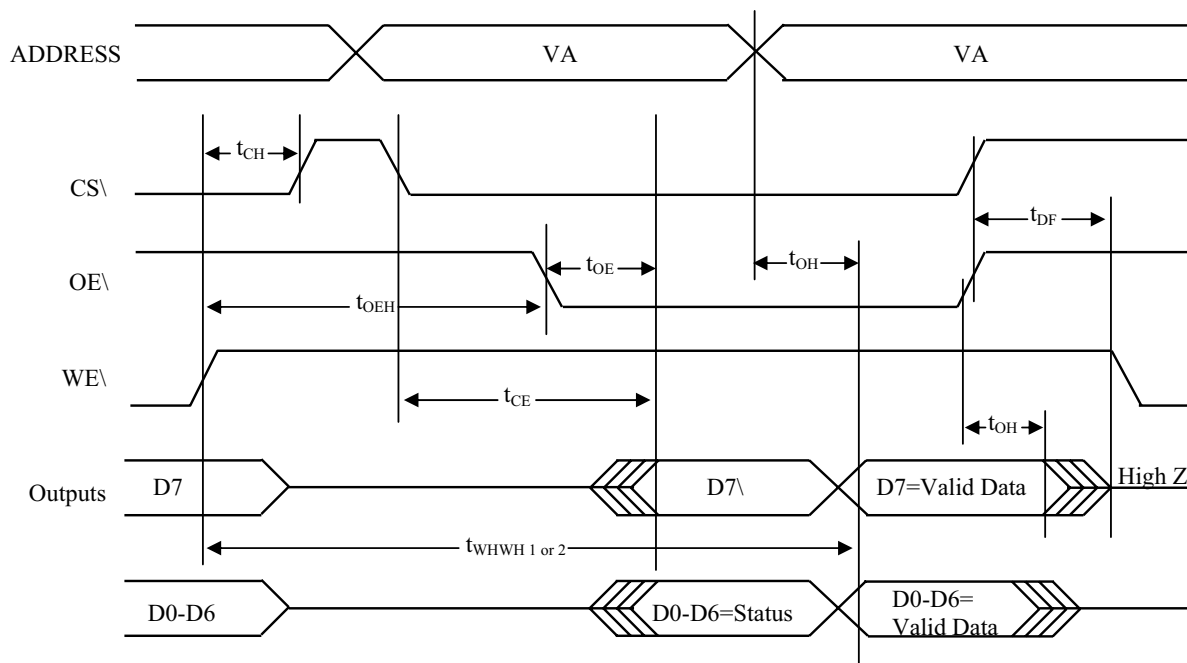
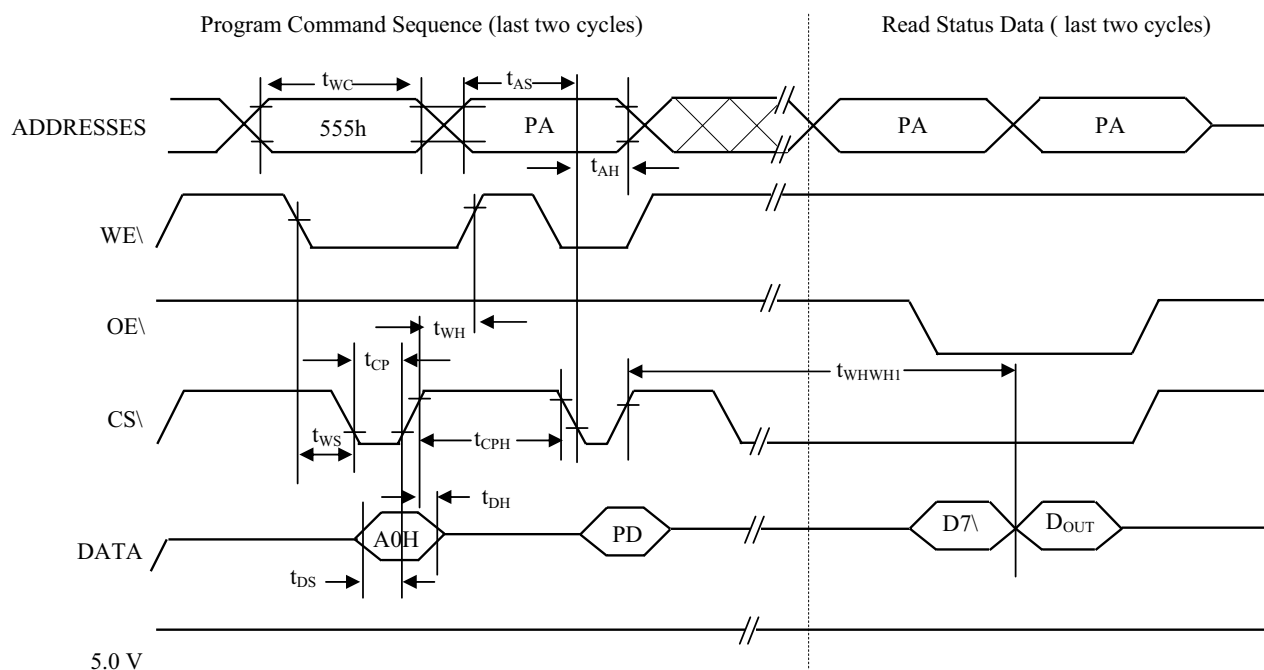


FIGURE 9: Alternate CS\ Controlled Programming Operation Timings

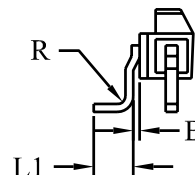
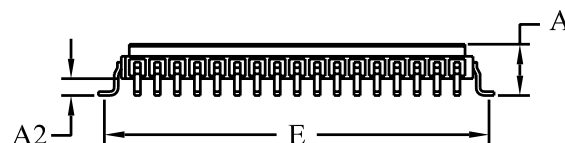
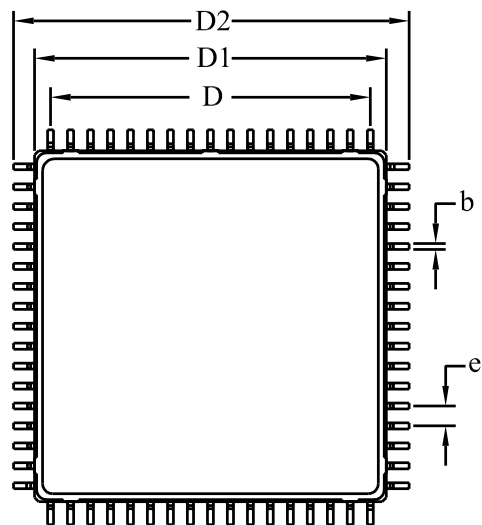


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MECHANICAL DEFINITIONS*

(Package Designator QT)



ASI PACKAGE SPECIFICATION		
Symbol	Min	Max
A	.120	.140
A2	.035	.049
B	.010 REF	
b	.013	.017
D	.800 BSC	
D1	.870	.890
D2	.980	1.000
E	.936	.956
e	.050 BSC	
R	.010 TYP	
L1	.035	.045
Dimensions in inches		



ORDERING INFORMATION

EXAMPLE: AS8F1M32QT-90/MIL

Device Number	Package Type	Speed ns	Process
AS8F1M32	QT	- 90	/*
AS8F1M32	QT	- 120	/*
AS8F1M32	QT	- 150	/*

***AVAILABLE PROCESSES**

IT = Industrial Temperature Range

XT = Extended Temperature Range

Q = MIL-PRF-38534, para 1.2

Temperature

-40°C to +85°C

-55°C to +125°C

-55°C to +125°C