

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

# TC74VHC4040FN

## 12-Stage Ripple Carry Binary Counter

The TC74VHC4040 is an advanced high speed CMOS 12-STAGE BINARY COUNTER/DIVIDER fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

Setting CLR to high resets the counter to low.

A negative transition on the  $\overline{CK}$  input brings one increment into the counter.

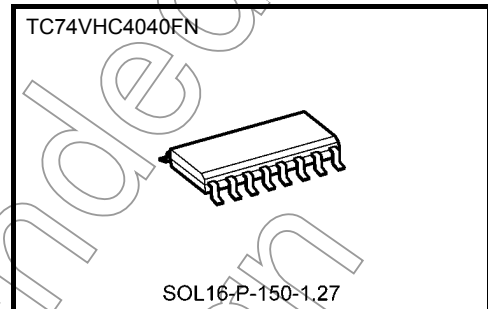
This counter provides all divided output stages, and at Q12, a 1/4096 divided frequency will be output.

An input protection circuit ensures that 0 to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

### Features

- High speed:  $f_{max} = 210$  MHz (typ.) at  $V_{CC} = 5$  V
- Low power dissipation:  $I_{CC} = 4$   $\mu$ A (max) at  $T_a = 25^\circ$ C
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\%$   $V_{CC}$  (min)
- Power down protection is provided on all inputs.
- Balanced propagation delays:  $t_{pLH} \approx t_{pHL}$
- Wide operating voltage range:  $V_{CC(opr)} = 2$  V to 5.5 V
- Low noise:  $V_{OLP} = 1.5$  V (max)
- Pin and function compatible with 74HC4040

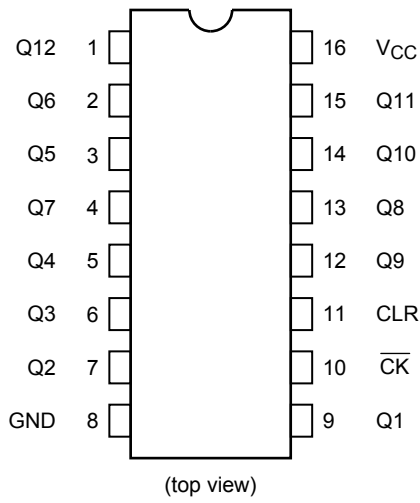
Note: xxxFN (JEDEC SOP) is not available in Japan.



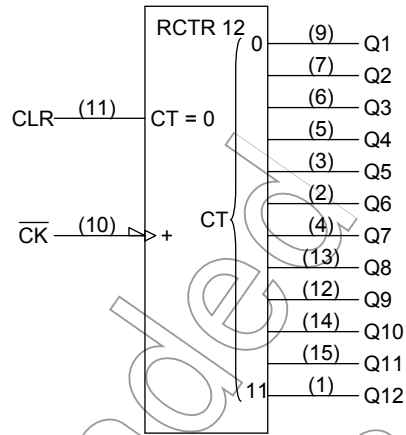
Weight  
SOL16-P-150-1.27 : 0.13 g (typ.)

Not for New Design

**Pin Assignment**



**IEC Logic Symbol**



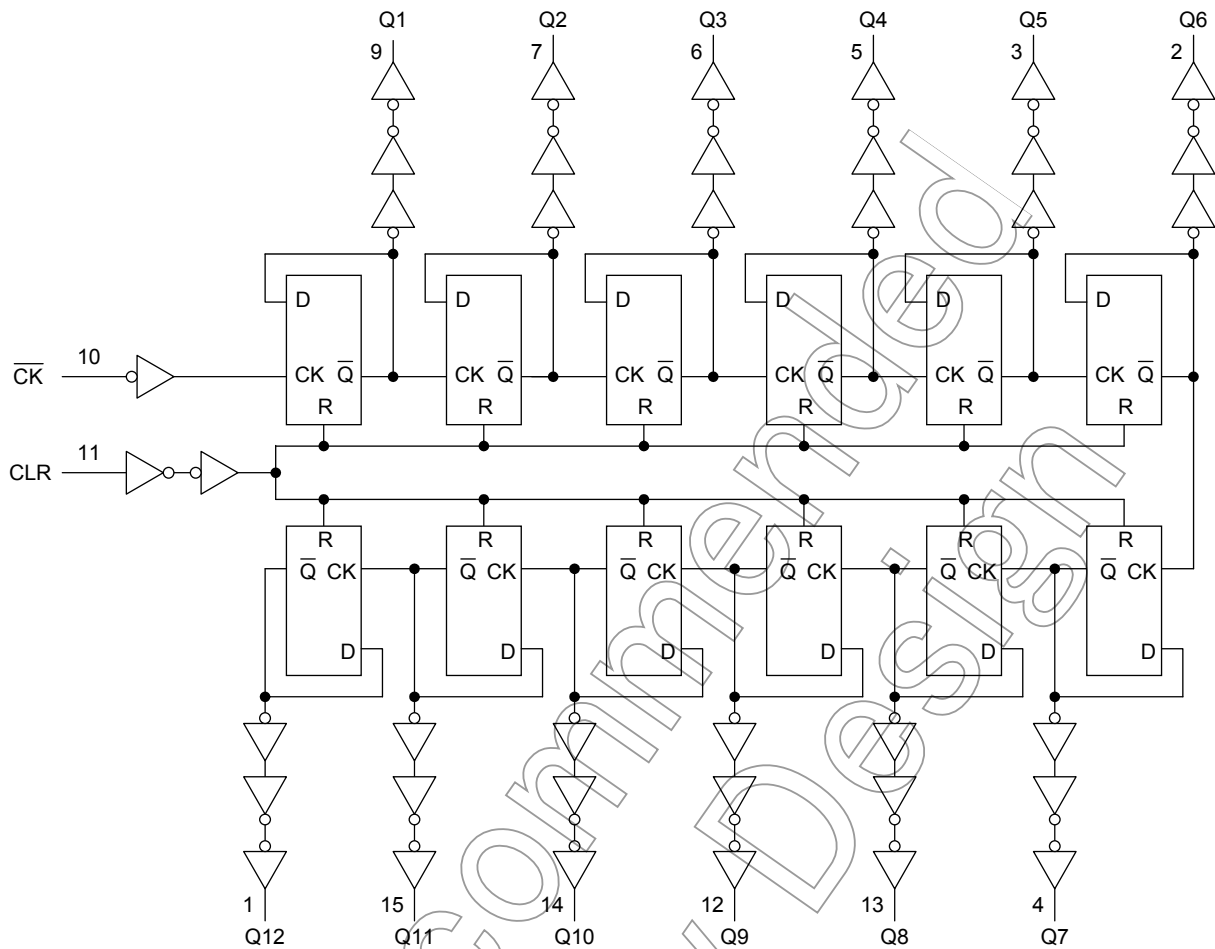
**Truth Table**

$\overline{CK}$	CLR	Output State
X	H	All Outputs = "L"
	L	No Change
	L	Advance to Next State

X: Don't care

Not Recommended for New Design

## System Diagram



## Absolute Maximum Ratings (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7.0	V
DC input voltage	$V_{IN}$	-0.5 to 7.0	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	-20	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 100$	mA
Power dissipation	$P_D$	180	mW
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}C$

Note: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

## Operating Ranges (Note)

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2.0 to 5.5	V
Input voltage	$V_{IN}$	0 to 5.5	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	°C
Input rise and fall time	dt/dv	0 to 100 ( $V_{CC} = 3.3 \pm 0.3$ V)	ns/V
		0 to 20 ( $V_{CC} = 5 \pm 0.5$ V)	

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs must be tied to either  $V_{CC}$  or GND.

## Electrical Characteristics

### DC Characteristics

Characteristics	Symbol	Test Condition		$T_a = 25^\circ\text{C}$			$T_a = -40$ to $85^\circ\text{C}$		Unit	
				$V_{CC}$ (V)	Min	Typ.	Max	Min		Max
High-level input voltage	$V_{IH}$	—	2.0	1.50	—	—	1.50	—	V	
			3.0 to 5.5	$V_{CC} \times 0.7$	—	—	$V_{CC} \times 0.7$	—		
Low-level input voltage	$V_{IL}$	—	2.0	—	—	0.50	—	0.50	V	
			3.0 to 5.5	—	—	$V_{CC} \times 0.3$	—	$V_{CC} \times 0.3$		
High-level output voltage	$V_{OH}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OH} = -50 \mu\text{A}$	2.0	1.9	2.0	—	1.9	—	V
				3.0	2.9	3.0	—	2.9	—	
			$I_{OH} = -4 \text{ mA}$	4.5	4.4	4.5	—	4.4	—	
				3.0	2.58	—	—	2.48	—	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 50 \mu\text{A}$	2.0	—	0.0	0.1	—	0.1	V
				3.0	—	0.0	0.1	—	0.1	
				4.5	—	0.0	0.1	—	0.1	
Low-level output voltage	$V_{OL}$	$V_{IN} = V_{IH}$ or $V_{IL}$	$I_{OL} = 4 \text{ mA}$	3.0	—	—	0.36	—	0.44	V
				4.5	—	—	0.36	—	0.44	
				3.0	—	—	0.36	—	0.44	
Input leakage current	$I_{IN}$	$V_{IN} = 5.5 \text{ V}$ or GND	0 to 5.5	—	—	$\pm 0.1$	—	$\pm 1.0$	$\mu\text{A}$	
Quiescent supply current	$I_{CC}$	$V_{IN} = V_{CC}$ or GND	5.5	—	—	4.0	—	40.0	$\mu\text{A}$	

### Timing Requirements (input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 to 85°C	Unit
			VCC (V)	Typ.	Limit	
Minimum pulse width ( $\overline{\text{CK}}$ )	$t_w$ (L)	—	3.3 ± 0.3	—	5.0	ns
	$t_w$ (H)		5.0 ± 0.5	—	5.0	
Minimum pulse width (CLR)	$t_w$ (H)	—	3.3 ± 0.3	—	5.0	ns
			5.0 ± 0.5	—	5.0	
Minimum removal time	$t_{\text{rem}}$	—	3.3 ± 0.3	—	5.0	ns
			5.0 ± 0.5	—	5.0	

### AC Characteristics (input: $t_r = t_f = 3 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit		
			VCC (V)	CL (pF)	Min	Typ.	Max		Min	Max
Propagation delay time ( $\overline{\text{CK}} - \text{Q1}$ )	$t_{\text{pLH}}$	—	3.3 ± 0.3	15	—	7.5	11.9	1.0	14.0	ns
				50	—	10.0	15.4	1.0	17.5	
	$t_{\text{pHL}}$	—	5.0 ± 0.5	15	—	4.8	7.3	1.0	8.5	
				50	—	6.3	9.3	1.0	10.5	
Propagation delay time ( $\text{Q}_n - \text{Q}_{n+1}$ )	$\Delta t_{\text{pd}}$	—	3.3 ± 0.3	50	—	2.4	4.4	—	5.0	ns
				5.0 ± 0.5	50	—	1.6	3.1	—	
Propagation delay time (CLR-Q)	$t_{\text{pHL}}$	—	3.3 ± 0.3	15	—	8.3	12.8	1.0	15.0	ns
				50	—	10.8	16.3	1.0	18.5	
			5.0 ± 0.5	15	—	5.6	8.6	1.0	10.0	
				50	—	7.1	10.6	1.0	12.0	
Maximum clock frequency	$f_{\text{max}}$	—	3.3 ± 0.3	15	75	140	—	75	—	MHz
				50	55	80	—	50	—	
			5.0 ± 0.5	15	150	210	—	125	—	
				50	95	125	—	80	—	
Input capacitance	$C_{\text{IN}}$	—	—	—	4	10	—	10	pF	
Power dissipation capacitance	$C_{\text{PD}}$	(Note)	—	—	21	—	—	—	pF	

Note:  $C_{\text{PD}}$  is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

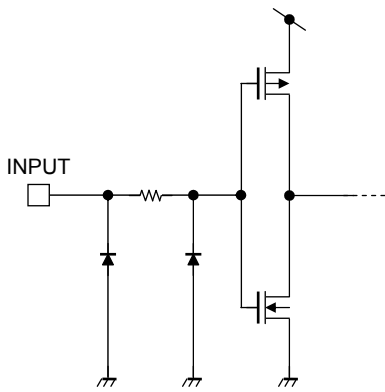
Average operating current can be obtained by the equation:

$$I_{\text{CC (opr)}} = C_{\text{PD}} \cdot V_{\text{CC}} \cdot f_{\text{IN}} + I_{\text{CC}}$$

**Noise Characteristics (input:  $t_r = t_f = 3$  ns)**

Characteristics	Symbol	Test Condition		Ta = 25°C		Unit
			V <sub>CC</sub> (V)	Typ.	Limit	
Quiet output maximum dynamic V <sub>OL</sub>	V <sub>OLP</sub>	C <sub>L</sub> = 50 pF	5.0	1.2	1.5	V
Quiet output minimum dynamic V <sub>OL</sub>	V <sub>OLV</sub>	C <sub>L</sub> = 50 pF	5.0	-1.2	-1.5	V
Minimum high level dynamic input voltage	V <sub>IHD</sub>	C <sub>L</sub> = 50 pF	5.0	—	3.5	V
Maximum low level dynamic input voltage	V <sub>ILD</sub>	C <sub>L</sub> = 50 pF	5.0	—	1.5	V

**Input Equivalent Circuit**

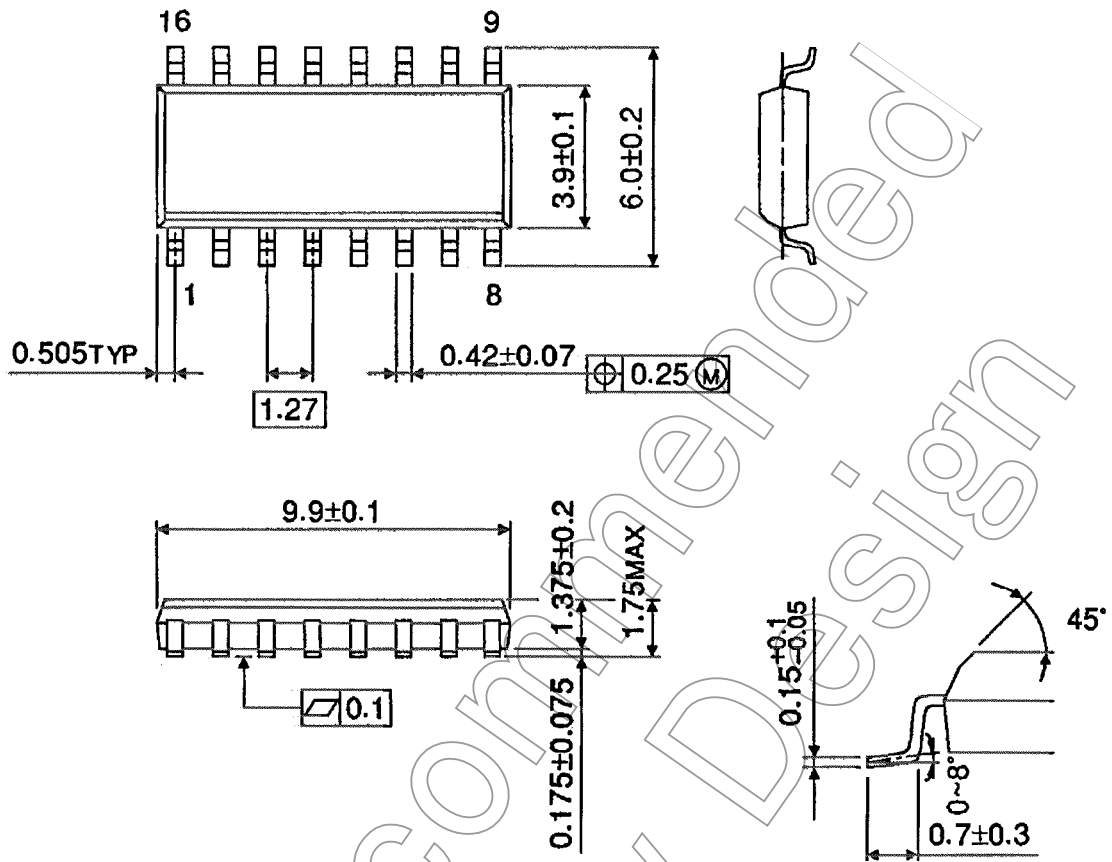


Not Recommended for New Design

Package Dimensions (Note)

SOL16-P-150-1.27

Unit : mm



Note: This package is not available in Japan.

Weight: 0.13 g (typ.)

Not Recommended for New Design

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