HARRIS

HC-55564/883

Continuously Variable Slope Delta-Modulator (CVSD)

January 1989

Features

- **This Circuit is Processed in Accordance to Mil-Std-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **All Digital**
- **Requires Few External Parts**
- **Low Power Drain**
- **Time Constants Determined by Clock Frequency; No Calibration or Drift Problems: Automatic Offset Adjustment**
- **Half Duplex Operation Under Digital Control**
- **Filter Reset Under Digital Control**
- **Automatic Overload Recovery**
- **Automatic "Quiet" Pattern Generation**
- **$\overline{AGC}$ Control Signal Available**

Applications

- **Voice Transmission Over Data Channels (Modems)**
- **Voice/Data Multiplexing (Pair Gain)**
- **Voice Encryption/Scrambling**
- **Voicemail**
- **Audio Manipulations: Delay Lines, Time Compression, Echo Generation/Suppression, Special Effects, etc.**
- **Pagers/Satellites**
- **Data Aquisition Systems**
- **Voice I/O for Digital Systems and Speech Synthesis Requiring Small Size, Low Weight, and Ease of Reprogrammability**

Description

The HC-55564 is a half duplex modulator/demodulator CMOS intergrated circuit used to convert voice signals into serial NRZ digital data and to reconvert that data into voice. The conversion is by delta-modulation, using the Continuously Variable Slope (CVSD) modulation/de-modulation.

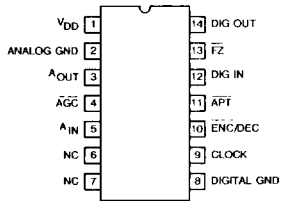
While the signals are compatible with other CVSD circuits, the internal design is unique. The analog loop filters have been replaced by very low power digital filters which require no external timing components. This approach allows inclusion of many desirable features which would be difficult to implement using other approaches.

The fundamental advantages of delta-modulation, along with its simplicity and serial data format, provide an efficient (low data rate/low memory requirements) method for voice digitization. The device may be easily configured with the HC-5512D PCM/CVSD filter.

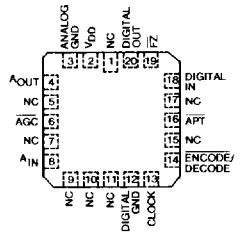
The HC-55564/883 is usable from 9K bits/sec to above 64Kbps. The unit is available in a 14 pin Ceramic DIP or a 20 pad Ceramic LCC package. For more applications information, see Application's Notes 576 and 607 (section 10 of Analog Data Book).

Pinouts

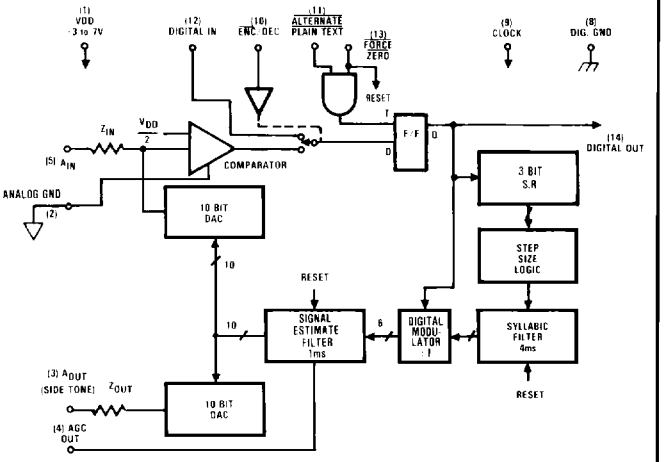
HC1-55564/883 (CERAMIC DIP)
TOP VIEW



HC4-55564/883 (CERAMIC LCC)
TOP VIEW



Functional Diagram



NOTE: Pin Numbers Correspond to DIP Package Only.

Pin Description

PIN NO. 14-PIN DIP	PIN NO. 20-PIN LCC	SYMBOL	DESCRIPTION
1	2	V_{DD}	Positive Supply Voltage. Voltage range is +3.0V to +7.0V.
2	3	Analog GND	Analog Ground connection to D/A ladders and comparator.
3	4	A_{OUT}	Audio Out recovered from 10 bit DAC. May be used as side tone at the transmitter. Presents approximately 150 kilohm source with D.C. offset of $V_{DD}/2$. Within ±2dB of Audio Input. Should be externally A.C. coupled.
4	6	$\overline{AGC}$	Automatic Gain Control output. A logic low level will appear at this output when the recovered signal excursion reaches ½ of full scales value. In each half cycle full scale is $V_{DD}/2$. The mark-space ratio is proportional to the average signal level.
5	8	A_{IN}	Audio Input to comparator. Should be externally coupled. Presents approximately 280 kilohms in series with $V_{DD}/2$.
6, 7	1, 5, 7, 9 10, 11 15, 17	NC	No internal connection is made to these pins.
8	12	Digital GND	Logic ground. 0V reference for all logic inputs and outputs.
9	13	Clock	Sampling rate clock. In the decode mode, must be synchronized with the digital input data such that the data is valid at the positive clock transition. In the encode mode, the digital data is clocked out on the negative going clock transition. The clock rate equals the data rate.
10	14	$\overline{Encode}$/ Decode	A single CVSD can provide half-duplex operation. The encode or decode function is selected by the logic level applied to this input. A low level selects the encode mode, a high level the decode mode.
11	16	$\overline{APT}$	Alternate Plain Text input. Activating this input caused a digital quieting pattern to be transmitted, however; internally the CVSD is still functional and a signal is still available at the A_{OUT} port. Active low.
12	18	Digital In	Input for the received digital NRZ data.
13	19	$\overline{FZ}$	Force Zero input. Activating this input resets the internal logic and forces the digital output and the recovered audio output into the "quieting" condition. An alternating 1-0 pattern appears at the digital output at ½ the clock rate. When this is decoded by a receive CVSD, a 10mVp-p inaudible signal appears at audio output. Active low.
14	20	Digital Out	Output for transmitted digital NRZ data.

NOTE: No active input should be left in a "floating condition."

Absolute Maximum Ratings

Voltage at Any Pin ..... GND -0.3V to V_{DD} +0.3V
Maximum V_{DD} Voltage ..... +7.0V
Minimum V_{DD} Voltage ..... +3.0V
Junction Temperature ..... +175°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering 10 Seconds) ..... +275°C
ESD Rating ..... < 2000V

CAUTION Absolute maximum ratings are limiting values, applied individually beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.

Thermal Information

Thermal Resistance	θ_{ja}	θ_{jc}
Ceramic DIP Package	75°C/W	15°C/W
Ceramic LCC Package	76°C/W	19°C/W

Package Power Dissipation Limit at +75°C for T_J at ≤ +175°C
Ceramic DIP Package 1.33W
Ceramic LCC Package 1.32W
Package Power Dissipation Derating Factor Above +75°C
Ceramic DIP Package ..... 13.3mW/°C
Ceramic LCC Package ..... 13.2mW/°C

Recommended Operating Conditions

Operating Temperature Range ..... -55°C to +125°C
Operating Supply Voltage (V_{DD} Range) ..... +3.0V to +7.0V

TABLE 1. D.C. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: Supply Voltage = +5V, fclk = 16kHz, Operating Temperature = -55°C ≤ T_A ≤ +125°C, Unless Otherwise Specified.

D.C. PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Supply Current	I_{DD}	Encode Mode: A_{IN} = 0V	1	+25°C	-	1.5	mA
			2, 3	+125°C, -55°C	-	1.5	mA
Logic Input High (Note 2)	V_{IH}	Input Level: '1' = +3.5V, '0' = +1.5V	1	+25°C	3.5	-	V
			2, 3	+125°C, -55°C	3.5	-	V
Logic Input Low (Note 2)	V_{IL}	Input Level: '1' = +3.5V, '0' = +1.5V	1	+25°C	-	1.5	V
			2, 3	+125°C, -55°C	-	1.5	V
Logic Output High (Note 3)	V_{OH}	I Load = -40μA	1	+25°C	4.0	-	V
			2, 3	+125°C, -55°C	4.0	-	V
Logic Output Low (Note 3)	V_{OL}	I Load = +0.8mA	1	+25°C	-	0.4	V
			2, 3	+125°C, -55°C	-	0.4	V
Quieting Pattern (Note 8) Amplitude	V_{QP}	$\overline{FZ}$ = 0; Clock Inputs Switched Statically	1	+25°C	-	14	mVp-p
			2, 3	+125°C, -55°C	-	14	mVp-p
AGC Threshold (Note 9)	V_{ATH}	Encode Mode	1	+25°C	0.45	0.65	F.S.
			2, 3	+125°C, -55°C	0.45	0.65	F.S

CAUTION: This device is sensitive to electrosatic discharge. Proper I.C. handling procedures should be followed.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Devices Characterized at: V_{DD} = +5V, T_A = +25°C Operating Temperature, fclk = 16kHz Clock Sampling Rate.
$\overline{ENC}$/DEC = $\overline{ENC}$ = Encode Mode, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTE	TEMP	LIMITS MIN	LIMITS MAX	UNITS
Sampling Rate	CLK	A_{IN} = 0.775 V_{RMS} at 20Hz	1, 12	+25°C +125°C, -55°C	9	64	KBS
CLK Duty Cycle	A_{IN}	A_{IN} = 0.775 V_{RMS} at 100Hz	12	+25°C +125°C, -55°C	30	70	%
Audio Input Voltage	A_{IN}	A_{IN} at 100Hz	4, 12	+25°C +125°C, -55°C	-	1.2	V_{RMS}
Audio Output Voltage	A_{OUT}	A_{IN} at 100Hz	5, 12	+25°C +125°C, -55°C	-	1.2	V_{RMS}
Input Impedance	Z_{IN}	A_{IN} at 100Hz	6, 12	+25°C +125°C, -55°C	150	500	kΩ
Output Impedance	Z_{OUT}	A_{IN} at 100Hz	6, 12	+25°C +125°C, -55°C	35	225	kΩ
Transfer Gain	A_{E-D}	A_{IN} = 0.775 V_{RMS} at 100Hz	11, 12	+25°C -55°C, +125°C	-2	+2	dB
Resolution	RES	A_{IN} at 100Hz	12, 13	+25°C	0.3	-	% of Supply
MIN Step Size	MSS		7, 12	+25°C	0.02	0.08	% of Supply
Clamping Threshold	V_{CTH}		10, 12	+25°C	0.70	0.90	F.S.

NOTES:

1. There is one NR (Non-Return Zero) data bit per clock period. Data is clocked out on the negative clock edge. Data is clocked into the CVSD on the positive going edge (see Figure 2). Clock may be run at less than 9Kbps.
2. Logic inputs are CMOS compatible at supply voltage and are diode protected. Digital data input is NRZ at clock rate.
3. Logic outputs are CMOS compatible at supply voltage and will withstand short-circuits to V_{DD} or ground; however, the short circuit duty cycle must not exceed 5% in order to maintain an acceptable current density level. Digital data output is NRZ and changes with negative clock transitions. Each output will drive two LS TTL loads.
4. Recommended voice input range for best voice performance. Should be externally A.C. coupled.
5. May be used for side-tone in encode mode. Should be externally A.C. coupled. Varies with audio input level by ±dB.
6. Presents series impedance with audio signal. Zero signal reference is approximately $V_{DD}/2$.
7. The minimum audio output voltage change that can be produced by the internal DAC.
8. The "quieting" pattern or idle-channel audio output steps at 1/2 the bit rate, changing state on negative clock transitions.
9. A logic '0' will appear at the AGC output pin when the recovered signal reaches 1/2 of full-scale value (positive or negative), i.e. at $V_{DD}/2$ ±25% of V_{DD}.
10. The recovered signal will be clamped, and the computation will be inhibited, when the recovered signal reaches 3/4 of full-scale value, and will unclamp when it falls below this value (positive or negative).
11. No load condition measured from audio in to audio out.
12. The parameters listed in this table are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.
13. The minimum audio input voltage above which encoding is guaranteed to take place.

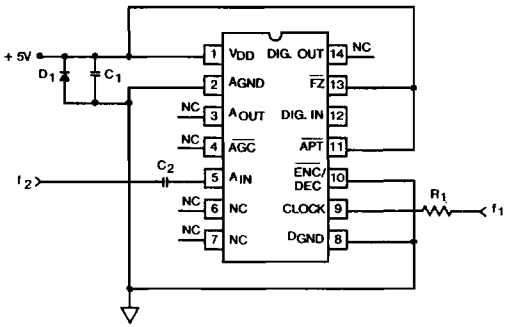
TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 & 3)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1*, 2, 3
Group A Test Requirements	1, 2, 3
Groups C & D Endpoints	1

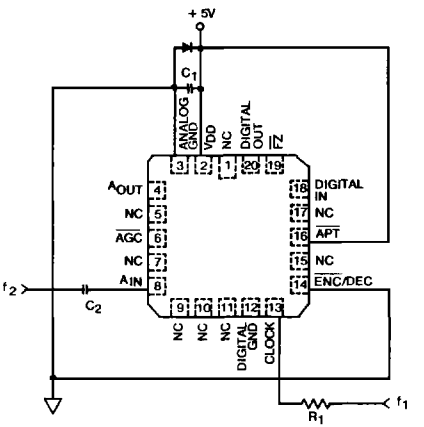
* PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

Burn-In Circuits

HC-55564/883 (CERAMIC DIP)



HC-55564/883 (CERAMIC LCC)



NOTES:

R_1 = 10KΩ ±5Ω, 1/4 Watt (per socket)

f_1 = 16kHz TTL Levels, 50% Duty Cycle, Square Wave

f_2 = ≃ 200Hz (Approximate); 3Vp-p Sinewave (or triangular wave), centered around ground.

C_1 = 0.01μF (per socket), or 0.1μF (per row) minimum.

C_2 = 0.1μF (per socket) minimum.

D_1 = IN4002 or Equivalent (per board)

Die Characteristics

DIE DIMENSIONS:
154 x 93 x 19 mils

METALLIZATION:
Type: SiAl
Thickness: 16kÅ ± 2kÅ

WORST CASE CURRENT DENSITY:
$2.0 \times 10^5 A/cm^2$
This device meets Glassivation Integrity Test requirement per Mil-Std-883 Method 2021 and Mil-M-38510 paragraph 3.5.5.4.

GLASSIVATION:
Type: Silox
Thickness: 8kÅ ± 1kÅ

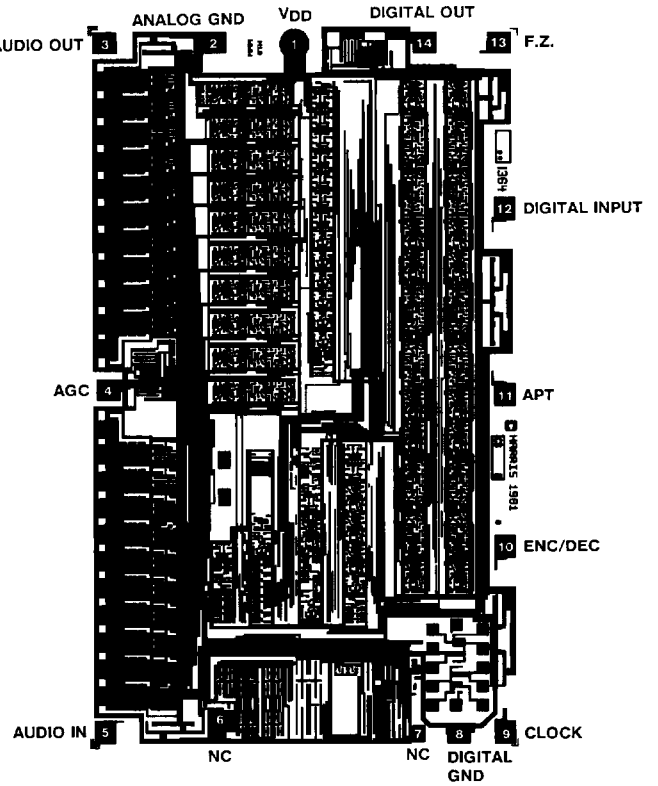
TRANSISTOR COUNT: 1896

PROCESS: CMOS; SAJI

DIE ATTACH:
Material: Gold/Silicon Eutectic Alloy
Temperature: Ceramic DIP — 460°C (Max)
Ceramic LCC — 420°C (Max)

Metallization Mask Layout

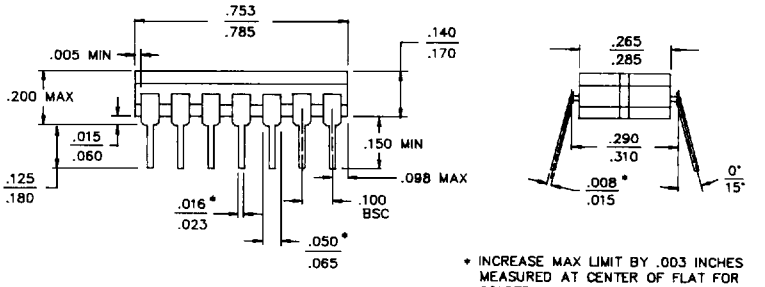
HC-55564/883



NOTE: Pad Numbers Correspond to DIP Package Only.

Packaging†

14 PIN CERAMIC DIP

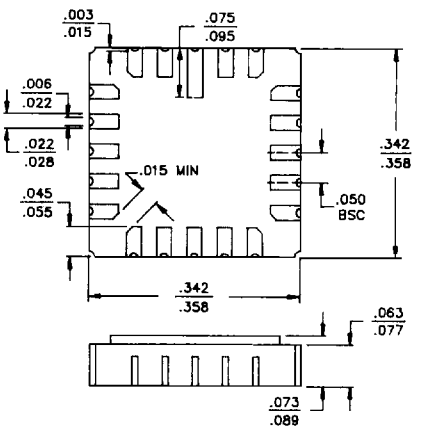


* INCREASE MAX LIMIT BY .003 INCHES MEASURED AT CENTER OF FLAT FOR SOLDER FINISH

LEAD MATERIAL: Type B
LEAD FINISH: Type A
PACKAGE MATERIAL: Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Glass Frit
Temperature: 450°C ± 10°C
Method: Furnace Seal

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 D-1

20 PAD CERAMIC LCC



PAD MATERIAL: Type C
PAD FINISH: Type A
FINISH DIMENSION: Type A
PACKAGE MATERIAL: Multilayer Ceramic, 90% Alumina
PACKAGE SEAL:
Material: Gold/Tin (80/20)
Temperature: 320°C ± 10°C
Method: Furnace Braze

INTERNAL LEAD WIRE:
Material: Aluminum
Diameter: 1.25 Mil
Bonding Method: Ultrasonic
COMPLIANT OUTLINE: 38510 C-2

NOTE: All Dimensions are $\frac{\text{Min}}{\text{Max}}$, Dimensions are in inches.

†Mil-M-38510 Compliant Materials, Finishes, and Dimensions.

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Typical Performance

The following typical performance distortion graphs were realized with the test configuration of Figure 1. The measurement vehicle for Total Harmonic Distortion (THD) was an HP-339A distortion measurement set, and for 2nd and 3rd harmonic distortion, an HP-3582A spectrum analyzer. All measurement conditions were at V_{DD} = +5V, and 2nd and 3rd harmonic distortion measurements were C-message filtered. 0dB = 1.2V_{RMS}.

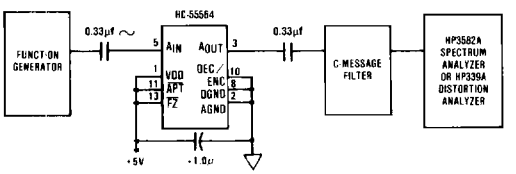


FIGURE 1. TEST AND MEASUREMENT CIRCUIT

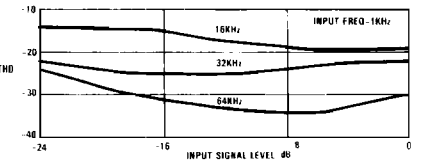
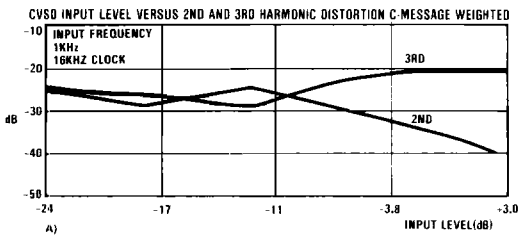
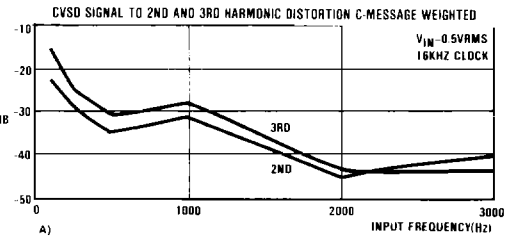
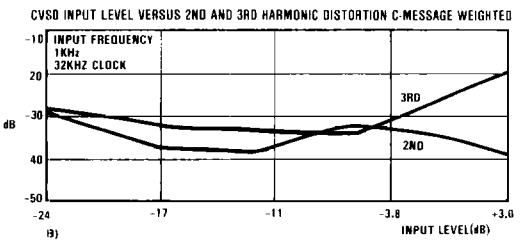
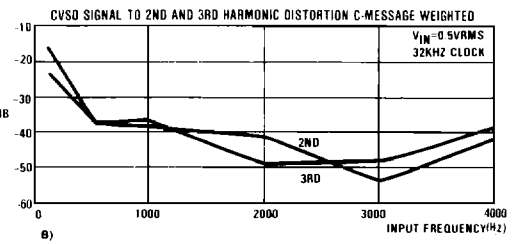


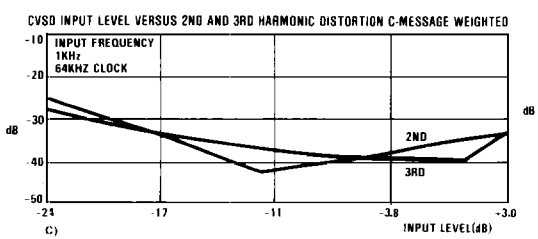
FIGURE 2. CVSD SIGNAL LEVEL vs. TOTAL HARMONIC DISTORTION











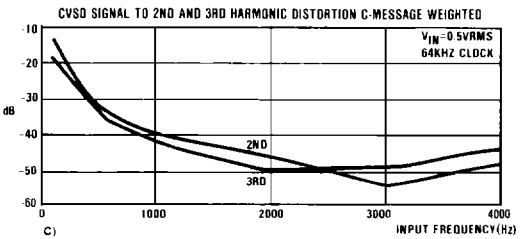


FIGURE 3A, B, C. CVSD INPUT LEVEL vs. 2ND AND 3RD HARMONIC DISTORTION

FIGURE 4A, B, C. CVSD INPUT FREQUENCY vs. 2ND AND 3RD HARMONIC DISTORTION

DESIGN INFORMATION (Continued)

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Typical Performance (Continued)

Figures 5, 6, and 7 illustrate the typical frequency response of the HC-55564 for varying input levels and for varying sampling rates. To prevent slope overload (slew limiting), the 0dB boundry should not be exceeded. The frequency response is directly proportional to the sampling clock rate. The flat bandwidth at 0dB doubles for every 16kHz increase in sampling rate. The output levels were measured in the encode mode, without filtering, from A_{IN} to A_{OUT}, at V_{DD} = +5V, 0dB = 1.2V_{RMS}.

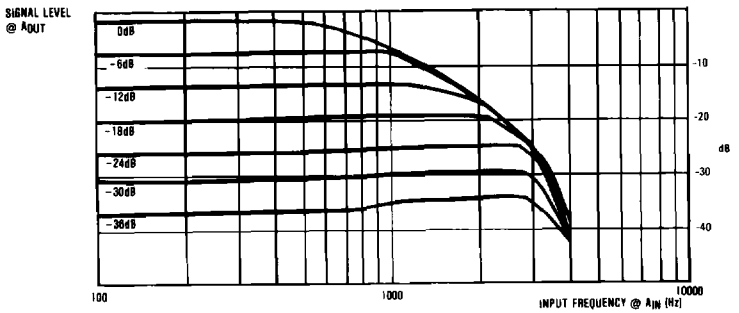

FIGURE 5. TRANSFER FUNCTION FOR CVSD AT 16Kbps

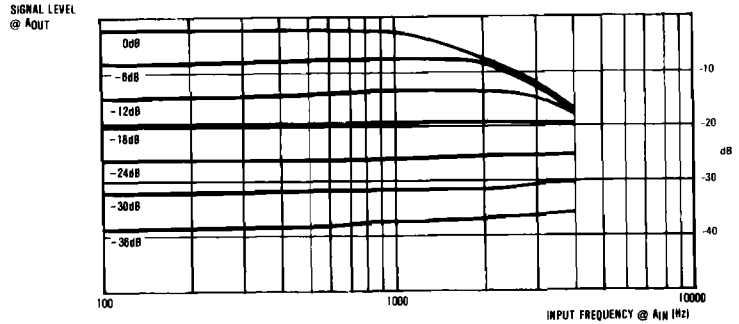

FIGURE 6. TRANSFER FUNCTION FOR CVSD AT 32Kbps

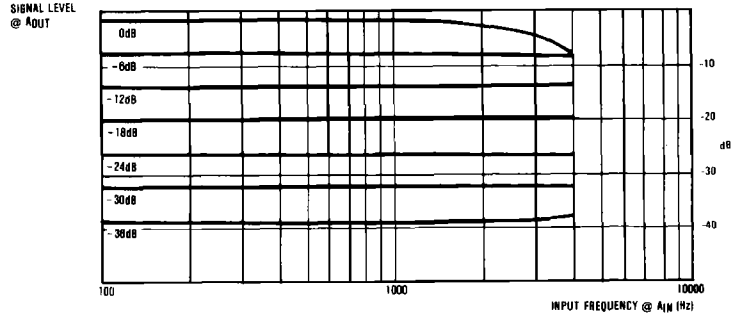

FIGURE 7. TRANSFER FUNCTION FOR CVSD AT 64Kbps

DESIGN INFORMATION (Continued)

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Interface Circuit for HC-55564 CVSD

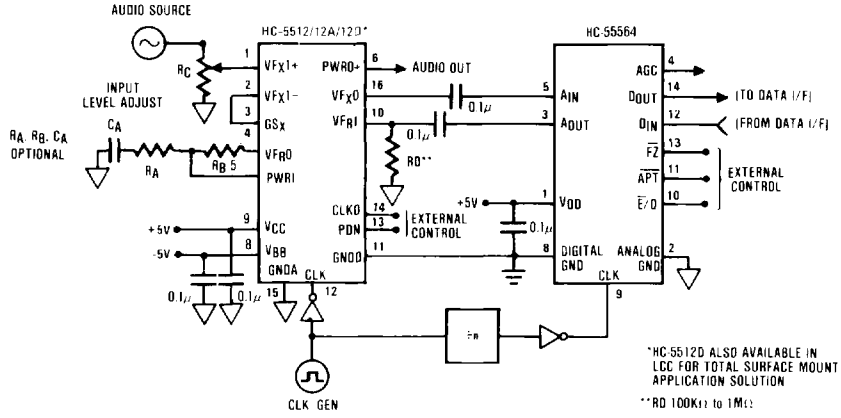
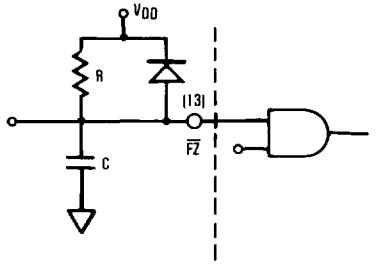


FIGURE 8.

CVSD Hookup for Evaluation

The circuit in Figure 8 is sufficient to evaluate the voice quality of the CVSD, since when encoding the feedback signal at the audio output pin is the reconstructed audio input signal. CVSD design considerations are as follows:

1. Care should be taken in layout to maintain isolation between analog and digital signal paths for proper noise consideration .
2. Power supply decoupling is necessary as close to the device as possible A 0.1µF should be sufficient.
3. Ground, then power, must be present before any input signals are applied to the CVSD. Failure to observe this may cause a latchup condition which may be destructive. Latchup may be removed by cycling the power off/on. A power-up reset circuit may be used that strobes Force Zero (Pin 13) during power-up as follows:



4. Analog (signal) ground (Pin 2) should be externally tied to Pin 8 and power ground. It is recommended that the A_{IN} and A_{OUT} ground returns connect only to Pin 2.
5. Digital inputs and outputs are compatible with standard CMOS logic using the same supply voltage. All unused logic inputs must be tied to the appropriate logic level for desired operation. TTL outputs will require 1kΩ pull-up resistors. Pins 4 and 14 will each drive CMOS logic or one low power TTL input.
6. Since the Audio Out pins are internally D.C. biased to $V_{DD}/2$, A.C. coupling is required In general, a value of 0.1µF is sufficient for A.C. coupling of the CVSD audio pins to a filter circuit.
7. The $\overline{AGC}$ output may be externally integrated to drive an $\overline{AGC}$ pre-amp, or it could drive an LED indicator through a buffer to indicate proper speaking volume.

DESIGN INFORMATION (Continued)

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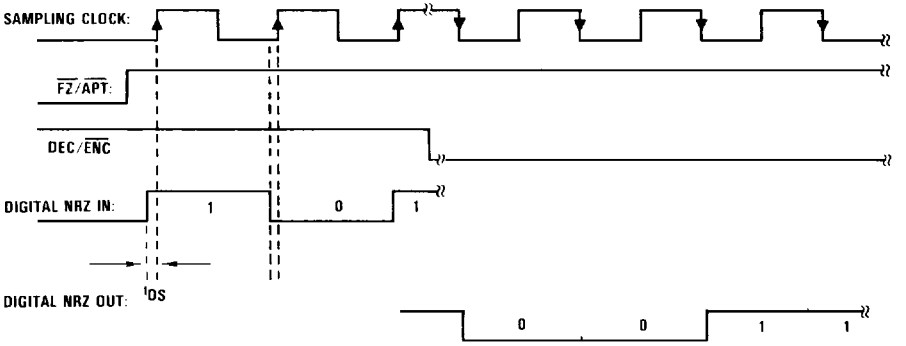
Timing Waveforms



t_{DS}: DATA SET UP TIME, 100ns TYPICAL

FIGURE 9. CVSD TIMING DIAGRAM

DESIGN INFORMATION (Continued)

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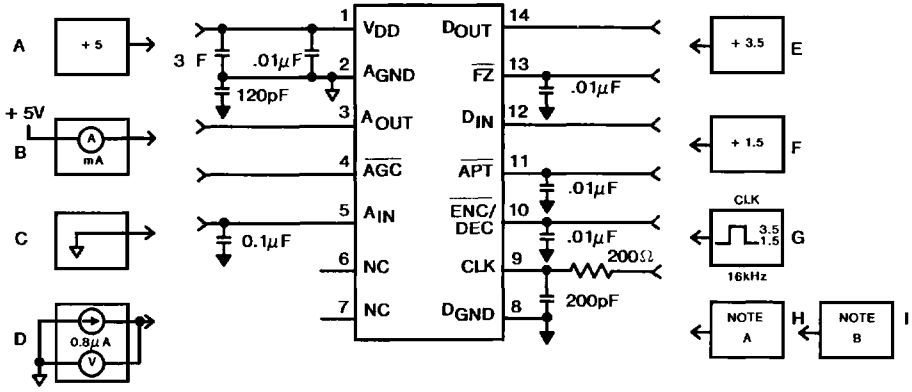
Test Configuration



TEST NO.	TEST NAME	IC PIN NUMBERS 1	2	3	4	5	6	7	8	9	10	11	12	13	14
1	I_{DD} Supply Current	B	NA	NA	NA	C	NA	NA	NA	G	F	E	F	E	NA
2	V_{IH} Input Logic 1	A	NA	NA	NA	NA	NA	NA	NA	G	E	E	E	E	NA
3	V_{IL} Input Logic 0	A	NA	NA	NA	NA	NA	NA	NA	G	F	F	F	F	NA
4	V_{OL} Dig Out Logic 0	A	NA	NA	D	NA	NA	NA	NA	H	E	E	F	E	D
5	V_{OL} AGC Out Logic 0	A	NA	NA	D	NA	NA	NA	NA	G	E	E	E	E	D
6	V_{OH} Dig Out Logic 1	A	NA	NA	D	NA	NA	NA	NA	I	E	E	E	E	D
7	V_{OH} AGC Out Logic 1	A	NA	NA	D	NA	NA	NA	NA	E	E	E	E	E	D

DESIGN INFORMATION (Continued)

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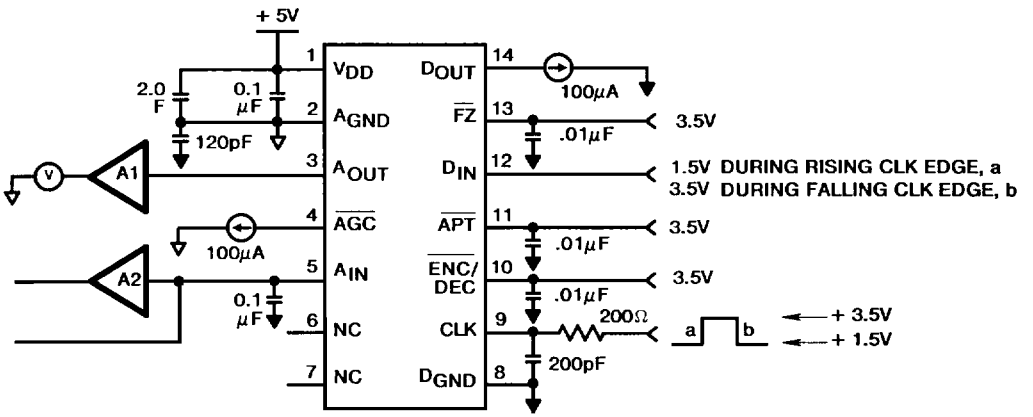
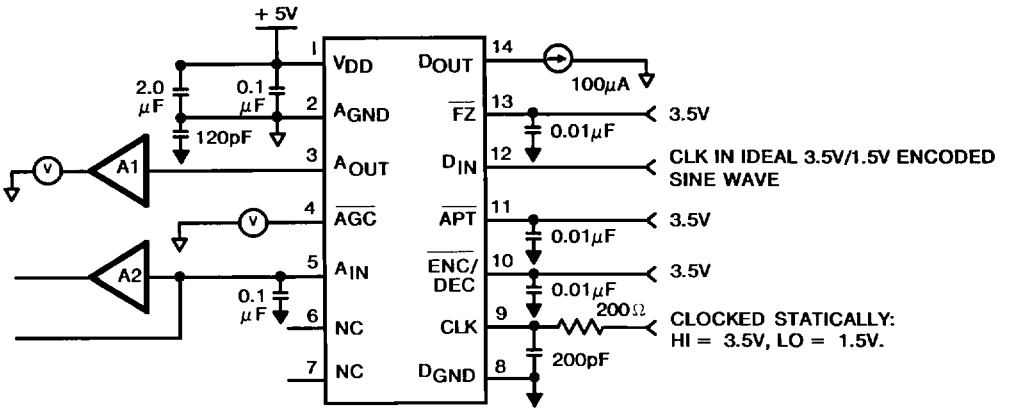
Test Configuration (Continued)

TEST: V_{QP}, QUIETING PATTERN AMPLITUDE



A1, A2 OP Amps are buffers for measurements taken at A_{IN} and A_{OUT}.
The difference in measurements at A_{OUT} when D_{IN} is HI and D_{IN} is LO is V_{QP}.

TEST: V_{ATH}, $\overline{AGC}$ THRESHOLD



A1, A2 OP Amps are buffers for measurements taken at A_{IN} and A_{OUT}.
For each CLK Cycle, measure A_{OUT} and AGC for CLK = HI and CLK = LO.
Following A_{OUT} wave form bit by bit, $\overline{AGC}$ LO is A_{OUT} voltage where $\overline{AGC}$ output goes from HI to LO. AGC HI is A_{OUT} voltage where $\overline{AGC}$ output goes from LO back to HI. V_{ATH} is the fraction of full scale of ($\overline{AGC}$ HI - $\overline{AGC}$ LO).

DESIGN INFORMATION (Continued)

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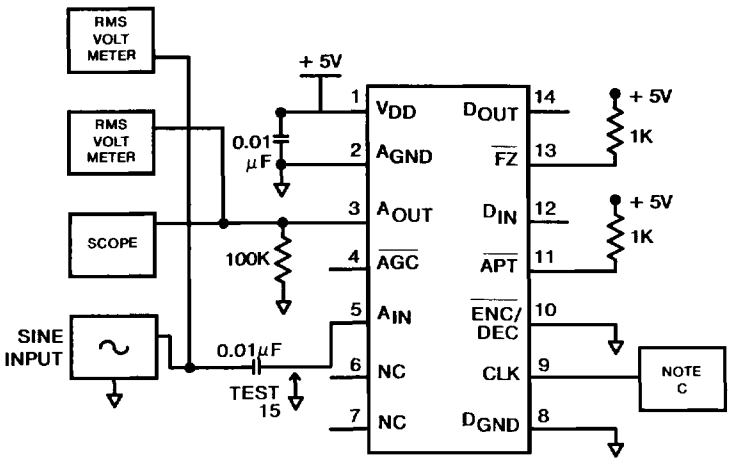
Test Configuration (Continued)

TEST: 10 THROUGH 16



TEST	TEST NAME	SINE WAVE CONDITIONS
10	Clock Sampling Rate	Sine Input 20Hz, 0.775 V_{RMS}
11	Clock Duty Cycle	Sine Input 100Hz, 0.775 V_{RMS}
12	Transfer Gain	Sine Input 100Hz, 0.775 V_{RMS}
13	Audio Input/Output (A_{IN}/A_{OUT}) Voltage Test	Sine Input 300Hz
14	Resolution	Sine Input 100Hz
15	Minimum Step Size	A_{IN} Grounded
16	Clamping Threshold	Sine Input 100Hz

* Resistor used only on Test 10 and 11.

DESIGN INFORMATION (Continued)

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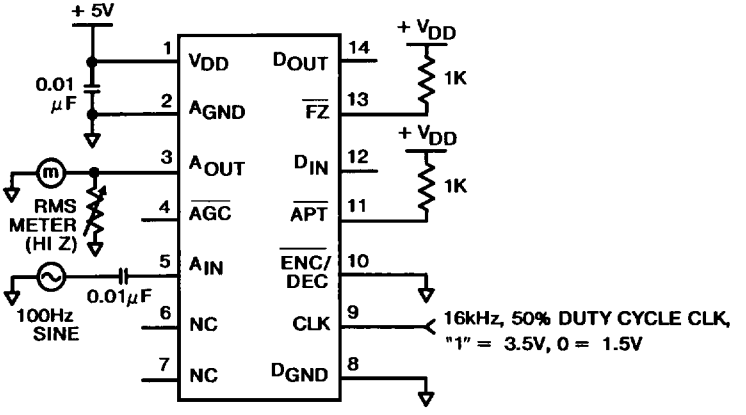
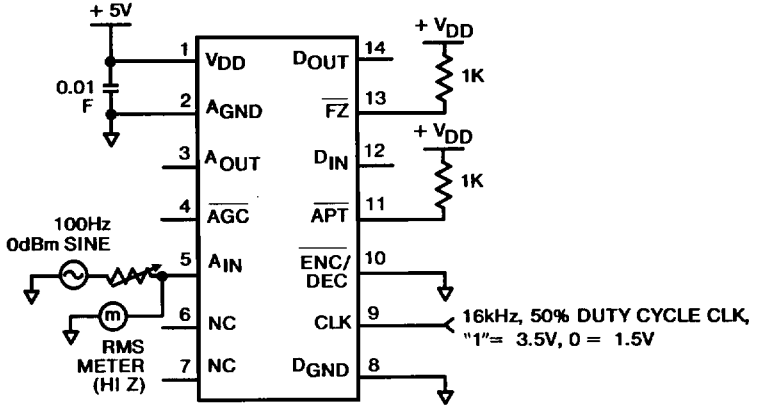
Test Configuration (Continued)

TEST: Z_{IN}, AUDIO OUTPUT IMPEDENCE



TEST: Z_{IN}, AUDIO INPUT IMPEDENCE



NOTES:

A: Clocked statically for 3 cycles.

B: Clocked statically for 5 cycles.

C: Clock used for Clock Sampling Rate test is a variable frequency square wave.Clock used for Clock Duty Cycle test is 16kHz variable duty cycle. All levels of clock are 3.5 = high and 1.5 = low. Clock used for Transfer Gain, Audio Input/Output and Resolution test is 16kHz 50% duty cycle.