DN74LS114 N74LS114

Dual J-K Negative Edge-Triggered Flip-Flops (with Set, Common Reset and Common Clock)

■ Description

DN74LS114 contains two negative-edge triggered J-K flip-flop circuits with common clock-CP and direct-coupled reset input terminals, and independent J, K, and direct-coupled set input terminals.

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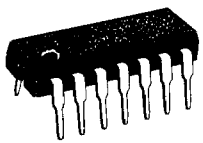


14-pin plastic DIL package

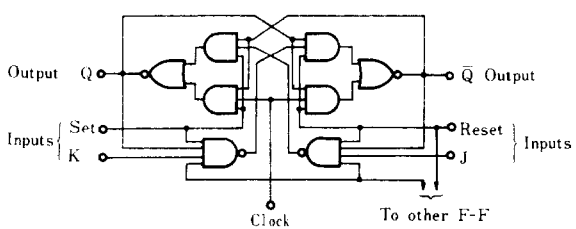
P-4

14-pin Panaflat package (SO-14D)

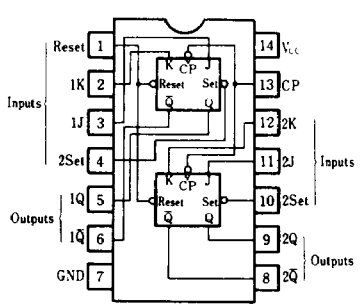
■ Features

- Negative-edge trigger
- Common clock and direct-coupled reset inputs
- Independent direct-coupled set input
- Q and $\overline{Q}$ outputs
- Wide operating temperature range (Ta = −20 to +75°C)

■ Logic diagram (1/2)



Pin configuration (top view)



■ Recommended operating conditions

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Parameter		Sym	Min	Typ	Max	Unit
Supply voltage		V_{CC}	4.75	5.00	5.25	V
Output current		I_{OH}			−400	μA
		I_{OL}			8	mA
Operating temperature range		Topr	−20	25	75	℃
Clock frequency		f_{clock}	0		30	MHz
Pulse width	Clock High	t_w	20			ns
	Set or Reset Low		25			ns
Set-up time	HIGH data	t_{su}	20 ↓			ns
	LOW data		20 ↓			ns
Hold time		t_h	0 ↓			ns

Notes

1. ↓: Indicates fall edge of standard clock pulse.

■ DC characteristics ($Ta = -20 \sim +75℃$)

Parameter		Sym	Test conditions		Min	Typ*	Max	Unit
Input voltage		V_{IH}			2.0			V
		V_{IL}					0.8	V
Output voltage		V_{OH}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$, $I_{OH}=-400\mu A$		2.7	3.4		V
		V_{OL1}	$V_{CC}=4.75V$, $V_{IH}=2V$, $V_{IL}=0.8V$	$I_{OL}=4mA$		0.25	0.4	V
		V_{OL2}		$I_{OL}=8mA$		0.35	0.5	V
Input current	J-K	I_{IH}	$V_{CC}=5.25V$, $V_I=2.7V$				20	μA
	Reset						120	μA
	Set						60	μA
	Clock						160	μA
	J-K	I_{IL}	$V_{CC}=5.25V$, $V_I=0.4V$				−0.4	mA
	Reset						−1.6	mA
	Set						−0.8	mA
	Clock						−1.6	mA
	J-K	I_I	$V_{CC}=5.25V$, $V_I=7V$				0.1	mA
	Reset						0.6	mA
	Set						0.3	mA
	Clock						0.8	mA
Output short circuit current**		I_{OS}	$V_{CC}=5.25V$, $V_O=0V$		−15		−100	mA
Input clamp voltage		V_{IK}	$V_{CC}=4.75V$, $I_I=-18mA$				−1.5	V
Supply current***		I_{CC}	$V_{CC}=5.25V$			4	8	mA

* When constant at V_{CC} = 5V, Ta = 25°C.

** Only one output at a time short circuited to GND. Also, short circuit time to GND within 1 second.

*** Measured with all outputs open, Q and $\overline{Q}$ outputs alternately HIGH, and clock inputs grounded.

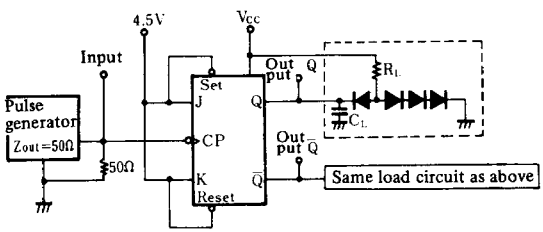
■ Switching characteristics ($V_{CC}=5V$, $Ta=25℃$)

Parameter	Sym	Inputs	Outputs	Test conditions	Min	Typ	Max	Unit
Maximum clock frequency	f_{max}			$C_L=15pF$, $R_L=2k\Omega$	30	45		MHz
Propagation delay time	t_{PLH}	Reset, Set, Clock	Q, $\overline{Q}$			11	20	ns
	t_{PHL}					15	30	ns

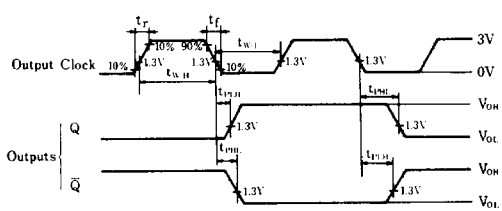
※ Switching parameter measurement information

〔1〕 f_{max}, t_{PLH}, t_{PHL} (Clock → Q, $\overline{Q}$)

1. Measurement circuit



2. Waveforms

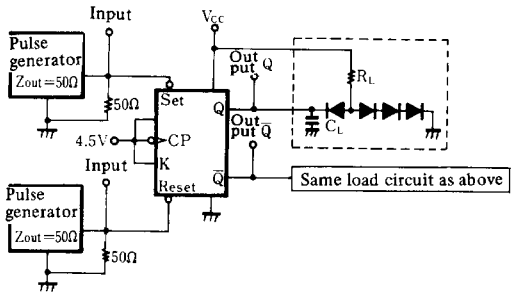


1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161 or equivalent.

1. Clock input waveform: $t_r \leqq 15ns$, $t_f \leqq 6ns$, PRR=1MHz, duty cycle 50%
2. When measuring f_{max}, t_r and $t_f \leqq 2.5ns$.

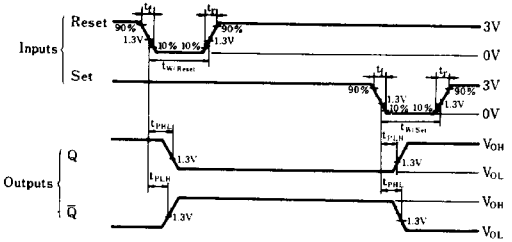
〔2〕 t_{PLH}, t_{PHL}(Reset, Set → Q, $\overline{Q}$)

1. Measurement circuit



1. Measurement made for each flip flop.
2. C_L includes probe and tool floating capacitance.
3. Diodes are all MA161.

2. Waveforms



Notes
1. Reset, Set Input waveform: $t_r \leq 15ns$, $t_f \leq 6ns$, PRR=1MHz

■ Truth tables

Inputs					Outputs	
Set	Reset	Clock	J	K	Q	$\overline{Q}$
L	H	×	×	×	H	L
H	L	×	×	×	L	H
L	L	×	×	×	H*	H*
H	H	↓	L	L	Q_0	$\overline{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	Toggle	
H	H	H	×	×	Q_0	$\overline{Q}_0$

Notes
1. H: HIGH voltage level.
2. L: LOW voltage level.
3. X: Either HIGH or LOW; doesn't matter.
4. ↓: Change from HIGH to LOW.
5. Q_0: Q level prior to determination of input condition shown in table.
6. $\overline{Q}_0$: $\overline{Q}$ level prior to determination of input condition shown intable.
7. Toggle: With ↓ change, outputs become compliment of previous condition.
8. H*: When set and reset are LOW, Q and $\overline{Q}$ are HIGH; however, when set and reset simultaneously change to HIGH, requirements of Q and $\overline{Q}$ cannot be predicted.