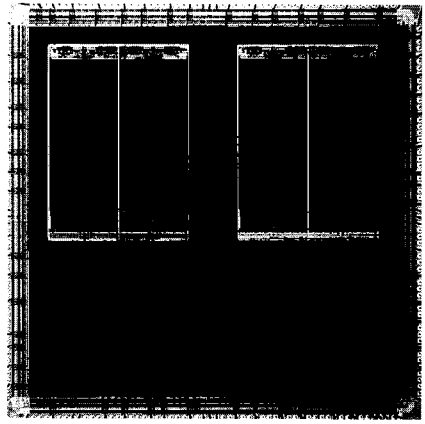
L64250 Histogram/Hough Transform Processor (HHP)

LSI LOGIC

Description

The L64250 computes histograms and modified Hough transforms for data sets up to 2^{24} points or images up to 4096 x 4096 pixels. In addition, pixel location operations may be performed in which the X and Y coordinates of pixels of designated grey values are stored. Data rates up to 20 MHz and data precisions up to nine bits are accommodated.



L64250 Chip

Features

- Histogram and Hough transform calculation performed on images up to 4096 x 4096 pixels
- Four 512 x 9 look-up tables provided to perform user-defined point-wise transformations
- Real-time histogram equalization
- High data rates

Commercial	Military
20 MHz	16 MHz
15 MHz	12 MHz

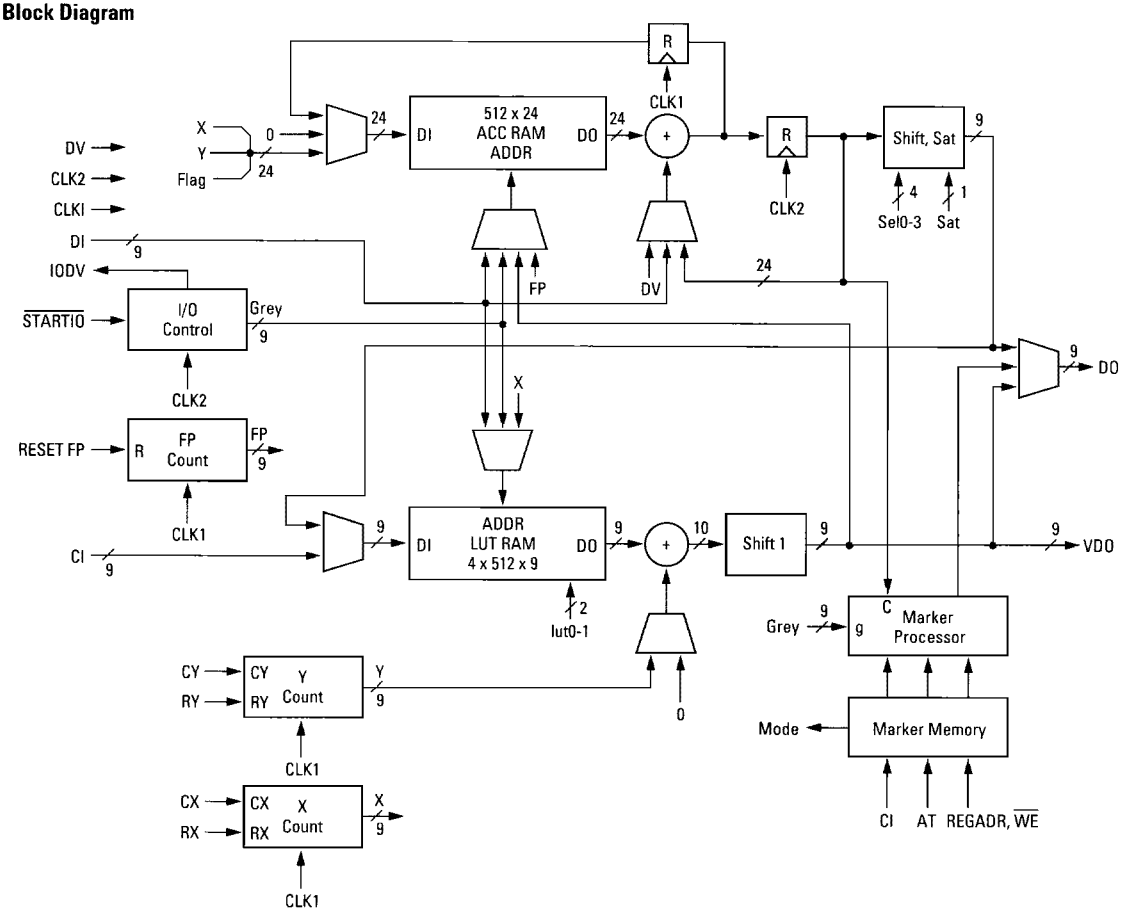
- Two system clocks provided for different pixel and host controller data rates
- Marker circuit allows users to flag points of interest on the histogram, modified Hough transform or accumulated histogram
- Available in a 68-pin CPGA (Ceramic Pin Grid Array) or 68-pin PLCC (Plastic Leaded Chip Carrier) package

Architecture

The architecture of the L64250 accommodates the implementation of multiple algorithms with the same memory-based circuitry. The particular operation that is to be performed is defined via a group of mode latches. The accumulation memory (ACC RAM) holds the histogram, modified Hough transform partial results or the X and Y pixel coordinates. Four 512 x 9 LUT RAMs hold any combination of the histogram-equalized transfer functions, the function needed to perform the modified Hough transform ($X\tan\phi$ or $Y\cot\phi$) or a table indicating which pixel locations should be stored. The X and Y counters are used when performing modified Hough transforms and pixel location and contain the X and Y coordinates within the image. The LUT, adder and counters compute the Hough transform parameter for each point in the image. The user controls the X and Y counters via the count (CX, CY) and reset (RX, RY) pins. The I/O controller is used to generate addresses for the RAMs when reading results from the processor or loading the LUTs. The processor output comes from either the ACC RAM, the LUT RAM or the marker memory depending on the type of operation being performed.

Two clocks control the flow of data in the system. CLK 1 is the pixel or input data clock. CLK2 is provided to allow the user to read data from or write data into the RAMs at a lower rate than the data input rate. CLK2 can be tied to CLK1 when all operations are performed at the data input rate (e.g. histogram equalization).

Block Diagram



Pin Description Summary

Pin	No. of Pins	I/O	Description
DI.0–DI.8	9	I	Data Input used to compute histogram or projection.
DV	1	I	Signifies that current DI value is valid when HIGH.
DO.0–DO.8	9	O	ACC RAM or LUT RAM data output (uses CLK2). Holds selected marker register data when AT is HIGH.
IODV	1	O	When HIGH, ACC RAM or LUT RAM data on the DO bus is valid.
VDO.0–VDO.8	9	O	LUT RAM data output (uses CLK1).
CIO.0–CIO.8	9	I	Control register and LUT input data bus.
$\overline{WE}$	1	I	Used to strobe data into mode latches when LOW.
REGADR.0–REGADR.5	6	I	Selects mode latch, marker or maximum registers.
AT	1	I	Selects marker and maximum registers when HIGH or mode latches when LOW. AT must be LOW to access the LUT or ACC RAMs via the DO bus.
CLK1	1	I	Pixel clock active at rising edge.
CLK2	1	I	User I/O clock (may be connected to CLK1).
$\overline{STARTIO}$	1	I	Initiates RAM I/O at HIGH to LOW transition.
CX, CY	2	I	Used to increment X or Y counters when HIGH.
RX, RY	2	I	Resets X or Y counters (overrides CX, CY) when HIGH.
RESET FP	1	I	Resets FP counter when HIGH.
PO	1	O	Test pin (LSI Logic use) should be left unconnected.

Note: The highest bit number represents the most significant bit.

Functional Overview

The L64250 can be configured to perform a number of tasks including histograms, modified Hough transforms and pixel location. Each of these functions can be broken down into three modes of operation: computation, I/O and initialization.

The computation mode of operation would typically occur during the display period of a video frame. During this period the histogram, modified Hough transform or pixel location data is computed. If equalization is being performed, the input data would also be equalized during the computation mode.

The I/O mode would typically occur during the vertical blanking time (or any other time the processor is not busy) and may be used to transfer data from the ACC RAM to an off-chip host or from the ACC RAM to the LUT RAM. The user may also use this period to read or write the LUT. For all operations, the active LUT is determined by lut0-lut1 control bits (see Initialization section). The I/O mode is initiated by asserting the $\overline{STARTIO}$ signal (active LOW). The I/O mode terminates after 512 read or write cycles or when $\overline{STARTIO}$ returns HIGH. Normal operation then resumes.

A "marker" processor is also available to quickly find points of interest on the histogram, modified Hough transform or accumulated histogram curves. The user can specify up to seven values on the grey level axis (for histograms) or the Hough transform parameter axis and obtain the corresponding value on the accumulation axis. Conversely, the user can specify accumulation values of interest and obtain the corresponding grey values. These functions allow users to quickly locate points of interest without reading the entire ACC RAM. The processor must, however, be put in the I/O mode to update the markers. The maximum value and the position of the maximum value are also computed.

Initialization defines the function to be performed, and determines the flow of data in the processor. The particular operation is determined by the values in the mode latches.

Computation Modes

Histogram Computation

When computing the histogram of a signal, the ACC RAM and the LUT form the active elements of the data path. The ACC RAM stores the histogram while the LUT may be used to implement a user-defined transfer function. The address of the ACC RAM is the DI signal. When the DV signal is HIGH, the value in the addressed bin is incremented. If DV is LOW, no computation takes place that cycle. The DV signal is used to ignore blanking signals or compute the histogram over a sub-region of the image. When all values have been processed, the RAM can be read as described in the I/O mode section. The histogramming operation is described by the following equation:

$$M[I(x,y)] \leftarrow M[I(x,y)]+DV$$

where I(x,y)=DI is the image intensity at the point (x,y) and M[x] is the value stored at the location x in the ACC RAM.

The LUT is not used in the computation of the histogram and can concurrently modify the image by a user-defined transfer function. The DI signal addresses the LUT and the LUT data appears on the VDO output pins two clock cycles later.

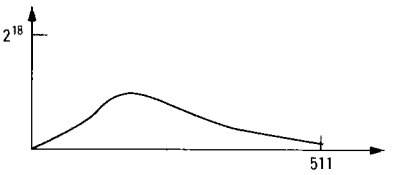
Histogram equalization can also be performed in real time. Typically CLK2 would be connected to CLK1 and $\overline{\text{STARTIO}}$ would be connected to the vertical blank signal. The histogram is stored in the ACC RAM. During the vertical blanking period, the equalization transfer function will be computed and transferred into the LUT RAM. The equalization transfer function for each input value of x, $0 \leq x \leq 511$, is characterized by:

$$f(x)= \frac{L}{N} \sum_{i=0}^{x} M[i]$$

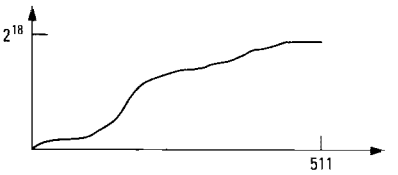
where L is the largest grey value and N is the number of pixels in the input window.

For values of L/N that are very close to a power of two, this operation can be performed on-chip. In the next frame, as a new histogram is being computed, data will also be equalized in real time and passed to the VDO output pins. An example, using a 512 x 512 image is shown.

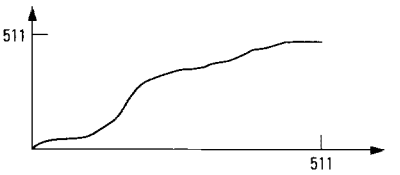
Histogram for 512 x 512 Image



Accumulation Histogram



Histogram Equalization Transfer Function



Hough Transform Computation

The L64250 also has the capability to compute modified Hough transforms. The ACC RAM will store the projection of the image along lines parameterized by r, the Y intercept of the line, and ϕ, the negative angle of the line. A single L64250 will accumulate the input signal DI over lines of constant r for a single value of ϕ. With multiple L64250s the range of ϕ can be expanded.

The algorithm implemented in the L64250 has four different parameterizations which depend on ϕ. The parameter r is given as a function of ϕ in the following table. The function to be loaded into one of the four LUTs and the use of the CX, CY, RX and RY pins are listed in the table.

Computation Modes (Continued)

Modified Hough Transform Parameterization

Case	ϕ	r(X, Y, ϕ)	LUT[i]	CX, RX Controls	CY, RY Controls
1a	$0 \le \phi < 45$	X tanϕ + Y	i tanϕ	X	Y
1b	$45 \le \phi < 90$	Y cotϕ + X	i cotϕ	Y	X
1c	$90 \le \phi < 135$	(YMAX - Y) cot (180 - ϕ) + X	(YMAX - i) cot (180 - ϕ)	Y	X
1d	$135 \le \phi < 180$	(XMAX - X) tan (180 - ϕ) + Y	(XMAX - i) tan (180 - ϕ)	X	Y

These four parameterizations keep r in the range from 0 to 1023 for all ϕ, $0 \le \phi \le 180$, for images of size up to 512 x 512. The use of YMAX and XMAX in parameterizations 1c and 1d prevents r from becoming negative for angles greater than 90. A shifter, controlled by internal signal sh1, determines which 9 bits of the 10-bit value of r to use as the ACC RAM address.

It can be seen that all of the equations for r can be broken down into the form f(X) + Y or f(Y) + X. The LUT is used to perform the function, f( ) and the addition is performed by an adder. Note that the X value is controlled by the CX, RX pins when f(X) is computed by the LUT and the Y value is controlled by the CX, RX pins when f(Y) is computed by the LUT.

The value of r at each point is computed using the LUT and an adder. During initialization, the LUT is loaded with the appropriate transfer function to compute f(x) or f(y). Once the LUT is loaded, the X and Y counters are used to generate the proper memory addresses. The X counter is incremented at each valid pixel and reset at the beginning of each line. The Y counter is incremented at the beginning of each line and reset at the beginning of each frame. As each pixel location along a line of constant r is addressed, the grey value at that point is added to the partial sum in the memory location r. The modified Hough transform operation is described by the following equation:

$$M[r(X,Y,\phi)] \leftarrow M[r(X,Y,\phi)] + DV \bullet I(X,Y)$$

A single processor can compute the projections for 512 values of r and a single value of ϕ. With multiple chips, each operating with a different value of ϕ, the full modified Hough transform may be computed. If some bound on ϕ is known in advance, fewer processors will be needed. Alternatively, a single L64250 could process an image in multiple passes, using a different value of ϕ in each pass. For very large images (which have more than 512 values of r for a particular value of ϕ), the image can be processed in subsections or the resolution of r can be reduced by incrementing the X and Y counters less frequently. Note that the counter marked X in the block diagram is actually used to hold the Y value and the counter Y holds the X value when $135° > \phi \ge 45°$. In this case, the user would use the CX, RX pins to control the Y value and the CY, RY pins to control the X value.

Intensity Averaging

Another computational mode is possible by generating ACC RAM addresses differently. An example of this is to compute the average intensity of an image as a function of position. Consider a 512 x 512 pixel image divided into 256 blocks (16 x 16) of 32 x 32 pixels each. To compute the average intensity, the Y counter would be incremented every 32 pixels and reset at the beginning of each line. The X counter would be incremented every 32 lines and reset at the beginning of a frame. The proper addresses will be generated by multiplying the X counter output by 16 (this is done via the LUT). After processing, the first 256 locations of the ACC RAM will hold the accumulated intensity in each 32 x 32 region. Setting sel0–3 = 10 will give the average intensity in each region.

Pixel Location

Pixel location is used to determine the X and Y coordinates of up to 64 specific pixels or group of pixels in an image. When performing pixel location, the user first loads one of the LUTs with a table indicating which pixels are of interest. Each pixel in the table is assigned a 6-bit flag that allows the user to distinguish groups of pixels.

Each time an interesting pixel (as specified in the LUT) is found, the X, Y and flag values are stored in the ACC RAM at the address given by the FP counter. The FP counter is then incremented. Note that only 512 values can be stored at any instance. In the event that more values are stored, the first RAM locations will be overwritten.

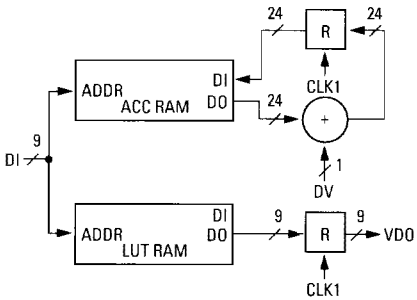
Computation Mode Data Flow

In each of the computation modes described in the previous section many of the same processing elements are used in a slightly different manner to accomplish various algorithms. The following sections detail the flow of data in each case.

Histogram Processing

In this mode pixel data presented on the DI bus addresses both the ACC RAM and the LUT. CLK1 controls the writing of the RAM, with DV determining whether data at a particular address will be incremented or not. The data on the DI bus is concurrently modified by a transfer function stored in the LUT. The transformed data will appear on the VDO bus two clock cycles after addressing the LUT.

Histogram Processing Diagram



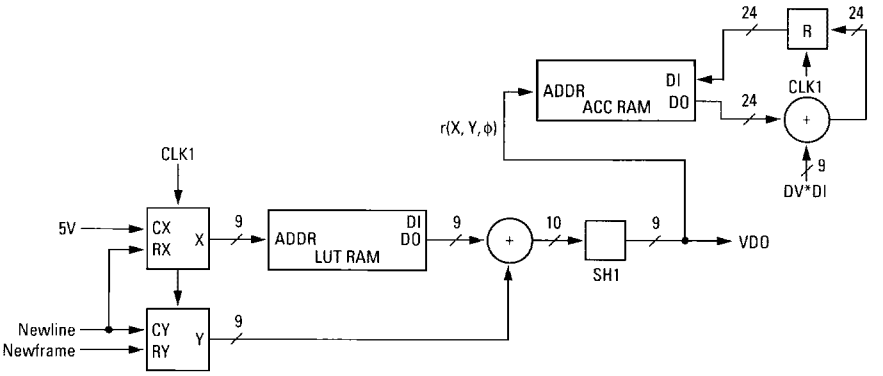
Hough Transform/Intensity Averaging

When performing the Hough transform, the X and Y counters are used to generate the proper address for the LUT RAM. CLK1 increments the X count every time a new DI value appears, and is reset at the beginning of a line. The value in the X counter is modified by the LUT. The Y counter is incremented at the beginning of a line and reset at the beginning of a frame. Note that for $135° > \phi \geq 45°$ the definition of the X and Y counters are reversed. The output of the LUT and the Y counter are then summed to form the address for the ACC RAM. The modified Hough transform address is also output on the VDO pins. The user does not need to be concerned with the synchronization of data and address because all pipeline skews are compensated internally. When RX and RY are reset, DI is assumed to be the (0,0) pixel.

SH1 is included in the address generation data path to allow the user to select the most significant or least significant 9 bits of the 10-bit value of r. For angles near 0° and 90° the least significant 9 bits would be most useful, while angles between these boundaries would best be represented by the most significant 9 bits.

Pixel Location

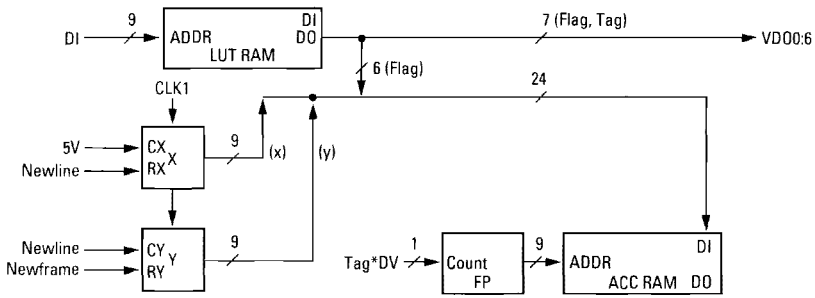
Pixel location uses the LUT and the X and Y counters to store a 6-bit code and location information about pixels of interest. The X and Y counters hold the coordinates of the grey value on the DI pins and are controlled in the same manner described in the Hough transform section. DI addresses the LUT producing a 1-bit tag and a 6-bit flag associated with the grey value. If the tag bit is HIGH and DV is HIGH the 6-bit flag and the X, Y coordinates are stored in the ACC RAM. Storage space is assigned sequentially as defined by the FP counter.



Modified Hough Transform Processing ($\phi \leq 45°$)

Computation Mode Data Flow (Continued)

Pixel Location Processing



I/O Mode

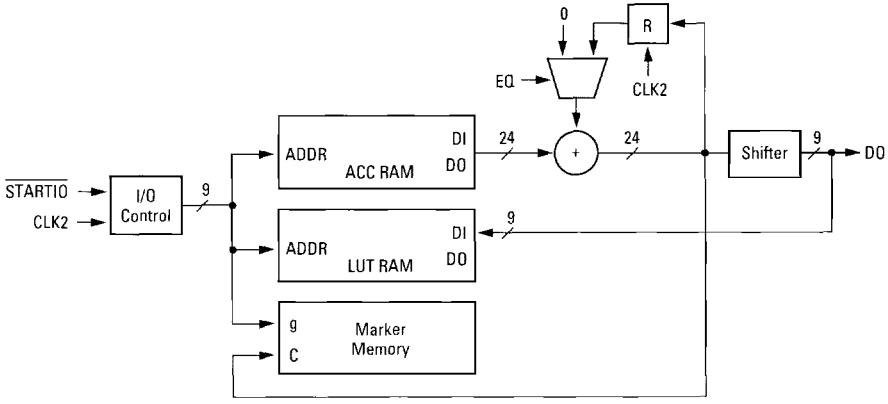
Once a computation has taken place, the user reads data from the LUT or the ACC RAM. These operations typically take place during a vertical retrace or some other period when the processor is not busy and AT is LOW. This mode is also to load the LUT with the desired transfer function. Generally, these operations are controlled by CLK2 so that data may be read or written at a different rate than the pixel clock. If the ACC RAM is accessed, the marker values will be updated.

The internal signals hclr0-hclr1 control whether or not the ACC RAM is cleared during I/O operations. If both hclr0 and hclr1 are HIGH then the ACC RAM will not be cleared during any I/O operation. If hclr0 is HIGH and hclr1 LOW, then each ACC RAM location will be cleared after it is read. If both hclr0 and hclr1 are LOW then each ACC RAM location is cleared when either the ACC RAM location or the corresponding LUT RAM location is accessed.

Read/Transfer ACC RAM

Once the histogram has been computed and stored in the ACC RAM, the user asserts $\overline{\text{STARTIO}}$ LOW to initiate reading of the data. One data value is read out of the ACC RAM during each clock cycle of CLK2 starting with address 0. If $\overline{\text{STARTIO}}$ remains LOW, all 512 data values will be read in sequential address order and the processor will return to pixel processing mode after 512 clock cycles. If $\overline{\text{STARTIO}}$ is returned HIGH, the I/O mode halts and the user can return to pixel processing operations. When the output flag IODV is HIGH, the processor has placed valid data from the LUT or ACC RAMs onto the I/O bus.

The user controls the destination of the ACC RAM data via the io0-1 bits in the control memory. Code 01 signifies that histogram data will be placed on the DO output bus, while code 00 will transfer data from the ACC RAM to the LUT RAM.



I/O Mode
(Continued)

In both cases the user can modify the histogram data. By setting the internal EQ control bit HIGH, an accumulated histogram will be output. Typically this would be useful when storing an equalization transfer function in the LUT. The shifter allows the user to determine which 9 bits of the 24-bit ACC RAM output will be directed to the DO bus and LUT RAM. Additional control over the output format can be obtained via the SAT pin in the control memory. When SAT is high, the resultant 9-bit shifted output will be forced to 511 (111111111) if overflow occurs in the shifter.

Marker Circuitry

When ACC RAM data is accessed, the marker circuitry in the marker memory is updated. The user can specify up to seven values of grey level and the associated count will be stored in the mode memory. Setting FUNC = 1 in the control memory will accomplish this. By setting FUNC = 0, the user can specify a particular count and the marker memory will be updated with the last grey value whose count is equal to (or just exceeds) the count of interest. More precisely, these operations are defined by the following equations:

if FUNC = 1, $C \leftarrow A[g]$
if FUNC = 0 $g \leftarrow$ largest value of i such that $A[i] \geq C$ and $A[i-1] < C$

where A[i] is the value stored in the ACC RAM at location i, C is the count stored in the marker memory and g is the grey value stored in the marker memory.

The maximum count, and the grey value which it occurred at, are also updated during each I/O cycle and stored in mode memory locations 0-3. This operation is defined by the following equations for the count M and grey value g:

$g \leftarrow$ the smallest i such that $A[i] \geq A[j]$,
where $0 \leq i, j < N$
$M \leftarrow A[g]$

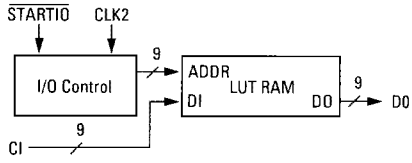
where N is the number of ACC RAM elements read.

If the accumulated histogram is being computed, i.e. the eq bit is set, then the maximum count register (M) will be equal to the number of pixels scanned, and the grey value will be the maximum grey level occurring in the image.

Reading and Writing LUT

Data input to and output from the LUT RAM is also controlled by CLK2 and $\overline{\text{STARTIO}}$. On the falling edge of $\overline{\text{STARTIO}}$, the I/O cycle is initiated with the LUT RAM addresses being read or written sequentially with each cycle of CLK2.

Reading and Writing LUT



LUT read/write operations are defined by the io0-1 bits in the control memory. Code 10 is used to read the LUT RAM. Data will be read sequentially and output on the DO bus. To write the LUT RAM, code 11 is used in the control memory. Input from the CI bus is stored in successive addresses with each cycle of CLK2.

The LUT RAM can also be addressed from the DI bus. A typical application would be histogram equalization. The LUT would contain the equalized transfer function generated by transferring ACC RAM data to the LUT with EQ high. Setting the FN0-FN1 bits for histogram computation configures data from the DI bus to address both the ACC RAM and the LUT. Equalized data is then output on the VDO bus. Histogram computation is taking place concurrently. In this case CLK2 should be connected to CLK1 to achieve an equalization rate equal to the pixel rate.

Initialization

The operation of the L64250 is defined by the mode and marker memories which store 66 9-bit words that define the operation of the part, contain marker information and set LSI Logic test modes. REGADR is used to select the proper register. Data is written over the CI bus and read on the DO bus. The AT pin controls whether data is a mode word or a marker. To prevent erroneous operation STARTIO should be high, IODV should be low and DV should be low during initialization.

Mode Memory

AT	REGADR	R/W	Bit Location								
		W	CI.0	CI.1	CI.2	CI.3	CI.4	CI.5	CI.6	CI.7	CI.8
		R	DO.0	DO.1	DO.2	DO.3	DO.4	DO.5	DO.6	DO.7	DO.8
0	0	W	sel0	sel1	sel2	sel3	lut0	lut1	sh1	sat	$\overline{\text{test}}$
0	1	W	fn0	fn1	eq	io0	io1	hclr0	hclr1	func	pdwn

Marker Memory

AT	REGADR	R/W	Contents
1	0	R	grey level of maximum acc count bits 0–8
1	1	R	maximum acc count bits 0–8
1	2	R	maximum acc count bits 9–17
1	3	R	maximum acc count bits 18–23*
1	16	W	test mode, do not access
1	17	W	test mode, do not access
1	18	W	test mode, do not access
1	19	W	test mode, do not access
1	32	R/W	R/W marker 0 grey level bits 0–8
1	33	R/W	R/W marker 0 acc count bits 0–8
1	34	R/W	R/W marker 0 acc count bits 9–17
1	35	R/W	R/W marker 0 acc count bits 18–23*
1	36	R/W	R/W marker 1 grey level bits 0–8
1	37	R/W	R/W marker 1 acc count bits 0–8
1	38	R/W	R/W marker 1 acc count bits 9–17
1	39	R/W	R/W marker 1 acc count bits 18-23*
			•
			•
			•
1	56	R/W	R/W marker 6 grey level bits 0–8
1	57	R/W	R/W marker 6 acc count bits 0–8
1	58	R/W	R/W marker 6 acc count bits 9–17
1	59	R/W	R/W marker 6 acc count bits 18–23*

* acc count bit 18-23 appears on bit location 0-5 respectively.

Mode Definitions

sel0-sel3: Selects 9 bits from the 24-bit output of the ACC RAM to be transferred to the DO output or to the LUT RAM.

sel0	sel1	sel2	sel3	sel	Window
0	0	0	0	0	select bits 0–8
1	0	0	0	1	select bits 1–9
0	1	0	0	2	select bits 2–10
1	1	0	0	3	select bits 3–11
0	0	1	0	4	select bits 4–12
•••					
1	1	1	1	15	select bits 15–23

lut0-lut1: Defines one of the four 512 x 9 LUTs as active.

sh1: When LOW, the least significant 9 bits of the 10-bit LUT and Y count sum will address the ACC RAM. When HIGH, the 9 most significant bits of the sum will be used.

sat: When HIGH, the 9 bits selected from the 24-bit ACC RAM output will be forced to 511 (111111111) if the 24-bit ACC RAM output contains a 1 in the range of bits from the sel + 9 to 23. Otherwise the 9 bits selected from the ACC RAM output will be unchanged.

$\overline{\text{test}}$: Used for testing when LOW. Should be HIGH for normal operation.

fn0-fn1: Determines the operation performed during the computational mode.

Mode Definitions (Continued)

fn0	fn1	Function
0	0	modified Hough transform computation
0	1	undefined
1	0	histogram computation
1	1	pixel location

eq: When HIGH, causes the output of the ACC RAM to be accumulated as it is read. This is commonly used to compute the histogram equalization transfer function. When LOW, the ACC RAM output is not modified.

io0-io1: Control the operations of the ACC and LUT RAMs during I/O mode (when the STARTIO signal has been asserted).

io0	io1	Function
0	0	transfer data from the ACC RAM to the LUT RAM
0	1	read the ACC RAM (data read from DO)
1	0	read the LUT RAM (data read from DO)
1	1	write the LUT RAM (data written from CI)

hclr0-hclr1: Control the clearing of the ACC RAM during I/O mode.

hclr0	hclr1	Function
0	0	ACC RAM cleared when either the ACC RAM or LUT RAM is accessed
0	1	undefined
1	0	ACC RAM cleared only when the ACC RAM is accessed
1	1	ACC RAM not cleared during an I/O operation

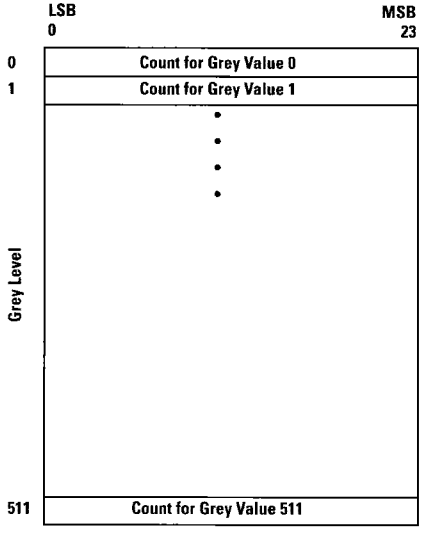
func: Determines the function performed by the marker processor. When HIGH, each marker circuit within the processor will locate an accumulated count from the ACC RAM corresponding to the previously given grey value. When LOW, each marker will locate the grey value corresponding to a previously given accumulation count from the ACC RAM.

pdwn: When HIGH, the ACC and LUT RAMs are placed in a inactive mode. Should be LOW for normal operation.

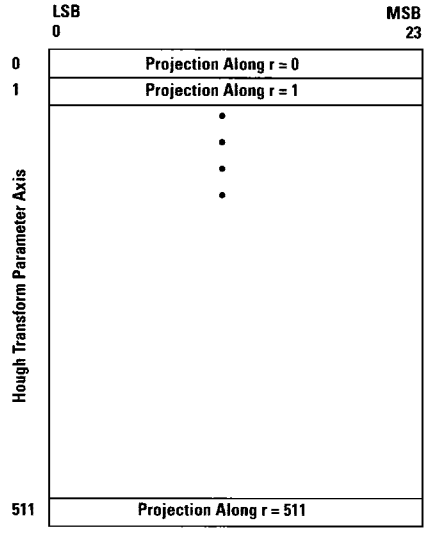
Memory Configurations

The following memory maps specify the configuration of the ACC RAM and the LUT RAM in the various computational modes.

ACC RAM Histogram Mode

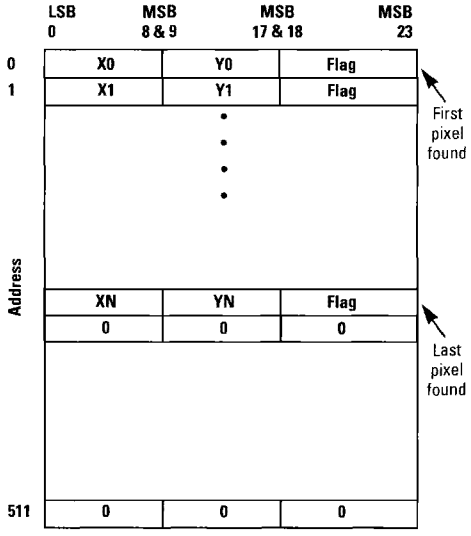


ACC RAM Modified Hough Transform Mode

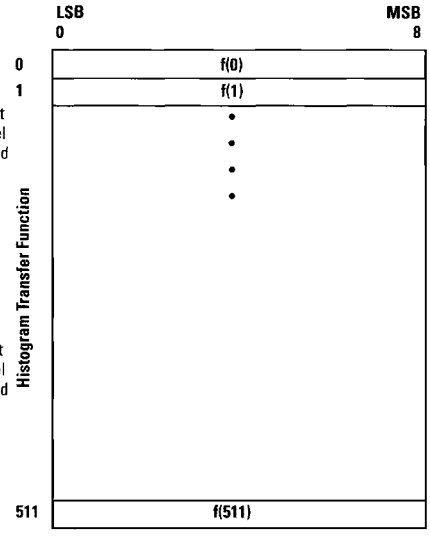


Memory Configurations (Continued)

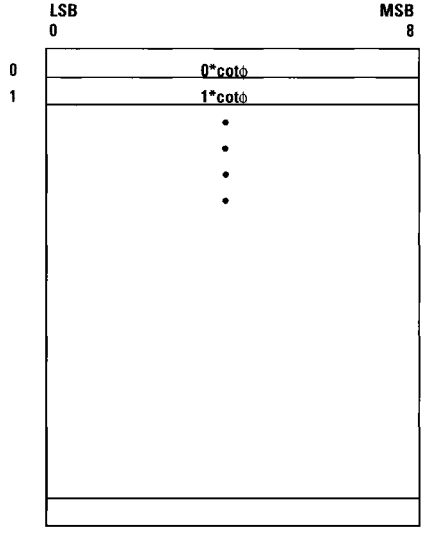
ACC RAM Find Pixel Mode



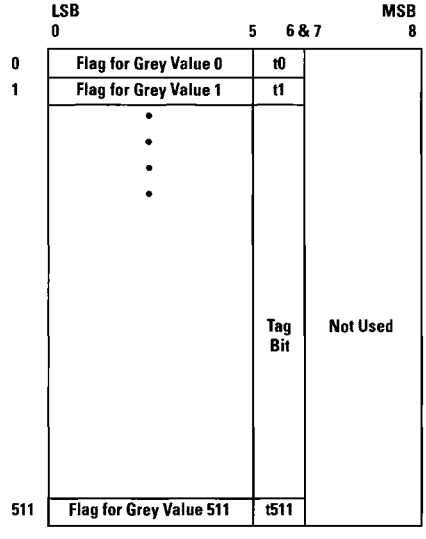
LUT RAM Histogram Computation



LUT RAM Hough Transform Mode ($45° < \phi \leq 90°$)



LUT RAM Find Pixel Mode



Note: For other ϕ values the LUT will contain different functions.

I/O Sequences

Read ACC, Read LUT, Transfer ACC to LUT
I/O operations can be divided into two groups: those that end before all 512 elements of the ACC or LUT RAM have been accessed (short cycle) and those that end after all 512 elements have been accessed (long cycle). All I/O cycles are initiated by a HIGH to LOW transition of $\overline{\text{STARTIO}}$. AT must be LOW in each case.

The short cycle is terminated when $\overline{\text{STARTIO}}$ is returned HIGH before all elements of the RAM have been read. The first data value appears on the DO pins three CLK2 cycles after $\overline{\text{STARTIO}}$ goes LOW. The IODV flag also goes HIGH after three cycles, indicating that the data is valid. After the desired number of memory elements have been read, the user returns $\overline{\text{STARTIO}}$ HIGH. The I/O mode completes three cycles later and IODV returns LOW to indicate the end of the I/O operation. As soon as IODV returns LOW, the processor returns to the pixel processing mode specifically by the mode latches.

The long cycle is terminated without user intervention after all elements of the ACC or LUT RAMs have been accessed. Again, valid data appears on the DO pins three CLK2 cycles after $\overline{\text{STARTIO}}$ goes LOW. In this case, IODV is HIGH for 512 CLK2 cycles and goes LOW after the last RAM element has been read. After IODV returns LOW, $\overline{\text{STARTIO}}$ can remain LOW or be raised HIGH at any time without affecting the operation of the L64250.

Write LUT
The writing of data into the LUT RAM is similar to the operations described above, except that the data to write into the RAM is placed on the CI bus when $\overline{\text{STARTIO}}$ is LOW. However, as described above, the processor will not return to the pixel processing mode until IODV returns LOW.

The net result of this is that the L64250 enters the I/O mode as soon as the $\overline{\text{STARTIO}}$ pin is pulled LOW and does not return to the pixel processing mode until IODV returns LOW. The I/O mode will last N + 3 CLK2 cycles, where N is the number of RAM elements written.

For each of these modes CLK2 must take at least N + 4 LOW to HIGH transitions to ensure proper I/O operation. The first transition occurs with $\overline{\text{STARTIO}}$ HIGH. After IODV returns LOW, CLK2 can remain LOW or continue to make LOW to HIGH transitions.

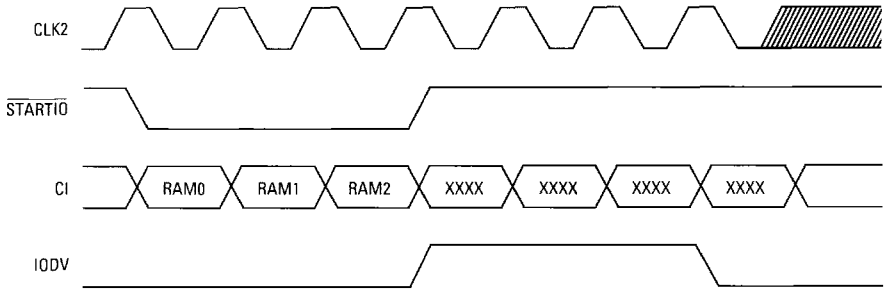
Pixel Processing Mode
When operating in the pixel processing mode, all operations are controlled by CLK1.

The X and Y counters are used when performing modified Hough transforms and pixel location operations. The counter controlling the X value is typically incremented at each valid pixel and is reset at the beginning of each line. The counter controlling the Y value is typically incremented at the beginning of each line and is reset at the beginning of the frame. When no valid data is available, DV is pulled LOW.

The output of the LUT RAM will appear on the VDO bus two CLK1 cycles after the image data appears on the DI bus. This data will either be the modified image (histogram mode), the flag and tag data (find pixel mode) or the modified Hough transform parameter, r (modified Hough transform mode).

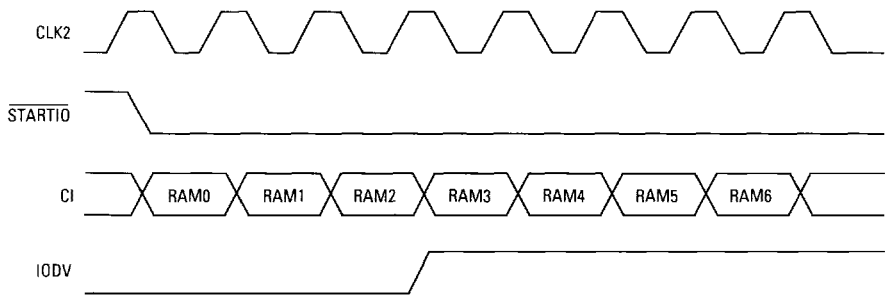
Writing LUT RAM

Short I/O Cycle

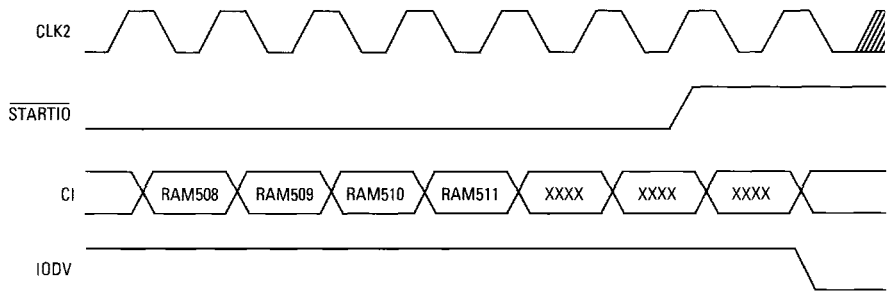


Writing LUT RAM
(Continued)

Start of Long I/O Cycle

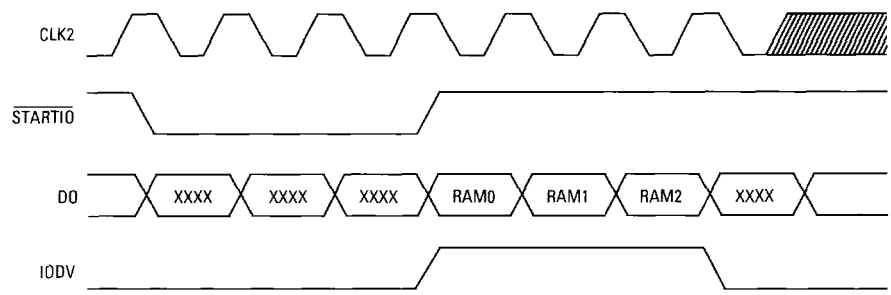


End of Long I/O Cycle



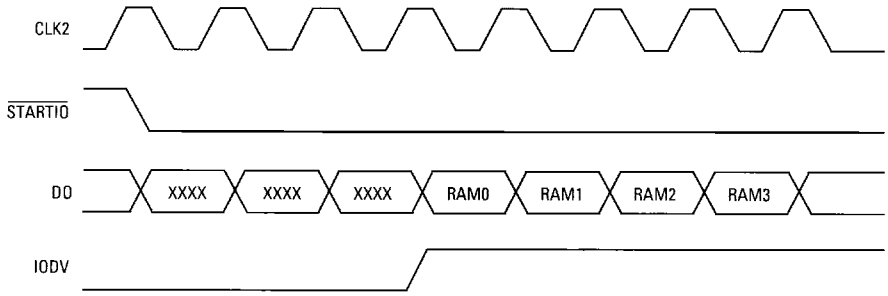
Reading ACC/LUT RAM or Transferring ACC to LUT

Short I/O Cycle

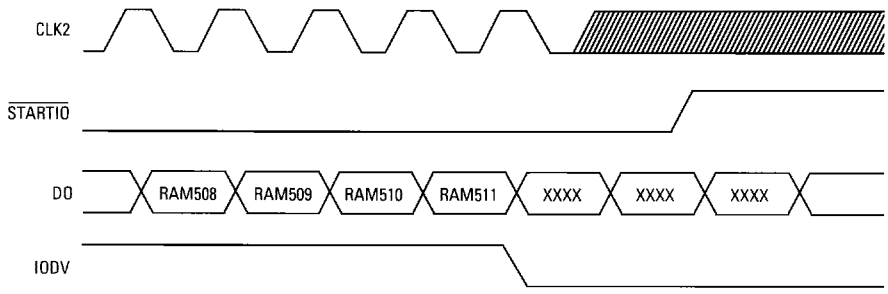


Reading ACC/LUT RAM or Transferring ACC to LUT (Continued)

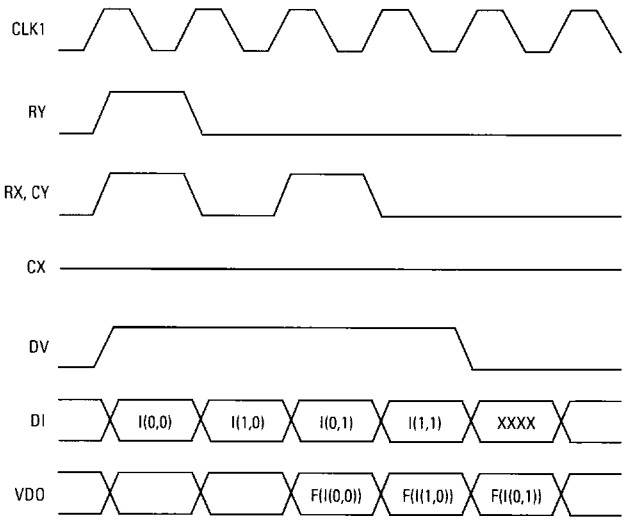
Start of Long I/O Cycle



End of Long I/O Cycle

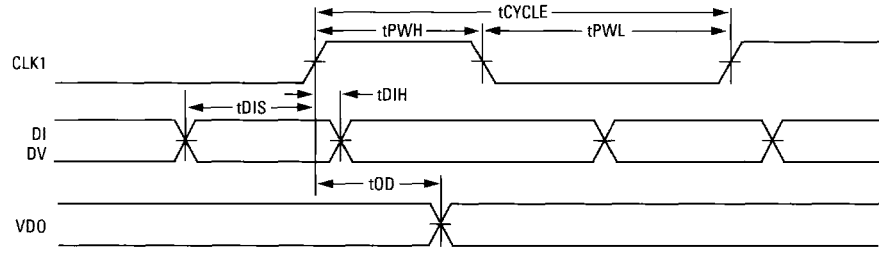


Pixel Processing (Small 2 x 2 Image)



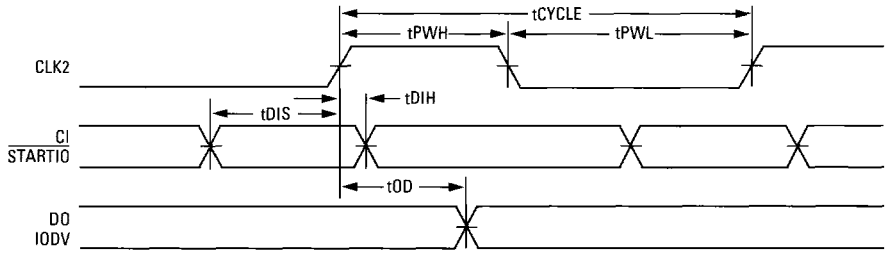
AC Timing Waveforms

Pixel Processing Operation



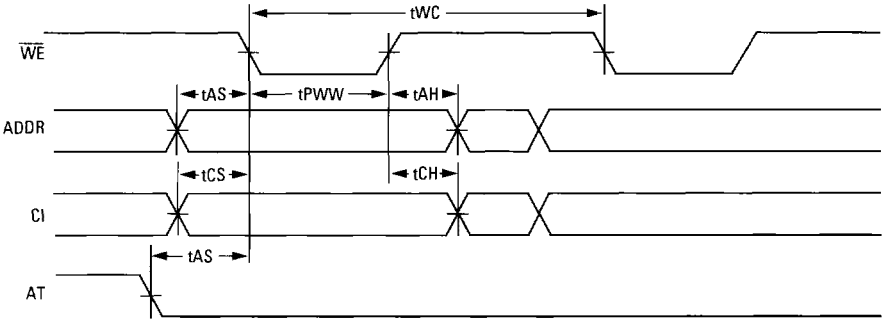
Note: CX, CY, RX, RY, and Reset FP maintain the same set-up and hold time requirements as DI and DV.

I/O Timing



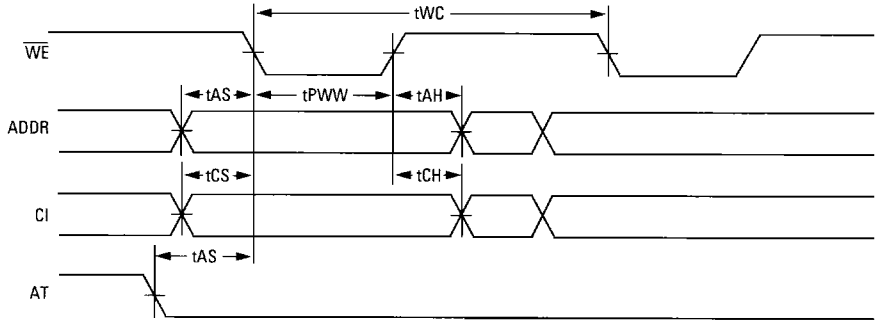
Note: When reading the LUT RAM, ACC RAM or transferring data from the ACC RAM to the LUT, DO is active. When writing the LUT RAM CI is active.

Control Memory Timing – Writing Mode Data



AC Timing Waveforms (Continued)

Control Memory Timing – Reading and Writing Markers



Note: Area 1 contains old marker data.

AC Switching Characteristics: Commercial (TA = 0°C to 70°C, VDD = 4.75 V to 5.25 V)

Symbol	Parameter	L64250-20		L64250-15	
		Min	Max	Min	Max
tCYCLE	Minimum clock cycle time	50		65	
tPWH	Minimum clock pulse width HIGH	20		25	
tPWL	Minimum clock pulse width LOW	20		25	
tDIS	Input data setup time	12		15	
tDIH	Input data hold time	4		5	
tOD	Output delay		12		15
tWC	Minimum $\overline{WE}$ cycle time	150		195	
tPWW	Minimum $\overline{WE}$ pulse width LOW	50		65	
tAS	AT, address setup time	50		65	
tAH	AT, address hold time	50		65	
tCS	Coefficient setup time	50		65	
tCH	Coefficient hold time	50		65	
tADO	Output delay from address valid		20		25
tWD	Output Delay frow $\overline{WE}\downarrow$		40		45

Note: All times are in ns.

AC Switching Characteristics: Military (TA = -55°C to 125°C, VDD = 4.5 V to 5.5 V)

Symbol	Parameter	L64250-16		L64250-12	
		Min	Max	Min	Max
tCYCLE	Minimum clock cycle time	60		75	
tPWH	Minimum clock pulse width HIGH	28		35	
tPWL	Minimum clock pulse width LOW	25		30	
tDIS	Input data setup time	25		30	
tDIH	Input data hold time	7		10	
tOD	Output delay		20		25
tWC	Minimum $\overline{WE}$ cycle time	180		240	
tPWW	Minimum $\overline{WE}$ pulse width LOW	75		90	
tAS	AT, address setup time	75		90	
tAH	AT, address hold time	75		90	
tCS	Coefficient setup time	75		90	
tCH	Coefficient hold time	75		90	
tADO	Output delay from address valid		40		45
tWD	Output Delay frow $\overline{WE}\downarrow$		50		55

Note: All times are in ns.

Operating Characteristics

Absolute Maximum Ratings (Reference to GND)

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	-0.3 to +7	V
Input voltage	VIN	-0.3 to VDD +0.3	V
DC input current	IIN	±10	mA
Storage temperature range	TSTG	-65 to +150	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC supply voltage	VDD	+3 to +6	V
Operating ambient temperature range			
Military	TA	-55 to +125	°C
Commercial	TA	0 to +70	°C

DC Characteristics: Specified at VDD = 5 V over the specified temperature and voltage ranges[1]

Symbol	Parameter	Condition			Min	Typ	Max	Unit
VIL	Low level input voltage						0.8	V
VIH	High level input voltage Commercial temperature range Military temperature range				 2.0 2.25			 V V
IIN	Input current	VIN = VDD			-150		200	µA
VOH	High level output voltage		Comm	Mil				
		IOH =	-4 mA	-3.2 mA	2.4	4.5		V
VOL	Low level output voltage		Comm	Mil				
		IOL =	4 mA	3.2 mA		0.2	0.4	V
IOS	Output short circuit current[2]	VDD = Max, VO = VDD			15		130	mA
		VDD = Max, VO = 0V			-5		-100	mA
IDDQ	Quiescent supply current[3]	VIN = VDD or VSS					15	mA
IDD	Operating supply current	tCYCLE = 50 ns				200		mA
CIN	Input capacitance	Any input				5		pF
COUT	Output capacitance	Any output				10		pF

Notes:
1. Military temperature range is -55°C to +125°C, ±10% power supply; commercial temperature range is 0°C to 70°C, ±5% power supply.
2. Not more than one output should be shorted at a time. Duration of short circuit test must not exceed one second.
3. In power down mode.

Application Example

Histogram Example

The sequence below details various ways in which the L64250 may be used when performing histogram operations.

Initialization – load mode memory with the following words:

AT	REGADR	R/W	CI.0-CI.8
0	0	W	000000001
0	1	W	100011010

This will configure the ACC RAM to clear itself after a read cycle. Once the control words have been written the grey values of interest are read into the marker portion of the mode memory. After initialization an I/O cycle would be performed under control of CLK2. This clears the ACC RAM initially in preparation for normal pixel processing operations. Mode memory word 0 is set for subsequent operations. The control word specifies no shifts to be performed, LUT RAM 0 to be used, the 9 LSBs of the LUT RAM to be output and no saturation of the output.

Pixel Processing – For computing the histogram, mode memory word 1 is reset to retain the grey value information after it has been read. The marker function is set to find the count associated with the grey values specified in the mode memory. Mode memory word 1 is configured as shown below.

AT	REGADR	R/W	CI.0-CI.8
0	1	W	100011110

Histogram computation is then initiated under control of CLK1. Once the histogram has been stored in the ACC RAM, an I/O cycle commences, governed by CLK2. This will update the markers specified in the mode memory. After completion of the I/O cycle, the counts associated with the markers may be read from mode memory.

Application Example
(Continued)

The L64250 may again be reconfigured to compute the accumulated histogram from the data in the ACC RAM. The result is transferred to the LUT. The control word necessary for this function is shown below.

AT	REGADR	R/W	CI.0-CI.8
0	1	W	101000000

The adder on the output of the ACC RAM is enabled during the transfer to compute the accumulated histogram. The clearing function is set to clear the ACC RAM after reading.

Read LUT – The data in the LUT table may also be read. Mode memory word 1 would be configured as follows.

AT	REGADR	R/W	CI.0-CI.8
0	1	W	100100010

An I/O cycle would then read data sequentially from the LUT.

Hough Transform Example
The first step in performing the Hough transform would be identical to that of the histogram operation. The mode memory would be set to clear the ACC RAM. After completion of an I/O cycle the ACC RAM is empty and ready for further processing.

The mode memory would then be set to load the LUT with the tanϕ function. The configuration is shown below.

AT	REGADR	R/W	CI.0-CI.8
0	0	W	000000101
0	1	W	000110000

The function is set for Hough transform, the I/O mode is configured to write the LUT, the nine MSBs will be output and no saturation is needed. An I/O cycle then begins, loading the tanϕ values with each CLK2 pulse.

With the LUT loaded, pixel processing can commence under control of CLK1. The Hough transform is stored in the ACC RAM. After completion of the Hough transform computation, mode memory word 1 is reset to perform an I/O cycle to read the ACC RAM. The control word for such an operation is shown.

AT	REGADR	R/W	CI.0-CI.8
0	1	W	000010000

The ACC RAM contents are read under control of CLK2.

Pixel Location Example
The pixel location operation begins by clearing the ACC RAM and loading the LUT with the pixels of interest. The mode memory is configured as follows.

AT	REGADR	R/W	CI.0-CI.8
0	0	W	000001001
0	1	W	110110000

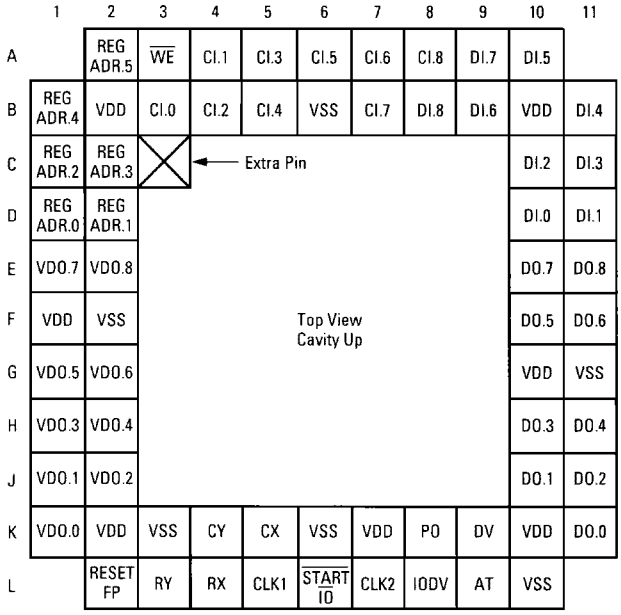
An I/O cycle will load the LUT and clear the ACC RAM.

Once the pixels have been stored in the LUT, pixel processing begins. The X and Y coordinates and a 6-bit flag are stored with each pixel. After the pixel processing cycle three I/O cycles are initiated. The shifter will be used to first read the X values, then the Y values and lastly the flags. The mode memory words needed for each I/O cycle are shown.

AT	REGADR	R/W	CI.0-CI.8
Read X			
0	0	W	000001001
Read Y			
0	0	W	100101001
Read Flag			
0	0	W	111101001

Pinout Diagram

68-Pin Ceramic Pin Grid Array (CPGA)

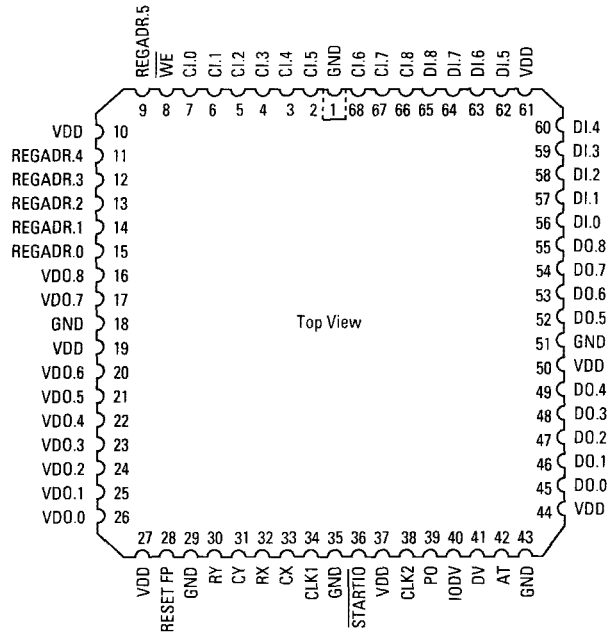


L64250
Histogram/Hough Transform Processor (HHP)

LSI LOGIC

Pinout Diagram

68-Pin Plastic Leaded Chip Carrier (PLCC)



Packaging

68-Pin Ceramic Pin Grid Array: See FB Package in Package Selector Guide
68-Pin Plastic Leaded Chip Carrier: See MC Package in Package Selector Guide

Ordering Information

L64250 G M -XX

- -XX — Speed in MHz
- M — Temperature Range/Flow Option
  - C = Commericial (0°C to 70°C)
  - M = Military (-55°C to + 125°C), Processed to MIL-STD-883C Level B
- G — Package Code
  - G = 68-Pin Ceramic Pin Grid Array
  - J = 68-Pin Plastic Leaded Chip Carrier
- L64250 — Device Type
  - Histogram/Hough Transform Processor